High resolution digitization system for the CROSS experiment

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CROSS experiment

CROSS (Cryogenic Rare-event Observatory with Surface Sensitivity) is a bolometric experiment devoted to the search of **neutrinoless double-beta decay** (0υ2β) that will be installed in Canfranc underground laboratory (LSC, Spain).

The main innovation of the CROSS experiment is the enhanced capability to discriminate surface background events from bulk ones by using **pulse-shape discrimination** (PSD). This improvement with respect to traditional bolometric experiments is possible thanks to **ultra-pure superconductive Aluminum thin foils**, deposited on the surface of the crystals, that act as energy absorbers for α surface events.

This technique has been already demonstrated both with **Lithium molybdate** (Li_2MoO_4) and **Tellurium dioxide** (TeO_2) crystals. The final choice of the 0υ2β candidate material is still subject to study.

Two types of phonon sensors are considered: **NTD Germanium thermistors** (widely used in bolometric experiments) and **NbSi thermistors** (faster and more sensitive to athermal phonons).

Figure 1: Photo of CROSS prototype setup

Pulse-shape discrimination

The adoption of PSD techniques must be considered when designing of the electronics.

For what concern the DAQ system, there are some different requirements with respect to present 0υ2β bolometric experiments (CUORE, CUPID-0, etc.):

- **Faster signals:** phonon signals in CROSS have rise times in the order of 1 ms (up to 500 Hz bandwidth).
- **Higher pile-up:** Lithium molybdate exhibits higher pile-up due to the 2υ2β background.
- **Higher resolution:** detector noise will be reduced thanks to the adoption of a quieter cryostat setup.
- **Continuous acquisition:** required in order to apply the offline trigger and optimum filtering techniques.

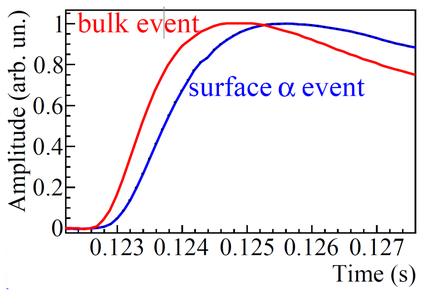

Figure 2: Typical pulse shape of bulk and surface events recorded with NbSi thermistor (image from arXiv:1906.10233)

All these characteristics require a DAQ which is sufficiently fast (5-10 kHz) and flexible in order to adapt to the characteristics of each detector.

DAQ board for CROSS experiment

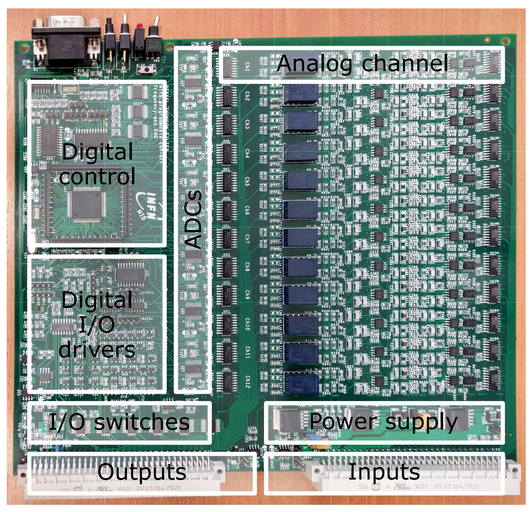

Figure 3: Photo of the antialiasing filter and DAQ board for CROSS

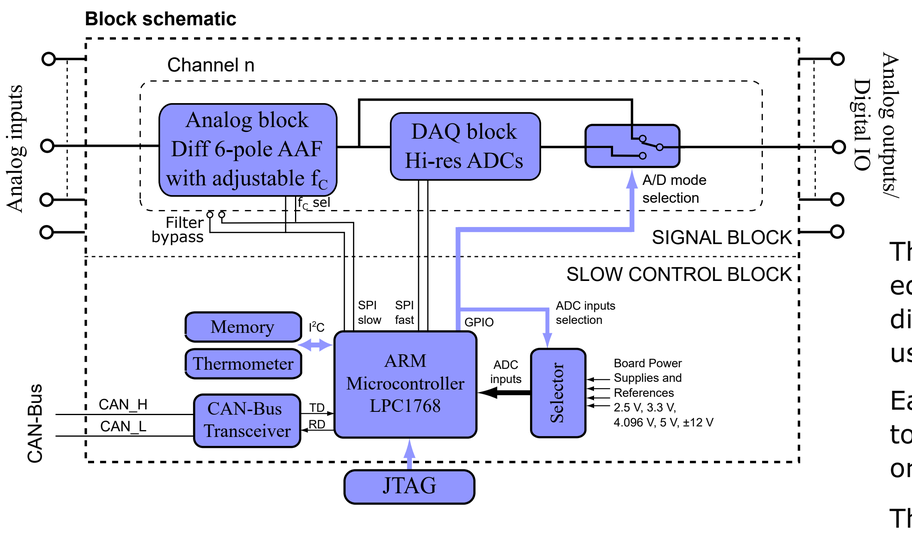

Figure 4: Block schematic of the DAQ board for CROSS

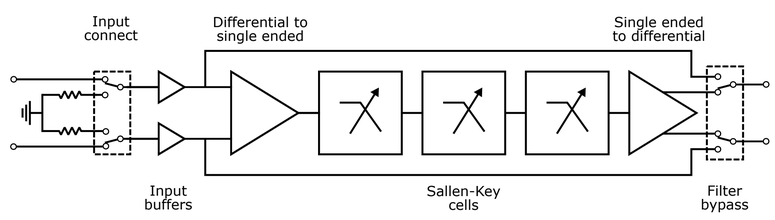

Figure 5: Analog filtering block with programmable cut-off frequency

The DAQ board for CROSS experiment features 12 channels, each one equipped with a 6-pole Bessel-Thomson antialiasing filter with 10-bit digitally **selectable cut-off frequency** from 24 Hz up to 2.5 kHz using high precision digital trimmers.

Each pair of channels is equipped with 24-bit ΔΣ ADCs which are able to digitize the signals up to **25 ksps** per channel in 12-channel mode or **250 ksps** in 6-channel mode.

The data transfer from the board is managed by a FPGA module installed on the backpanel that will collect the data from 8 boards.

Specifications and performance

Channels	12
Power supply	± 12 V, + 5.5 V
Power consumption	250 mW/channel
Filter	6-pole Bessel-Thomson
Cut-off frequency	24 Hz - 2.5 kHz
Cur-off frequency resolution	10 bit
Input differential signal	± 10 V
Gain	1 V/V
Noise (analog)	< 7 µV RMS
PSRR (DC to 10 kHz)	-70 dB
CMRR (DC to 100 Hz)	-70 dB
ADC resolution	24 bit
Maximum sampling frequency	25 kHz (250 kHz with 6 ch.)
Cumulative sampling frequency	1.5 MHz
Effective resolution (1 kHz)	22 bits
Effective resolution (5 kHz)	21.3 bits
Effective resolution (25 kHz)	19.7 bits
Offset drift	10 µV/°C (1 ppm/°C)
Gain error (calibrated)	20 ppm
Gain drift	10 ppm/°C

Table 1: Main specifications and measured performance

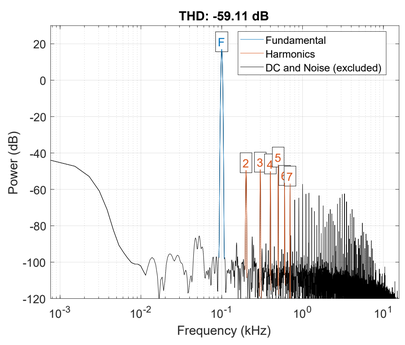

Figure 6: Measurement of THD with a 100 Hz sine (cut-off at 2.4 kHz) using internal DAQ (32 ksps)

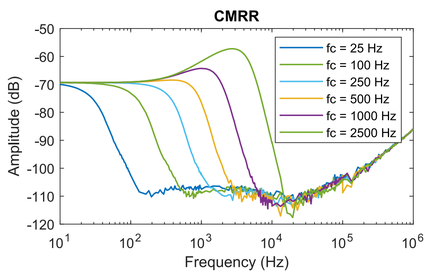

Figure 7: CMRR measurement

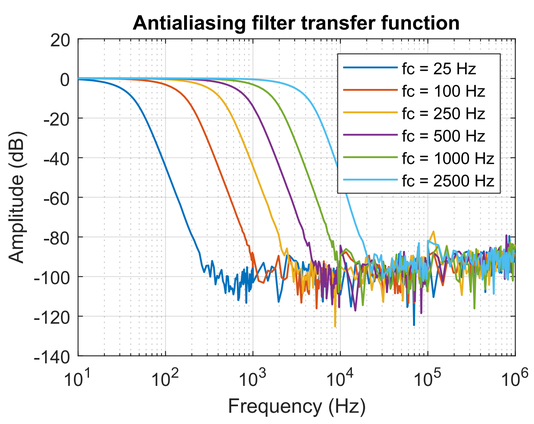

Figure 8: Analog filter transfer function at different cut-off frequency settings

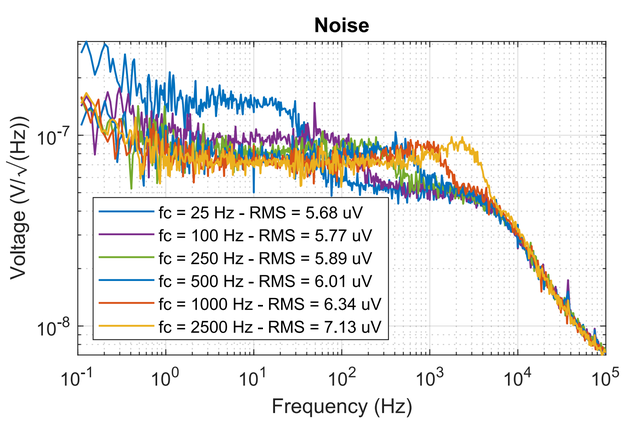

Figure 9: Analog noise spectra at different cut-off frequency settings

Back-end data transfer

Data transfer from the FPGA module (Enclustra Mars MA3) to the storage system is done with **inexpensive 1 Gbps Ethernet** interface (optically decoupled). Data protocol is UDP, with a maximum data rate of 768 Mbps (6 channels per board at 250 kHz and 64 bit data length).

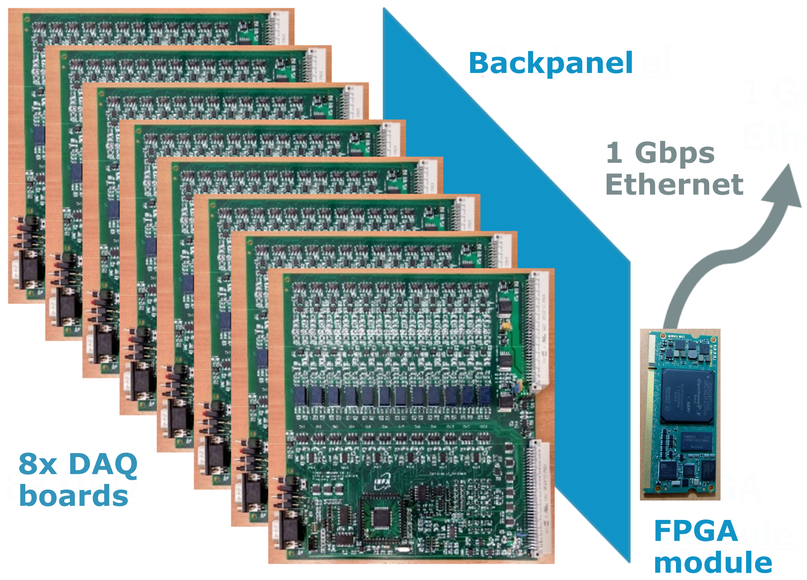

Figure 10: Back-end block schematic

Future developments

The board is already fully operational and data read-out from the FPGA module has been demonstrated using a provisional backpanel. Next steps:

Test with detectors: test with signals from CROSS detectors in Sept-19.
Design full backpanel: will allow to test full output data rate.
Slow control through FPGA: at the moment CAN bus configuration to the single boards is managed independently.
Inter-module syncronization: synchronization between FPGA modules will be implemented once the full backpanel is available.

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