CROSS experiment

CROSS (Cryogenic Rare-event Observatory with Surface Sensitivity) is a bolometric experiment devoted to the search of neutrinoless double-beta decay ($0
\nu \beta\beta$) that will be installed in Canfranc underground laboratory (LSC, Spain).

The main innovation of the CROSS experiment is the enhanced capability to discriminate surface background events from bulk ones by using pulse-shape discrimination (PSD). This improvement in respect to traditional bolometric experiments is possible thanks to ultra-pure superconductive Aluminum thin foils, deposited on the surface of the crystals, that act as energy absorbers for surface events.

This technique has been already demonstrated both with Lithium molybdate ($\text{Li}_2\text{MoO}_4$) and Tellurium dioxide ($\text{TeO}_2$) crystals. The final choice of the 0$\nu \beta\beta$ candidate material is still subject to study.

Two types of phonon sensors are considered: NTD Germanium thermosts (widely used in bolometric experiments) and NiSi thermosts (faster and more sensitive to athermal phonons).

Pulse-shape discrimination

The adoption of PSD techniques must be considered when designing of the electronics.

- Faster signals: phonon signals in CROSS have rise times in the order of 1 ms (up to 500 Hz bandwidth).
- Higher pile-up: Lithium molybdate exhibits higher pile-up due to the 2$\nu \beta\beta$ background.
- Higher resolution: detector noise will be reduced thanks to the adoption of a quiter cryostat setup.
- Continuous acquisition: required in order to apply the offline trigger and optimum filtering techniques.

Specifications and performance

The DAQ board for CROSS experiment features 12 channels, each one equipped with a 6-pole Bessel-Thomson antialiasing filter with 10-bit selectable cut-off frequency using high precision digital trimmers.

- ΔΣ Each pair of channels is equipped with 24-bit ΔΣ ADCs are able to digitize the signals up to 250 ksps per channel in 12-channel mode or 250 ksp/s in 6-channel mode.
- The data transfer from the board is managed by a FPGA module installed on the backpanel that will collect the data from 8 boards.

Back-end data transfer

Data transfer from the FPGA module (Endiustra Mars MA3) to the storage system is done with Inexpensive 1 Gbps Ethernet interface (optically decoupled). Data protocol is UDP, with a maximum data rate of 768 Mbps (6 channels per board at 250 kHz and 64 bit data length).

Future developments

The board is already fully operational and data read-out from the FPGA module has been demonstrated using a provisional backpanel. Next steps:

- Test with detectors: test with signals from CROSS detectors in Sept-19.
- Design full backpanel: will allow to test full output data rate.
- Slow control through FPGA: at the moment CAN bus configuration to the single boards is managed independently.
- Inter-module synchronization: synchronization between FPGA modules will be implemented once the full backpanel is available.

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