

ECLIPSE, THE CRYOGENIC READOUT CIRCUIT OF THE POLARIMETRIC CAMERA B-BOP FOR THE SPICA SPATIAL OBSERVATORY PROJECT



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Context - objectives

> SPICA :

- a spatial infrared observatory project,
- initially proposed by JAXA, and selected in May 2018 (with 2 other projects), as M5 medium mission candidate, by ESA.

B-BOP

- one of the 3 instruments of SPICA,
- dedicated to polarized imaging in the far infrared (mainly intended for the measurement of the magnetic field structure in the molecular clouds of the galaxy).

B-BOP characteristics :

- a 3-bands imager, with the ability to measure the polarization at the level of each pixel,
- made of five 16 x 16 bolometric pixels matrices and one 8 x 8 pixels matrix working simultaneously,
- with a sensitivity improved by 2 magnitude orders.



SPICA satellite project

A new assembling mode :

The classical hybridizing between detection part and reading circuit is replaced by a new assembling mode : sensor is directly built on its readout circuit, used as a mechanical substrate during its manufacturing process.

 \Rightarrow the **distance** between detector and readout electronics is minimized, and so the parasitic capacitance of the interconnections.

> Consequences :

- The working temperature of the detector and the readout circuit is the same: 50 mK.
- This imposes extremely severe constraints on the power consumption of the circuit, with a thermal budget of only <0.2 µW per matrix of 16 x 16 pixels, each pixel requiring 4 or 5 readout channels.
- > Manufacturing :
- ASIC by AMS foundry, in its CMOS 350 nm technology.

Implementation









B-BOP innovations

It inherits from Herschel/PACS detectors, but with a number of technological innovations, mainly :

- the detection layer is sensitive to the polarization by including 2 sets of absorbing dipoles in each **pixel**, placed orthogonally;
- the assembling mode of the detector and the readout circuit (see next section).



B-BOP focal plane : 6 matrices, 3 wavelengths

• Detection layers by CEA/LETI, in its Above-IC technology

 \rightarrow deposition of an oxide layer and a sacrificial layer on the ASIC, with reservation of holes then filled with copper, in order to create "nails" for interconnecting ASIC and detector, then deposition and etching of the detection layers, removing of the sacrificial layer.

 \Rightarrow creation of a separated bolometric structure, supported by the interconnection nails.

Technological qualification

Test of the AMS CMOS 350 nm technology at 100 mK : (A. Rhouni et al., J. Phys.: Conf. Ser. 834 012005 (2017))

- A special ASIC, "RoBo", has been designed and tested.
- It contained NMOS and PMOS transistors with different sizes.
- I(V) characteristics and noise have been measured.



Technological characterization circuit and test bench

PMOS output characteristics (transistor size : 1250 µm x 10 µm)



> Reading schemes :

- Each pixel converts the incident photons energy in heat \Rightarrow temperature increasing, measured by 4 thermometers, in series with biasing resistances, forming a kind of Wheatstone bridge.
- 2 thermometers are connected to absorbers sensible to the vertical light polarization, and the 2 others to the horizontal one.
- 2 possible schemes of readout are implemented in the ASIC :
- single-ended scheme : access individually to all the thermometers signals (v1 to v4, and vx),
- differential scheme : access to the total light intensity signal (v1-v2), and to the polarization differential signal (v3-v4), saving one readout channel per pixel.
- We wanted to evaluate both readout schemes \Rightarrow we have implemented them simultaneously by designing 6 channels per pixel, each one biased or not. This is the position of the detector regarding to the ASIC (little shift) that sets what readout scheme is used.







> Operating phases (for multiplexing and minimization of power consumption):

• Phase 1 : pre-charging

The follower of the pixel is not powered, and the circuit output is connected to another pixel. The input capacity (for avoiding glitches on detector when switching) is pre-charged, and the follower input is connected to a reference level, which is set to the mean voltage of the input, to minimize the changing of the transistor grid voltage when reading will occur (phase 4)

 \Rightarrow we take advantage of the rest time (15/16th of time) to prepare the future commutation. The input capacitance value can be adjusted, by static switches, to the thermometer resistance : high capacitances reduce more efficiently glitches, but also the passband.

Phase 2 : separation

The output is disconnected from any pixel, to

avoid any charge transfer between pixels. Since the current source is still active, this one causes linear charging of the parasitic output capacitance : an undesired effect avoided by an external device.

The sweep delay is the time between two consecutives measurements

> Conclusions :

- CMOS transistors still work at 100 mK for low drain currents.
- PMOS have usual characteristics \Rightarrow PMOS will be used in the analog chain.
- NMOS presents anomalies in characteristics (probably freeze out of silicon substrate)
- \Rightarrow NMOS will be reserved to digital functions and switches.

- Electronics constraints :
- Very low temperature (50 mK) \Rightarrow transistors noise decreases, but their threshold voltages increase, and temperature induces anomalies \Rightarrow taken into account in the :
- schematics,
- choice of biasing tensions,
- type of transistors (\rightarrow PMOS for the analog chains).
- Extremely low dissipation budget \Rightarrow
- very low biasing currents (typically ~10 nA),
- very simple schematics (a source follower with a current source),
- biasing of input stage only when the corresponding pixel is read (\Rightarrow one 16th of time).
- Very high detector impedance (typically 1 $G\Omega$)
- \Rightarrow This requires :
- low parasitic capacitance between detector and electronics, to preserve the passband \rightarrow ensured by the Above-IC technology.
- a mechanism for avoiding charges injection on the detector when commutation.



Phase 3 : reference reading The follower is connected to the current

source and starts to conduct. The circuit output copies the reference voltage (to within the threshold voltage), which can be used for a correlated double sampling.

The reference level being low impedance, the charging of the follower parasitic capacitances is fast.

• Phase 4 : thermometer reading

The **follower** is disconnected from the reference and then connected to the

thermometer.

The charging of the parasitic capacity is immediately (but partially) corrected by the much higher input capacity (charges sharing), and then the rest of the charge correction is done through the thermometer, much more slowly because of its very high impedance. The variation speed at the output is also limited by the strength of the bias current, and by the magnitude of the parasitic output capacitance.

Clocks :

• In order to minimize the charge injection on the detector due to the switches themselves (NMOS + PMOS in //), the internal clock signals are differential, with adjusted values of their high and low levels, so that to compensate the charges flux when switching.

Simulation 1,5 *m*s > Temporal diagram resulting from simulation : /179/10/cmdref<2: 1,5 ms (41,7 Hz) • Multiplexing : N and P complementary clocks, - 16 pixels are multiplexed together (= a row of the 16 x 16 matrix)

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with their adjusted analog high and low levels

Conclusion

> An integrated circuit has been designed to perform the buffering, the 16 to 1 multiplexing, and the input stage intermittent powering of the polarimetric

- one pixel is read every 24 ms (41.7 Hz),
- its readout takes : 1.5 ms.

• Signal injection :

- a sinusoid is injected on one of the 16 pixels, no signal on the others,
- with a frequency of 20.8 Hz (the highest measurable frequency at 41.7 Hz).
- Perturbation of the thermometer by the electronics switching :
- before the reading of a pixel, the electronics input node and its parasitic capacitances have been pre-charged to a reference mean level;
- when switching \Rightarrow perturbations: this level is suddenly imposed to the thermometer;
- then the thermometer node returns to the voltage induced by temperature, but slowly because of the very high resistance of the thermometer (~1 G Ω).
- This perturbation is attenuated :
- thanks to a capacitance placed at the input, pre-charged at the mean value of the voltage,
- thanks to the complementary clocks with adjusted levels, that avoid charge injection due to switches when they operate.
- By this means the output voltage has (just) time to settle before the switching to another pixel.

Power consumption (crucial feature) :

- Simulation gives 518 nW for 4 reading nodes per pixel and a current biasing of 16 nA. Lower power will be experimentally tested.
- A very sharp over-consuming appears during the switching, representing a mean consumption of only 36 nW: this is the fundamental consumption of the circuit when multiplexing at 667 Hz and when the biasing current is null.



camera of the future SPICA satellite.

- This circuit contains two main innovations : • its working temperature : 50 mK, • its assembling mode with detector : the LETI's Above IC technology.
- It fulfils very sharp constraints : • extremely low power budget : <0.2 µW for 256 pixels with each 4 to 5 channels, • switching of very high impedances (1 G Ω).
- It has been produced and recently delivered.

\succ It will be tested soon at 50 mK :

- first without its detector over-layer,
- then with the detector (more than one year is necessary for the detector manufacturing).
- The main test work will consist in controlling the proper working of all its functionalities, and in evaluating its noise performances according to its consumption.

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