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Fabrication of Planar Integrated SIS Mixer Circuit with High Uniformity and High Yield

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We have been developing Superconductor-Insulator-Superconductor (SIS) mixer integrated circuits (ICs) for highly compact multi-beam heterodyne receivers. The distinctive feature of the SIS mixer ICs is the incorporation of membrane-supported waveguide probes for signal and local oscillator coupling. This idea makes it possible to compactly accommodate many pixels on the focal plane and to broaden the field of view of mm/sub-mm wave radio telescopes.

The SIS mixer IC on a silicon-based chip in this study have a much larger area than a conventional SIS mixer on a glass chip. It is because the IC contains many planar circuit RF components which are implemented with metal waveguide structures in a conventional mixer. In this study, the area of the single pixel prototype IC chip we have designed is about 45 times larger than that of the conventional mixer chip at 2 mm wave length that has been developed before in our lab. The area of the IC chip will become even larger if multiple pixels are incorporated. In consequence, the on-wafer uniformity of circuit geometries and the SIS junction yield turn out to be essential.

We have been carrying out fabrication of prototype SIS mixer ICs with applying machine-aligned via-hole etching process together with insulator layer deposition with plasma enhanced chemical vapor deposition. This approach shows much improved circuit uniformity and SIS junction yield in comparison with the self-aligned lift-off process together with RF-sputtering of the insulator layers. In this presentation, we will report the fabrication processes and the characteristics of the prototype SIS ICs.

Less than 5 years of experience since completion of Ph.D

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