Fabrication of Planar Integrated SIS Mixer Circuit with High Uniformity and High Yield

ID: 189-234

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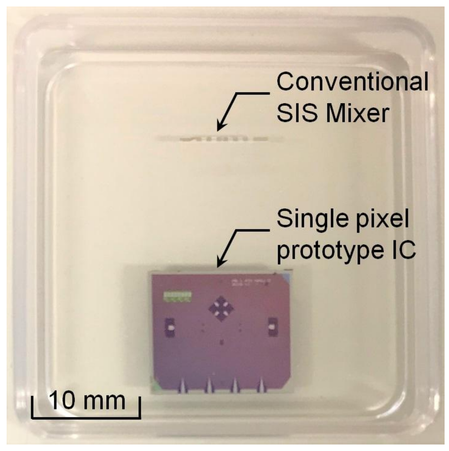
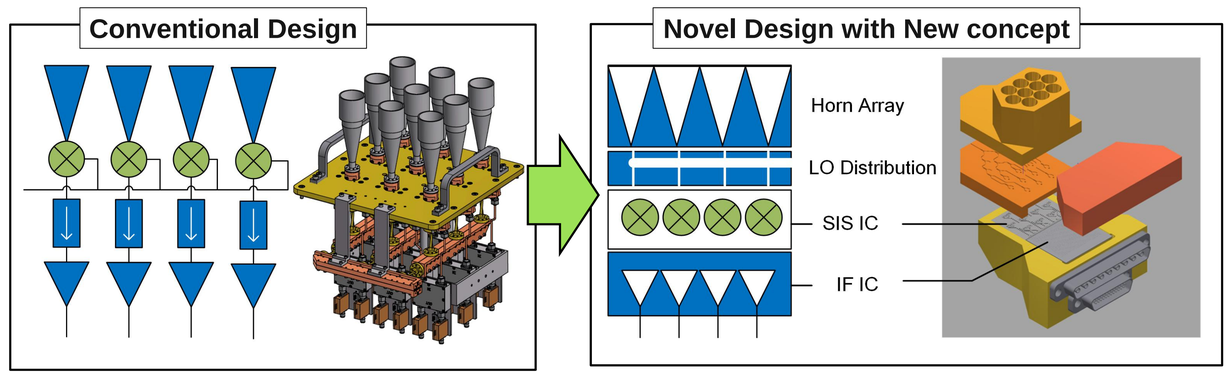
Overview



We have been developing Superconductor-Insulator-Superconductor (SIS) mixer integrated circuit (IC) for highly compact multi-beam heterodyne receivers. The SIS mixer IC has many planar rf components which have not been introduced in conventional SIS mixers. The area of a SIS mixer IC chip becomes much larger than that of a conventional SIS mixer chip due to the introduction the planar rf components The across-wafer uniformity of circuit geometries and the SIS junction yield become essential for the IC fabrication with increasing the area of the SIS mixer IC chip. We succeeded to improve yield and uniformity of the single pixel prototype SIS mixer IC by applying machine-aligned via-hole etching together with an insulator layer deposition with plasma-enhanced chemical vapor deposition (PE-CVD).

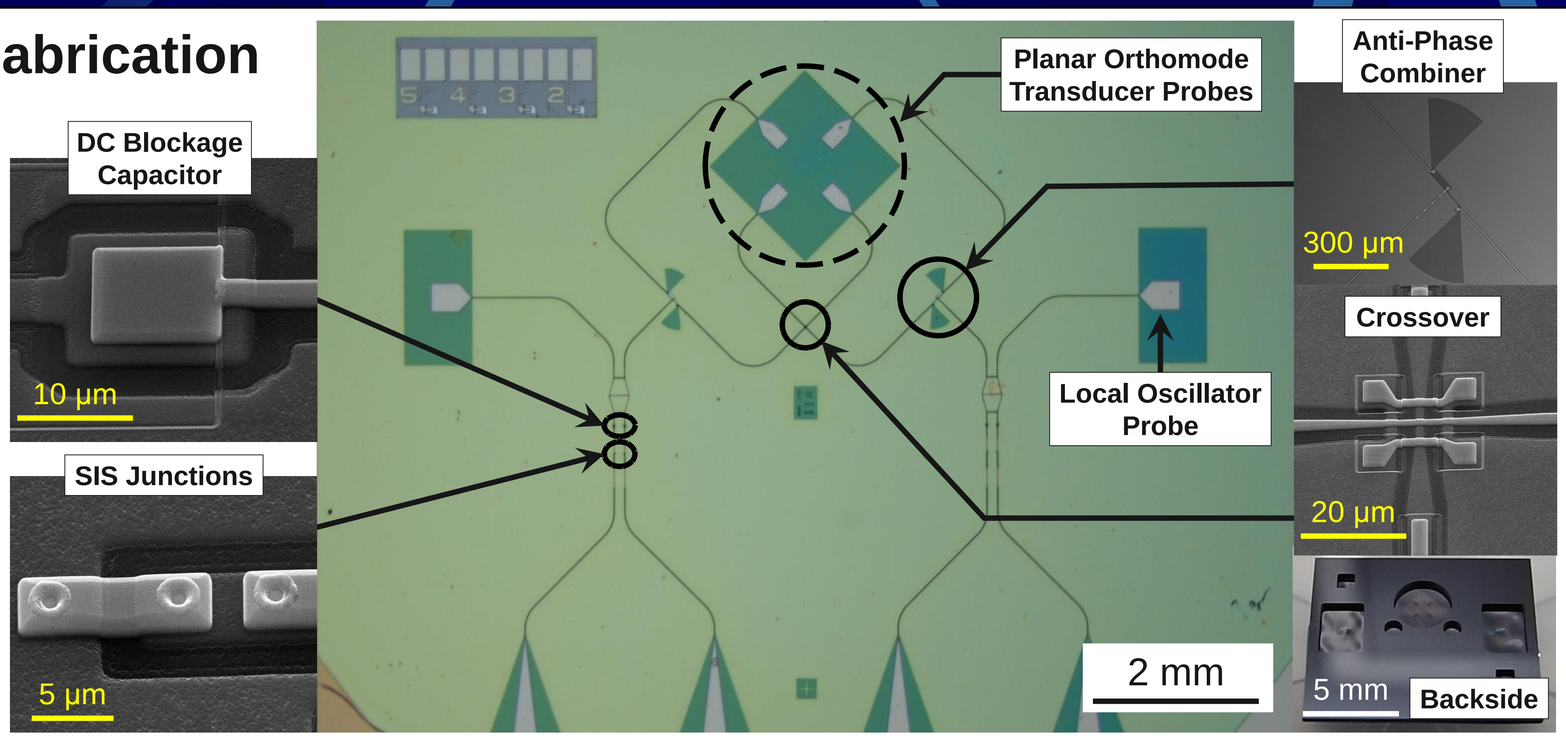
Concept design



The principal idea for a highly compact multi-beam receiver is the incorporation of membrane-supported waveguide probes into the ICs for signal and Local Oscillator (LO) coupling. This approach significantly facilitates the LO distribution and therefore enables a large pixel count.

Reference: W. Shan, *et al.*, IEEE Trans. Terahertz Sci. Technol. **8** (4), 472 (2018).
W. Shan, *et al.*, Proc. SPIE **10708**, 1070814 (2018).

Fabrication



Process Step

1. Substrate protection layers sputtering (Al_2O_3/ SiO_2)
2. Nb/Al-AlO_x/Al/Nb sputtering (SIS multi-layer)
3. Base patterning (Lift-off)
4. Al_2O_3 sputtering (DC blockage capacitor)
5. DC blockage capacitor (Al_2O_3) definition (Lift-off)
6. Junction mask deposition (PE-CVD SiO_2)
7. Junction definition (ICP-RIE)
8. Anodization
9. Insulator layer deposition (PE-CVD SiO_2)
10. Via-hole etching
11. Wire sputtering (Nb)
12. Wire patterning (ICP-RIE)
13. Membrane fabrication (Deep-RIE)

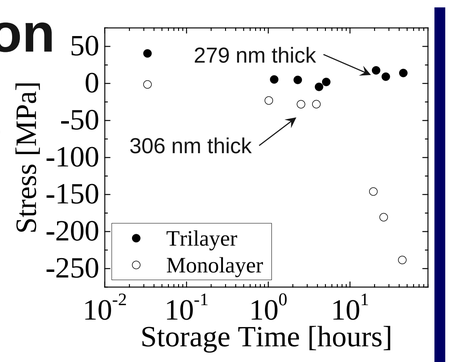
Plasma-enhanced Chemical Vapor Deposition

Advantage of PE-CVD

PE-CVD realizes SiO_2 deposition with superior step coverage, low damage, low stress and at low temperature.

Trilayer SiO_2 film (Compressive/Tensile/Compressive SiO_2 film)

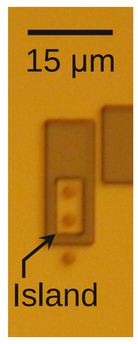
Low stress SiO_2 film is desirable for SIS junction fabrication. On the other hand, low or tensile stress of SiO_2 film changes to more compressive over time. Trilayer (Compressive/Tensile/Compressive) SiO_2 film allows us to control the stress without stress change.



Stress change of SiO_2 as a function of storage time

Step	Power [W]	TEOS [sccm]	O_2 [sccm]	Pressure [Pa]	Time [s]	Thickness [nm]	Stress [MPa]
1	350	15	680	40	36	94	-230
2	150	15	680	40	55	95	+510
3	350	15	680	40	44	115	-230
Trilayer	-	-	-	-	-	~300	-80

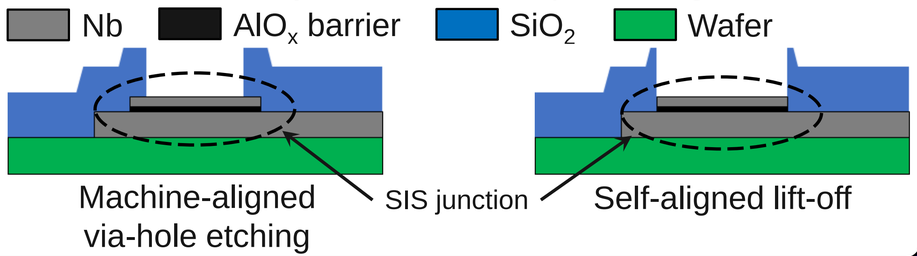
Via-hole Etching



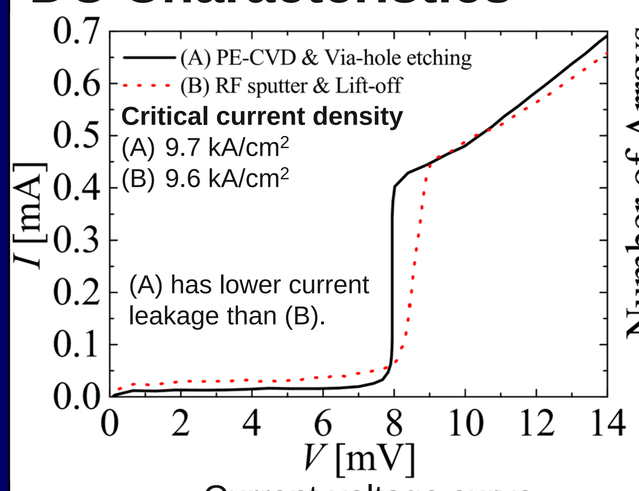
A self-aligned lift-off method may cause current leakage from sidewall of junctions in this SIS mixer IC, because the junctions on the island patterns cannot be anodized. This via-hole etching process can avoid current leakage around the junctions, even though without the anodization treatment.

Equipment for via-hole etching:

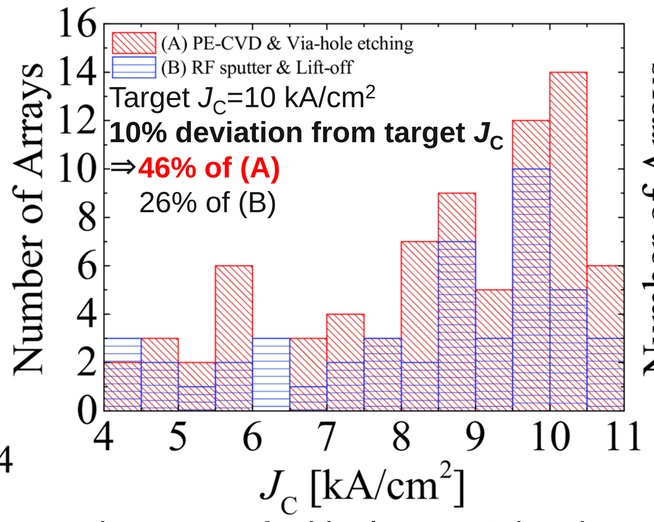
Stepper with excellent alignment accuracy exposure
ICP-RIE system for anisotropic etching



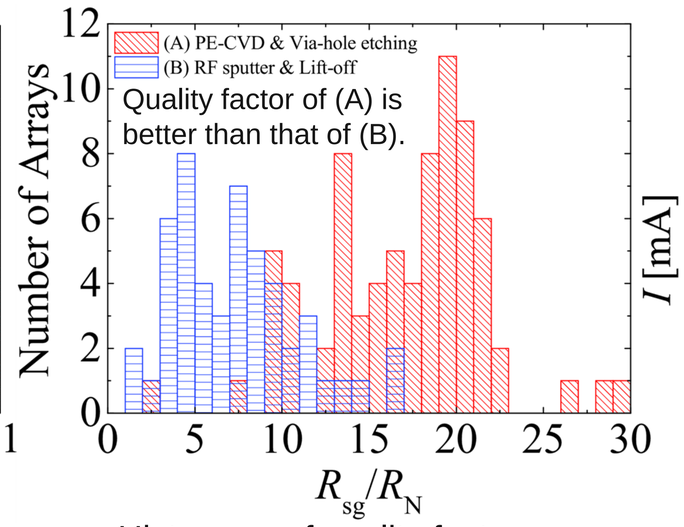
DC Characteristics



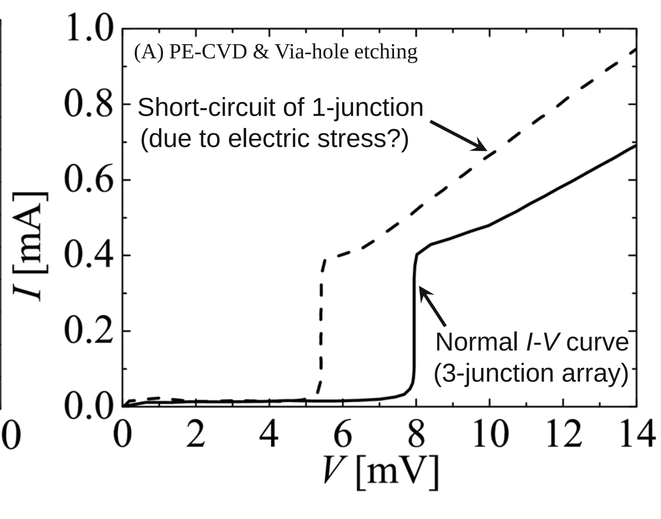
Current-voltage curve



Histogram of critical current density



Histogram of quality factor



Current-voltage curves

Summary: We have fabricated prototype SIS mixer ICs for the multi-beam heterodyne receiver application by applying PE-CVD for SiO_2 deposition and a via-hole etching for contact-hole definition on top of SIS junctions. The quality factor and the deviation of the critical current density were much improved by introducing the PE-CVD and the via-hole etching. Efforts are being done for even higher uniformity and higher yield. Some of the SIS junction arrays show one of the three junctions in an array is short circuit. We attribute this problem to the electric stress during plasma processes, though more studies are necessary to achieve final conclusion.

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