

Simplifying FPGA Complexity



Since 2014

Headquarter Polo Tecnologico di Navacchio, Pisa

Staff

4 engineers and 3 physicist with +15 years experience in DSP, FPGA, HDL, high speed digital design.

We are a specialized group of skilled peoples, focused on FPGA and SoC-based solutions. We provide services from high-speed hardware processing boards or high performance firmware through to embedded software.




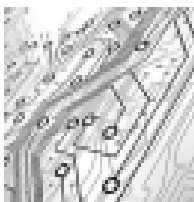
Partnership and Cooperation





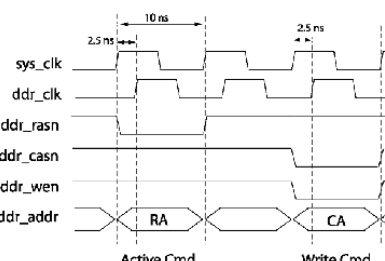
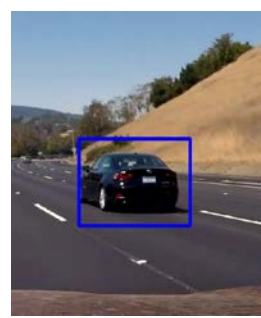
Italian Companies at CERN, 19 September 2018

www.campera-es.com

Offer and Services

HDL Design	IP Cores
 <p>A unique mixture of know-how from DSP up to HDL module. We developed high performance, vendor independent "off the shelf" VHDL Digital Signal Processing Libraries (Utility, Math, I/O, HW driver).</p>	 <p>Application Specific IP core, tailored to a particular application from basic up to complex macro functions, such as Radar Processor, Real Time Channelizer or fully configurable FFT. Each IP Cores is certifiable for safety critical applications.</p>
SoC	Hardware Design
 <p>High experience in SoC based system (Zynq, Zynq UltraScale+, Altera HPS) both for baremetal and OS project.</p>	 <p>High speed digital board design, from design concept down to prototype production. Design for testability, multiple FPGA based board, high-speed link interface, Power and Signal Integrity Analysis.</p>

FPGA Design Expertise

R&D	Radar
 <p>SKA is an international effort to build the world's largest radio telescope, with more than 32.000 FPGA involved.</p> <ul style="list-style-type: none"> Fully parallel FFT up to 100 Gsaps PFB (Polyphase Filter Bank): real time bandwidth of up to 4.6 GHz, rejection out of band up to 63 dB and in band ripple 0.2 dB Beamforming 	 <p>Radar Signal Processing</p> <ul style="list-style-type: none"> Pulse Compressor Core (>100 GSaps) Waveform Generator (CW, LFM, Barker, Chirp) 2D Rectangular Array RX/TX Digital Beam Synthesis Digital Up and Down Conversion 1D/2D FIR and IIR Filter
High Speed Interface	Video Processing
 <p>High-speed interface control design:</p> <ul style="list-style-type: none"> PCIe Enet up to 10Gbps Memory controller for DDR3 and DDR4 Design for SDI protocol (SD and HD) Design for ATA protocol 	 <p>Real Time Video Processing:</p> <ul style="list-style-type: none"> Real time tracking <ul style="list-style-type: none"> Segmentation CCL (connected component labeling) Predictive filter Real time stabilization High speed Interface and data Format