Simplifying FPGA Complexity

ABOUT US

Campera Electronic Systems Srl is a high-technology, privately held, startup based in Polo Tecnologico Navacchio (Pisa), Italy. Established in March 2014 has grown rapidly with a focus on FPGA and its applications.

- **The Staff has more than 10 years of experience on FPGA design, Digital Signal Processing and board level design for Telecommunication, Aerospace and Defense, Test and Measurement and High Performance Computing markets.**
- **Campera Electronic Systems provides services covering the whole range of FPGA-based systems development: from high-speed hardware processing boards or high performance HDL firmware through to embedded software, from specification and implementation through to prototype production.**

PREMISES	STAFF	ASSETS
Headquarter: Livorno 	• 4 engineers with +10 years experience in DSP, FPGA, HDL, high speed digital design; • Cooperation with the University of Pisa and Rome;	1. IP(s) HDL: about 500.000 lines of proprietary source code (VHDL, Verilog, Tcl, C/C++)

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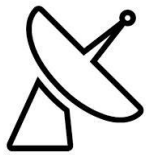
OFFER

HDL Design
A unique mixture of know-how from DSP up to HDL alongside a vast, fully verified, collection of HDL IP core

CES HDL Library
High performance, vendor independent "off the shelf" VHDL Digital Signal Processing Libraries

Safety Critical Design
FPGA design, certifiable IP Cores and V&V for safety critical applications.



ASIPs
Application Specific IP core , tailored to a specific application

V & V
Simulation, documentation and independent Verification and Validation services.

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HDL Design

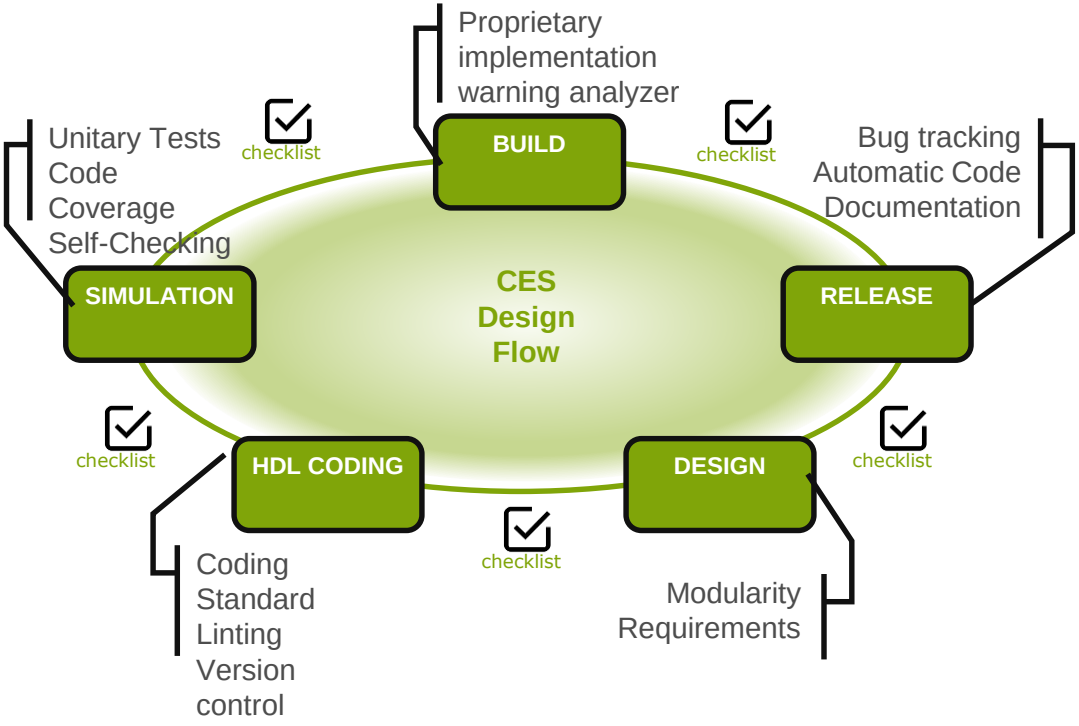
HDL design flow

- Proprietary VHDL/Verilog/Tcl/Matlab Coding Standard
- Automatic linting and code review with proprietary tools.
- Repository with version control system.
- Modular based design for maximum code reusability.
- Functional RTL level simulation and comparison between fixed-point model and the reference floating point model to address quantization error (for DSP fixed-point modules)
- Code Coverage to ensure testing of the entire code
- Safe FSM design, safety critical applications
- Synthesis Verification (post PAR and Synthesis simulation when feasible, dual synthesizer and comparison, formal equivalence and code instrumentation)

IPs are developed according to the highest standards of development and coding, the self-checking testbenches are compared with the fixed point model, which are, in turn, functionally verified against the golden reference floating point model

Design Flow

FPGA design complexity is managed by means of a Design Flow that details every step of the design process and proper checklists to advance between design phases.



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FPGA Design Expertise

HDL FPGA design

- PCIe Design
- Optical Link with Aurora protocol
- Microblaze Embedded processor
- Signal Processing on FPGA
  - FFT (1D, 2D),
  - High performance Filters (IIR, FIR, 1D/2D),
  - Radar Processing
  - Sonar Processing
  - Image Processing
  - Digital Down/Up Conversion
- UART, Serial protocols (RS-232/485), I2C, SPI
- GbEthernet
- Verification and Validation (EN-61508, DO-254, DO178)
- Memory controllers: QDR, DDR2, DDR3, EEPROM
- ADCs, DACs interfaces

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VHDL IPs

PROBLEM

Dimension and complexity of ultimate generation FPGAs are extremely increasing. The FPGA design presents challenges growing at the same rate, hence project costs, life span and related risks are high. Thus, the need to have fully verified library modules with which create user applications arises for Customers which want costs and deadlines surely defined and a de-risked process.

SOLUTION

Campera Electronic Systems (CES) **Library Modules** range from simple registers or combinatorial functions, through to FIFOs, MATH and DSP modules, up to complex macro functions, such a Radar Processing Core or a Channelizer based on a Polyphase Filter Bank architecture, which we call **ASIP** (Application Specific IP).
Building such libraries is usually out of the scope of Customers which tends to concentrate on the user application, rather than a general purpose, reusable, fully verified and documented libraries of modules.

BENEFITS

Using our commercially supported library reduces costs, time to market and greatly improve the quality of results, opening new possibilities to our Customers.

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FFT Core

- **FFT IP Core** is a beyond state of the art forward/inverse Fast Fourier Transform Processor, capable of up to 200 GSaps real time continuous data processing in a single ASIC/FPGA.

- The FFT Processor is a highly parameterized ASIP cores that can be easily configured to meet the size and processing performance needed by the most demanding applications. The VHDL libraries implement pipelined modules for mixed radix-2/4/8 both for real and complex data stream.

Application
- Channelizers
- High performance Pulse Compressors
- Wideband real-time spectral analysis

Key features
•Configurable FFT length up to > 1M points
•Configurable input, output and twiddle factors word length
•Configurable time multiplexing factor
•Architecture allows real-time continuous data processing up to 200 GSaps
•Support of interleaved input signals
•Support real and complex input signals
•Optimized algorithm for real-value input signals
•Minimizing spectral leakage using standard or polyphase windowing

•**FFT VHDL IP** Core is fully vendor independent, with support for different EDA tools and target technologies

ASIP

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CHANNELIZER Core

- The channelizer is based on a highly configurable Polyphase Filter Bank architecture capable of analyze over 4GHz BW in real time with up to 512.000 channels, using our super fast CES FFT Core
- The polyphase filter uses a Weight-Overlap-Add (WOLA) operation on a serial data stream, multiplying segments of the stream by a filter function and adding together individual frames of the result.
- Oversampling and overlapping between segments are implemented to extend alias free region.

Applications

- Radio Astronomy
- Radar\Sonar\Lidar
- Communications Systems (SDR)
- Wireless Communications
- Electronic Warfare
- Real-time spectral analysis

ASIP

Key features

- Real Time bandwidth of up to 4.6 GHz, rejection out of band up to 63 dB and in band ripple 0.2 dB
- Configurable filter length and coefficient taps bit width
- Configurable oversampling factor and overlapping length
- Configurable Number of channels
- Configurable input/output data width
- Configurable time multiplexing factor for highly parallel operating architecture
- Optimized algorithm for real-value input signals
- Support interleaved input signals
- Continuous data rate up to 10 GSps
- The VHDL library is fully vendor independent, with support for different EDA tools and target technologies

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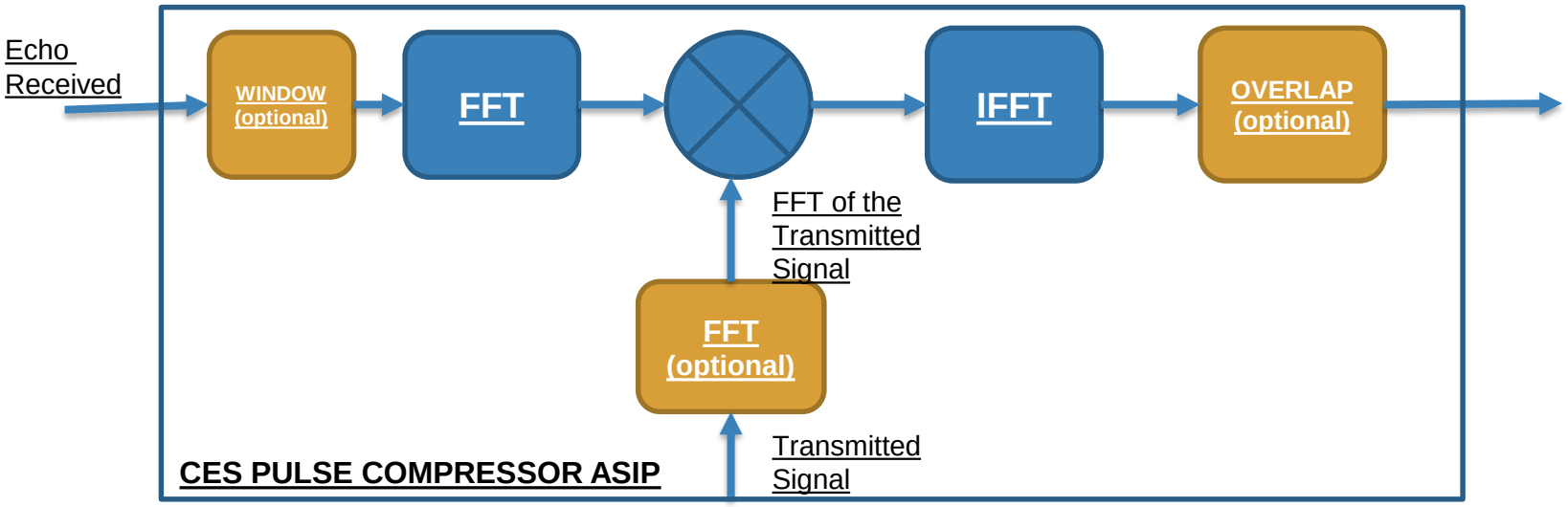
PULSE COMPRESSOR Core

Pulse compressor methods and CES Radar Pulse Compressor ASIP

- Direct Convolution: Hyper Speed FIR Filter ASIP
- FFT Cyclic Convolution: Weigthed OverLap-Add (WOLA) Pulse Compressor ASIP

Comparison on the number of operations (multiply/add)

N	FFT	FIR
4	176	16
32	2,560	1,024
64	5,888	4,096
128	13,312	16,384
2048	311,296	4,194,304



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PROJECTS

SKA	
Project Description	Square Kilometre Array (SKA) project (https://www.skatelescope.org/). SKA is an international effort to build the world's largest radio telescope, with a square kilometre (one million square metres) of collecting area. As one of the largest scientific endeavors in history, the SKA will bring together a wealth of the world's finest scientists, engineers and policy makers to bring the project to fruition. Within this project, Campera is the FPGA and algorithms designer with The Arcetri Astrophysical Observatory, that is a public center for scientific research, and it is part of the National Institute for Astrophysics (INAF). Campera is carrying out the implementation of a polyphase filter bank (PFB) channelizer IP. Starting from modeling and simulation, the system will be designed in HDL at RTL level for the FPGA implementation. The channelizer together with a beamformer will be implemented on 32.000 Kintex Ultrascale
System skills involved	Digital Signal Processing, High speed serial links (JESD204B, Gb Tranceivers)
Hardware used	32.000 x Kintex Ultrascale xcku040
Software used	Xilinx Vivado 2014.2, Active-HDL, Riviera-Pro, Alint, Matlab (toolboxes), Synopsys Synplify, Mentor Precision

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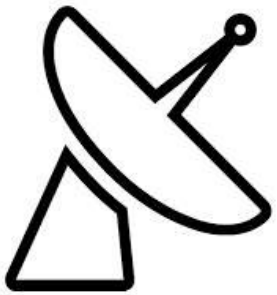
PROJECTS

PROGRAMMABLE RADAR SIMULATOR	
Project Description 	Design of 4 different FPGAs on 4 different boards, 3 Virtex 5 SX50T and 1 Spartan 6 LX45T. • Two FPGAs manages PCIe bus to and from a PC, Optical Link with Aurora protocol and control another FPGA via proprietary parallel bus. • One FPGA is a digital Receiver, controlling 4 ADCs, and implementing high performance Radar signal processing. Data are then transmitted on a high-speed PCIe lane to a microprocessor for post processing • The Spartan 6 FPGA controls a digital down converter board with DACs and DDS
System skills involved	Radar Signal Processing, High speed serial links (PCIe, Optical Link), FPGA design
Hardware used	3 x Virtex 5 SX50T, 1 x Spartan 6 LX45T
Software used	Xilinx ISE 14, Modelsim, Scilab 5.4

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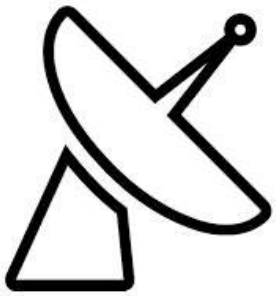
PROJECTS

METEO RADAR	
Project Description 	Design of 2 different FPGAs (Virtex5 SX50T) on 2 different boardsconnected with an Optical Link and a GbEthernet. • One FPGAs is a digital Receiver, controlling 4 ADCs, and implementing high performance Radar signal processing. Board control is handled via a Microblaze embedded processor which communicates with a remore PC via a GBEthernet connection. Data are then transmitted on a high-speed Optical Link with Aurora Protocol • One FPGA on a different board captures data from the optical link, process them and send them again to a PC for post processing operations via a high speed PCIe connection. The FPGA also controls QDR memories and DACs for arbitrary waveform generation.
System skills involved	Radar Signal Processing, High speed serial links (PCIe, Optical Link), FPGA design
Hardware used	2 x Virtex 5 SX50T
Software used	Xilinx ISE 14, Modelsim, Scilab 5.4

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UTILITY VHDL Library

CES UTILITY Library Modules

Part Number	Product Name
CES_U010	priority encoder
CES_U020	parity generator
CES_U030	debouncer
CES_U040	multiplexer
CES_U050	demultiplexer
CES_U060	CRC calculator
CES_U070	decoder
CES_U080	encoder
CES_U090	pulse generator
CES_U100	clock generator
CES_U110	multi-purpose delay-shift_reg_pipeline
CES_U120	delay
CES_U160	ram, single, simple dual, true dual, multi aspect ratio (read before write, write before read, no change)
CES_U170	Asynchronous FIFO
CES_U180	Synchronous FIFO
CES_U190	ECC decoder/encoder
CES_U200	Parallel Search Algorithm (heap sort)
CES_U210	Hamming Encoder/decoder

The ces_util_lib is the «Swiss Army Knife» of every FPGA designer

Key features

- Language; VHDL (1993-2002, 2008)
- Suitable to be used also in Safety and Mission critical applications (EN 61508, DO 254).
- Portable, vendor independent
- No hidden costs during projects life time
  - **NO COSTS FOR DEVICE UPGRADE (if the project shall be migrated to different target there's no need to regenerate the core)**
  - **NO MAINTENANCE COSTS FOR SOFTWARE UPDATE (usually older version of the cores are not supported by vendors in newer versions of their SW, hence each IP shall be updated)**
- Hundreds of useful functions in a package

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CES MATH Library

CES MATH Library Modules

Part Number	Product Name
CES_M010	accumulator
CES_M020	adder_substractor
CES_M030	multiplier
CES_M040	divider
CES_M050	dB calculator
CES_M060	complex multipler
CES_M070	Pseudo random number generator
CES_M080	square_root
CES_M090	ALU
CES_M100	abs
CES_M110	Variance
CES_M120	Floating Point Unit
CES_M130	Standard Deviation
CES_M140	CORDIC

Key features

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- Hundreds of useful functions in a package
- Fixed point and floating point

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CES DSPeeD Library

CES DSPeeD Library Modules

Part Number	Product Name
CES_D010	Parallel FFT/IFFT
CES_D020	Serial FFT/IFFT
CES_D030	Mixed architecture FFT/IFFT
CES_D010_OPT 1	Real value input optimization, Input and output data ordering, 2D FFT support, Hyper length FFT
CES_D040	Windows generator: Chebichev, Hanning, Hamming, Rect, Cosine, Bartlett, Blackman, Gaussian, Kaiser
CES_D050	Waveform Generator (SIN/COS LUT)
CES_D060	Direct Digital Synthesis
CES_D070	cascaded biquad IIR (opt. array 1D and matrix 2D support)
CES_D080	FIR (opt. array 1D and matrix 2D support)
CES_D110	CIC Decimation, Interpolation Filter
CES_D120	Kalman Filter (optional Extended or Alpha-Beta Filter)
CES_D130	Digital Up/Down Converter

Key features

- Language; VHDL (1993-2002, 2008)
- Suitable to be used also in Safety and Mission critical applications (EN 61508, DO 254).
- Portable, vendor independent
- Fixed point and floating point (single or double precision) IEEE-Standard-754 compliant
- Each module is designed to serve a niche of ultra high performance applications with extreme requirements of data rate, resource usage , power and speed.
- Each library module has a fixed point and floating point implementation and can be validated to be used in safety critical applications.

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VIDEO PROCESSING Library

CES Image Processing Library Modules

Part Number	Product Name
CES_V010	Color scheme converters
CES_V020	RGB to HSV (or logHSV) Converter
CES_V030	Sobel Edge Detector
CES_V040	Canny Edge Detector
CES_V050	Median Filter
CES_V060	Blob Extraction
CES_V070	Component Connected Labelling
CES_V080	Object Recognition and tracking
CES_V090	Video tracker
CES_V100	Mahalanobis Distance Calculator
CES_V100	Digital Stabilisation

Key features

- Language; VHDL (1993-2002, 2008)
- Suitable to be used also in Safety and Mission critical applications (EN 61508, DO 254).
- Portable, vendor independent
- Real-time, low-latency computation, well-suited to high-performance object tracking.
- Up to 150 fps
- Up to 1080p
- Vendor independent ASIP cores, AXI4 and full Xilinx Zynq support

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CES RADAR Library

CES Radar/Sonar/Lidar Library Modules

Part Number	Product Name
	Waveform Generation: CW, FM, Barker, Linear Frequency Modulated CW, Non
CES_R010	Linear Frequency Modulated CW
CES_R020	IQ Calibration
CES_R030	Moving Target Processor Unit
CES_R040	Pulse Compressor Core
CES_R050	Pulse Doppler Processor
	2D Rectangular Array Space-Time
CES_R060	Adaptive Processing
CES_R070	Peak detection and spikes removal
CES_R080	Radar Detector Core
CES_R090	CFAR
	2D Rectangular Array RX/TX Digital Beam
CES_R100	Synthesis

Key features

- Language; VHDL (1993-2002, 2008)
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Partners

"Campera Electronic Systems collaborates with world leading companies within the FPGA market.
The Company has been developing a network of partners including FPGA vendors, design tool suppliers, equipment manufacturers and also other organizations world-wide."

Andrea Campera, CEO

Mentor Graphics

achronix SEMICONDUCTOR CORPORATION

MathWorks Partner

ALDEC THE DESIGN VERIFICATION COMPANY

TELEDYNE LECROY Everywhereyoulook™

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