Pixel Endcap
Type-0/Type-I Services

- Assumptions
- Why we have done what we have done
- Status of prototyping

v2: with bug fixes and a few additions from discussion

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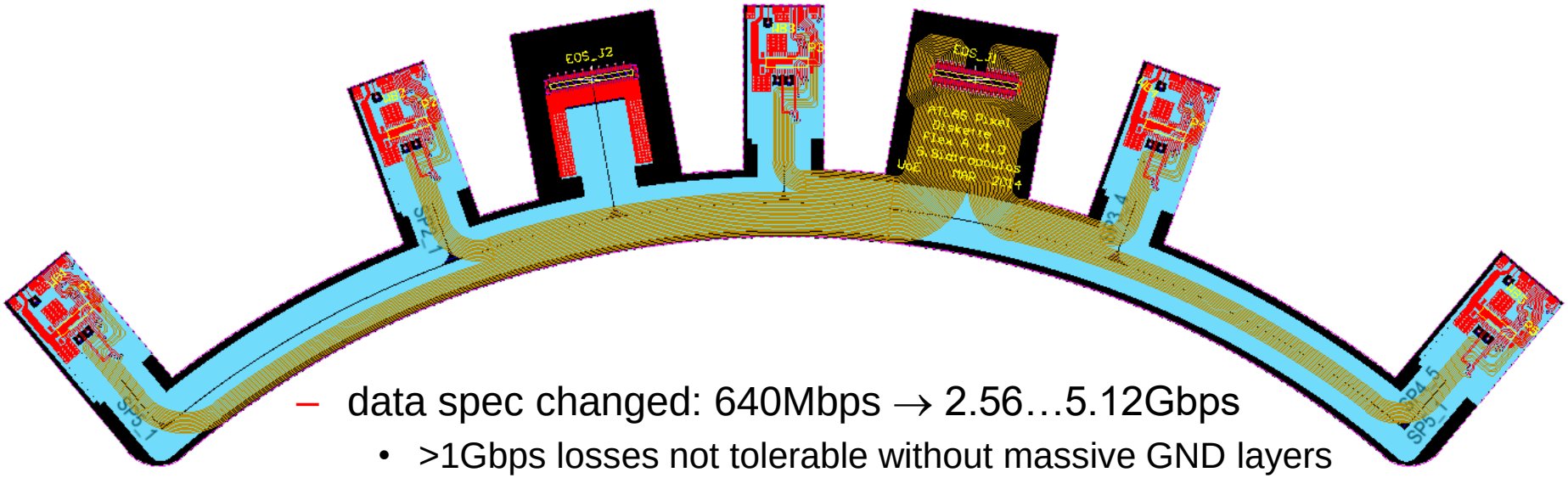
Type-0 Ring Flex Tapes

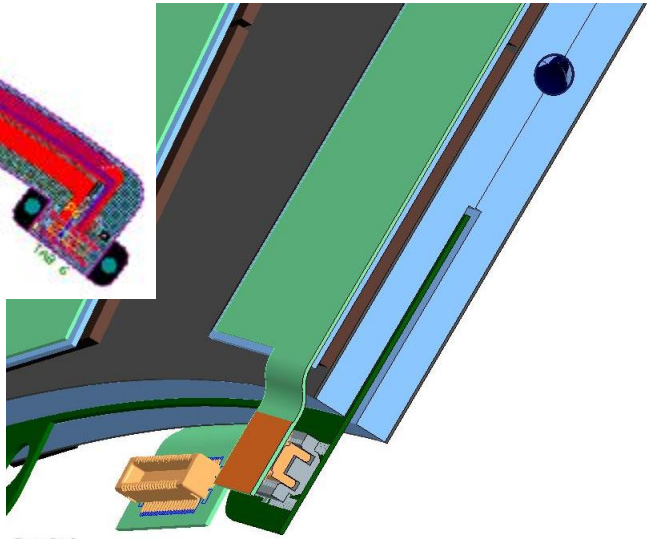
- 3 prototype generations:
  - v1: 2015, manufacturer: Flexible Technologies → ~OK quality
    - for inner ring prototype: LV (SP 6.4A), HV fan, data (640Mbps), Clk/Cmd (160Mbps)
    - 4-layer tape, supporting 5 quad-modules per tape, outward pointing tabs
    - Molex/Panasonic connectors (limited in current bearing → multiple pins for SP)
    - tabs with sacrificial extensions for bond pads
    - also used for (destructive) HV tests



  - data spec changed: 640Mbps → 2.56…5.12Gbps
    - >1Gbps losses not tolerable without massive GND layers
  - HV fan abandoned (no switching available)

Type-0 Ring Flex Tapes

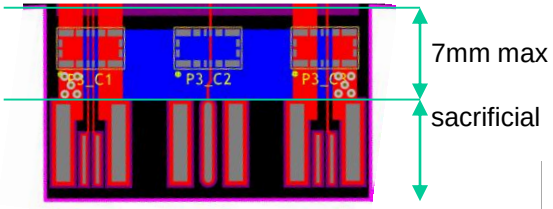
- 3 prototype generations:
  - v2: 2016, manufacturer: Zot → good quality
    - for middle ring prototype: LV (SP 8.0A), HV bus, Clk/Cmd, but no DCS yet
    - 4-layer tape, supporting 6 quad-modules per tape, inward pointing tabs
    - Molex/Panasonic connectors (limited in current bearing → multiple pins for SP)
    - with positioning holes on tabs, as alignment support for module mounting
    - design criterion: fit tabs with connectors into 9mm inner gab

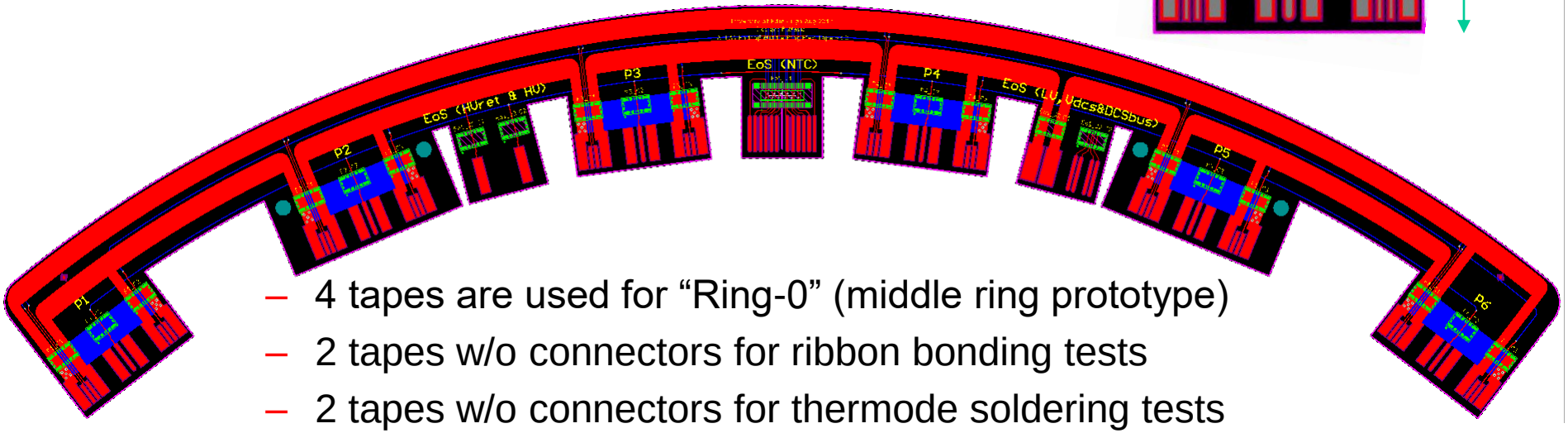


  - used for thermal middle ring prototype
  - Clk/Cmd spec changed: together with data, also taken off the module from the other side

Type-0 Ring Flex Tapes

- 3 prototype generations:
  - v3: 2017, manufacturer: Zot → good quality
    - for middle “Ring 0”: LV (SP 8.0A), HV bus, NTC, DCS bus, but no PSPP yet
    - 2-layer tape, supporting 6 quad-modules per tape, 4 tapes per half-ring
    - provision for interconnection trials: assuming 7mm inner gap space
      - ribbon bonding
      - BM25 connectors (10A rated)
      - thermode soldering (on sacrificial extensions)



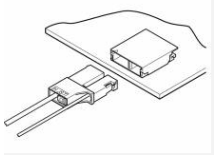


  - 4 tapes are used for “Ring-0” (middle ring prototype)
  - 2 tapes w/o connectors for ribbon bonding tests
  - 2 tapes w/o connectors for thermode soldering tests
  - 1 tape w/o connectors sent to Genova, 1 kept at Edinburgh

"Ring 0": Type-0 EoS Cards

- For this implementation (v3):
  - simple feed through cards will be used
  - there is no DCS bus on the tape
  - HV and HV-return (at the request of module flex designer)
- Connectors for the outer edge of the EoS cards:
  - low profile chosen
  - may change before the final design

JST – BH series
SM02(8.0)B-BHS-1-TB



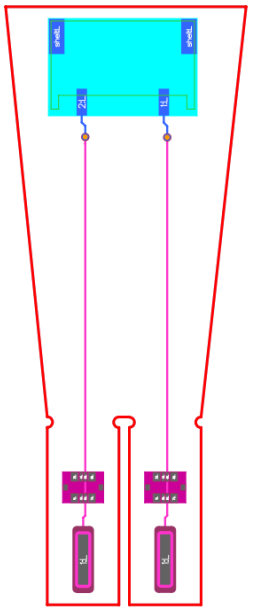
Mike Perry

Molex
5040501291

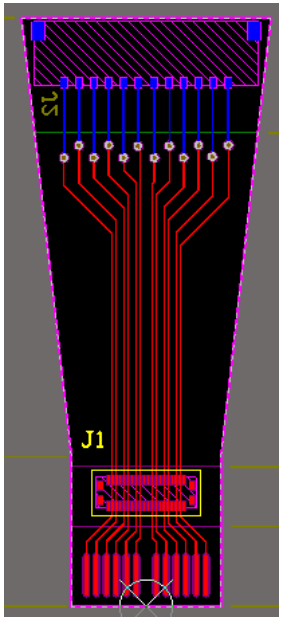
Jim Stuart

Molex
5040500891

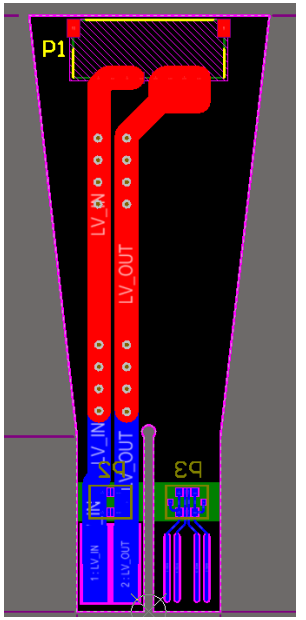
Graham Miller



HV EoS



NTC EoS



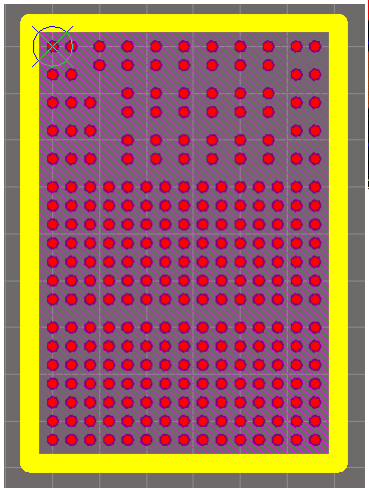
SP & DCS EoS V2

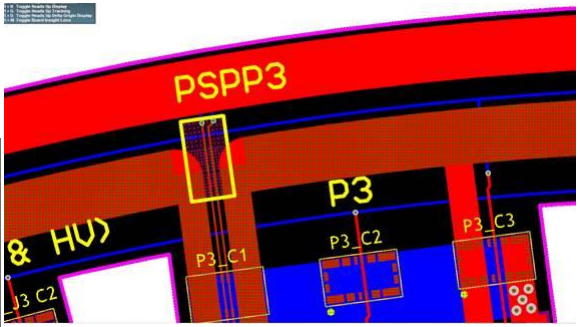
The ring flex J2 and J3 connectors are Hirose BM25 header part number BM25-4P/2-V(53).
The Eos J1 connector is Molex 55909-0474.

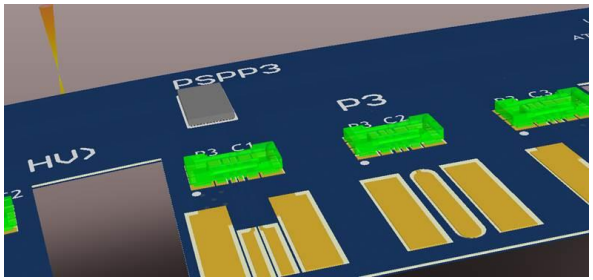
Studies

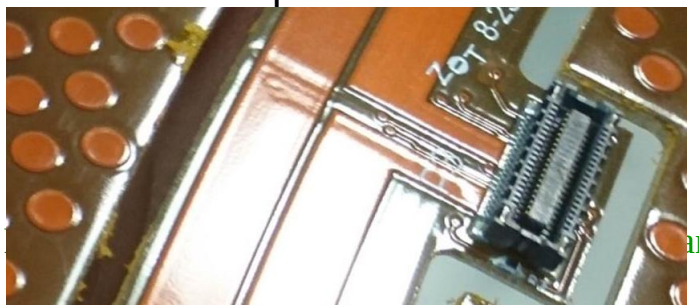
- PSPP placement:
  - for best functionality: on flex tape
  - pros:
    - best protection (bridges module connection)
    - easiest access to DCS bus
  - cons:
    - needs cavern in foam, large than PSPP package, due to peripheral circuitry
    - cavern obstructs thermal path for heat from modules
    - uneven flex tape surface

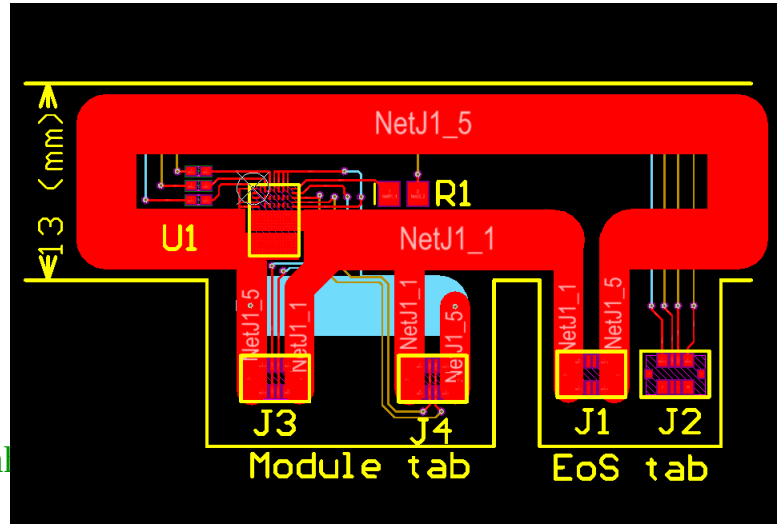
PSPP3
BGA footprint





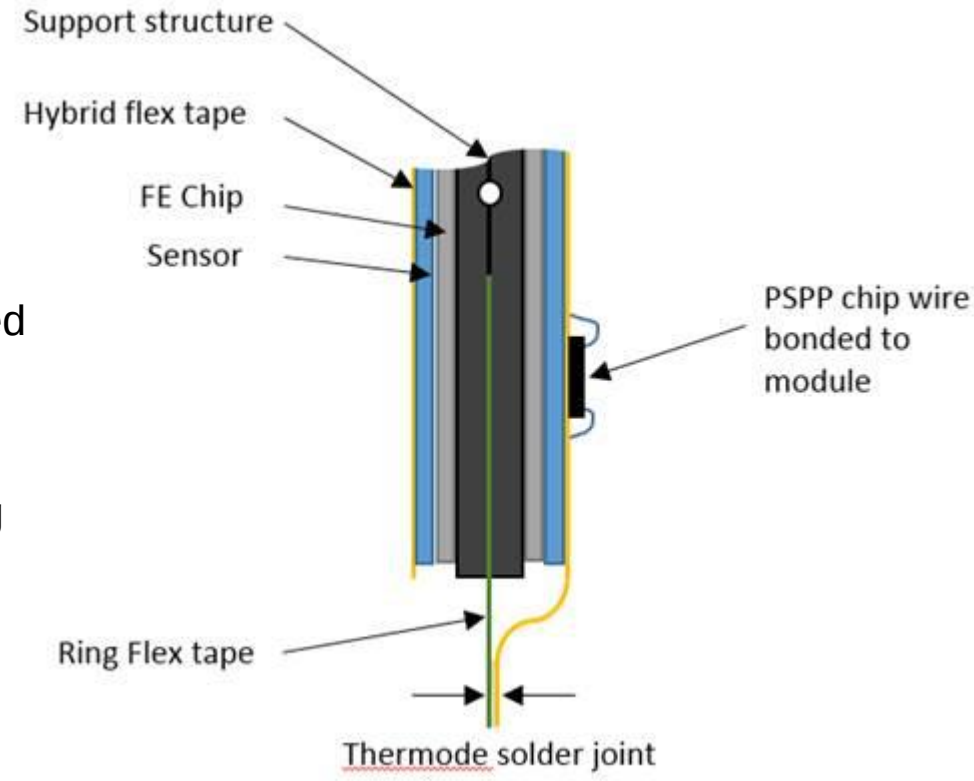






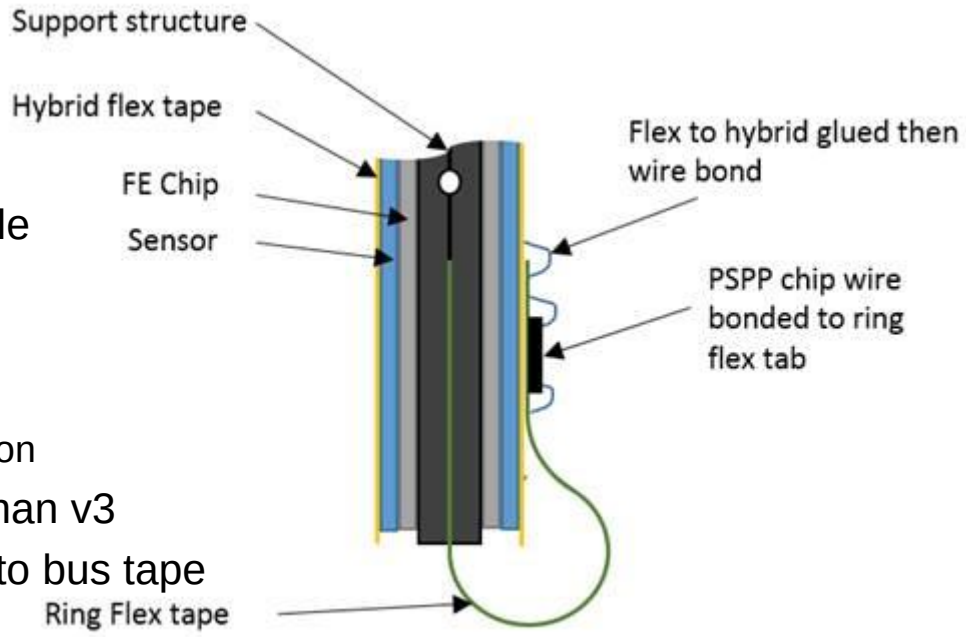
Studies

- PSPP placement:
  - to avoid cavity problem: on module
  - pros:
    - thermal path for modules not blocked by cavity/PSPP chip
    - cooling of PSPP provided via module
    - relatively simple flex tape design
    - PSPP can be wire or bump bonded
    - ring assembly simpler
  - cons:
    - thermode soldering needs proving and be deemed reliable
    - needs real estate on module
    - module assembly more complicated
    - adds heat source to module
    - flex tape design may run into problems for only 2-layers



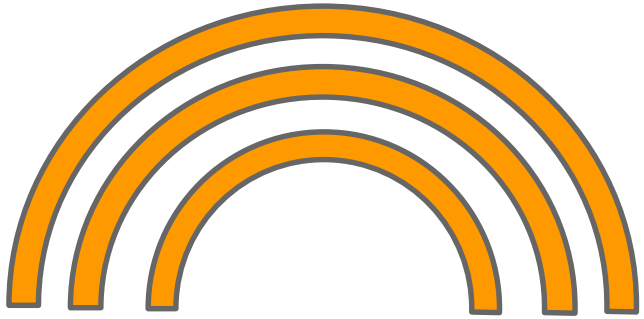
Studies

- PSPP placement:
  - to avoid cavity problem & protect connection to module: on extended tab
  - pros:
    - thermal path for modules not blocked by cavity/PSPP chip
    - connection to module protected
    - cooling of PSPP provided via module
  - cons:
    - needs large real estate on module
    - complex manufacture
      - glue ring tab to module
      - glue & wire bond PSPP
      - wire bond flex-module connection
    - flex tape more complex design than v3
    - thermal path more resistive due to bus tape
    - very poor re-workability



Studies

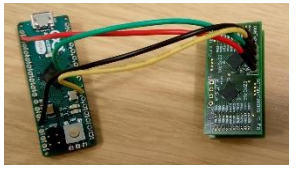
- Unsolved issue: manufacturer for largest flex tape sheet size
  - Zot: max sizes
    - PCB: 574mm x 416mm
    - vapour phase reflow: 500mm x 400mm
  - this does not match the dimensions needed for the outer rings:
    - outer: ~= 590mm x 295mm – problem
    - middle: ~= 465mm x 233mm – OK
    - inner: ~= 340mm x 170mm – OK

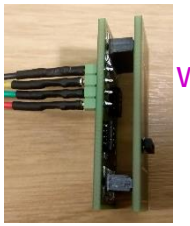


  - only 1 in 4 requested quotations so far yielded a reasonable result:
    - Q-Flex (recommended by Italian Team ENDCAP) — Quote received (USA manufacture) (max 734mm x 367mm, cost similar to Zot)
    - Alta-Flex (recommended by Italian Team ENDCAP) — No response (USA manufacture)
    - Fineline (recommended by Sébastien VILALTE) — No quote received (China manufacture)
    - Elgoline – (recommended by Vladimir Cindro) — TBD, no feedback (Solvenia manufacture)

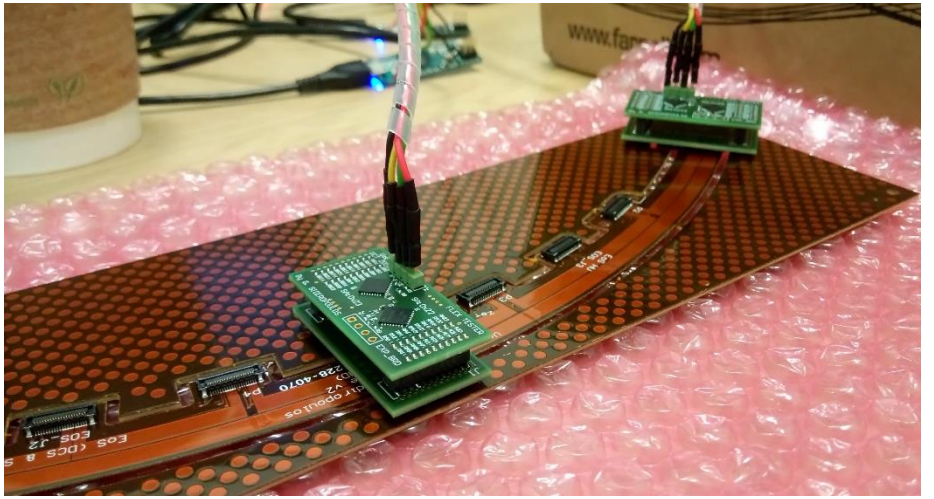
Studies

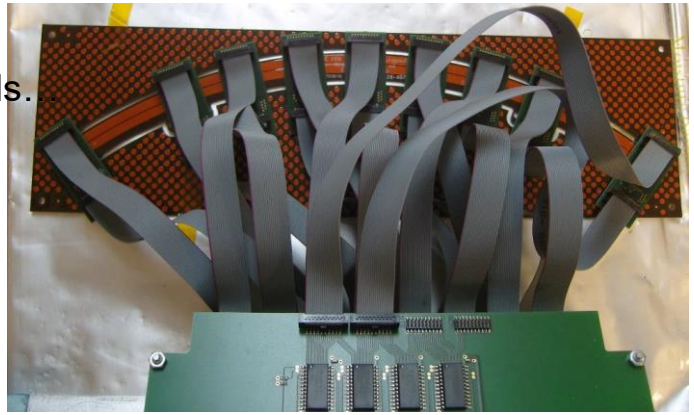
- Flex tape Quality Control:
  - test: network for shorts and breaks
  - first attempt:
    - Raspberry Pi, I2C port expanders
    - use interface PCBs which can be thrown away after X mating cycles
    - nice & neat, but too slow
  - second system:
    - build from a more capable controller
    - can handle multi connector assembly with 384 test points
    - USB interface, user interface in Vee also can be LabView, C++ or MatLab
    - can learn setup:
      first test a known good tape & record network layout
      then compare unknown tapes… test & report takes seconds…





I2C expander with expendable interface PCB

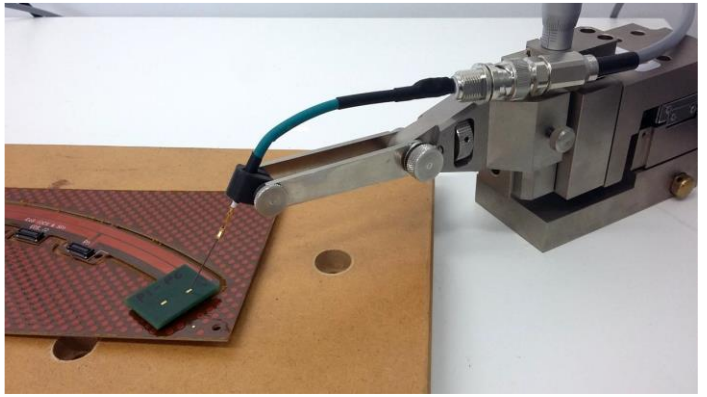




Studies

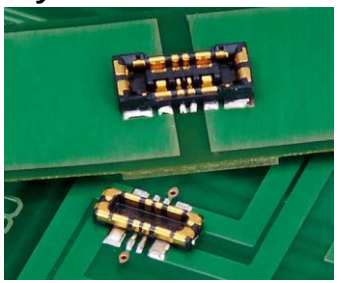
- HV Quality Assurance:
  - tested breakdown
    - where: at pads, through air
    - HV level: dependent on spacing and air condition
    - test flex with uncovered tracks tested up to 3kV
    - discharges started between 1.3kV and 2.5kV

- HV Quality Control:
  - use Keithley 237 HV SMU to measure LC
  - GΩ resistance through glue layer
  - triax cables & custom made probes yield noise floor of 19 pA
  - custom made interface PCBs to provide probe pads increase noise floor to 26pA
  - measured 100-300 pA LC @ 1V depending on track length, for flex tape v2 scaling to 100-300 nA @ 1000

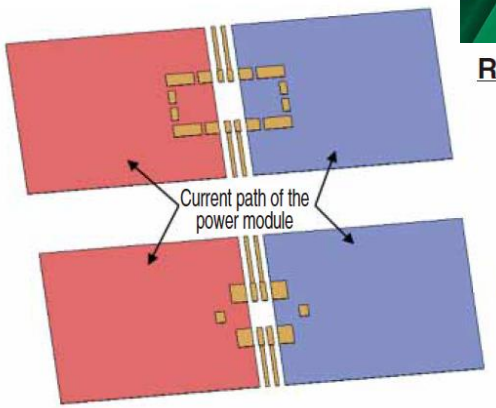


Studies

- Power dissipation on Flex tape:
  - v3 design goal: <2.5W with worst case 7.4A for 13-module tape
    - traces: 70μm copper for top layer (SP) and 35μm copper for bottom layer
    - 2 SP I/O per module, for better load balancing on module hybrid
    - loop through 27 connectors (2/module + 1/EoS): Hirose BM25
  - BM25 study:
    - recommended test board layout
    - multiple insertions & measurements:



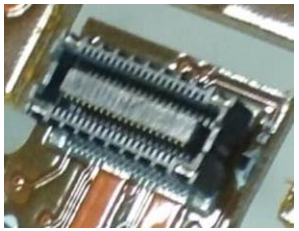
Receptacle board



Header board

Insertions	Resistance
1	0.7 mΩ
5	0.7 mΩ
10	0.8 mΩ
20	0.9 mΩ
25	1.3 mΩ → signs of deterioration

  - For comparison: previously used Molex connector measured 6 mΩ
    - Serial power loop resistance: flex tape v3: 45 mΩ
      v2: 125 mΩ

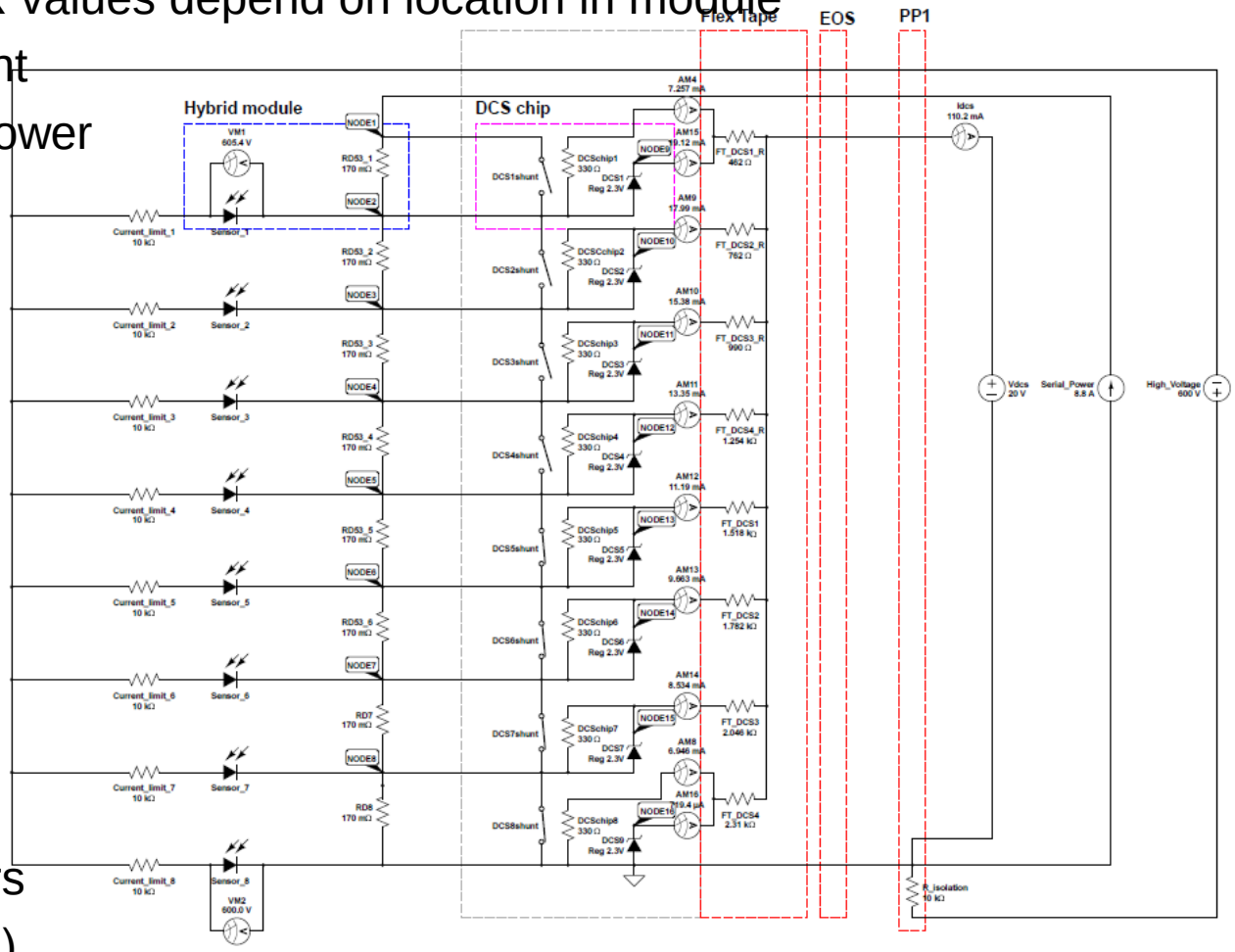


Studies

- Power dissipation: Type-0 & Type-I combined
  - its all about cross-section and material (the latter can vary from manufacturer to manufacturer…)
  - Jim demonstrated that it is possible to have a *combined* power dissipation in the region of ~10% (specification requires individual dissipation <10%, i.e. combined <20%)
  - 10% combined can be achieved using 35μm double sided flex tapes for SP & either 21AWG (∅=0.723mm) copper or 19AWG (∅=0.912mm) aluminium wires
  - but we need to use maximum SP-chain lengths (13 modules on outer ring), if we would have to split SP-chains, this adds more mass (cables…) and O(2%) power dissipation per additional split (more chains…)
  - while aluminium is the preferred material to have less dense mass distributions in the detector volume, we learned that it cannot be crimped (induced stresses let the cables easily break just behind the crimp) – so Al is out…

Studies

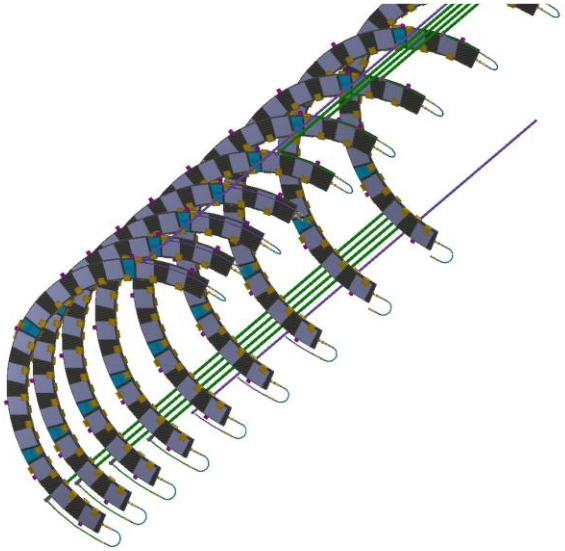
- Reminder: the issue with the local GND adjustment resistors in the SP chain
  - DCS system: needs R values depend on location in module
  - draw significant current
  - → dissipate significant power
  - worst case:
    SP off & DCS on
  - dissipation up to 1W
  - R have to be rated
    for worst case
  - if one R blows the
    whole chain is lost
  - this needs big resistors
    (in area and volume…)

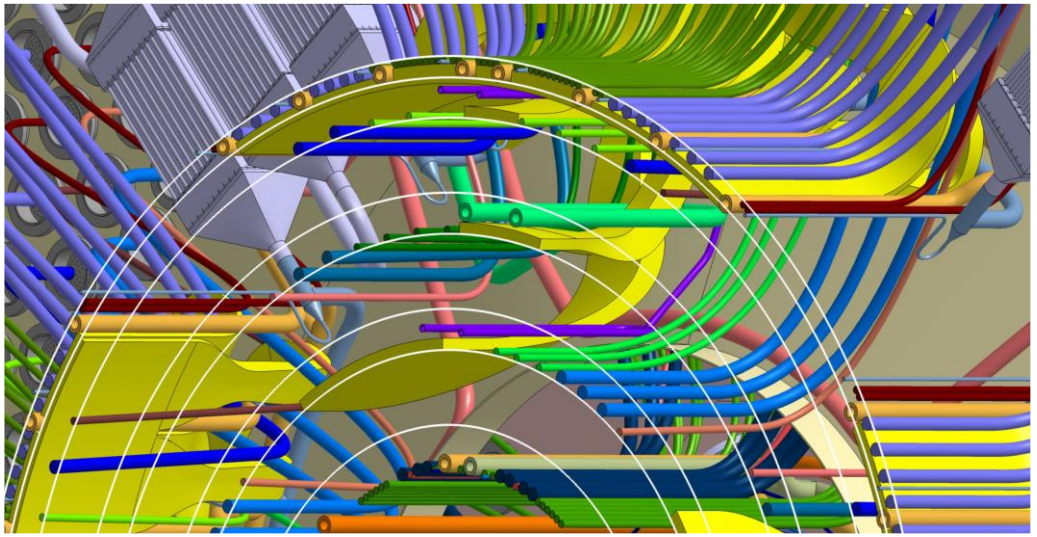


Type-I Services

- Desired routing principles:
  - while Jim's routing studies from October 2017 are outdated…
  - … his principles still should be adhered to:
- We need to:
  - be able to plan, manufacture, test, assemble & survey the interconnection

from here (EoS, agrregator) to here (PP1)



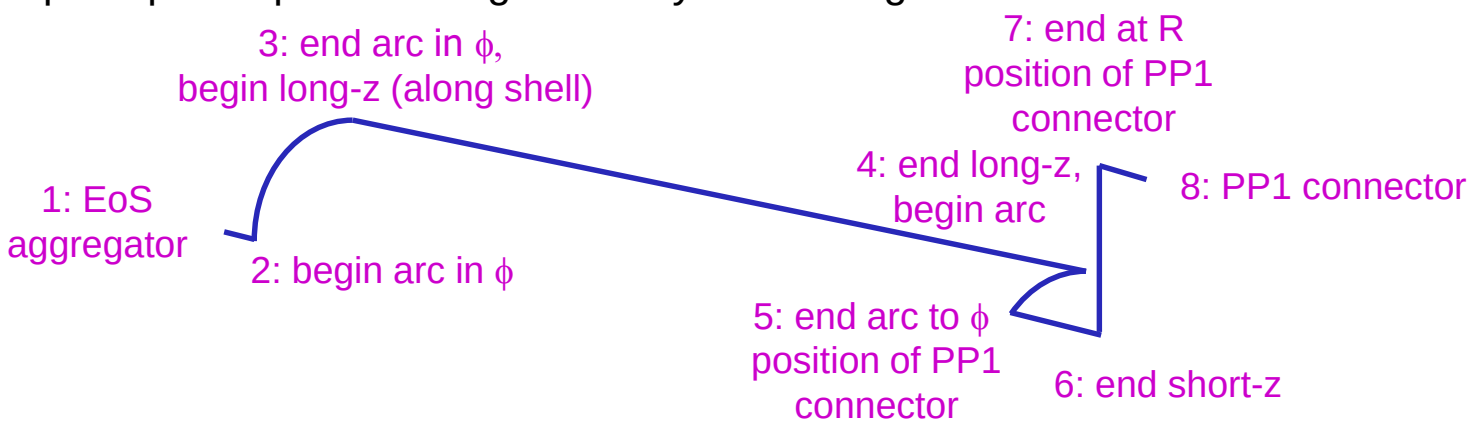


Type-I Services

- Type-I Harness goals:
  - separate branches of the cable tree of one half-endcap as much as possible:
    - to have subsections, which can be assembled, tested and installed independently
    - to least complex intertwining between branches
  - dis-entangling the cables running form PP1 to PP2:
    - three types of PP1 connectors:
      - LV (includes DCS, Tinterlock)
      - HV
      - Clk/Cmd
    - between PP1 and PP2 they run in different paths & to different end-points
    - Clk/Cmd: run parallel to data to optoboxes
    - these should already be separated in Type-I services, otherwise we have spaghetti in the endcap…
  - maximise SP-chain length:
    - this minimises the cable count (mass, cross section)
    - this minimises the number of PP1 connectors needed
    - … makes all aspects of the job for the Type-I services easier…

Type-I Services

- Next steps:
  - build a (big!) spread sheet of space points:
    linking (pin-for-pin) all input and output points
    - inputs: EoS cards, aggregator/active cable connectors
    - output: PP1 plugs, opto-box equalizer/lpGBT
    - need 8 space points per line for generic lay out routing to PP1:



    - for routing to opto-box more steps are needed (how many?)
      - all data cables have to be of same length, i.e. they need space below opto-boxes to curl up
    - refine later with factors to account curvatures
    - maybe also start first with generic connector space points and only later refine to pin space points

Type-I Services

- Next steps (continued):
  - derive cable lengths & masses
  - assign PP1 connectors / pin positions
  - group into harnesses
  - identify/resolve clashes/complications
  - develop QC procedures
- Further jobs:
  - understand cable shrinking at cool-down & develop model to allow for cable movement due to shrinking
  - … that needs to be solved together with the mounting/attachment of the services inside the end-cap
  - bending tests for cable types
  - understand cable movements (e.g. due to mag. field and power cycles, …)
  - evaluate TPI-coated (LV & DCS) services
    - gain in used cross-section
    - cost differential to cables with rad-hard flexible insulation
    - getting handling of cable stripping and connector assembly under control
    - evaluate risk of damage to coating during manufacture, handling, assembly, …
  - evaluate split between commercial and in-house production

Type-I Services

- Mock-up:
  - who builds the first mock-up, where and when?
    - first mock-up probably for middle layer (matching current prototype rings)
    - use that to test
      - wiggling of cables
      - clip options and positions
      - 1mm move of pipes during cool-down:
        - » see where they can slide best
        - » hopefully U-bend is sufficient
  - clips to mount (sub-)harnesses in CF half-cylinders:
    - no through-hole attachment to half-cylinders, only glue
    - how to deal with differential shrinking at cool down:
      - what are the changes in lengths for different materials? (O(1mm)?)
      - where to put fix points and where to allow for sliding/slipping?
      - prevent stress to EoS (& PP1) connectors
    - movement/wiggling of cables between clip positions
      - how much is allowed
      - how many clip positions are needed

Type-I Services

- Jigging:
  - need to design jigs to mount cable sub-harnesses as in half-cylinders:
    - which tolerances does it have to have?
    - how to (temporarily) mount sub-harnesses?
    - who will design/build these jigs?
    - mounting sequence has to be developed and needs to account for:
      - entangling of lines around half-rings
      - routing around cooling pipes
      - transfer sequence to CF half cylinders
  - assumptions:
    - there will be sets of jigs for electrical services (LV, HV, clk/cmd, data)
    - min. 3 sets per endcap (one per layer)
    - A&C sides of endcap have 1cm shift in ring position: if we cannot absorb that with intelligent jig design we would have 6 jigs per encap…
    - design should be common for UK & It Endcap
    - cooling pipe work will have their own jigging, as they will be mounted to the half-shells first

Spare Slides