DAQ for End Cap Integration

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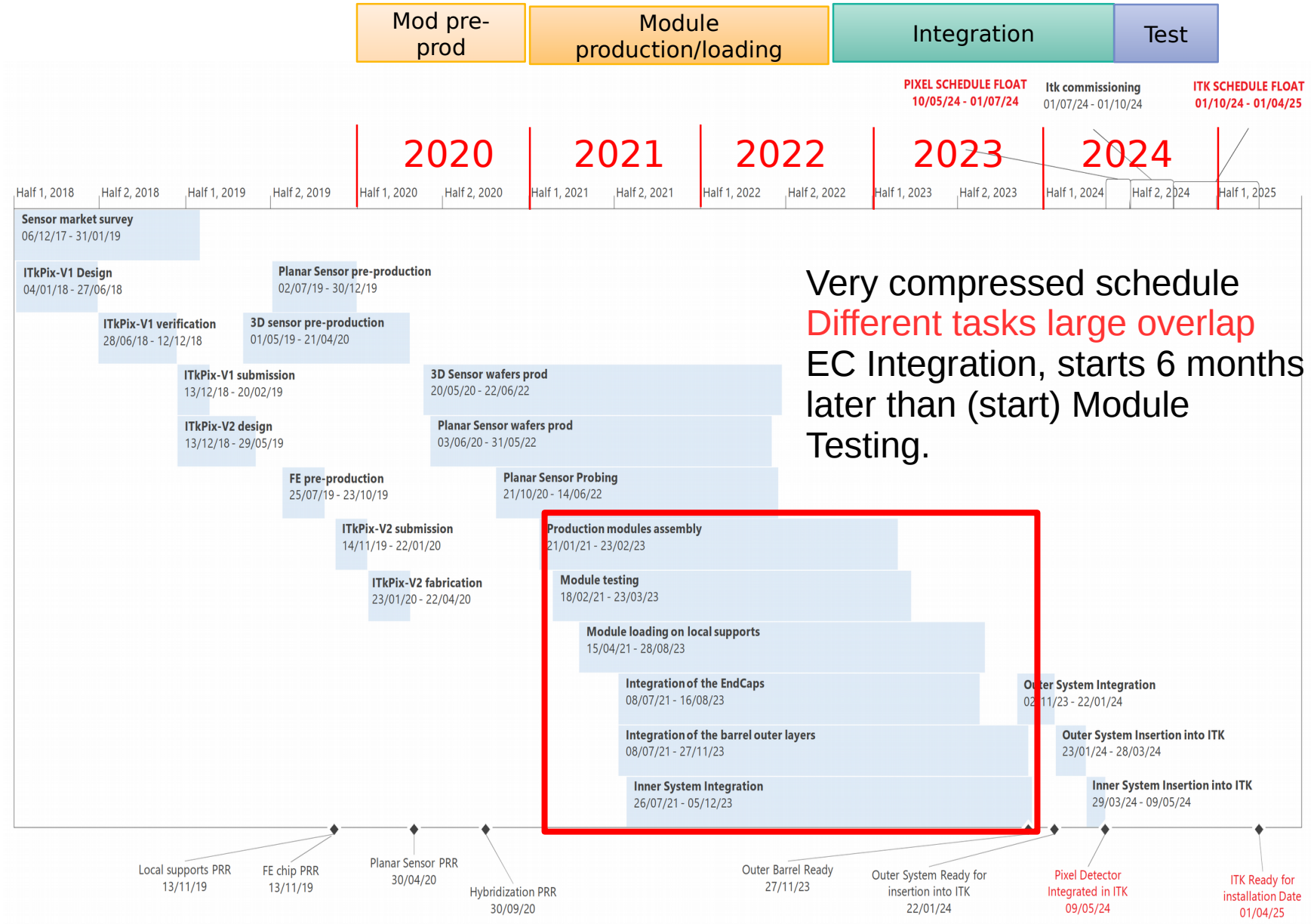
Questions

Not expecting to answer them today → Initiate the discussion

- Understand which are the requests on DAQ during integration of the EndCap
  - How many modules should me readout concurrently?
  - Which rate to expect?
  - Connections?
  - Which tests to perform?
- Which DAQ system should be used?
  - What is available today? And during integration?

Short review of DAQ and Readout (mainly from Pixel TDR)

Pixel schedule



Very compressed schedule

Different tasks large overlap

EC Integration, starts 6 months later than (start) Module Testing.

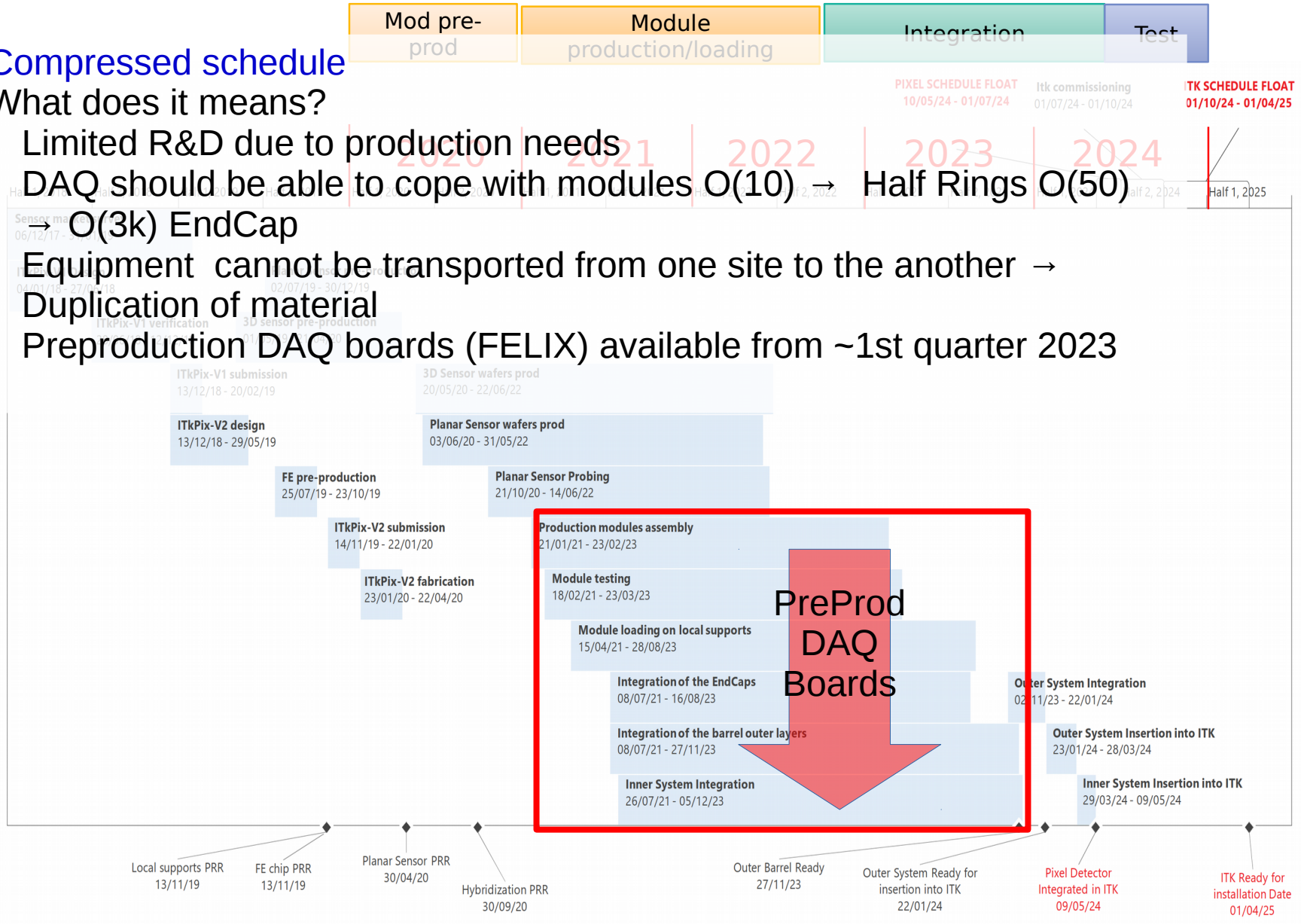
From P. Morettini last ITk IB presentation https://indico.cern.ch/event/704355/

Pixel schedule

Compressed schedule

What does it means?

- Limited R&D due to production needs
- DAQ should be able to cope with modules O(10) → Half Rings O(50) → O(3k) EndCap
- Equipment cannot be transported from one site to the another → Duplication of material
- Preproduction DAQ boards (FELIX) available from ~1st quarter 2023



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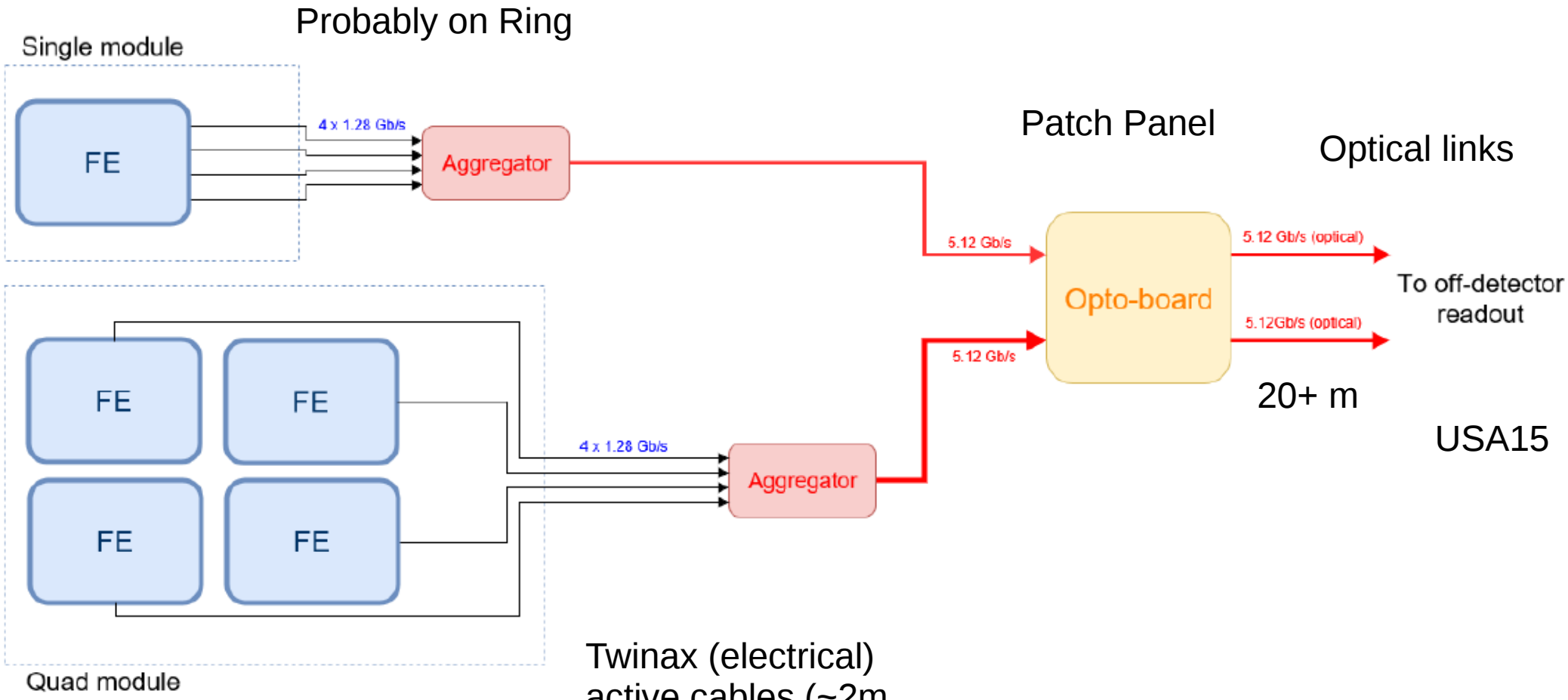
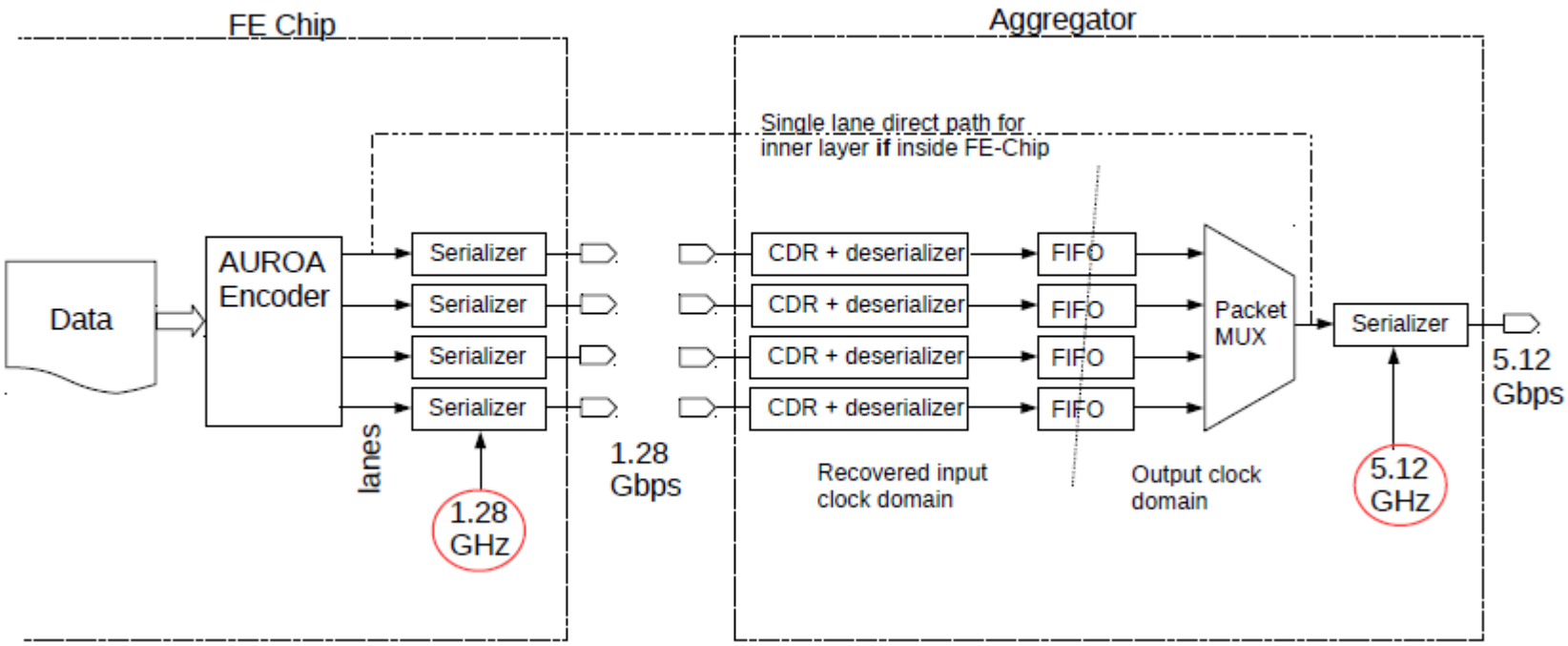
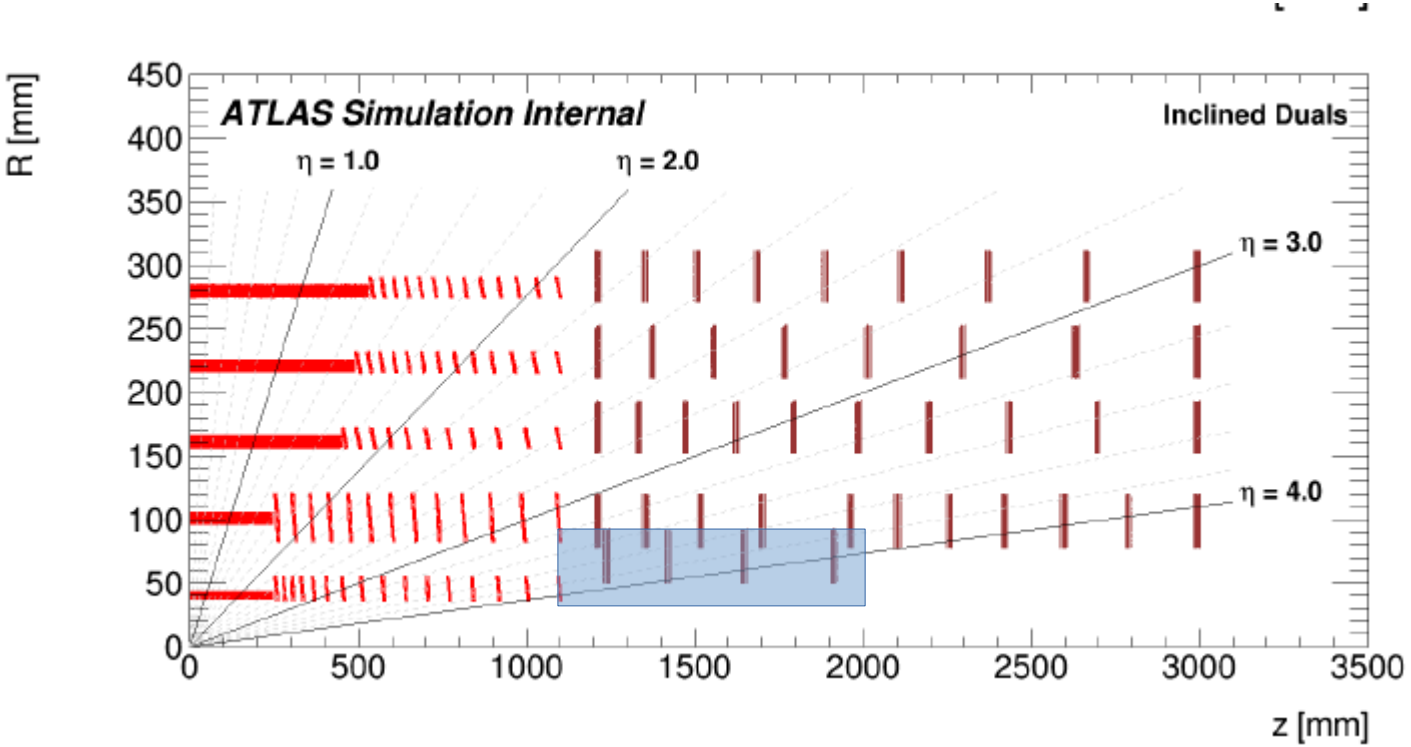
DAQ Chain


Probably on Ring
Single module
FE
4 x 1.28 Gb/s
Aggregator
Patch Panel
Optical links
5.12 Gb/s
Opto-board
5.12 Gb/s (optical)
To off-detector readout
5.12Gb/s (optical)
5.12 Gb/s
20+ m
USA15
FE
FE
FE
FE
4 x 1.28 Gb/s
Aggregator
Quad module
Twinax (electrical) active cables (~2m long for smaller z rings)
From Pixel TDR

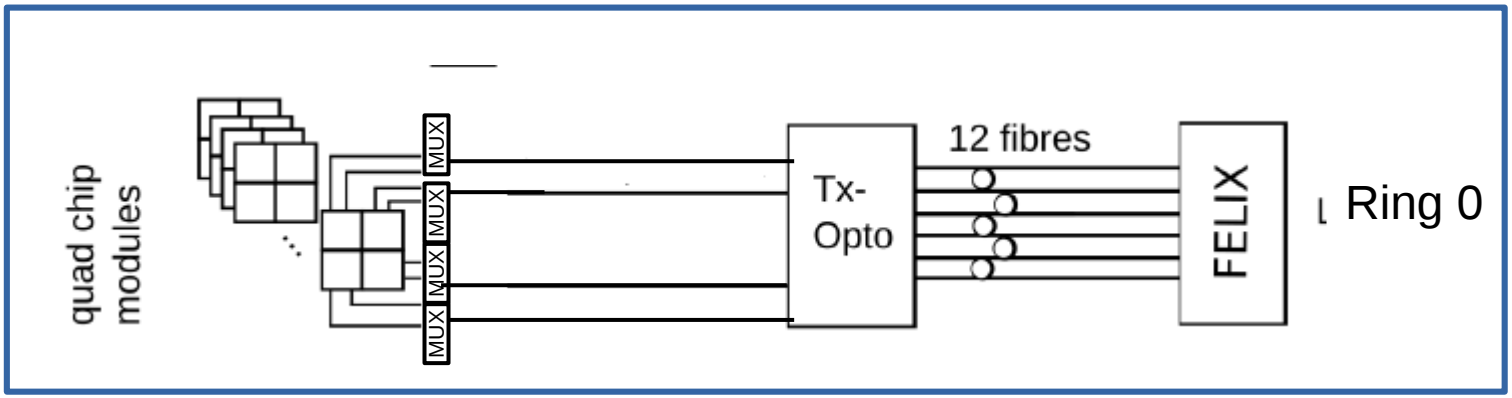
FE – Aggregator



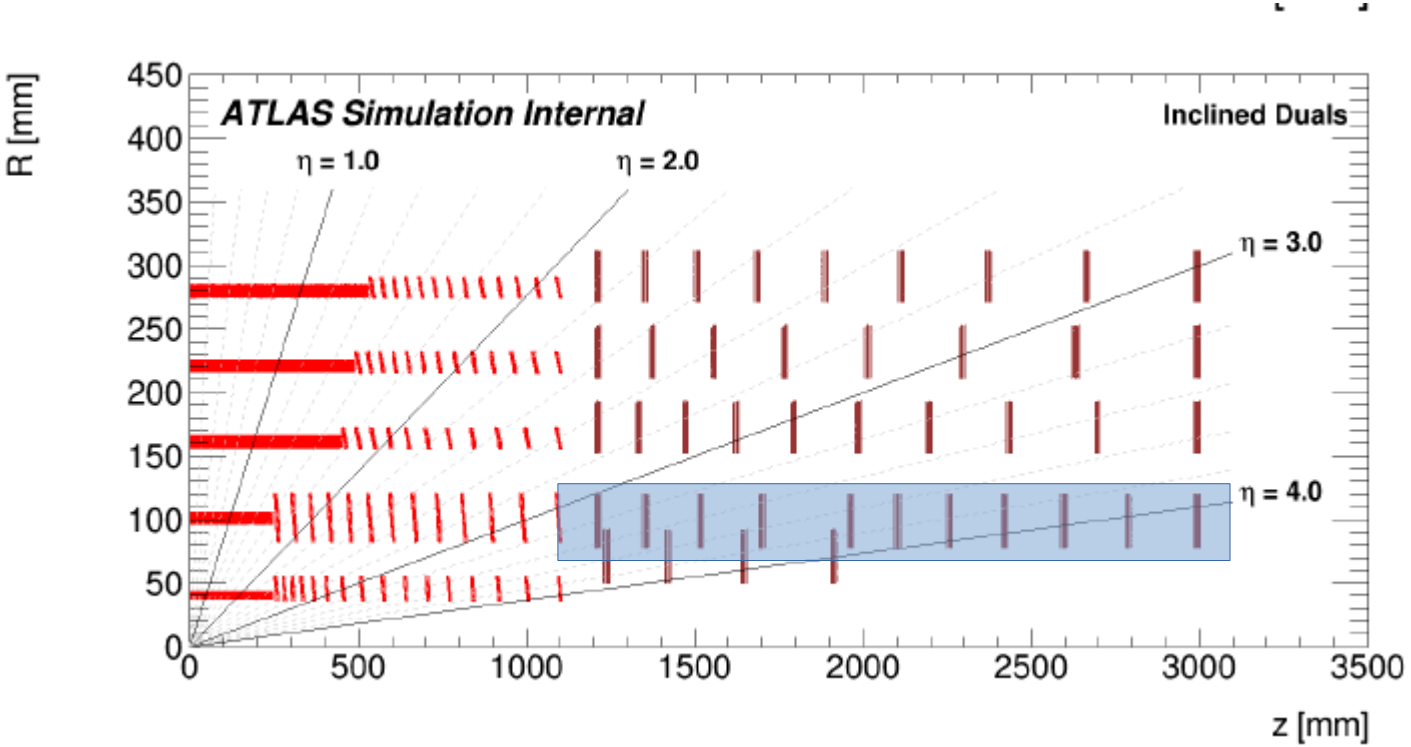
Aggregator chip from Pixel TDR
Input 4 lanes (1.28 Gbps) from FE → Ouput 5,12 Gbps electrical connection

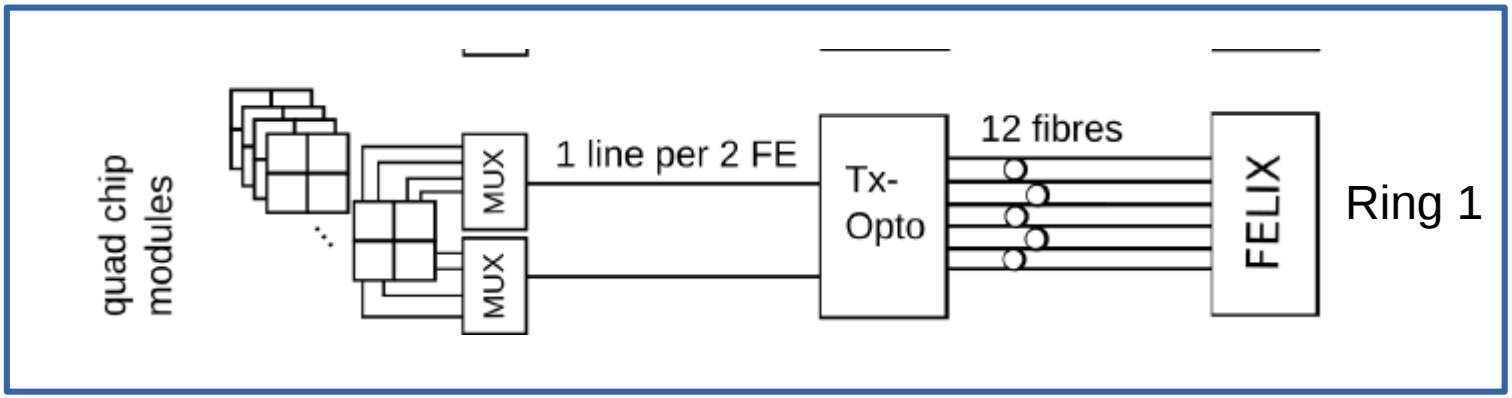


Showing connections in case L0 accept @1 MHz

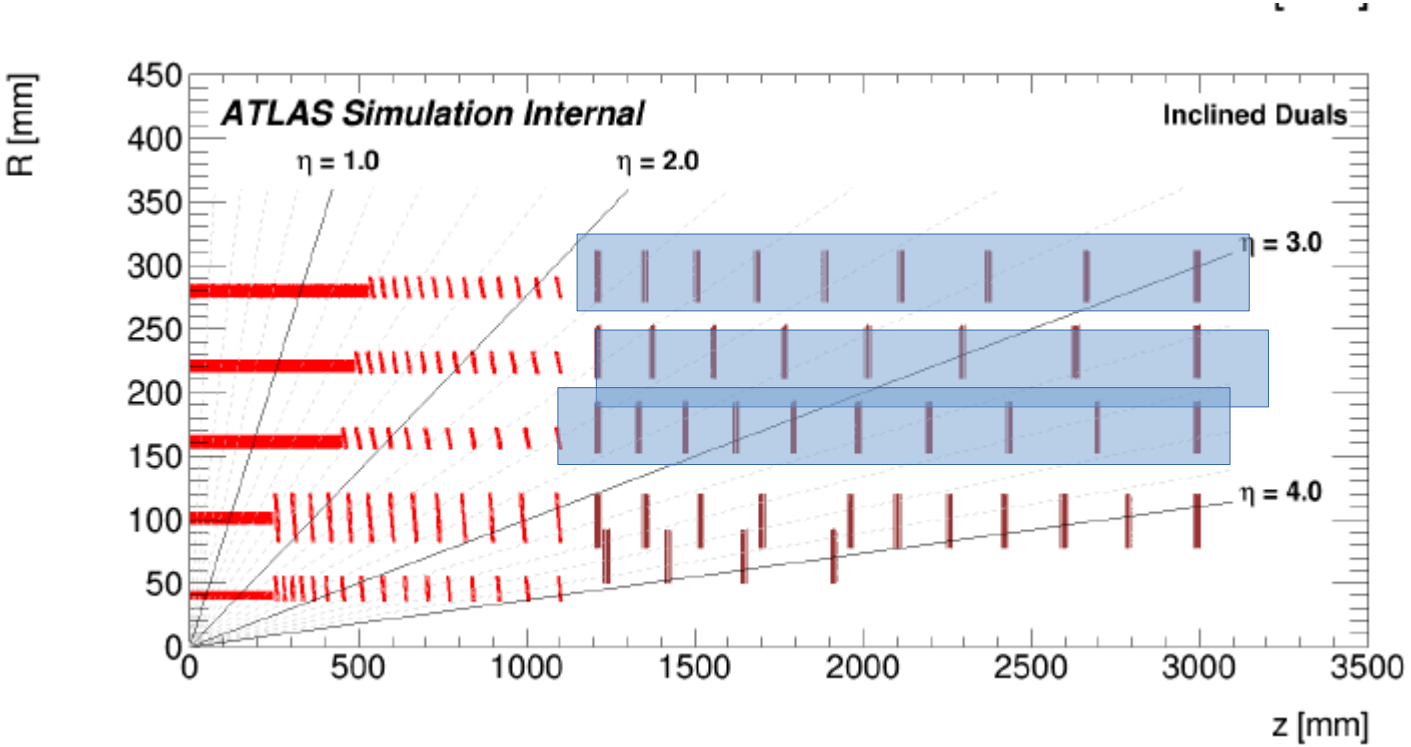


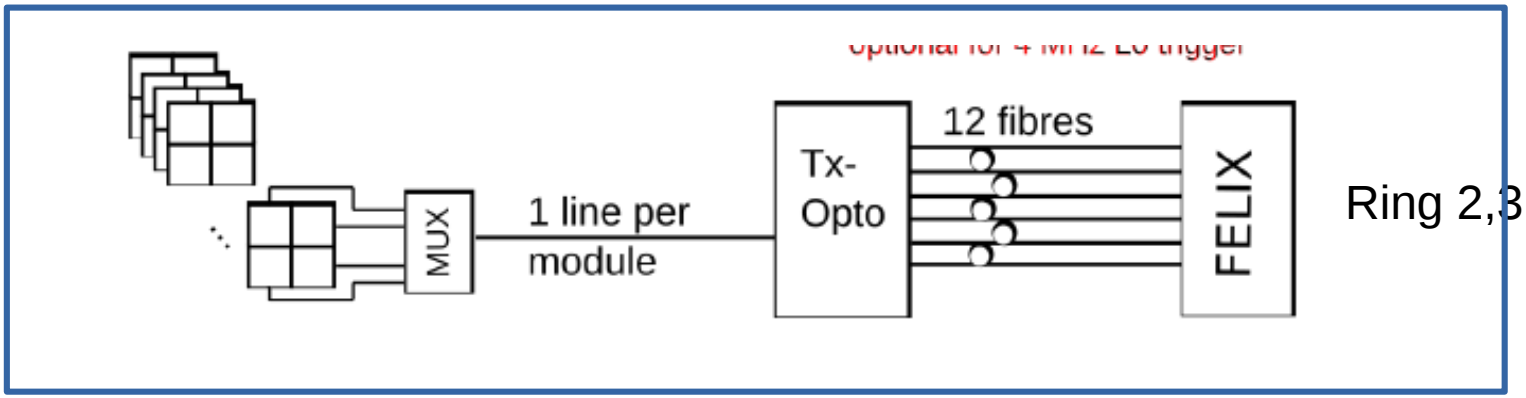
From Pixel TDR





From Pixel TDR





Ring 2,3,4

From Pixel TDR

For a L0 @ 4 MHz Ring 2 → Ring 0
Ring 3 → Ring 1

L0 @4 MHz implies different data connections

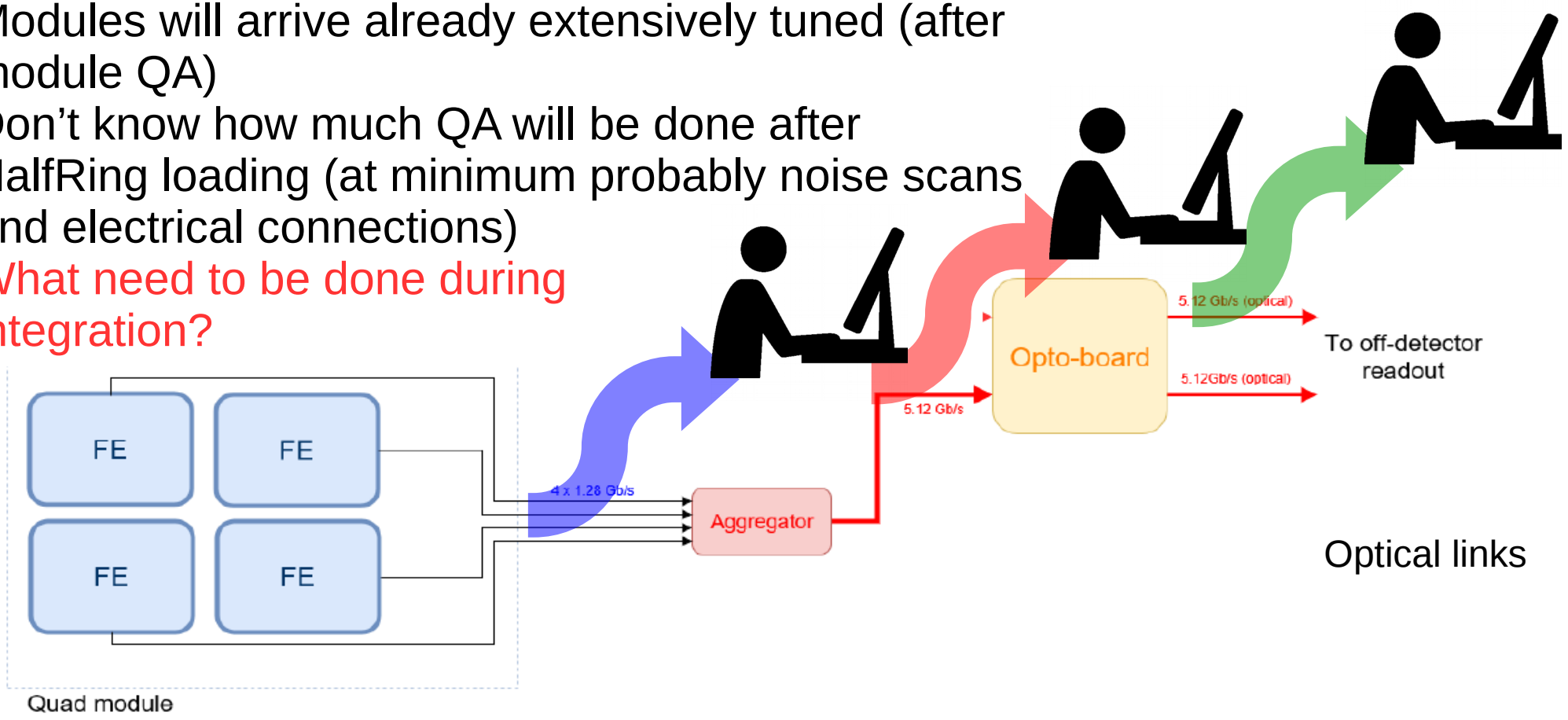
Where to readout during tests?

- Before the aggregator (if not performed during Half Ring loading QA)
- After aggregator (i.e. after mounting single HR) → electrical connection → mezzanine

alternatively optical if ad hoc optical tranceiver implemented

- After optoboard → optical connection → could use “final” system

Modules will arrive already extensively tuned (after module QA)
Don’t know how much QA will be done after HalfRing loading (at minimum probably noise scans and electrical connections)
What need to be done during integration?



Rate exercise

Standard X-Ray tube → Rate 2.10^5 per cm^2 per s @ 10cm
2.21 10^6 counts on single module @ 6 cm
Using 64/66b data stream 66b → 2 x 4-pix regions
One hit → 2.5 4-pix regions
→ 360Mb/s per single module
→ 1.47 Gb/s per quad module

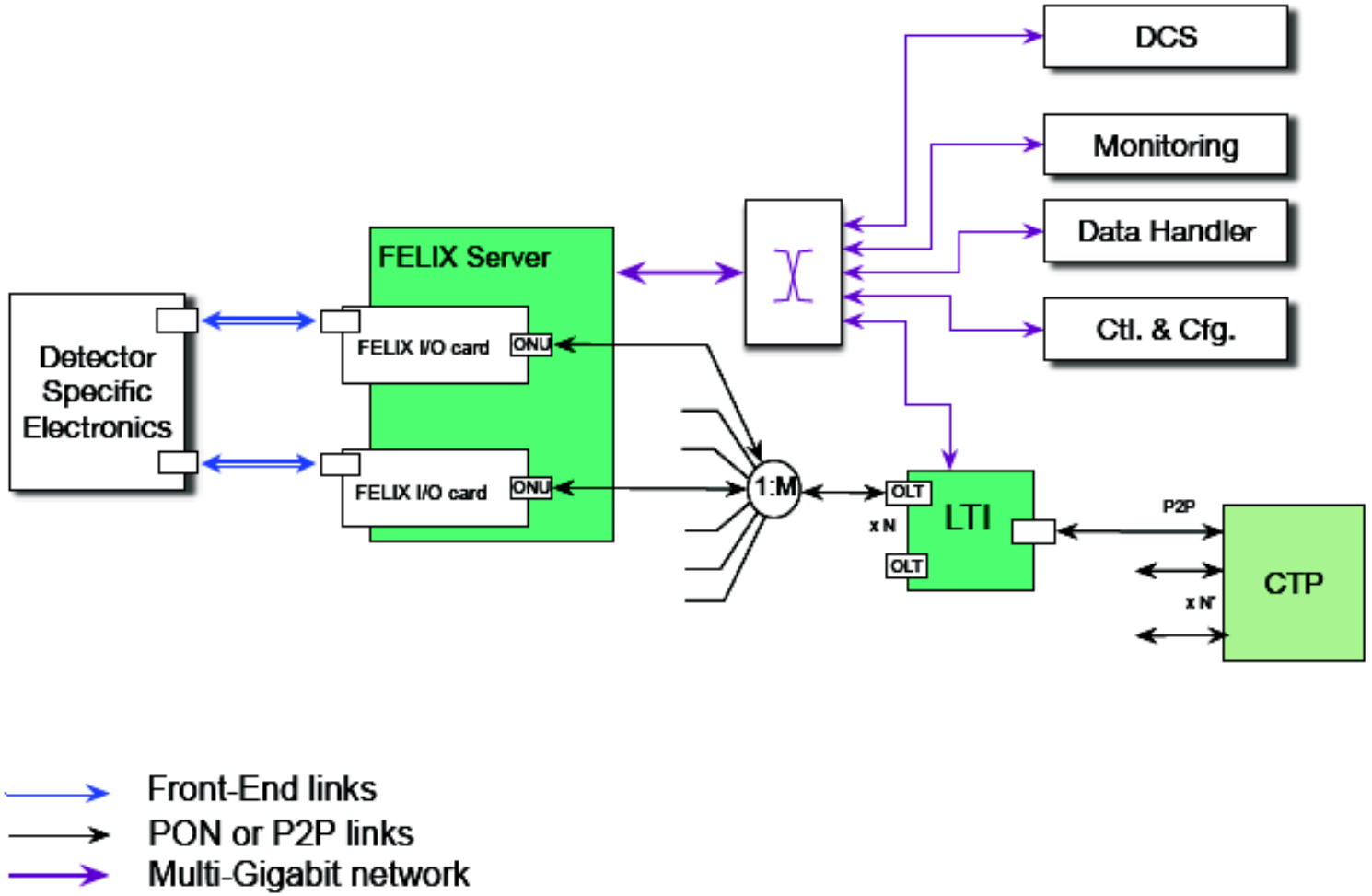
Note: This is for an X-ray tube that will be probably used during Module QA
→ Expect much smaller rates

Cooling power to cool down 10% of EndCap (@LNF)
→ probably 4~6 rings (depending on the layer)
→ 64 to 260 Modules
→ 256 FE to ~1000 FE
Possibility ro run FE in low powering mode?
Power dissipated? → number of rings concurrently tested could increase (may be double?)

Different systems available

Name of the systems	I/O	Total Bandwith (GBps)	#FE Chips	
USBPix3	2 MGT	>2	1 or 2	Used for IBL module QA
YARR (XPressK7)	8 GTX	12.5	4(?)	RD53
RCE (HSIO2)	1 lpGBT (optical)	5.12	Bandwidth limited	TB, AFP, demo
BDAQ53 (Bonn)	8 MGT	>8	4	RD53
Mini-Felix (VC-709)	4 lpGBT (optical)	20	Bandwidth limited	demo,
Felix Phase2 preproduction (beginning 2023)	24/48 lpGBT (optical)	~1k	Bandwidth limited	Final ?

Felix Phase 2



Pro and Cons of systems

Very personal (partial/wrong/biased view) ….
YARR, VC709 (Mini Felix) and RCE (HSIO2) are being used in various TB, demonstrators (UK, Wuppertal hands-on, SR1)
USBPix used in Module QA of IBL

USBPix and YARR:
Pros: Used for IBL (USBPix), used during testbeams, plug and play, ~~relatively easy to get a board~~ (YARR)
Cons: Not many modules can be tested concurrently (4?), different from the “final” system
With YARR it seems to be possible to test more modules (how many?)
However scalabilty issues for YARR too
VC 709:
Pros: In the FELIX TDAQ project → Firmware development carried out by TDAQ team.
Very small FW devlopment specific to ITk
Possibility to use the “same framework” for modules QA, loading and integration (and final system) →Same DAQ architecture used in operation
→ Boards will change, FW will evolve, but SW should be transparent
optical input
Cons: Slightly more expensive than YARR (~x2.5), still to demonstrate “plug and play”

RCE HSIO2:
Pros: Used already in TB → optical input
Cons: Different SW than what will be used in Run4, need ATCA crate (more expensive)

Personal Outlook

- DAQ for Integration is definitely no rate limited
  - Need to connect a significant number of modules
  - Layout of connection close to final
- 2 (may be 3) kind of tests → electrical link/optical links
  - For electric link tests temporary connectors/mezzanine/electrical →optical converted (a` la VLDB?)
- Are we going to use the same DAQ system in UK and Italy?

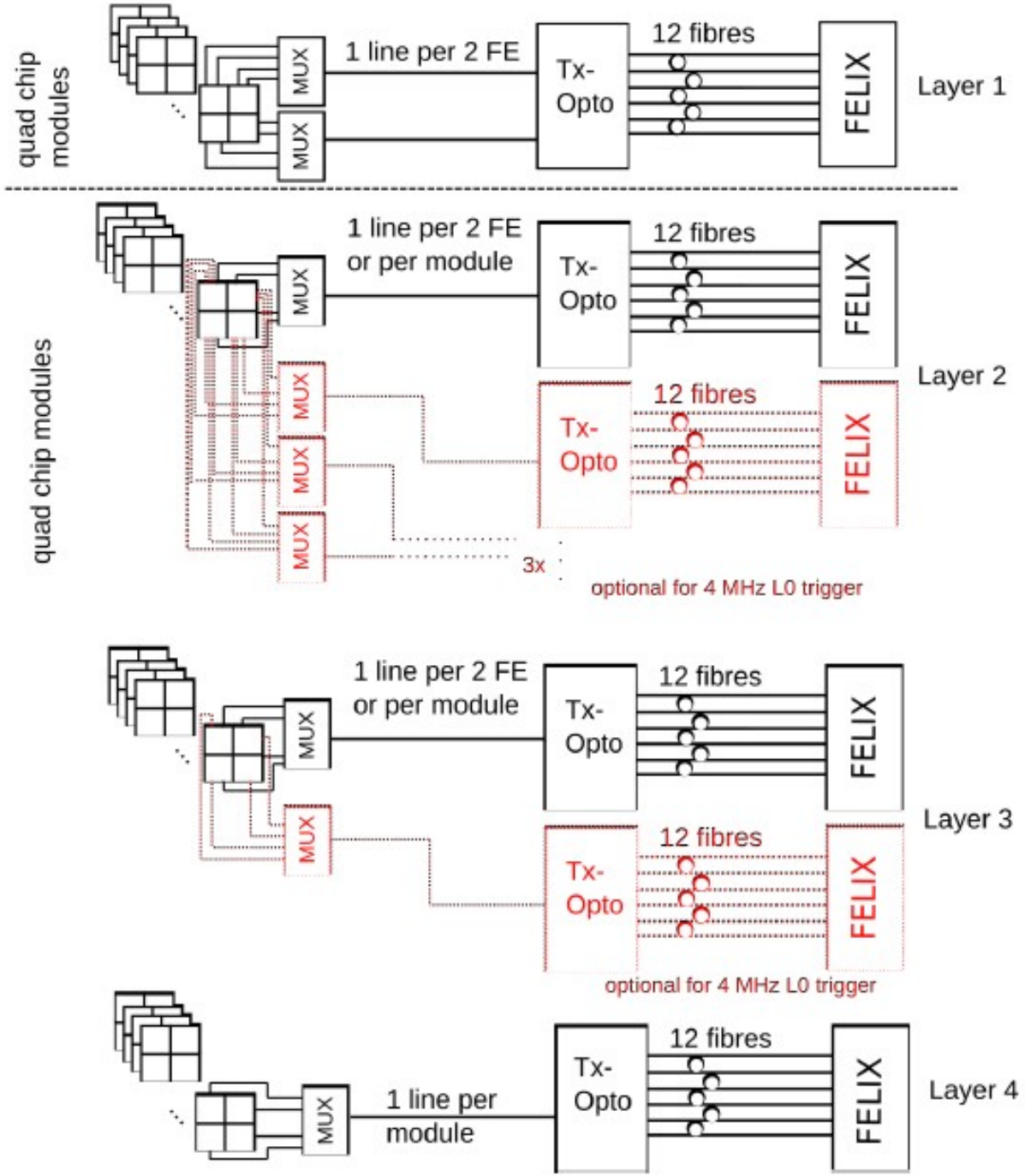
BackUp

Expected Data Rates

Layer/Ring	Data rate (1 MHz L0) (Gb/s)	Data rate (4 MHz L0) (Gb/s)	Design data rate per FE chip (Gb/s)
Layer 0	3.97	-	5.12
Layer 1	0.89	-	2.56
Layer 2	0.52	2.08	5.12
Layer 3	0.32	1.28	2.56
Layer 4	0.22	0.88	1.28
Ring 0	2.15	-	5.12
Ring 1	1.07	-	2.56
Ring 2	0.65	2.60	5.12
Ring 3	0.39	1.56	2.56
Ring 4	0.27	1.04	1.28

Layer	Maximum data rate/chip (Gb/s)		
	Flat Barrel	Inclined Barrel	End-cap
0	3.58	3.97	2.15
1	0.55	0.89	1.07
2	0.38	0.52	0.65
3	0.28	0.32	0.39
4	0.22	0.22	0.27

End-cap Layer	Radius [mm]	Rings	Sensors Per Ring	Type	Hits
0	50	4	16	quads	3
1	78	11	22	quads	3–4
2	152	10	32	quads	2
3	211	8	44	quads	1
4	271	9	52	quads	1


quad chip modules
MUX
MUX
1 line per 2 FE
Tx-Opto
12 fibres
FELIX
Layer 1
1 line per 2 FE or per module
Layer 2
3x
optional for 4 MHz L0 trigger
Layer 3
Layer 4
1 line per module

From TDR