Low-Power CPU: experience from the COSA project

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http://www.cosa-project.it

Istituto Nazionale di Fisica Nucleare

INFN COSA project

- COSA: Computing On SOC Architecture
- Duration: ~~3~~ **Extended to 4** years from January 2015
- Departments: 7 INFN
  - CNAF, PI, PD, ROMA1, FE, PR, LNL
- Budget: 50 kEuro for year
  - Funded by INFN CSN5

Objectives of COSA project

- Acquire know-how
  - Porting and benchmarking of low power/low cost System On Chip
  - Operations of Linux system on SoCs
  - Benchmarking hybrid architectures
- Unification of INFN HW testing activities
  - Continuation of the COKA project
    - Computing on Knights Architecture
    - Porting on traditional accelerator (GPU/MIC)
  - Continuation of the HEPMARK projects
    - X86 benchmarking
- Study of custom low latency interconnection built with ARM+FPGA devices
- Prepare H2020 proposals on LowPower computing calls

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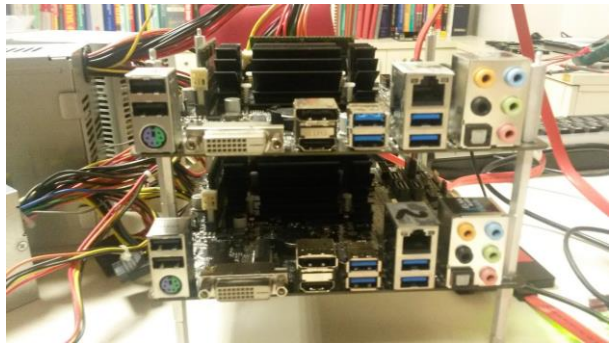
I. New Intel SoC architectures
II. Scientific Computing on SoCs
III. Parallel File System with SoCs and Storage Bricks
IV. SoCs for Edge/Fog Computing
V. Conclusions

Low-Power COSA cluster @ CNAF

16xARMv7
2xARMv8

4xINTEL AVOTON C-2750
4xINTEL XEOND-1540

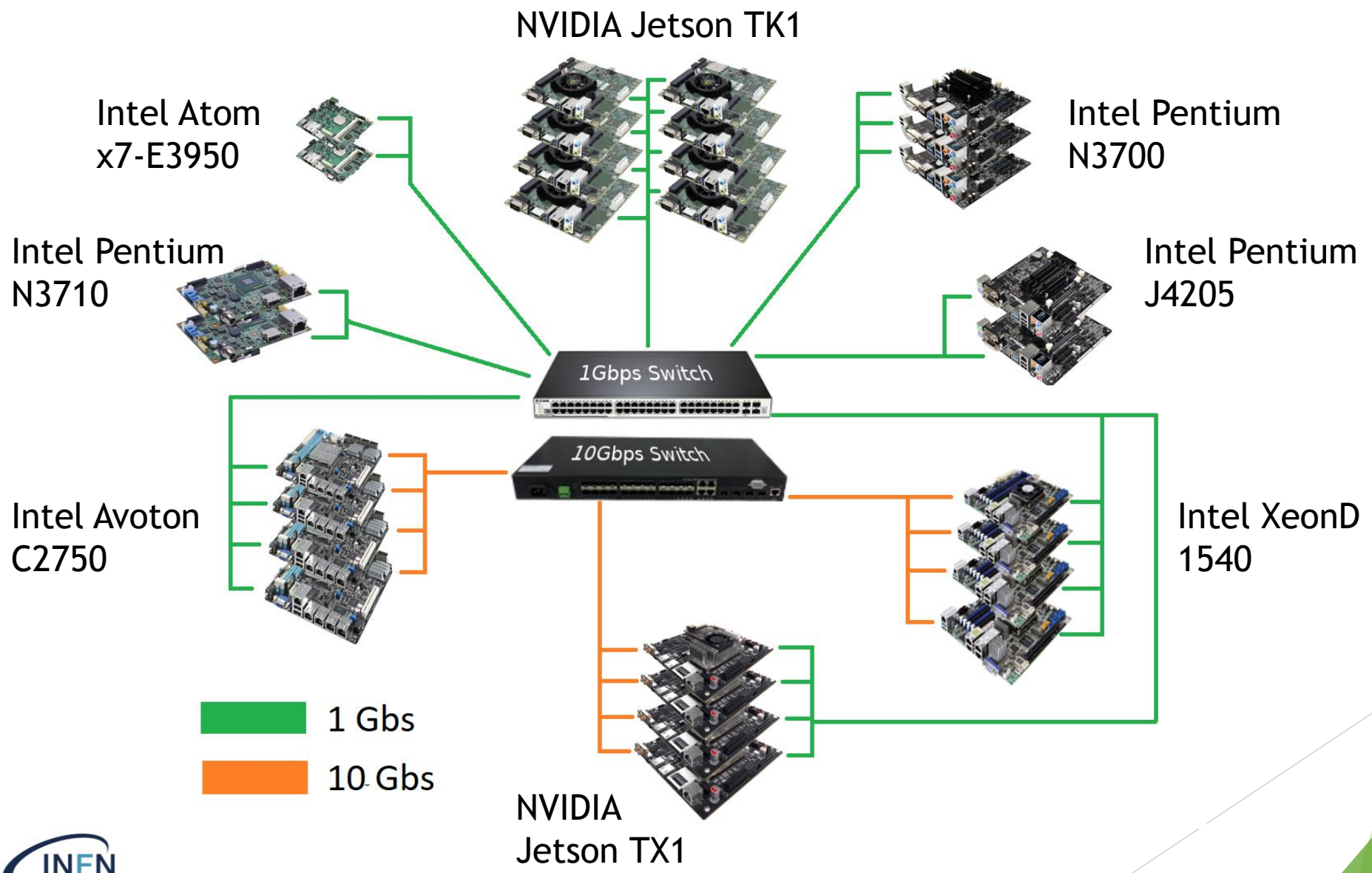


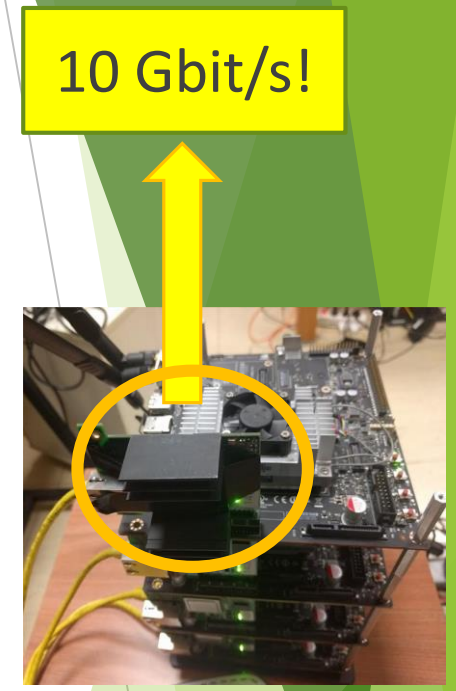
2xINTEL N3700
2xINTEL N3710
2xINTEL J4205

2xINTEL x7-E3950

2xINTEL C3958

COSA power network @ CNAF





Low-Power from Intel - 1

Product Name	2x Intel Xeon Processor E5-2683 v3 (35M Cache, 2.00 GHz)	Intel Xeon Processor D-1540 (12M Cache, 2.00 GHz)	Intel Atom Processor C2750 (4M Cache, 2.40 GHz)
Brand	XEON	XEON	ATOM
Microarchitecture	Haswell	Broadwell	Silvermont
Family	Haswell-EP	Broadwell DE	Avoton
Processor Nr.	E5-2683V3	D-1540	C2750
Launch Date	Q3'14	Q1'15	Q3'13
Cache	35 MB SmartCache	12 MB	4 MB
RAM (GB)	128	16	16
CORES	56 (HT)	16 (HT)	8
TDP (W)	2x120	45	20
Processor freq.	2.00 GHz (max 3.00 GHZ)	2.00 GHz (max 2.60 GHz)	2.40 GHz (max 2.60 GHz)
CPU Price	2x $1846.00	$581.00	$171.00

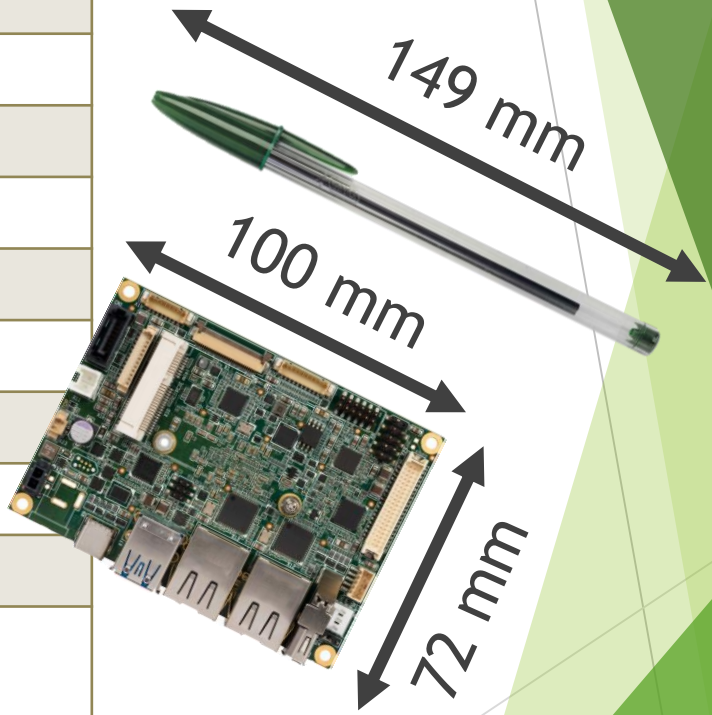
NOT LOW-POWER!
USED AS REFERENCE

Low-Power from Intel - 2

Product Name	Intel Pentium Processor N3700 (2M Cache, up to 2.40 GHz)	Intel Pentium Processor N3710 (2M Cache, up to 2.56 GHz)	Intel Pentium Processor J4205 (2M Cache, up to 2.60 GHz)
Brand	Pentium	Pentium	Pentium
Microarchitecture	Airmont	Airmont	Goldmont
Family	Braswell	Braswell	Apollo Lake
Processor Nr.	N3700	N3710	J4205
Launch Date	Q1'15	Q1'16	Q3'16
Cache	2 MB L2	2 MB L2	2 MB
RAM (GB)	8	8	8
CORES	4	4	4
TDP (W)	6	6	10
Processor freq.	1.60 GHz (max 2.40 GHZ)	1.60 GHz (max 2.56 GHz)	1.50 GHz (max 2.60 GHz)
CPU Price	$161.00	$161.00	$161.00

Low-Power from Intel – 3

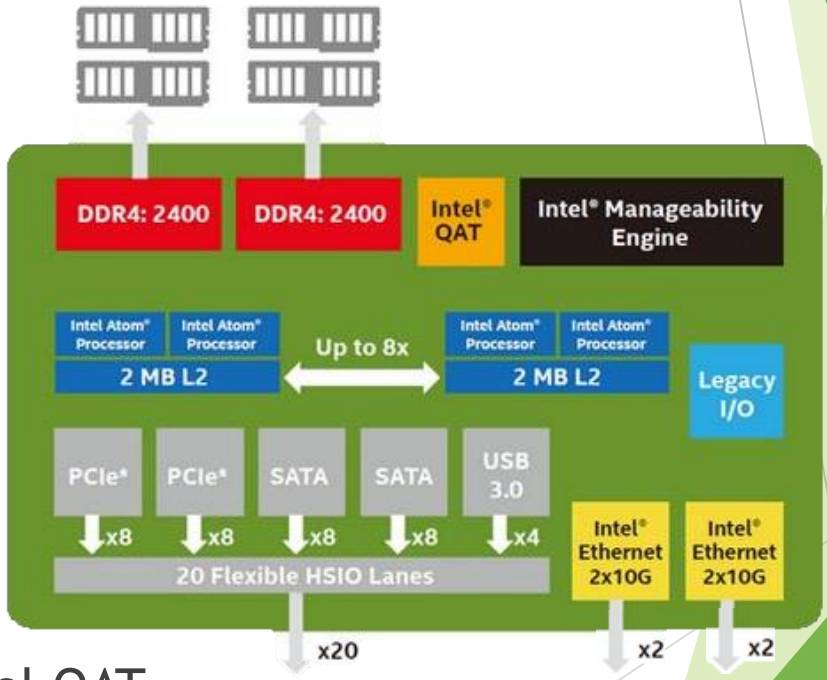
Product Name	Intel Atom Processor C3958 (16M Cache, up to 2.00 GHz)	Intel Atom x7-E3950 Processor (2M Cache, up to 2.50 GHz)
Brand	Atom	Atom x7
Microarchitecture	Goldmont	Goldmont
Family	Denverton	Apollo Lake
Processor Nr.	C3958	x7-E3950
Launch Date	Q3'17	Q4'16
Cache	16 MB	2 MB L2
RAM (GB)	256 max	8
CORES	16	4
TDP (W)	31	12
Processor freq.	2.00 GHz (max 2.00 GHZ)	1.60 GHz (max 2.00 GHz)
CPU Price	$449.00	$430.00



Intel Atom C3958

Intel's new generation Atom platform is a single-chip SoC that offers extensive high-speed HSIO options and **16 low-power cores**.
With some of the highest power density (performance/watt) of Intel's Enterprise line up, this platform is ideal for lightweight, storage-heavy applications.

- Extensive I/O
  - Flexible I/O Adapter
  - PCIe/SATA/USB port
- Performance/Watt Leadership
  - SoC TDP of **31 W** (2W per core)
- Networking
  - **4 × 10Gbs** full duplex encryption with Intel QAT



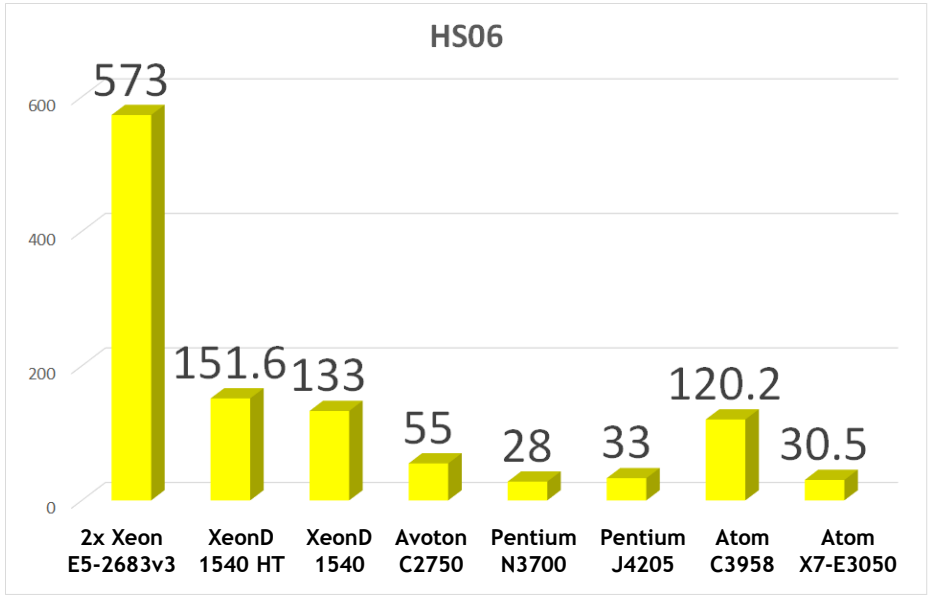
Intel Atom x7-E3950

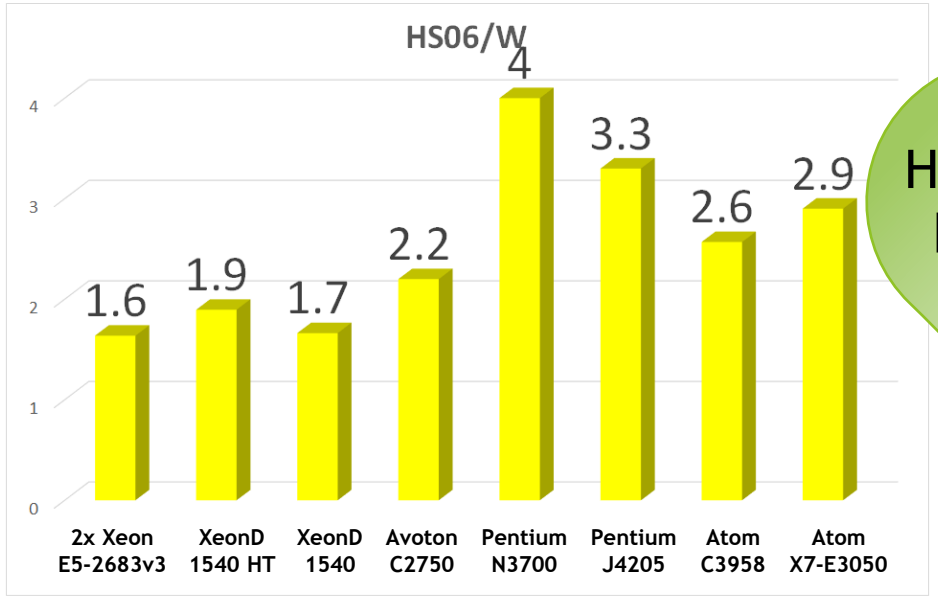
- Designed both industrial and commercial applications including **IoT**, factory automation, self-service kiosks and POS system
- RAM 8 GB
- TDP 12 W
- Integrated with the **Intel Gen9 graphics** engine equipped with 18 execution units for high throughput and acceleration

Applications:

- Synthetic Benchmark (HS06)
- Experimental Physics:
  - LHCb Montecarlo software (Gauss sw)
  - ATLAS KitValidation (EVGEN, SIMUL, DIGIT)

HS06 on Intel platforms





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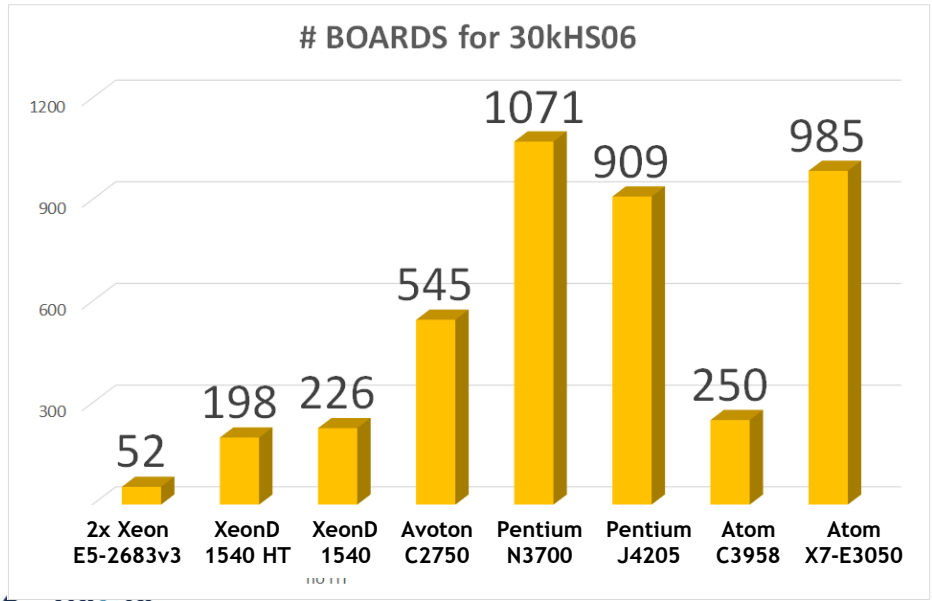
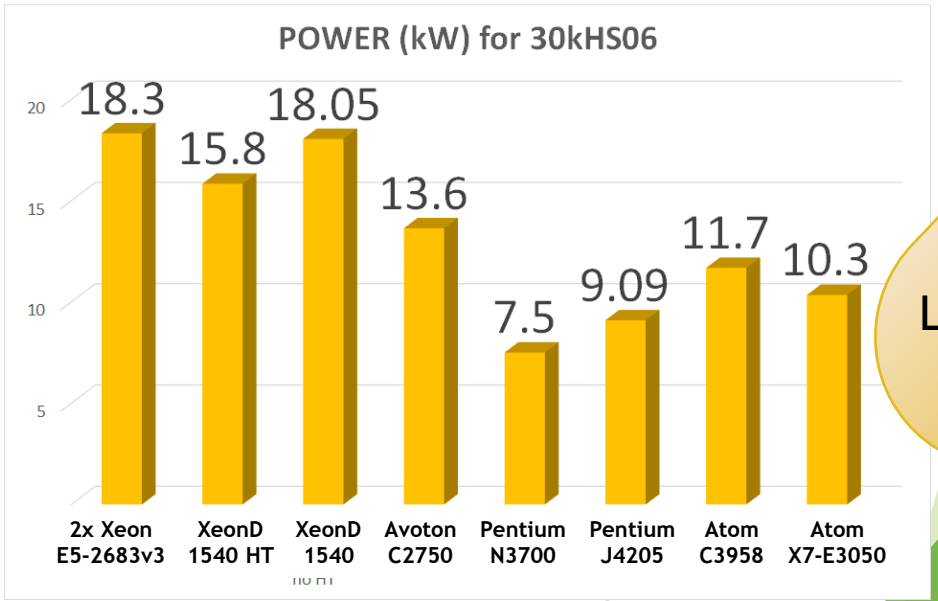
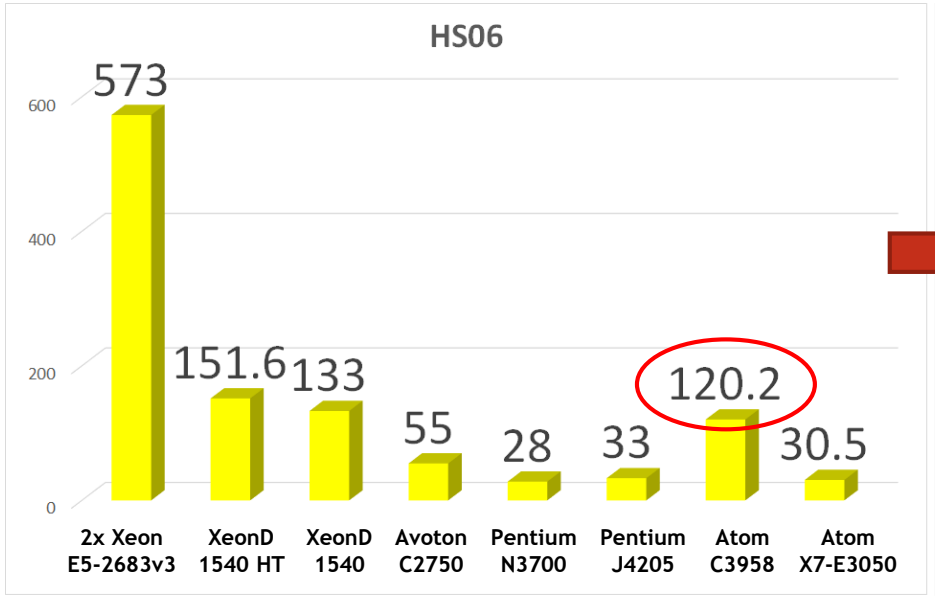
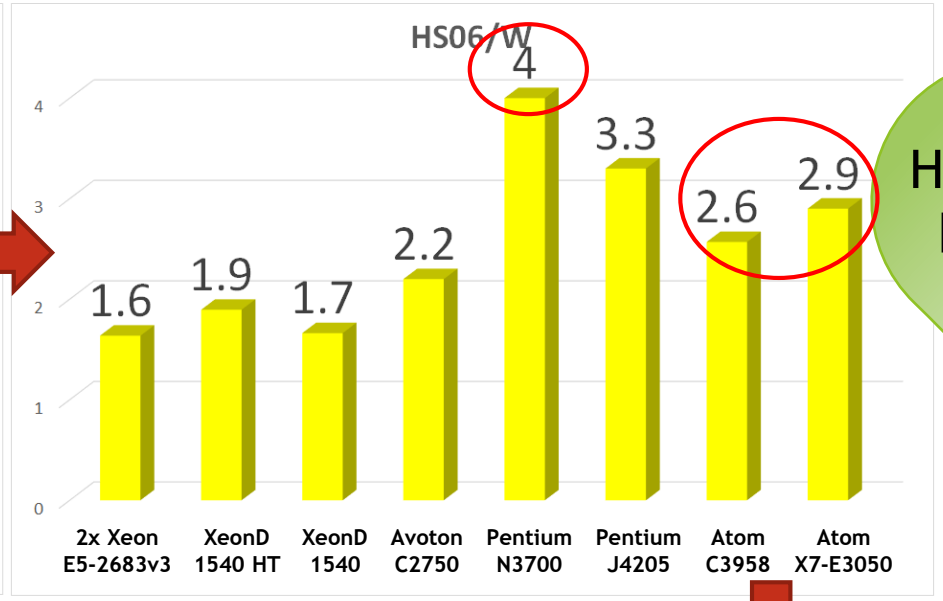




Lower is better

HS06 on Intel platforms





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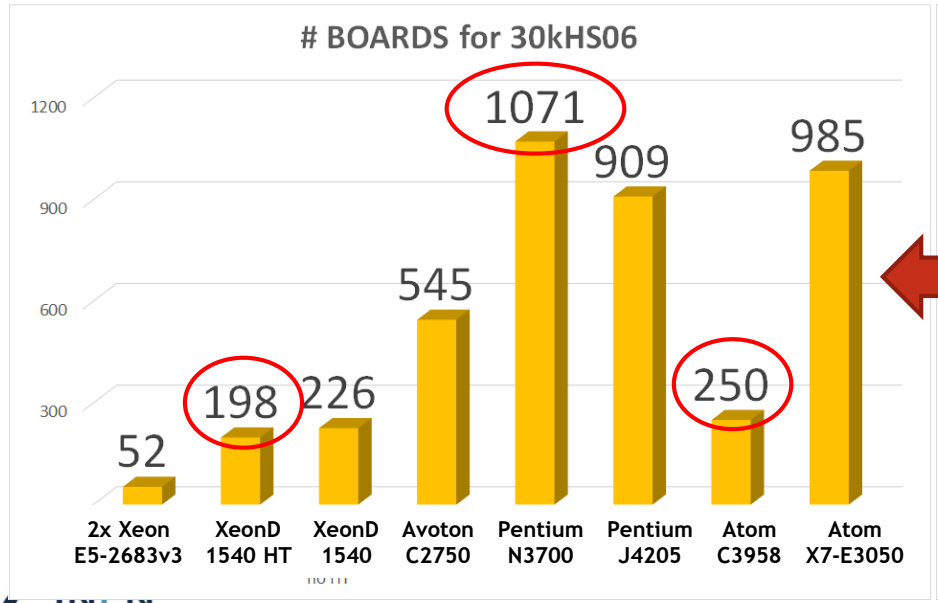
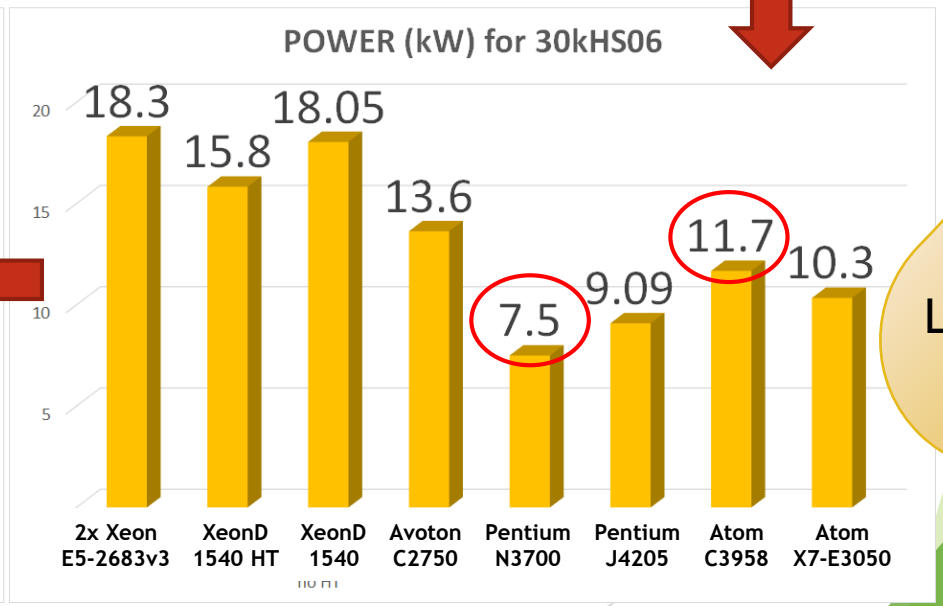
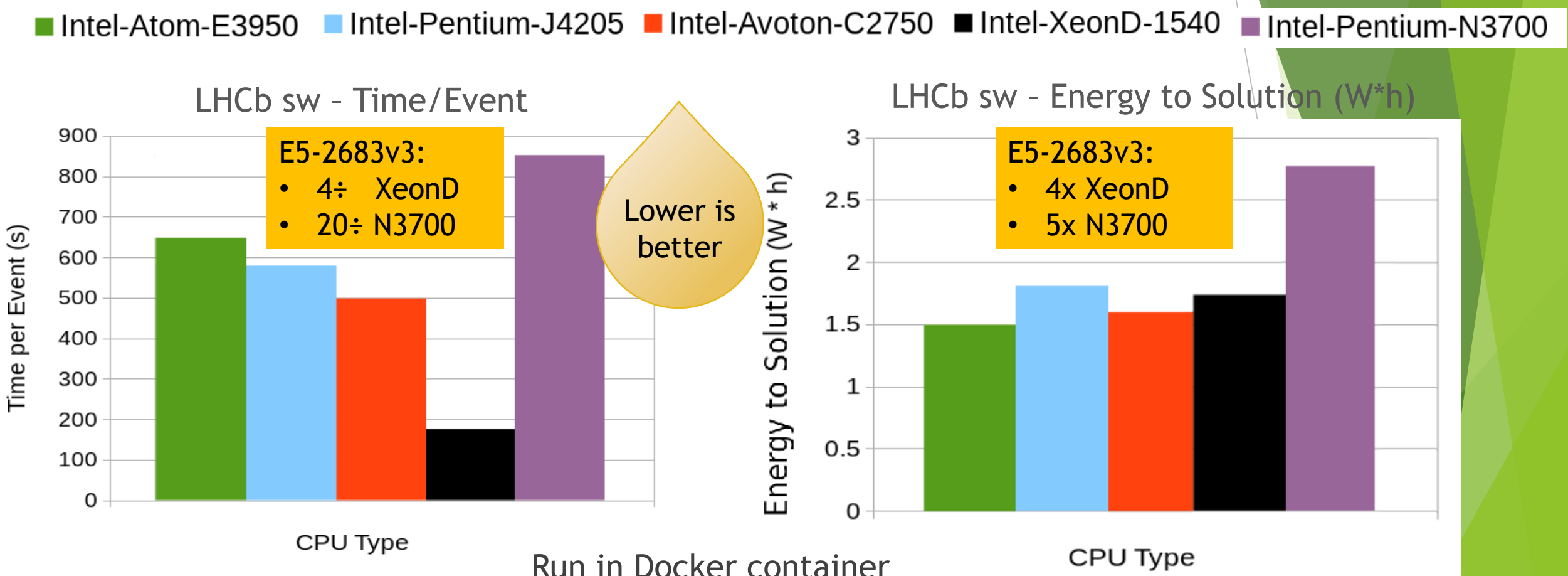




Lower is better

Experimental Physics: LHCb Gauss software



Run in Docker container

Used all cores available

A.Falabella @ INFN-CNAF and
M.Soares @ INFN-CNAF

Clemencic, M.; others. The LHCb Simulation Application, Gauss: Design, Evolution and Experience. Journal of Physics: Conference Series 331 2011, 3

Experimental Physics: ATLAS KitValidation

A. De Salvo e F. Brasolin, «Benchmarking the ATLAS software through the Kit Validation engine, in Proceedings of Computing in High Energy and Nuclear Physics», Praga, Repubblica Ceca, 22-28 Marzo 2009

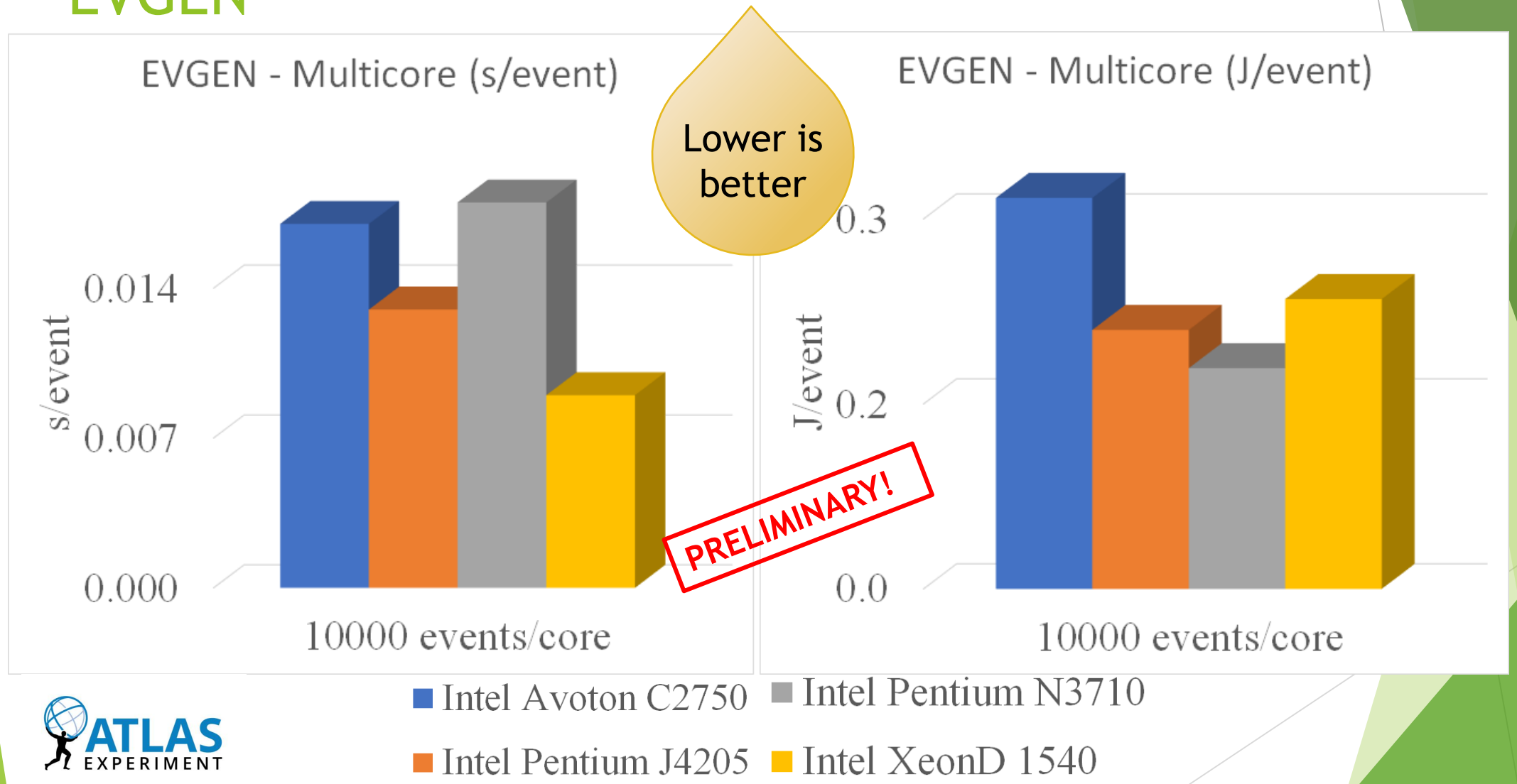
Three Steps:

1. Events GENeration (EVGEN step): simulation of the collision between two protons and simulation of the decay of the particles produced in the primary collision
2. Detector SIMULation (SIMUL step): simulation of the particles behavior and all their interactions in the ATLAS detector
3. Events DIGITalization (DIGIT step): conversion of the signals produced by the previous simulation into a digital format similar to that of the real data

- Event = proton-proton collision

Stage of Andrea Bonantini under supervision of prof. Lorenzo Rinaldi:
Studio e misura di performance di applicazioni software dell'esperimento ATLAS a LHC su architetture SoC

Experimental Physics: ATLAS KitValidation: EVGEN



ATLAS EXPERIMENT

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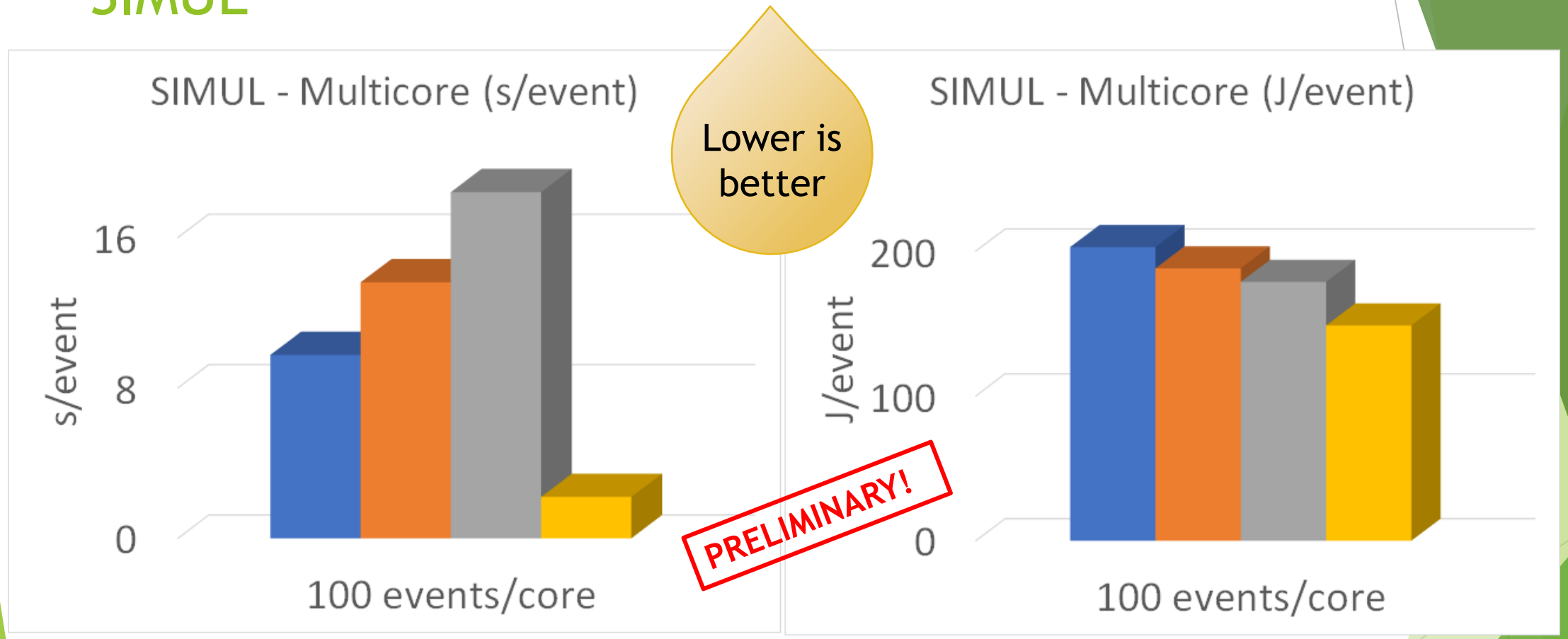
Stage of Andrea Bonantini under supervision of prof. Lorenzo Rinaldi:
Studio e misura di performance di applicazioni software dell'esperimento ATLAS a LHC su architetture SoC

Experimental Physics: ATLAS KitValidation: SIMUL



ATLAS EXPERIMENT

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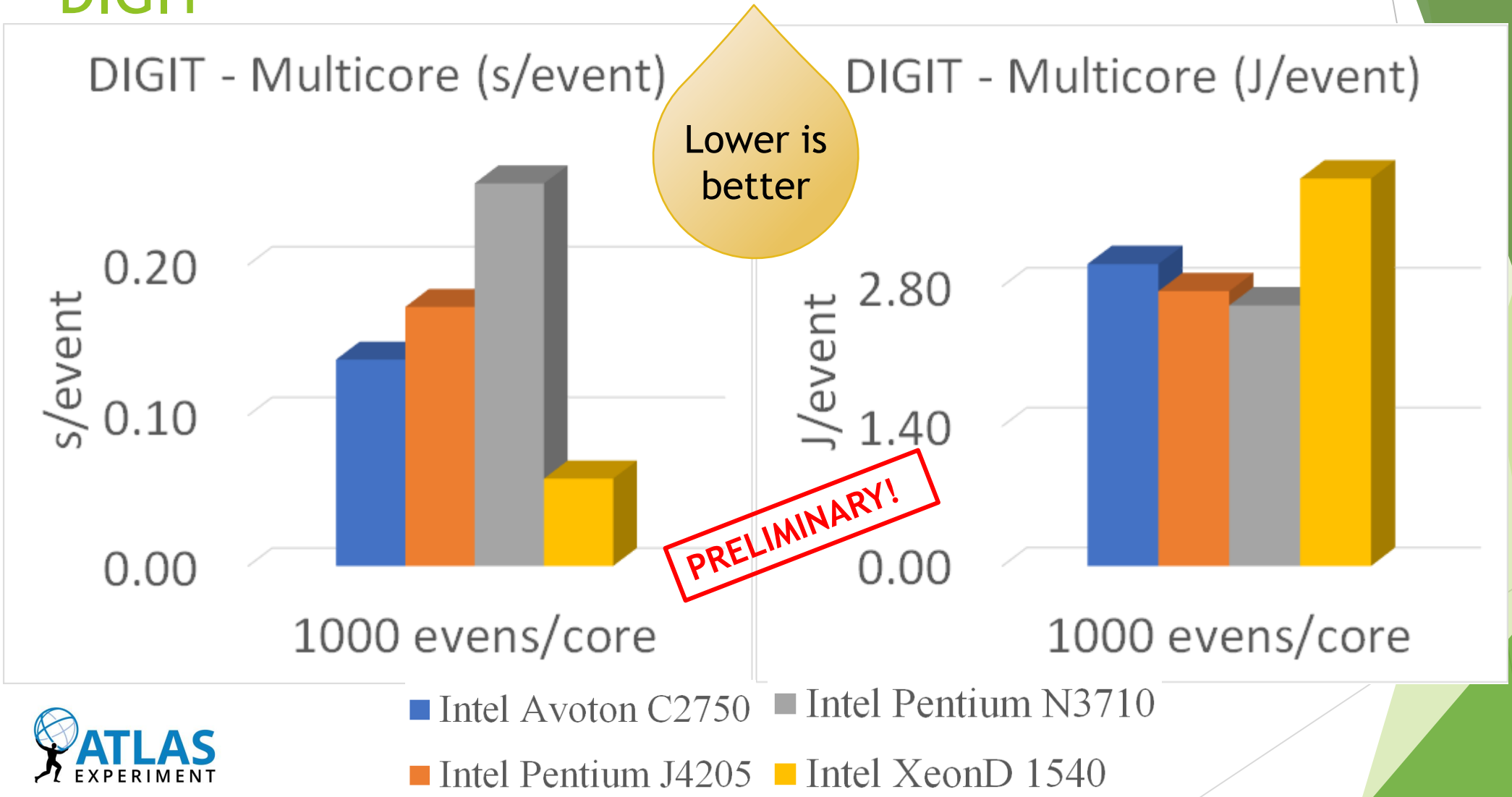
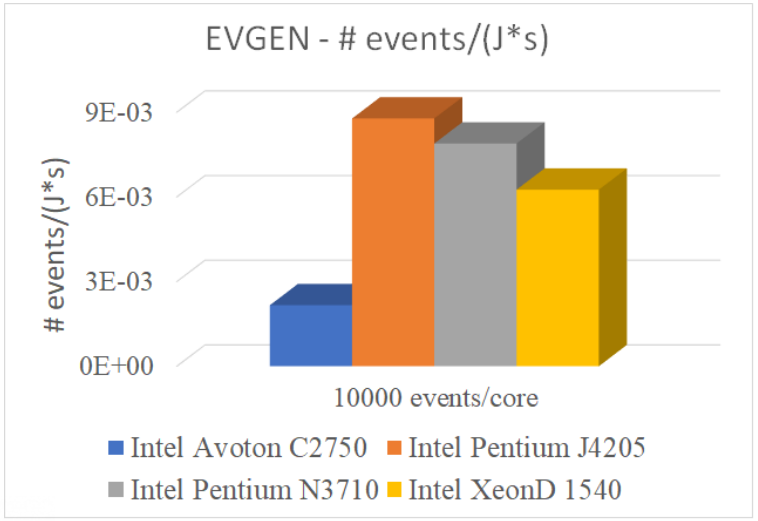
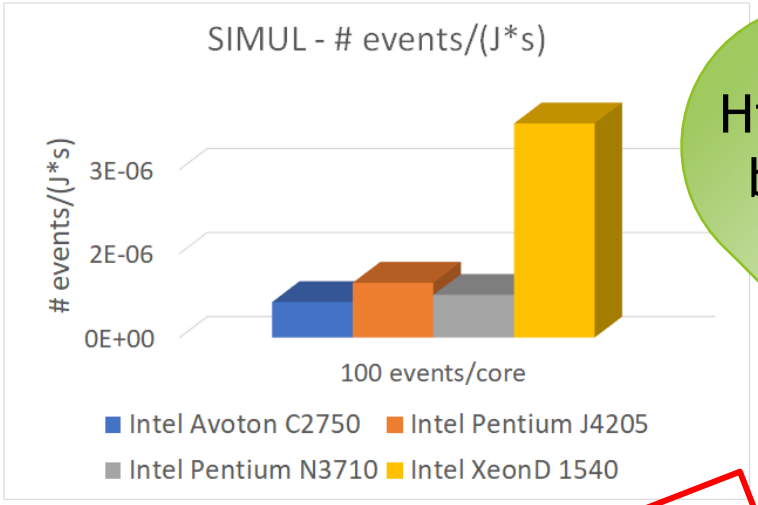
Studio e misura di performance di applicazioni software dell'esperimento ATLAS a LHC su architetture SoC

Experimental Physics: ATLAS KitValidation: DIGIT



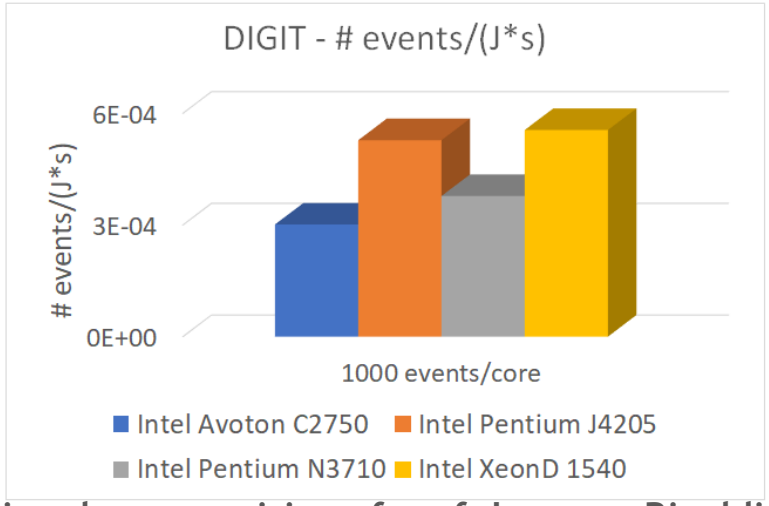
Experimental Physics: ATLAS KitValidation: Efficiency parameter: # events/(J*s) Multicore





Higher is better

For Atom C3958 and x7-E3950 work in progress…



PRELIMINARY!

Stage of Andrea Bonantini under supervision of prof. Lorenzo Rinaldi:
Studio e misura di performance di applicazioni software dell'esperimento ATLAS a LHC su architetture SoC

Parallel File System with SoCs and Storage Bricks

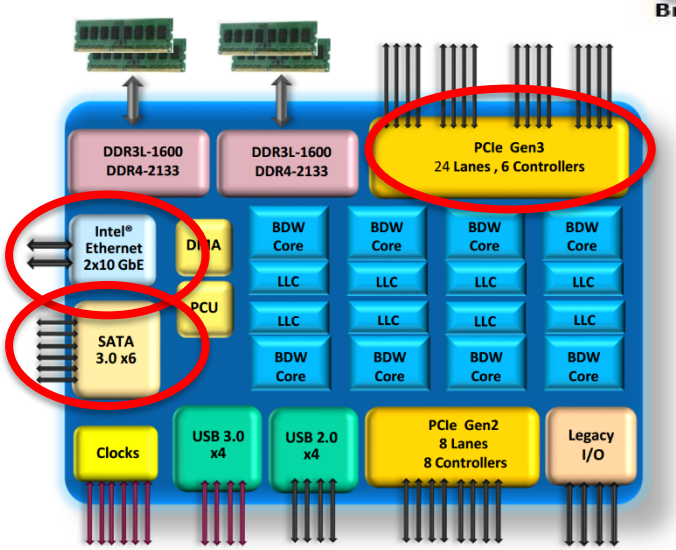
BeeGFS®
developed by Fraunhofer

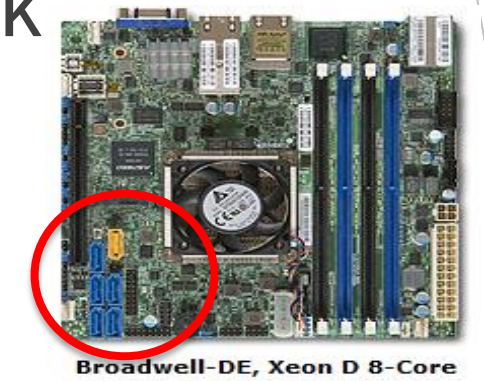
Parallel FS with SoCs and Storage Bricks

- XeonD processors for a storage brick
- BeeGFS as a filesystem

Intel® Xeon® Processor D - SoC Architecture

CPU	2-8 Core Intel® Xeon™ (14nm) CPUs
L1 cache	32K data, 32k instruction per core
L2 cache	256K per core
LLC cache	1.5MB per core
Addressing	46 bits physical / 48 bits virtual
Memory	DDR4 up to 2133 MT/s DDR3L up to 1600 MT/s Two Channels (2 DIMMs/Channel)
Memory Capacity	RDIMM: 128 GB (32 GB/DIMM) UDIMM/SODIMM: 64 GB (16 GB/DIMM)
DIMM Types	SODIMM, UDIMM, RDIMM with ECC and non-ECC
Memory RAS	Enhanced ECC Single bit Error Correction – Dual bit Error Detection (SEC-DED) covers address and data paths, DDR scrambler to reduce error rate.
PCI-E*	x24 PCIe Gen3 with up to 6 controllers x8 PCIe Gen 2 with up to 8 controllers
Integrated IO	Intel® Ethernet 2x10 GbE , x4 USB 3.0, x4 USB 2.0, and x6 SATA 3
Technologies	Intel® VT, Core RAPL, PECI over SMBUS, PSE
Power Management	FIVR, PCPS, EET, UFS Hardware PM
Legacy I/O	SPI for boot flash, SMBus, UART LPC, GPIO, 8259, I/O APIC, 8254 Timer, RTC

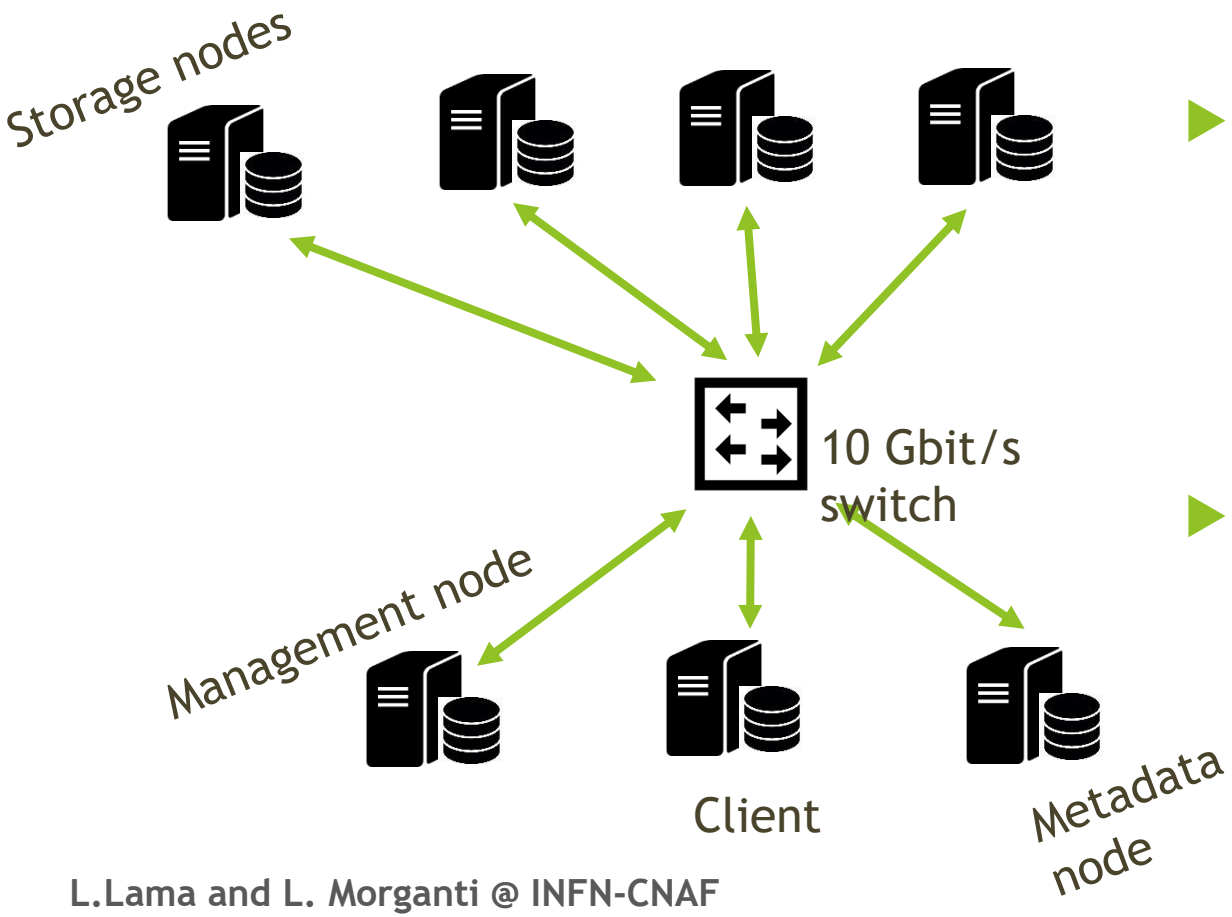



Broadwell-DE, Xeon D 8-Core

For Atom C3958 work in progress...

BeeGFS®
developed by Fraunhofer

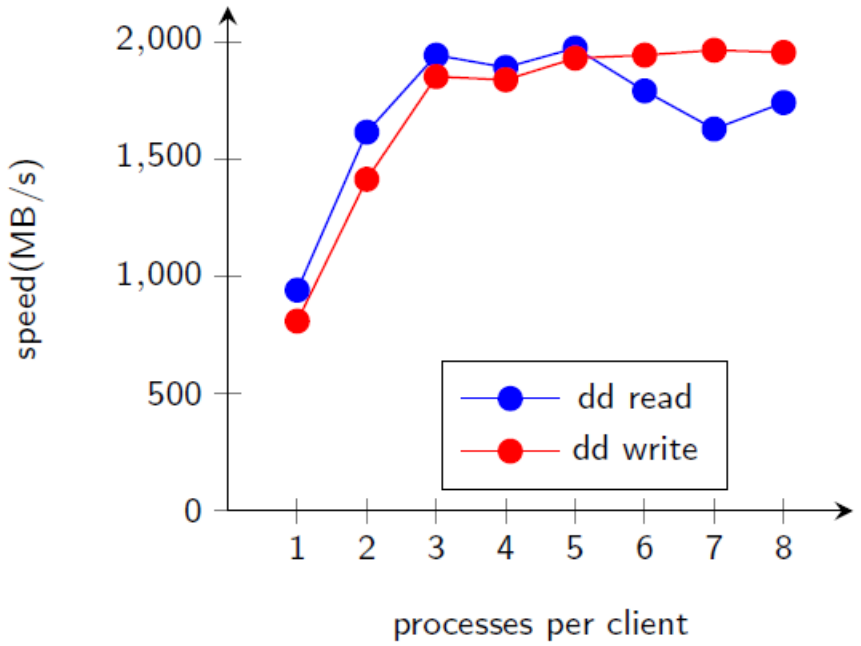
Parallel FS with SoCs and Storage Bricks: configuration

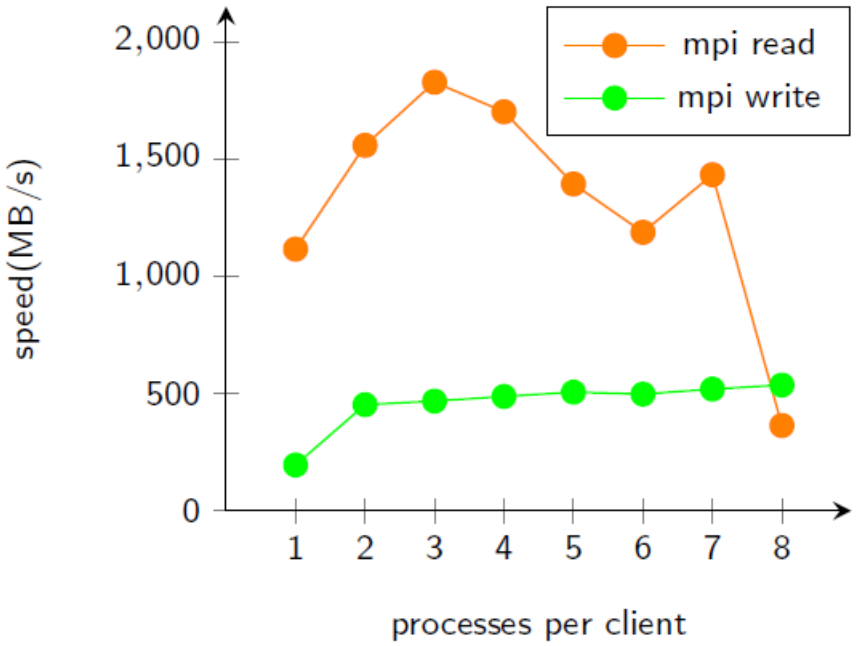


- Storage nodes and management node have dedicated 8TB HDDs (one or more)
- The metadata node has a 500 GB SSD

BeeGFS® developed by Fraunhofer

Parallel FS with SoCs and Storage Bricks: multiclient test – R/W speed

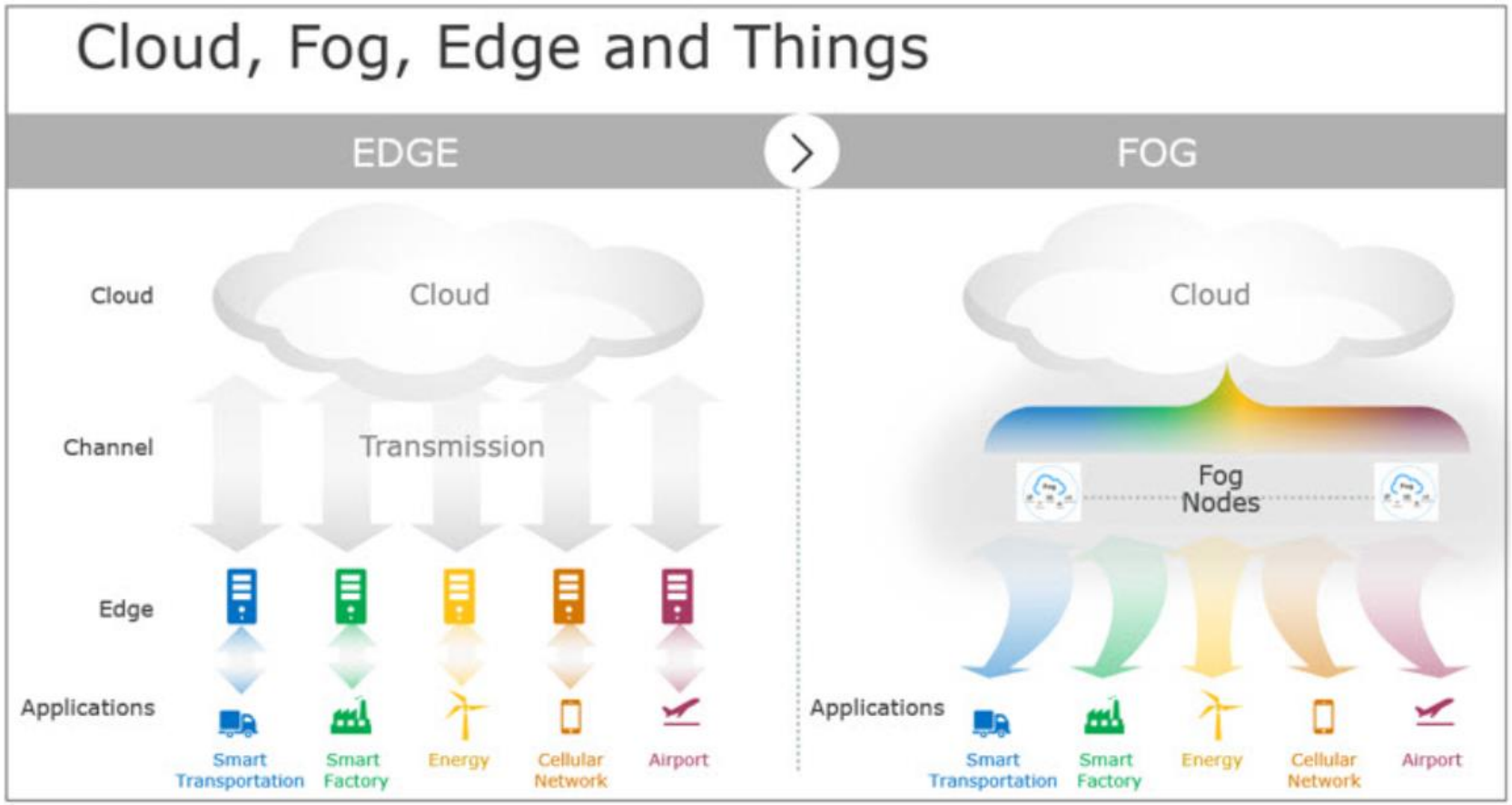




Tests on metadata work in progress…

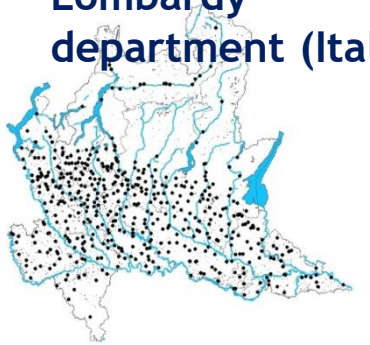
- 2 clients: avoton boards
- Used 4 storage servers
- Read and write 10GB file using *dd* and *checkpoint&restart*

SoCs for Edge/Fog Computing



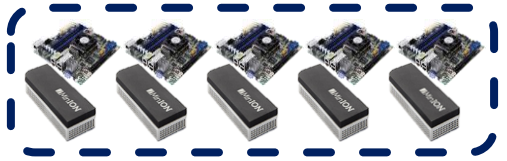
SoCs for Edge/Fog Computing: use case

Lombardy department (Italy)

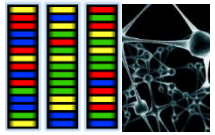


> 400 stations for monitoring surface water

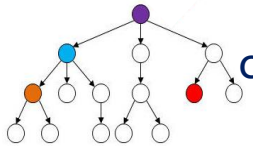
Massive parallel sequencing with MinION + SoC devices



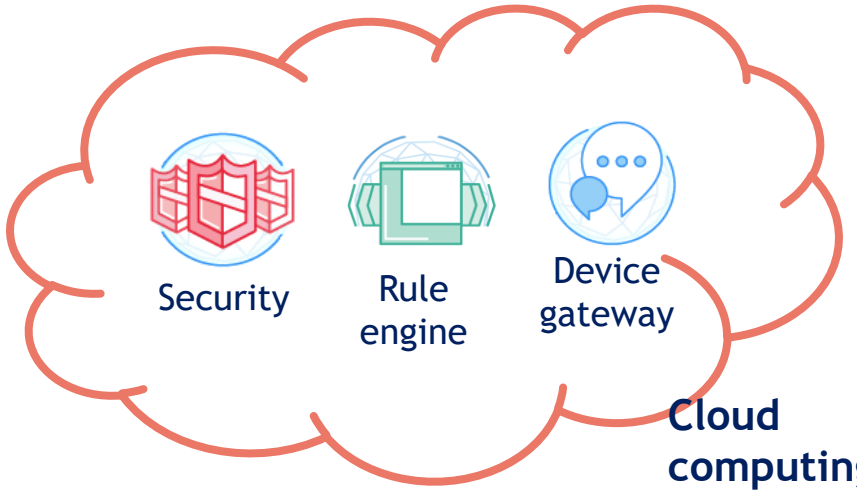
Fog computing



DNA basecalling with **Deepnano** to identify genomic sequences



Bacteria classification with **Kraken** to assign taxonomic labels

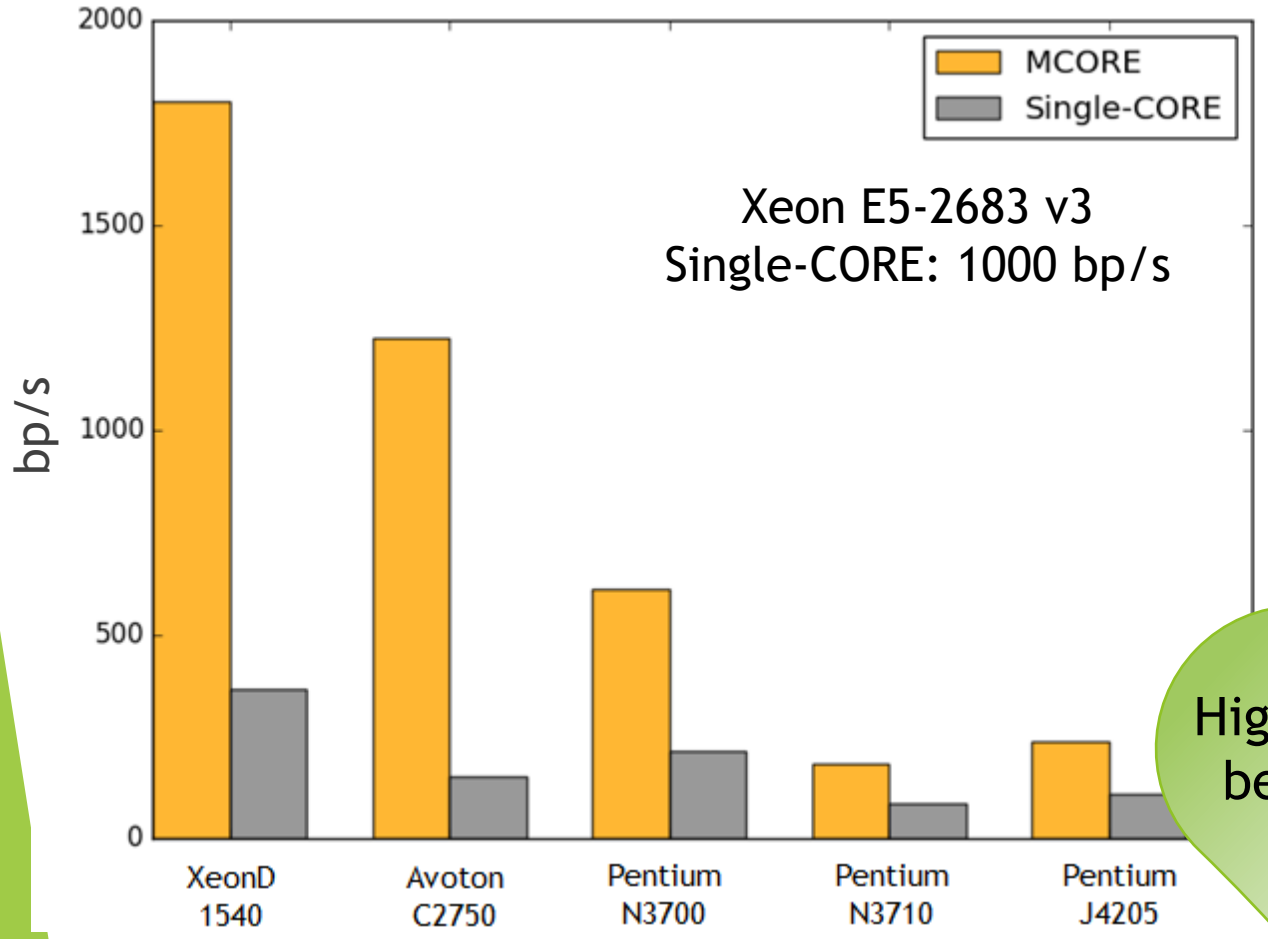


Cloud computing

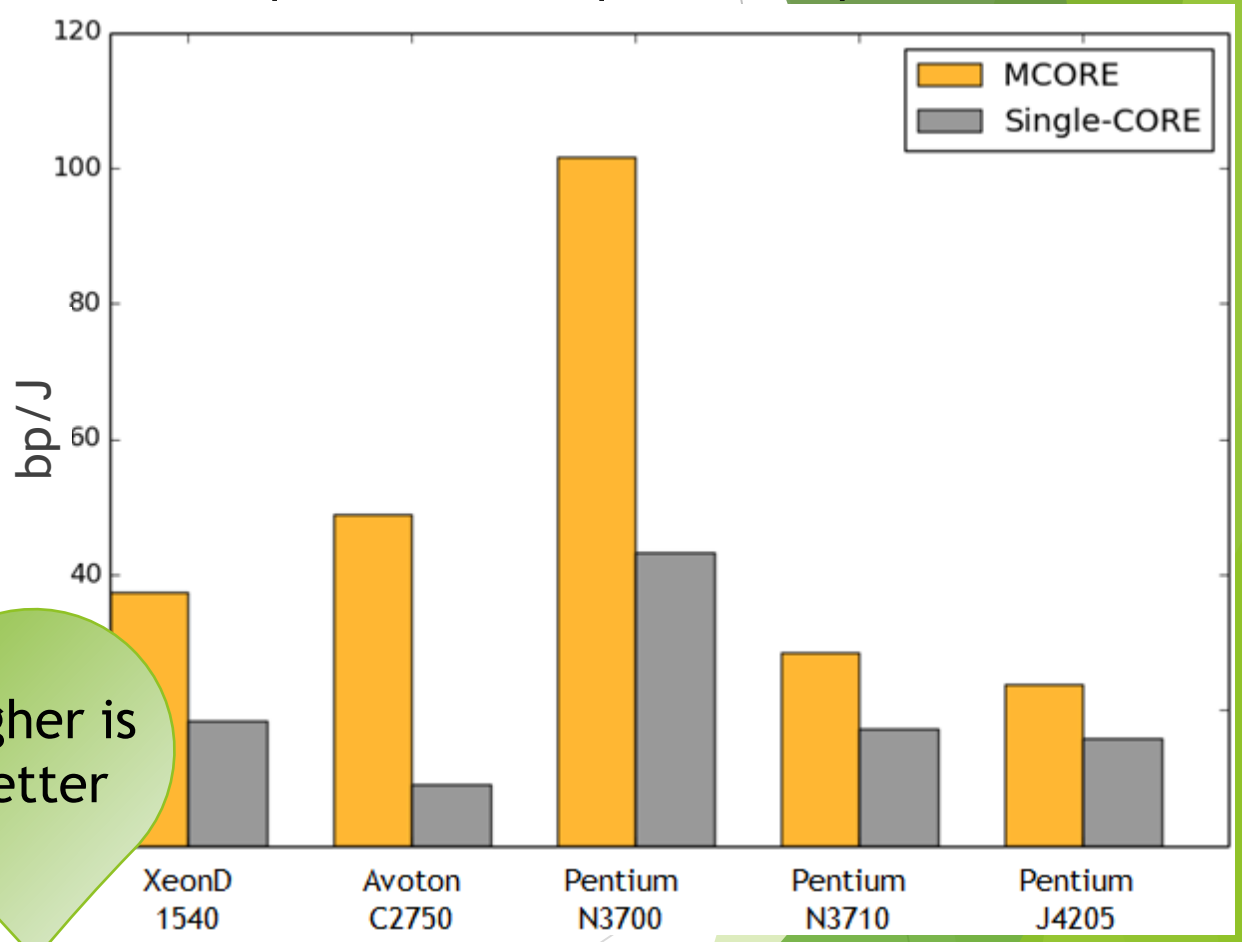
Low-Power Portable Devices for Metagenomics Analysis: Fog Computing Makes Bioinformatics Ready for the Internet of Things, Future Generation Computer Systems, 2017

SoCs for Edge/Fog Computing: Deepnano test

Deepnano - Bases processed per second



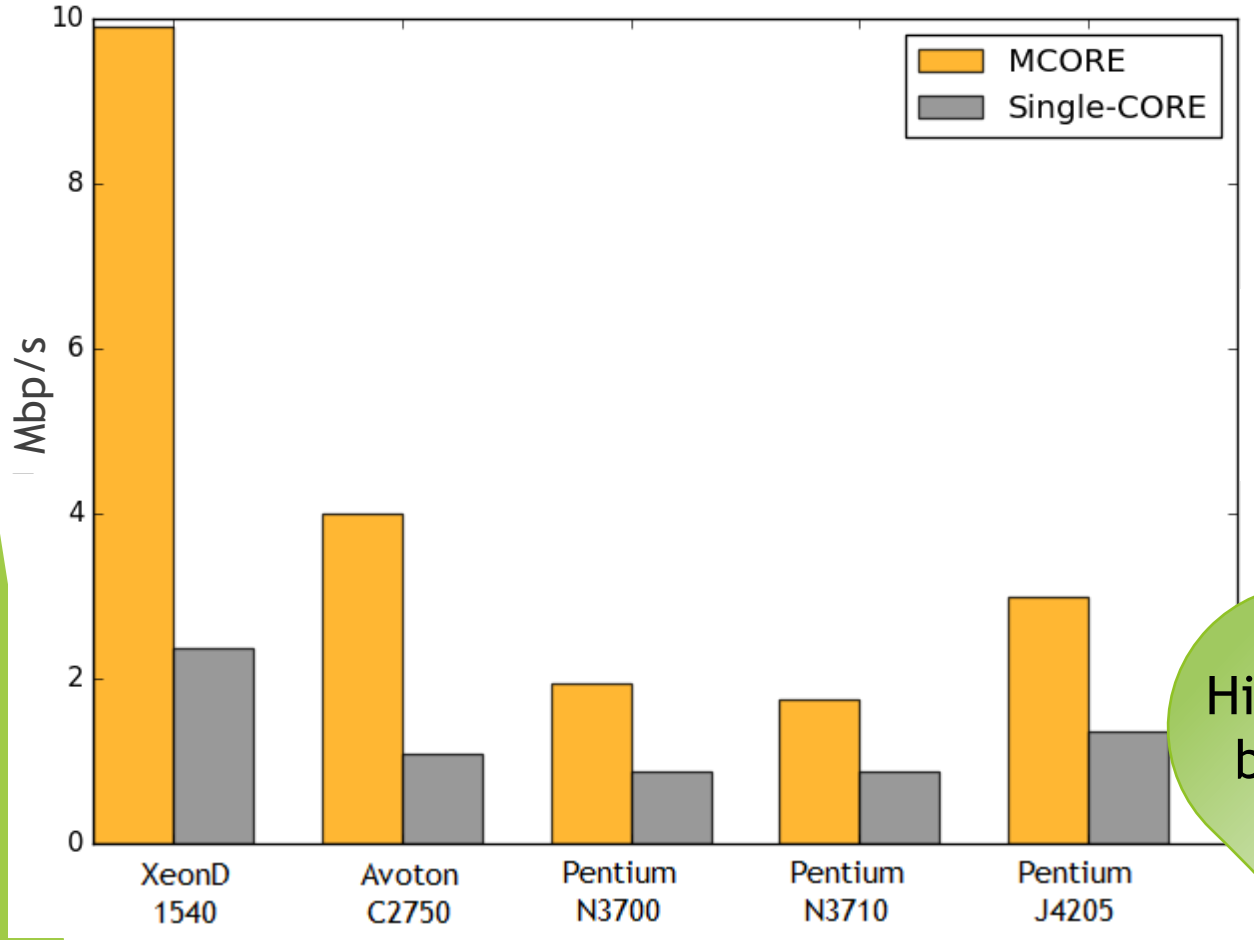
Deepnano - Bases processed per Joule



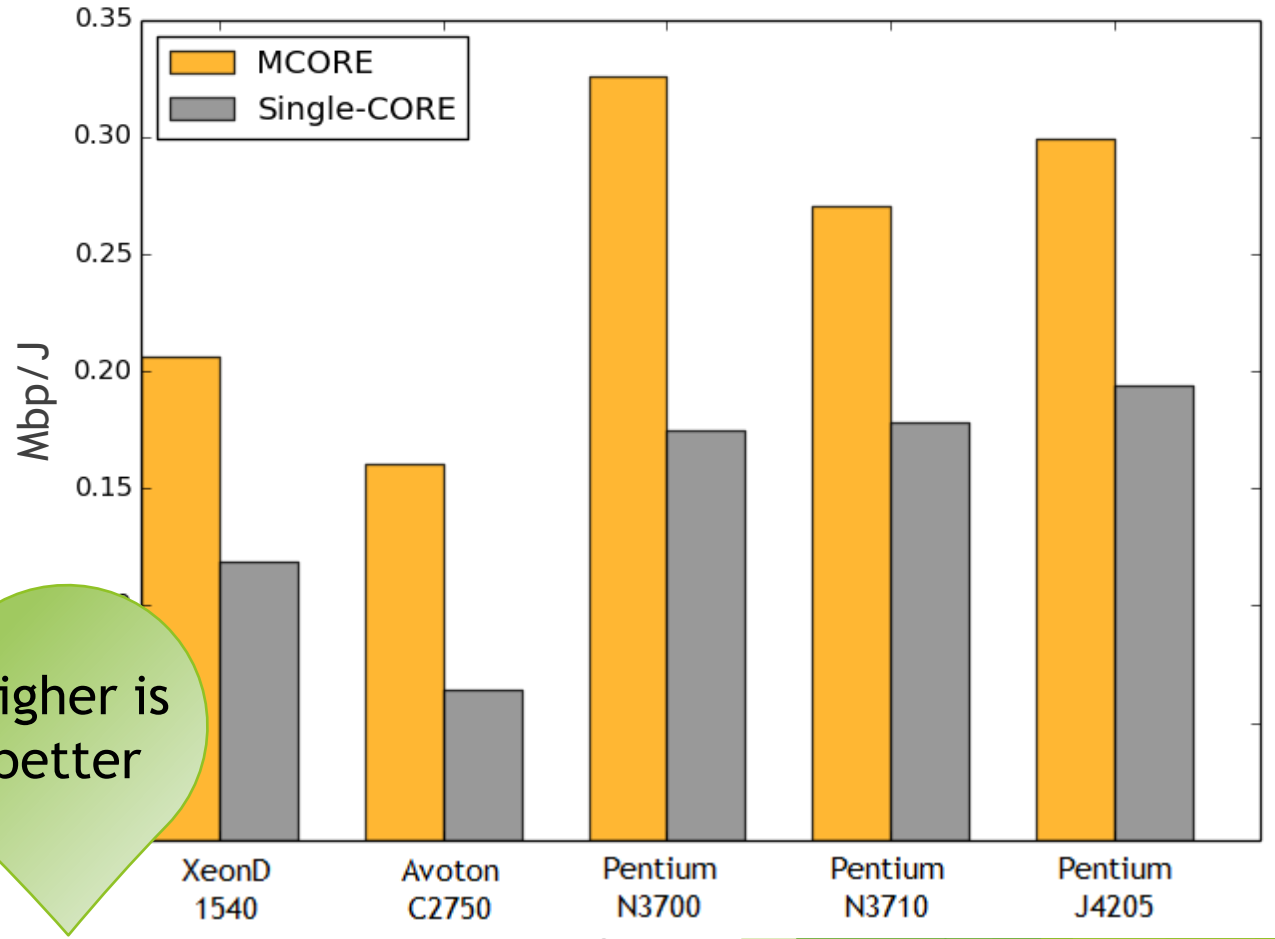
Higher is better

SoCs for Edge/Fog Computing: Kraken test

Kraken SW - Bases processed per second



Kraken SW - Bases processed per Joule



Higher is better

SoCs for Edge/Fog Computing: realistic scenario

- To achieve real time computations:
  - 9 XeonD 1540 + 13 Avoton C2750 boards
- If the time is not a problem:
  - Single board (XenonD or Avoton) can support the throughput of a single day analysis and it can be battery-powered
- Xeon E5-2683v3 (HPC server – 14 core) up to 1 Gbases/day

Realistic Scenario:

- MinION produces 30 bases per second per pore
- 512 pores
- Data stream: 15'360 bases/second, i.e 2.64 Gbases in 48 h.

Conclusions -1

- In this talk we have seen:
  - An overview on of the Intel low power SoC architectures made available on the COSA project
  - Results for 3 different use cases:
    - Scientific Computing
    - Storage brick
    - Edge/Fog Computing
- Intel SoCs are becoming attractive for real life scientific applications
- Low power/low cost dominated by ARM until two years ago, since last year INTEL started to be competitive in this segment

Conclusions - 2

- Advanced HW integration needed to maintain a reasonable size of the system
- XeonD 1540 and Atom C3958, that have both fast links, can be exploited to build a parallel FS using storage bricks
- Intel low power boards are available solution fo Edge/Fog computing use case.

Thanks!!

Special thanks to:

A. Falalbella, A. Ferraro, C. Pellegrino, D. Cesini, F. Giacomini, L. Lama, L. Morganti, & M. Soares from CNAF,

A. Bonantini & L. Rinaldi from Bologna/ATLAS,

I. Merelli from CNR ITB Milano & D. D'Agostino from CNR IMATI Genova,

R. Alfieri & R. De Pietri from PR,

F. Schifano & E. Calore from FE,

T. Boccali from PI,

P. Vicini, A. Lonardo & P.S. Paolucci from ROMA1,

M. Michelotto from PD.

http://www.cosa-project.it

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