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Signal digitization for multi-PMTs for E61 and HK

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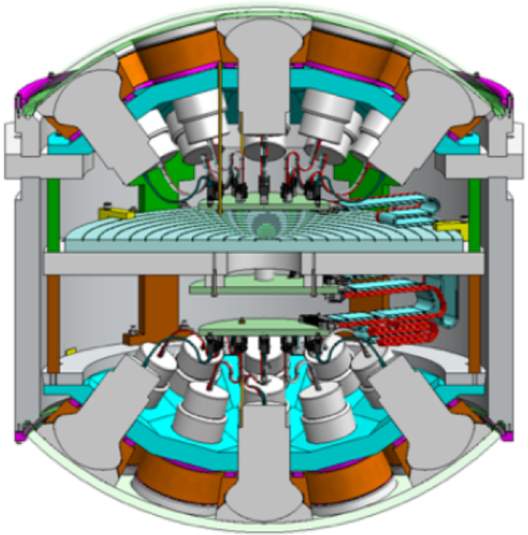
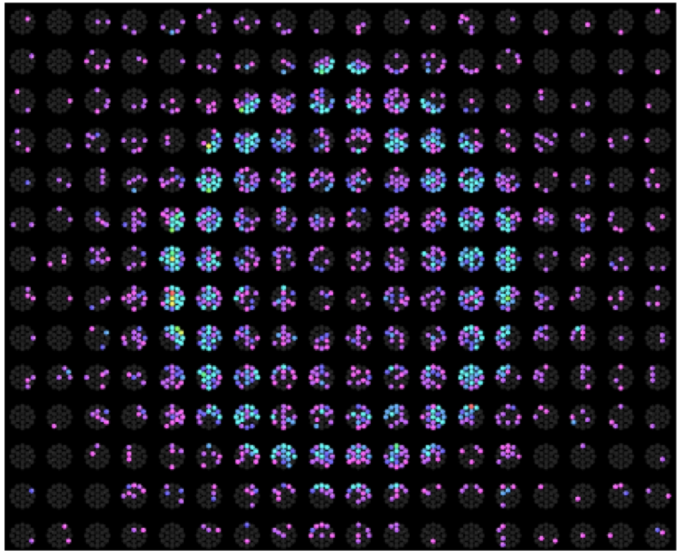
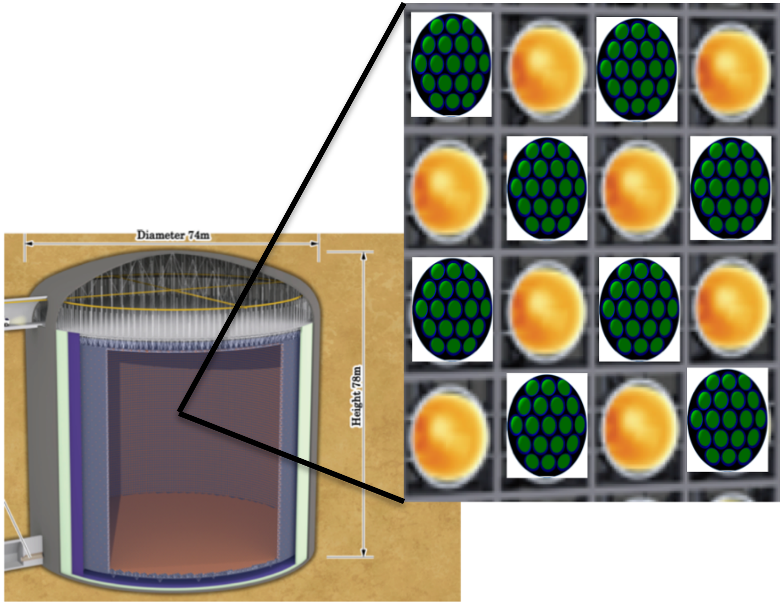
- Hyper-K and E61 mPMT electronics requirements
- Digitization design options
- Communication, clock and cabling



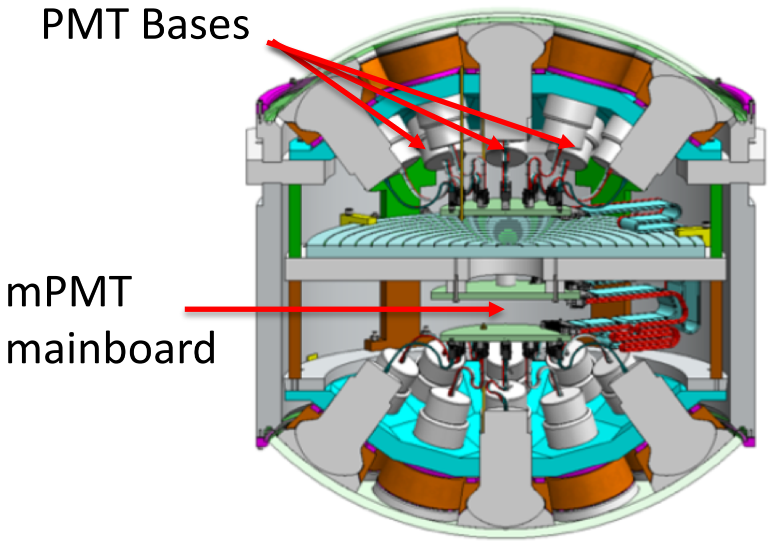
- mPMTs for all E61 photosensors
- Better granularity for small WC detector (4m radius).





- For Hyper-K, option to have up to 20k mPMTs, in addition to 20k 20” PMTs.

- Need electronics for **20-26** 3” PMTs (19 towards inner detector, 1-7 towards outer detector) per mPMT
- In-water electronics: too many cables/penetrations to route every PMT signal to surface.
- Re-use KM3NET scheme for PMT HV (on PMT base).
- Develop new digitization: KM3NET single time-over-threshold does not give sufficient information for large pulses.

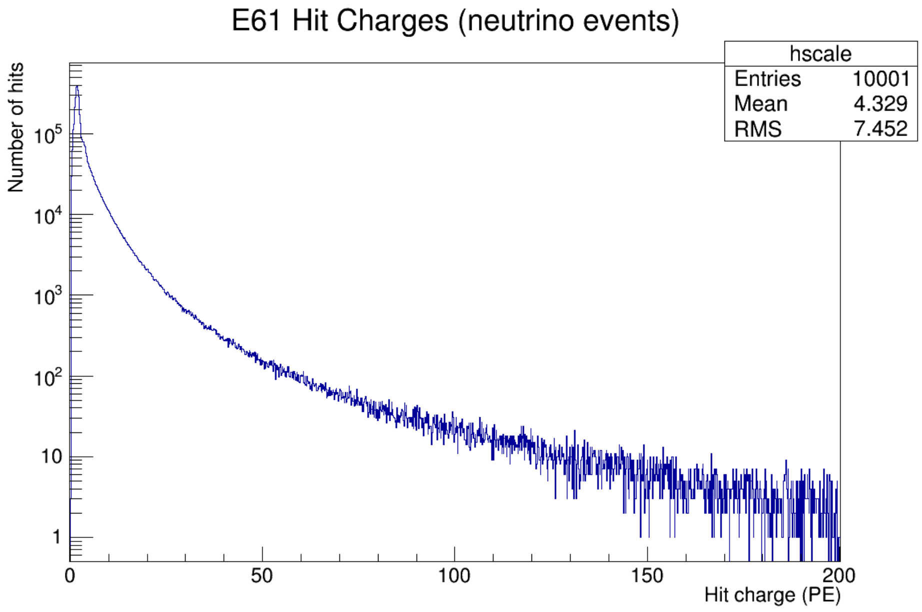


Early E61 mPMT design (actual design has fewer OD PMTs)

- Performance Requirements
  - Timing resolution: better than 3” PMT TTS
    - hopefully 3” PMT TTS (σ) <1ns for 1PE.
    - So ~300-500ps timing resolution from electronics for 1PE.
    - Better timing resolution (100-200ps) for large PE pulses.
    - E61 Vertex resolution strongly depends on hit timing resolution.
  - Charge resolution ~0.05PE up to 25PE.

Dynamic range requirements: single PE up to 50-100PE

- For E61
  - 0.49% of hits > 50PE
  - 0.13% of hits > 100PE
- Study needed about how much saturated hits would effect energy reconstruction.

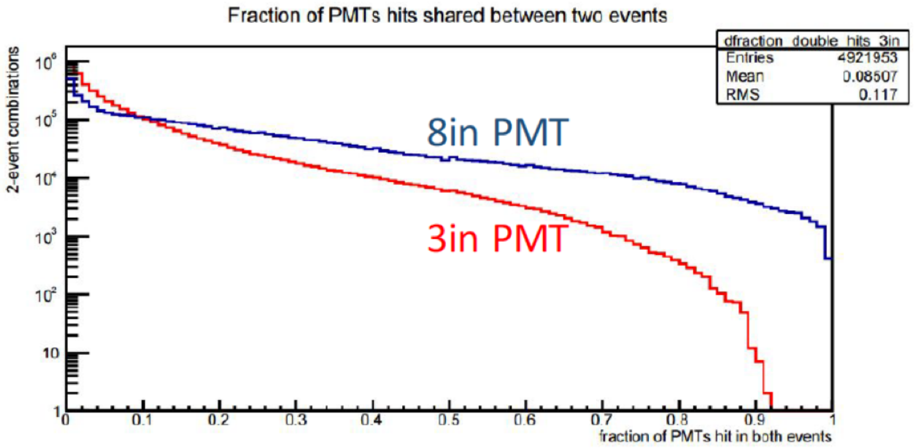


Simulated number of PE per hit for E61 neutrino interactions (improved higher-eff 3” PMTs)

E61 Pile-up Requirements

- J-PARC beam structure:
  8 bunches of ~15ns width, separated by ~600ns.
- Up to 10% of bunches will have two fully contained events (after outer detector veto) for 1^0 off-axis position.
- Single PMTs will often get hit multiple times in the same spill and sometimes multiple times in the same bunch.
- Ongoing studies on separating different events in same bunch.
- At a minimum we need separate measurements for each bunch. More information would be better.

# of pmts hit twice in both events/
# of pmts hit

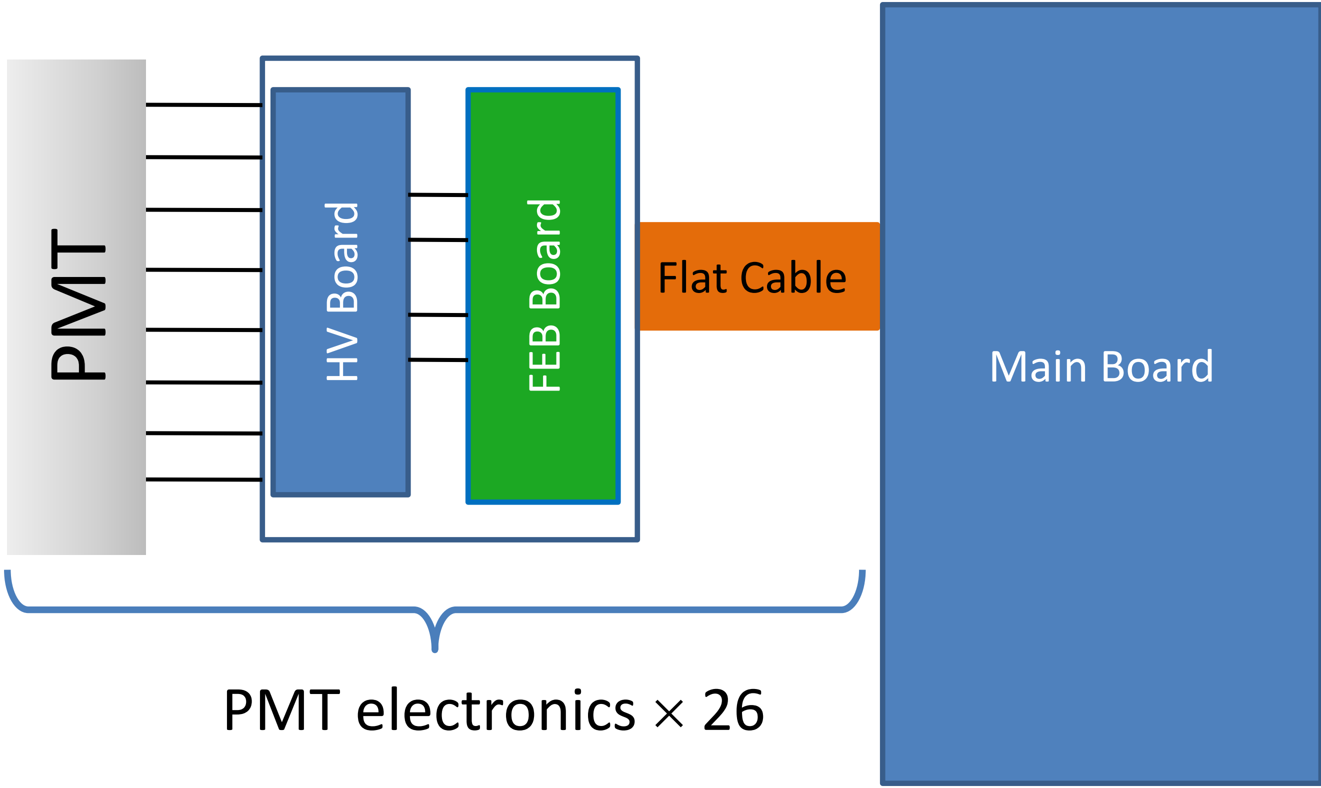


mPMT Electronics Other Requirements

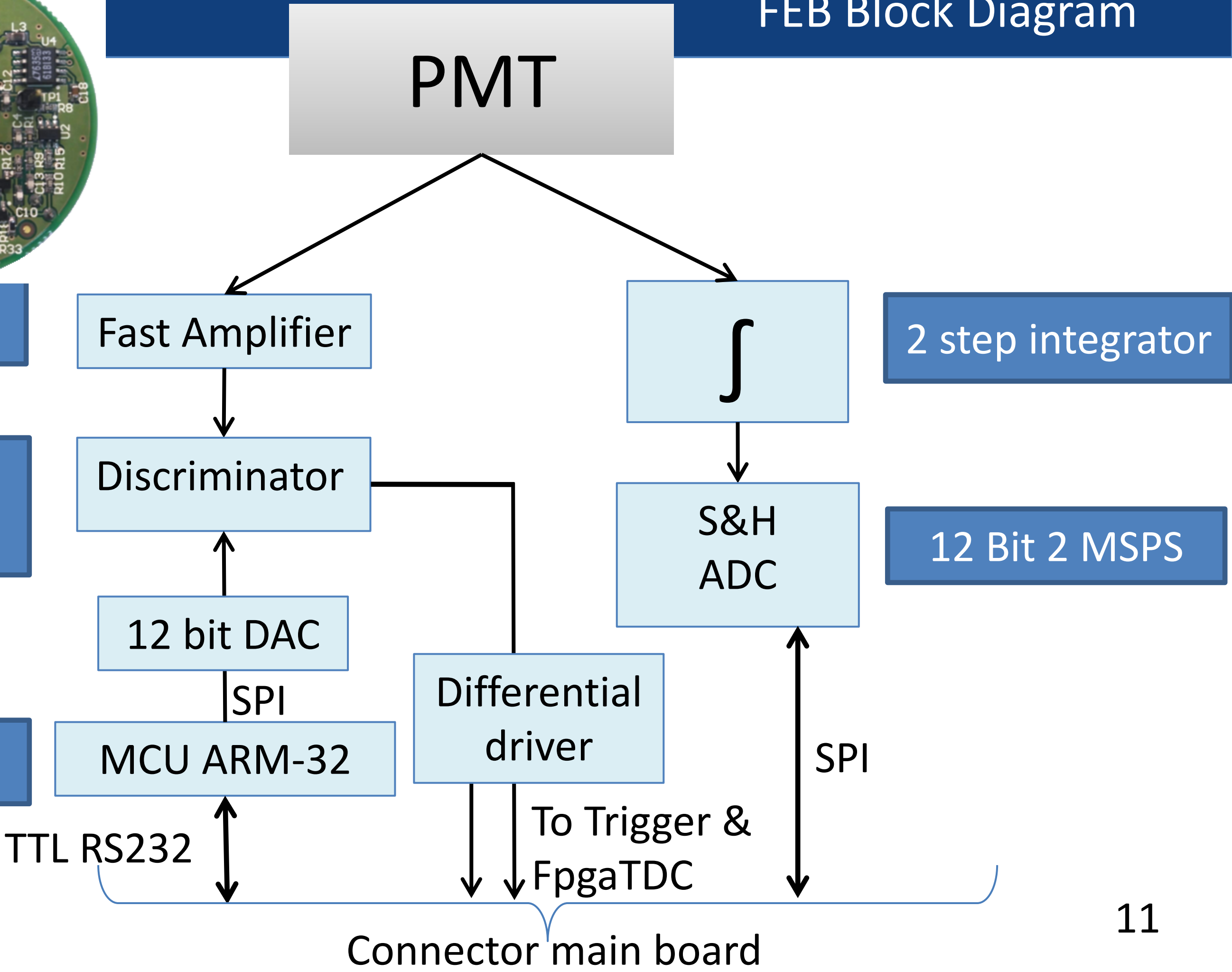
- Power consumption:
  - For Hyper-K <3-4W per mPMT
    - Driven by water circulation requirements
  - For E61 ~5-10W per mPMT
    - Not as strongly constrained as Hyper-K
- Moderately low cost: ideally ~$50 per channel for digitization part.

- Currently working on two different designs for HK/E61 mPMT digitization
    1. Q/T digitization based on discrete components
        - Advantages: simplicity, low power, low cost.
        - Lead by INFN group.
    2. FADC digitization, with on-board signal processing
        - Advantages: fully active during spill and reflections, noise suppression in FPGA.
        - Lead by WUT and TRIUMF groups.
- Ideally use same design for Hyper-K and E61.

- Digitization starts in Frontend Board (FEB) attached to PMT base.

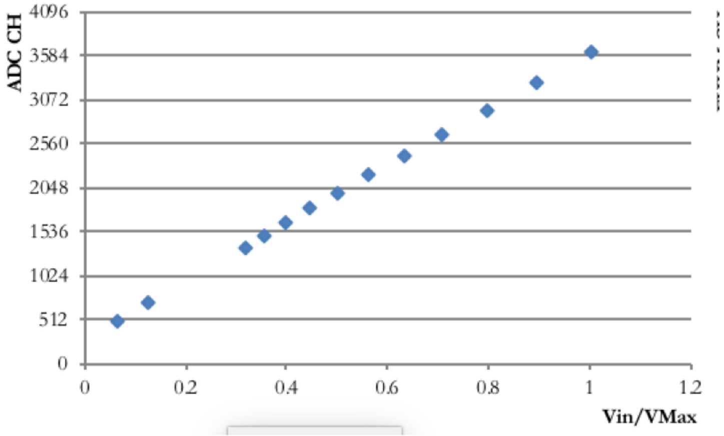


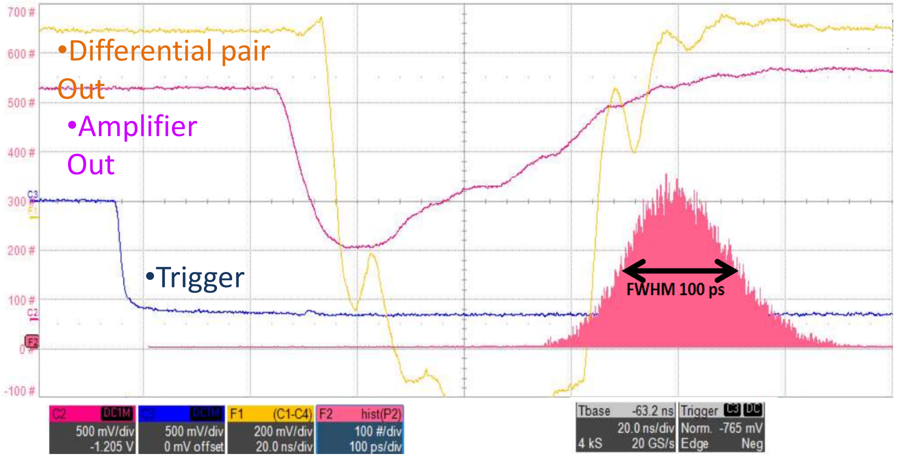
FEB Block Diagram



Q/T Digitization Performance

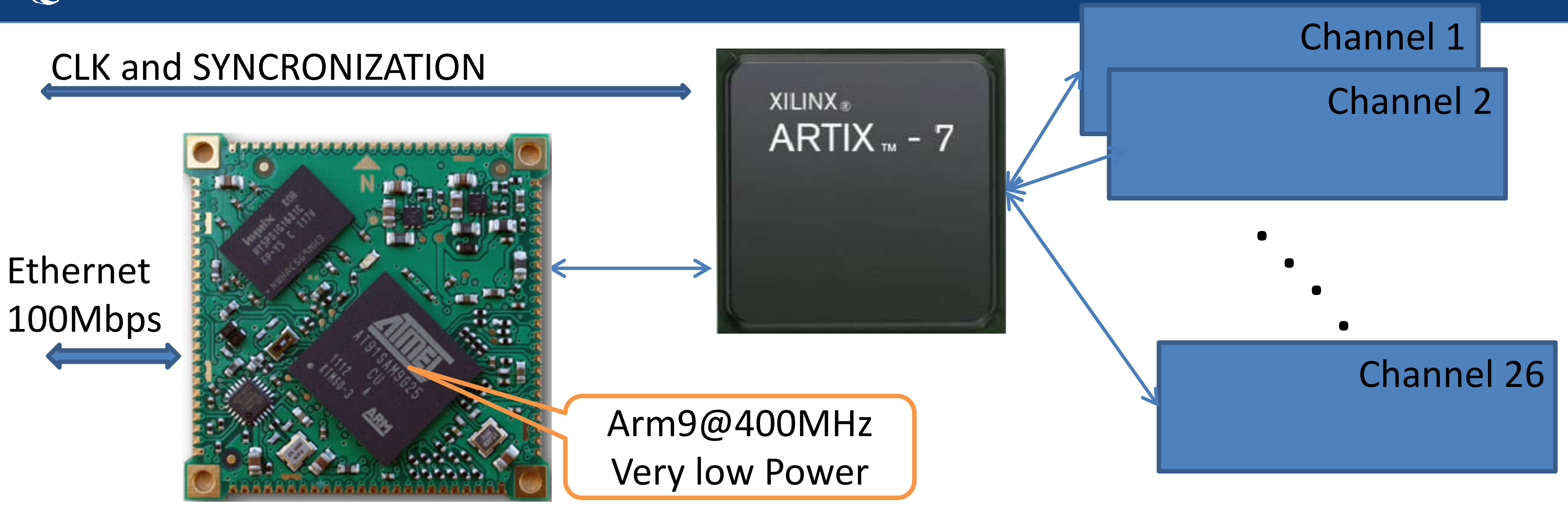
Tests of linearity of charge measurement





Tests of timing resolution of the FEB

Mainboard Overview



Single Board Computer(SBC)-Linux:

N × Single channel Slow control (HV and Threshold set, Current and Voltage monitor)

Data acquisition and transmission

Remote Single channel uP programming /debug

Remote FPGA programming /debug

FPGA Artix-7

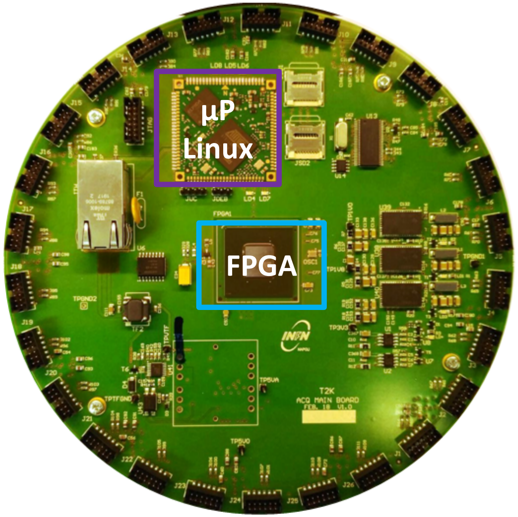
N × Single channel TDC/ADC control

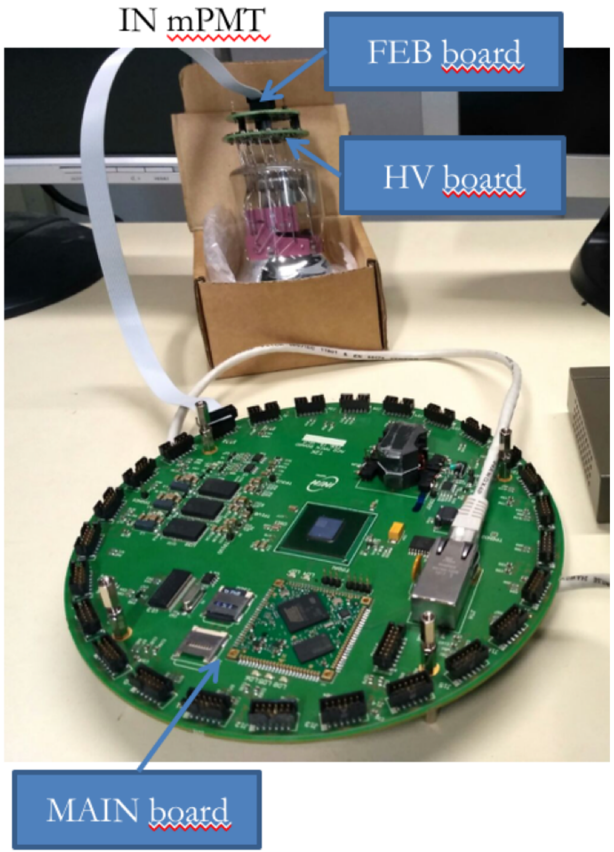
Time stamp (FPGA-TDC)

Trigger logic

Trigger ratemeter

- Prototypes available for PMT base, FEB and mainboard.



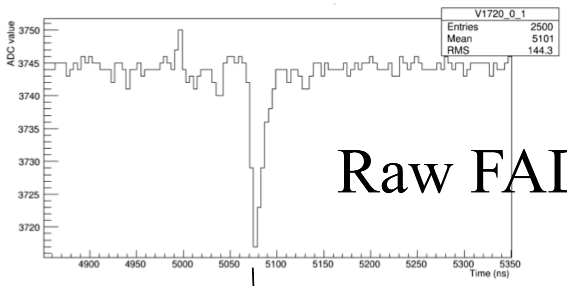


Q/T Digitization Power Estimates

- PMT HV: 12.5mW / ch, 250mW per mPMT
- FEB: 40.5mW / ch, 810mW per mPMT
- Mainboard (uP + FPGA + comm): ~3W
- Total: ~4.1W

Design 2: FADC Digitization Overview

- FADC continuously processed with FPGA; finds hits and send pulse summary to backend.
  - Pulse summary is either just Q/T (for small pulses) or a set of ADC samples (for large pulses).
- FPGA data processing also allows for more sophisticated techniques for noise suppression.
- Challenges:
  - Ensure we can meet timing resolution and dynamic range requirements.
  - Possibly high cost & power.



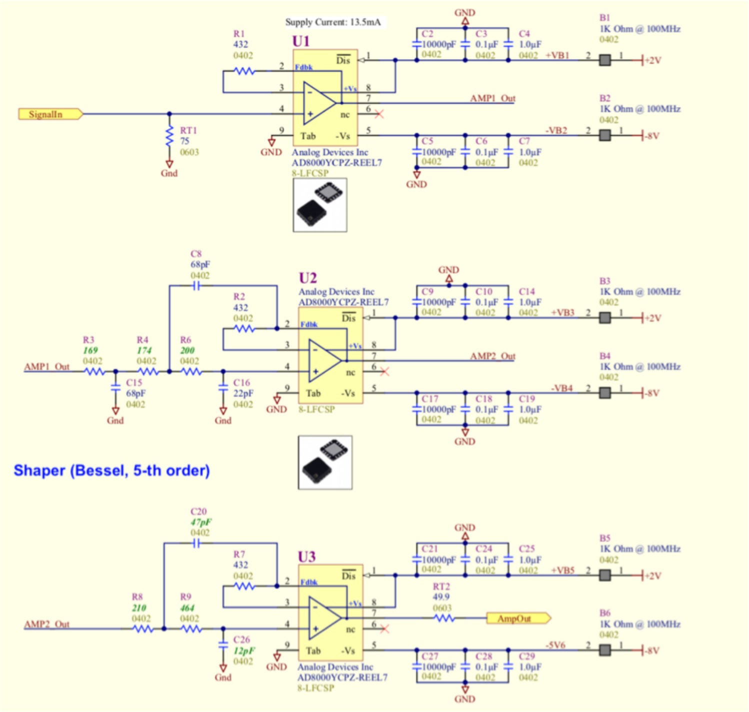
Raw FADC data

Process FADC waveform in FPGA on mPMT

Pulse charge/time or ADC samples

Backend computer

- Current shaper design:
  - 5-th order Bessel filters (smooth impulse response)
  - Optimized for 100 MSPS system, with rise time = 15 ns or 30 ns.
- Still optimizing design and considering other options.



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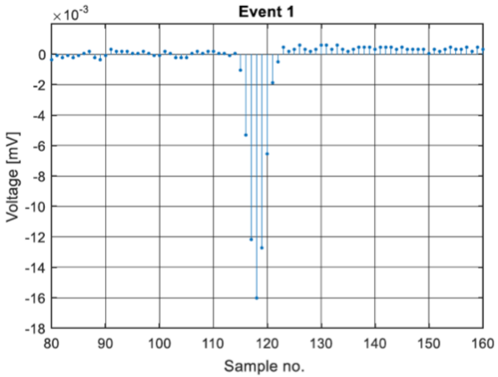
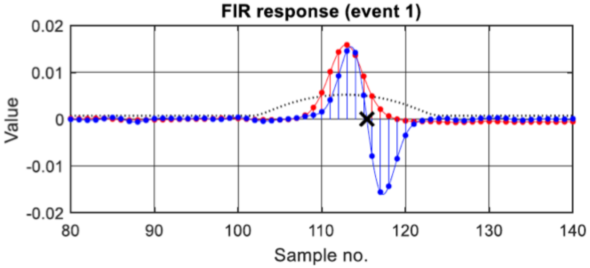
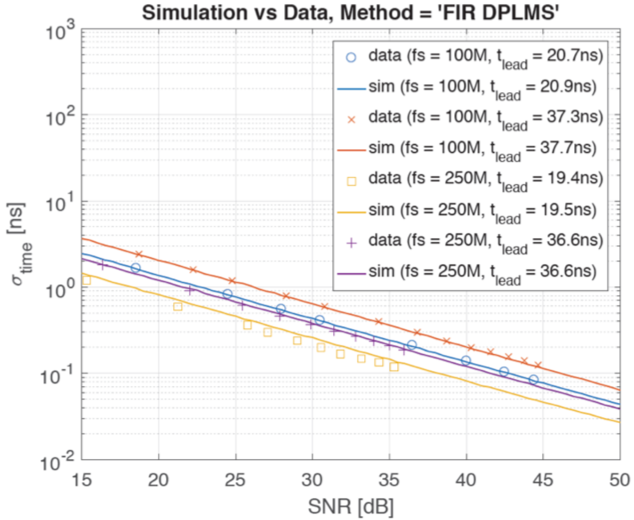
Techniques for extracting hit time

- Tested different techniques for extracting hit time.
- Constant Fraction Discriminator or Finite Element Response (FIR) can be implemented in FPGA.
- Find that FIR filtering gives timing resolution that is slightly worse than by fitting pulses



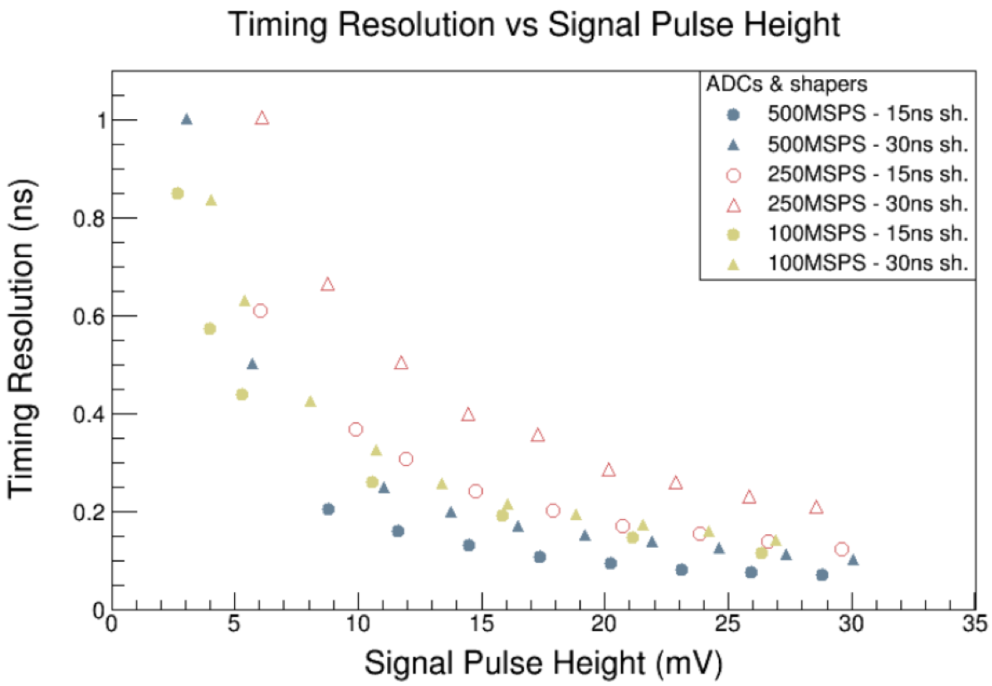


Timing resolution using FIR filtering on waveform



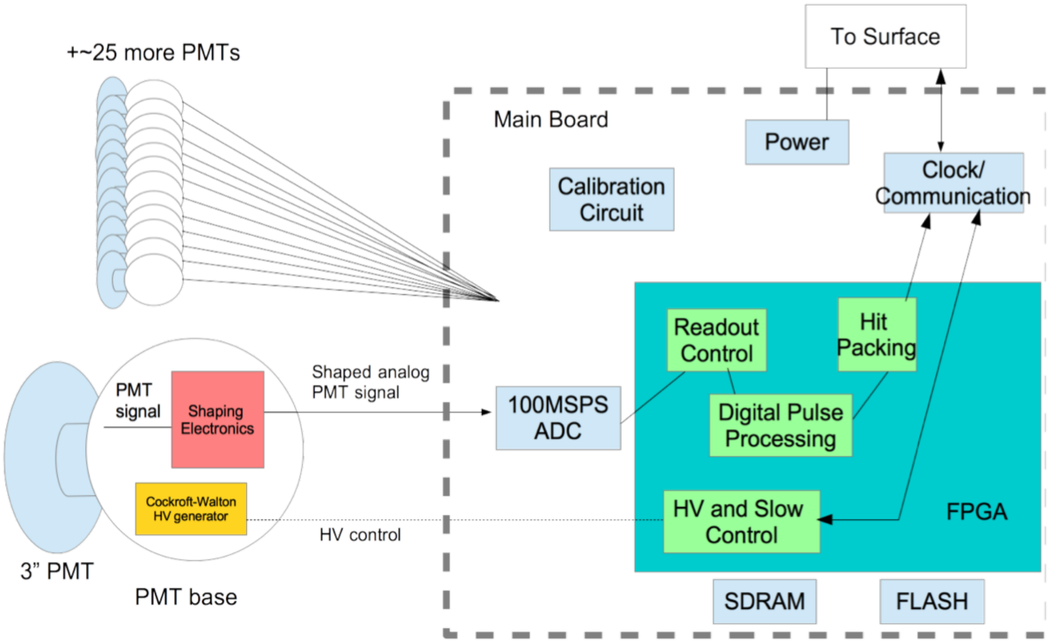
Timing Resolution for FADC Digitization

- Tests of performance with different CAEN ADCs:
  - 100MSPS 14bit
  - 250MSPS 12 bit
  - 500MSPS 14 bit
- Assume 1PE pulse is 5mV high -> ~0.5ns timing resolution from electronics.
- With 2V ADC get 0-400PE dynamic range.



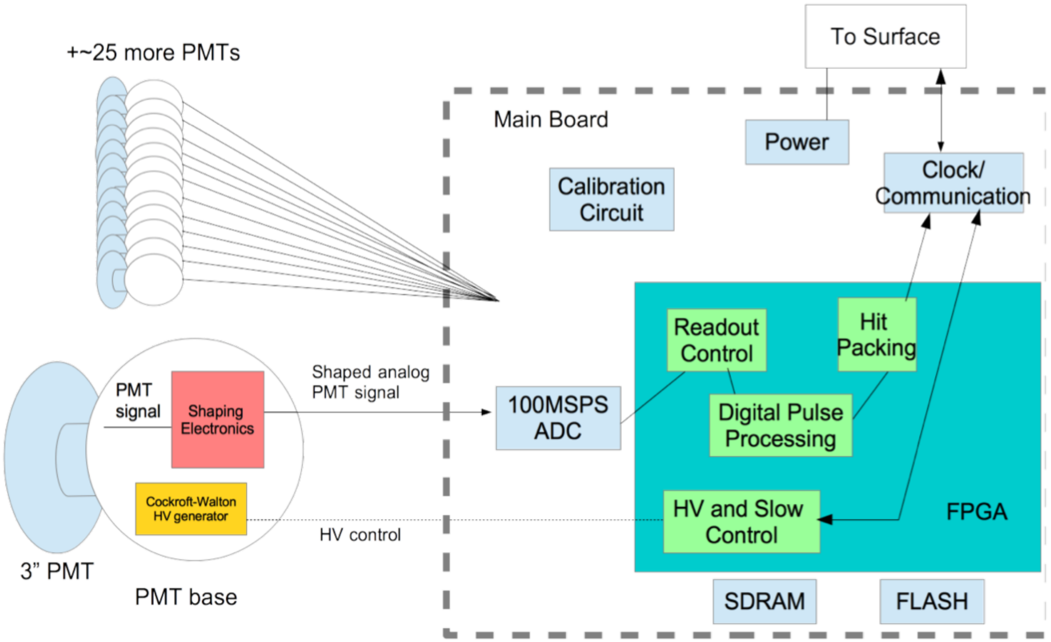
FADC Electronics Design

- 100—200MSPS ADC on mainboard.
- Need to test that cable doesn't degrade noise performance.
- Hope to produce prototype over next year.

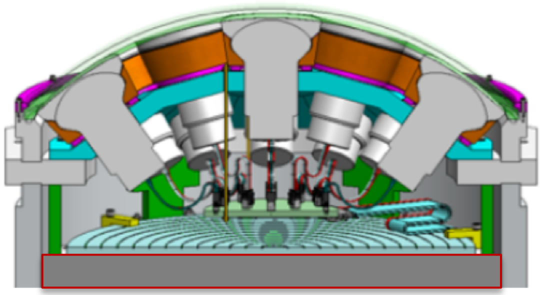


FADC Electronics Design

- Power: aim for ~100mW per channel for ADC: ~2-3W for mPMT digitization.
  - Higher than sample/hold measurement.

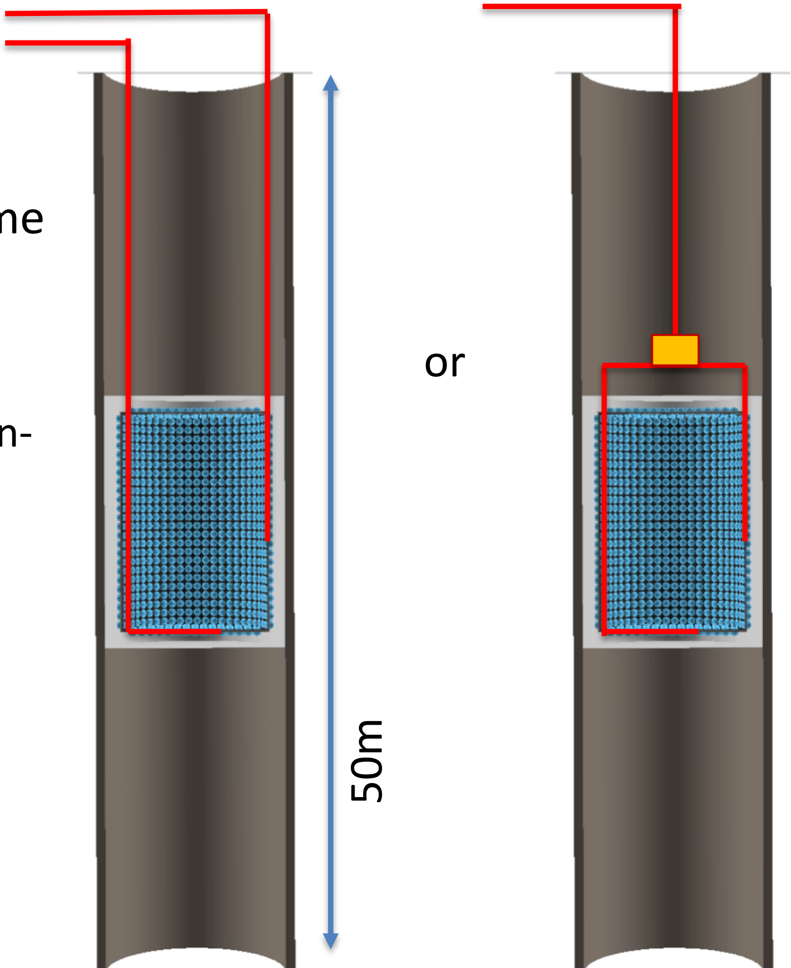


- Depends strongly on design of mPMT
- Considering option with just half mPMT; metal plate on backside of mPMT would provide good cooling path to water.



Cable lengths

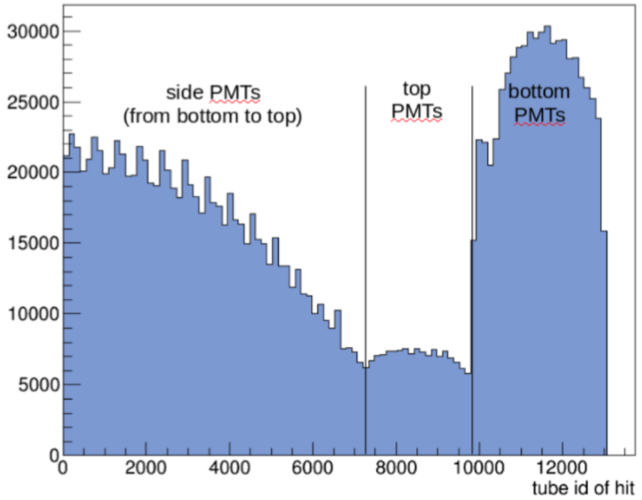
- E61 mPMT cable lengths:
  - nominal pit depth of 50m.
    - ~80m for direct cable routing and some safety factor.
    - Could be shorter if we concentrate cables above the detector
      - Concentration could be in-water or in-air.
- Hyper-K mPMT cable lengths:
  - Nominal ~100m cable run from mPMT to backend.
  - Potentially cable concentration in water to reduce cable count to backend.



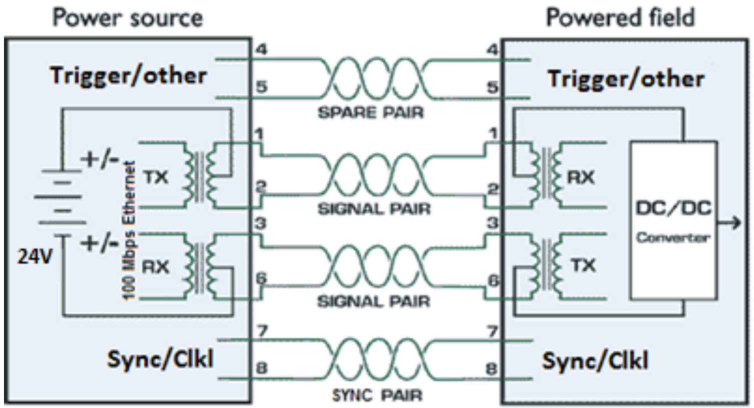
Data Transfer and Rate Estimates

- Nominally want to save every hit and send to backend computers
- For Hyper-K this should be ok; hit rates dominated by dark noise and relatively low.
  - but need to be able to buffer the large rate of events during nearby supernova.
- For E61 hit rates will be dominated by hits from cosmic-rays (particularly when detector is at top of pit).
  - Assume 24bytes per hit, saving 10 ADC samples.
  - Estimate ~2MB/s from each mPMT, higher for mPMTs at bottom of detector.

E61 Hit rates as a function of mPMT position.



- Investigating two different options for mPMT cabling for power, clock, communication at triggering.
  1. White rabbit optical cable for clock and communication; separate cable for power.
     - Seems to work well for many other projects.
     - Need to understand cost and power requirements.
  2. Single cat-6 style cable.
     - 100Mbps data limit.
     - 100m limit for copper ethernet
     - Water-tightness?
- Need some specialized equipment on backend in either case.



Conclusion

- Key drivers of E61/HK electronics design:
  timing performance, dynamic range and cost.
  - Power is important, but not as critical as KM3NET and ICECUBE.
- Working on two alternate schemes for mPMT digitization:
  - Sample/Hold prototypes working and being tested.
  - FADC digitization gives more information, but at higher cost and power.
- Deciding on clock, communication, power scheme is important for moving forward.

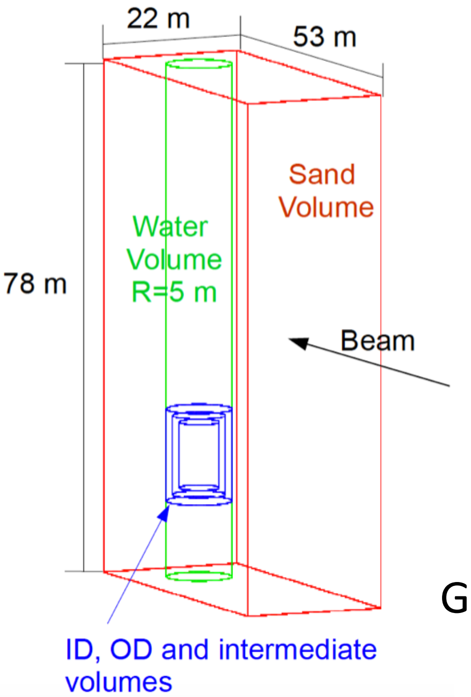
Backup Material

E61 concept

- Measure neutrino interactions at different off-axis angles -> different energy spectrums.
- WC detector moves up/down in 50m shaft.
  - Detector:
    - 8m diameter inner diameter
    - 8-12m high

Event rates per microbunch for E61 with horn currents at 320 kA and ID radius of 4 m before any cuts.
For detector at 1km from production target.

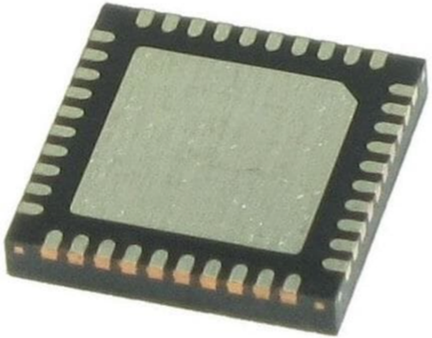
	Interaction Outside OD			Interaction Inside OD			Interaction Inside ID		
	Producing light in:								
Off-axis Angle (°)	OD only	ID only	ID & OD	OD only	ID only	ID & OD	OD only	ID only	ID & OD
0.0-0.6	0.612	0.004	0.488	0.763	0.007	0.265	0.008	0.807	0.479
1.0-1.6	0.193	0.001	0.147	0.227	0.002	0.079	0.002	0.227	0.134
2.0-2.6	0.061	0.000	0.044	0.077	0.001	0.026	0.001	0.084	0.042
3.0-3.6	0.025	0.000	0.016	0.033	0.000	0.011	0.000	0.036	0.015



Geant4 pile-up simulation

- TI ADC 3424
- Quad 125MSPS ADC
- 12 bit (11.4 ENOB)
- Power 98mW per channel
- ~$17 USD per channel

- AD LTC2260-12
- Single 125MSPS ADC
- 12 bit
- Power 146mW per channel
- ~$36 USD per channel



- Two separate analog memories per channel; during digitizationof first pulse, other analog memory can store second incoming pulse.
  - Readout of hole chip happens at the same time.
- Get problems when multiple extra pulses in 3-10us after first pulse.
- During spill we will often have multiple hits per mPMT during the 5us spill period.
- Chances are high that the chip will be busy for the later hits.
- CATIROC has slow shaped pulse outputs and trigger outputs of each channel. Could digitize them to handle pile-up cases; but not ideal.