JUNO
(SPMT readout electronics)

NEPTUNE Workshop
INFN / Università Napoli — Napoli (Italia)

Anatael Cabrera
on behalf of the SPMT group
CNRS / IN2P3 @ APC (Paris) — LNCA (Chooz)

LPMT⊕SPMT complementarity systems…

Large PMT (LPMT)
(~18,000 20" PMT)

Small PMT (SPMT)
(~25,000 3" PMT)

20 laboratories (9 countries) so far...

our (international) team...

Armenia
- Yerevan Physics Institute (Yerevan)

Brasil
- FABC (Sao Paulo)
- PUC (Rio de Janeiro)

Belgium
- UBL (Brussels)

Chile
- PUC (Santiago) **(project/physics coordination)**

China
- IHEP (Beijing) **(project/physics coordination)**
- SYSU (Guangzhou)

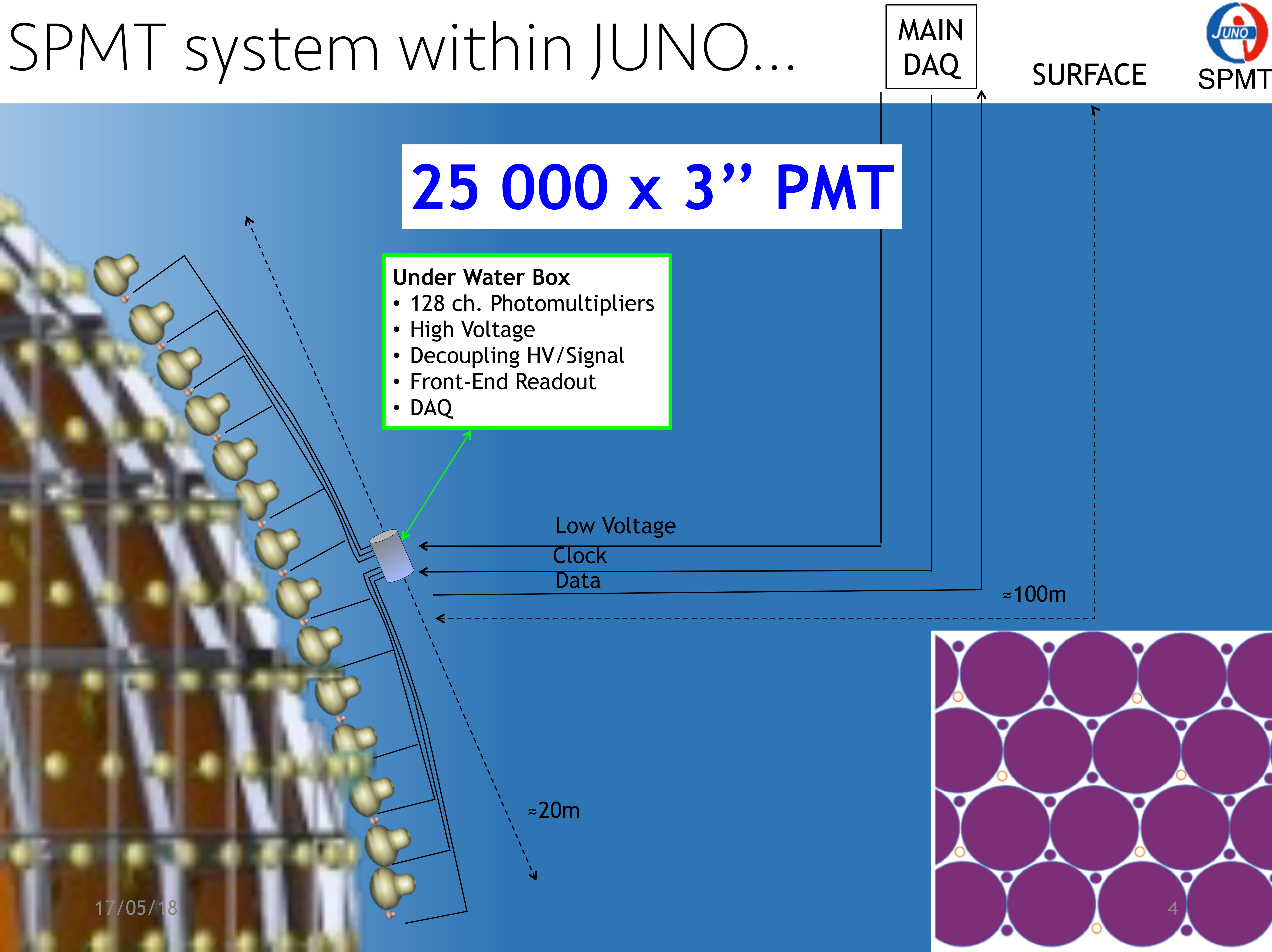
France
- APC (Paris) **(project/physics coordination)**
- CENBG (Bordeaux) **(technical coordination)**
- CPPM (Marseille)
- LLR (Paris)
- OMEGA (Paris)
- SUBATECH (Nantes)

Italy
- Padova-INFN (Padova)

Russia
- Moscow State University (Moscow)
- Institute of Nuclear Research & Russian Academy of Science (Moscow)

Taiwan
- National Taiwan University NTU (Taipei)
- National Chiao Tung University NCTU (Hsinchu)
- National United University NUU (Miaoli)

SPMT system within JUNO…



the SPMT ingredients…

3" PMT
(industrial)

MARCO'S TALK: STEREO CALORIMETRY
BEDA'S TALK: PHYSICS SPMTS

CEDRIC'S TALK: SPMT FULL SYSTEM
LI'S TALK: 3" PMTS
WEI'S TALK: 20" PMTS

design criteria:
- simple
- **high reliability**
- **industry-driven**
- installation (JUNO)
- recycle/integration (JUNO)

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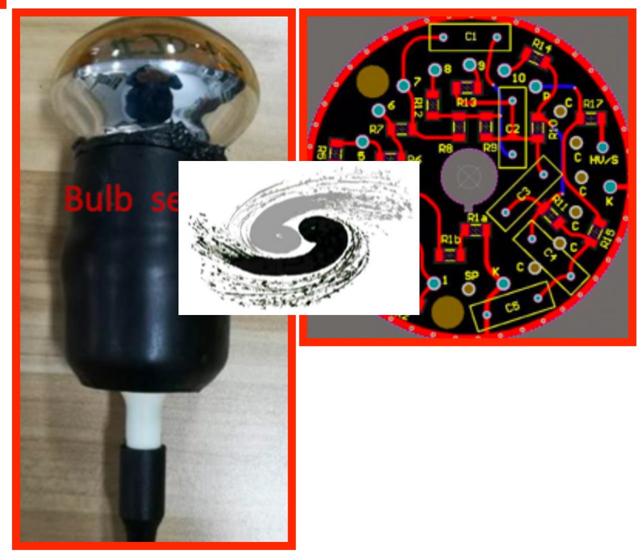

PMT HW
(same LPMT)

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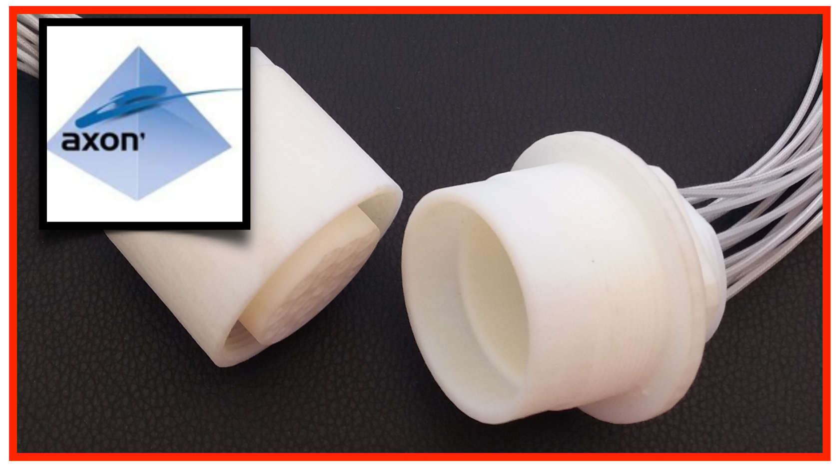

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Anatael Cabrera (CNRS-IN2P3 & APC)

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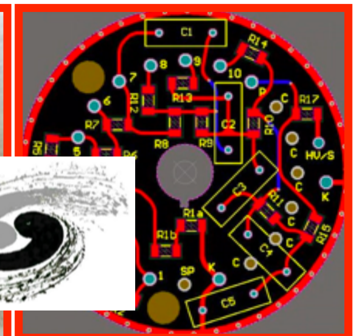

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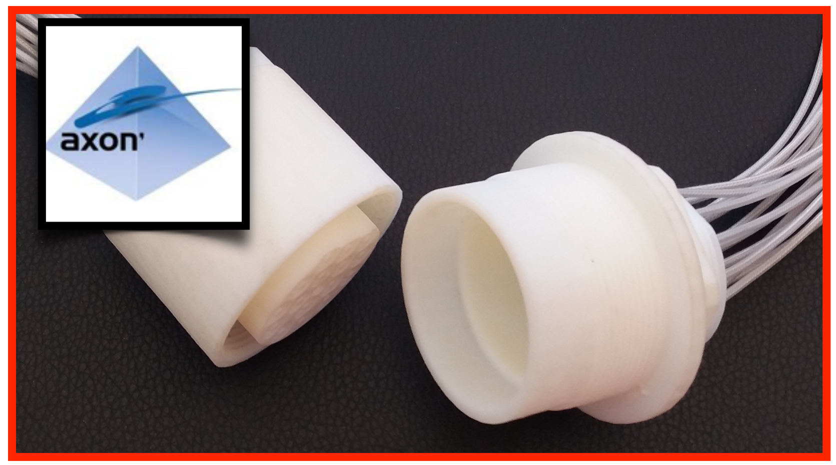

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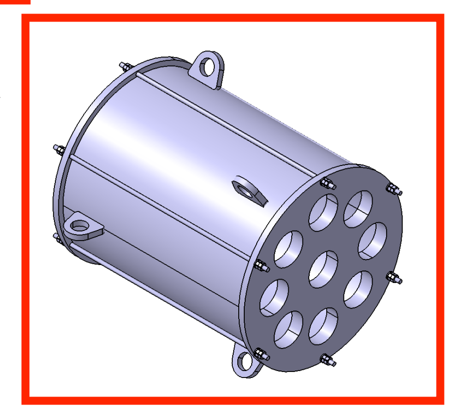
underwater housing
(academic)



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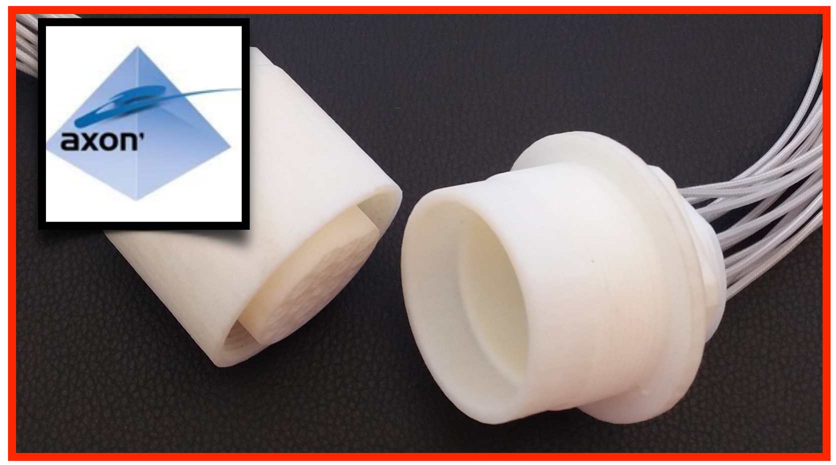

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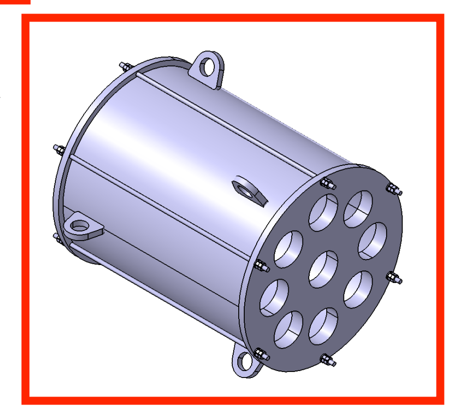
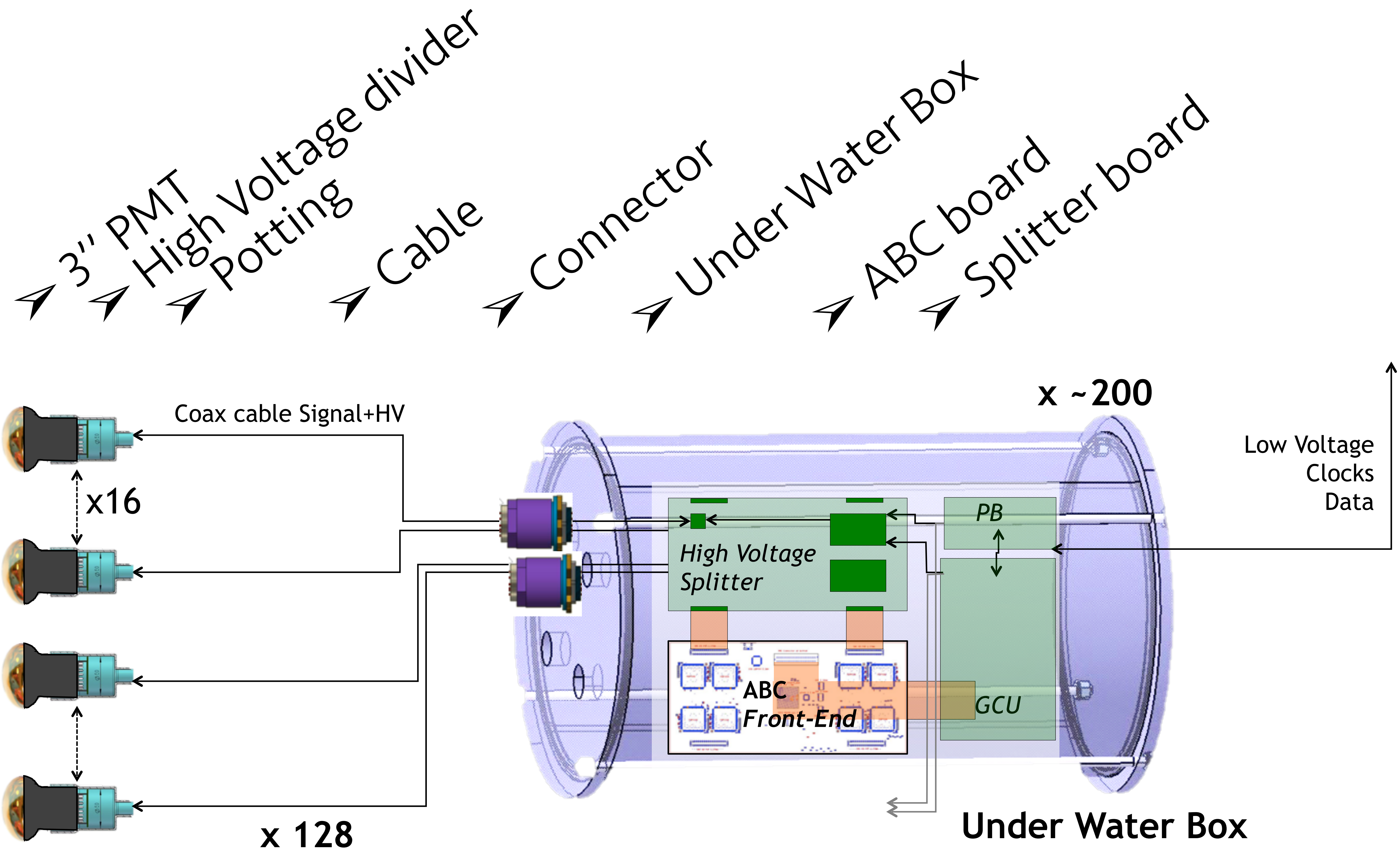


electronics
(academic)

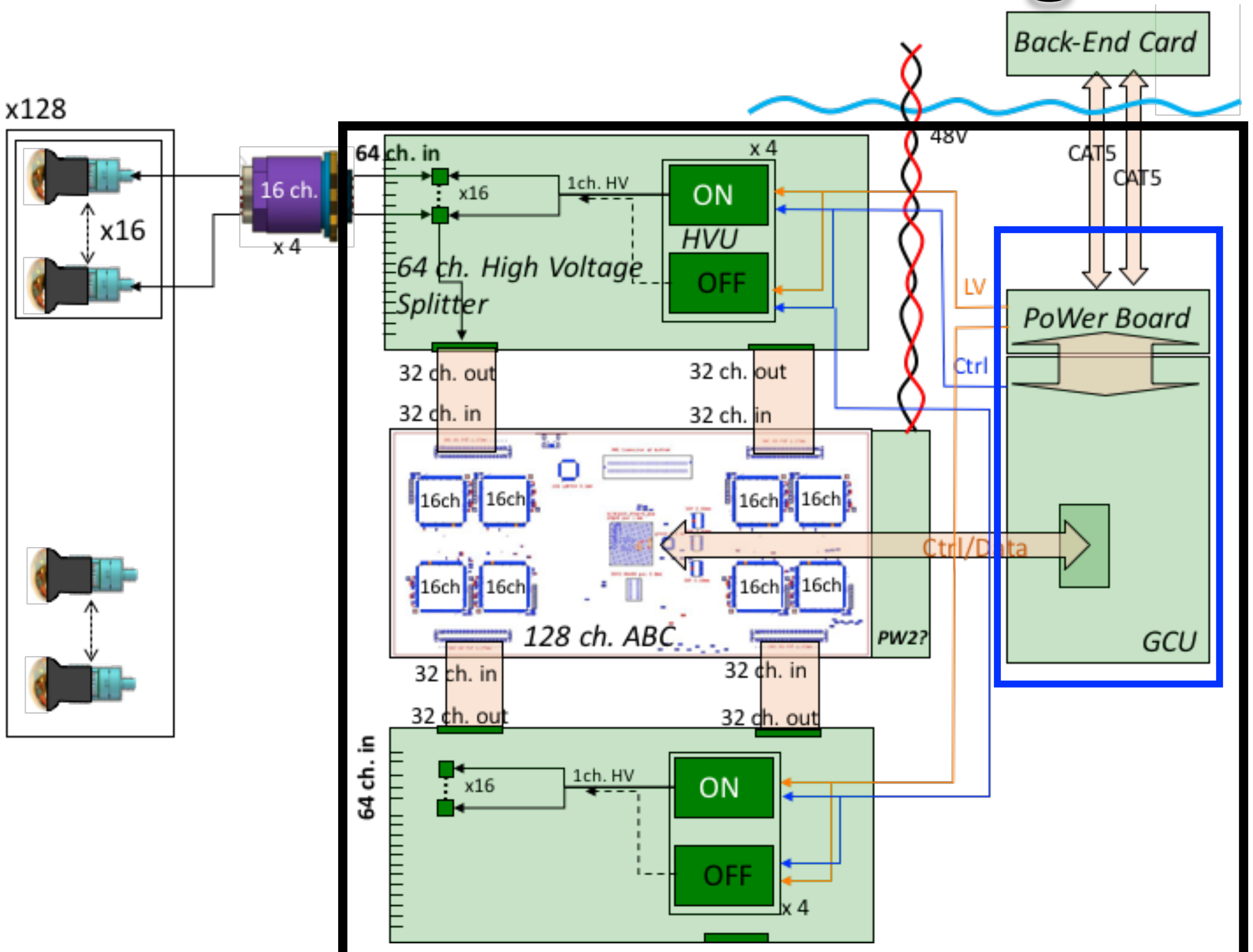
Anatael Cabrera (CNRS-IN2P3 & APC)

System schematics

our construction brick

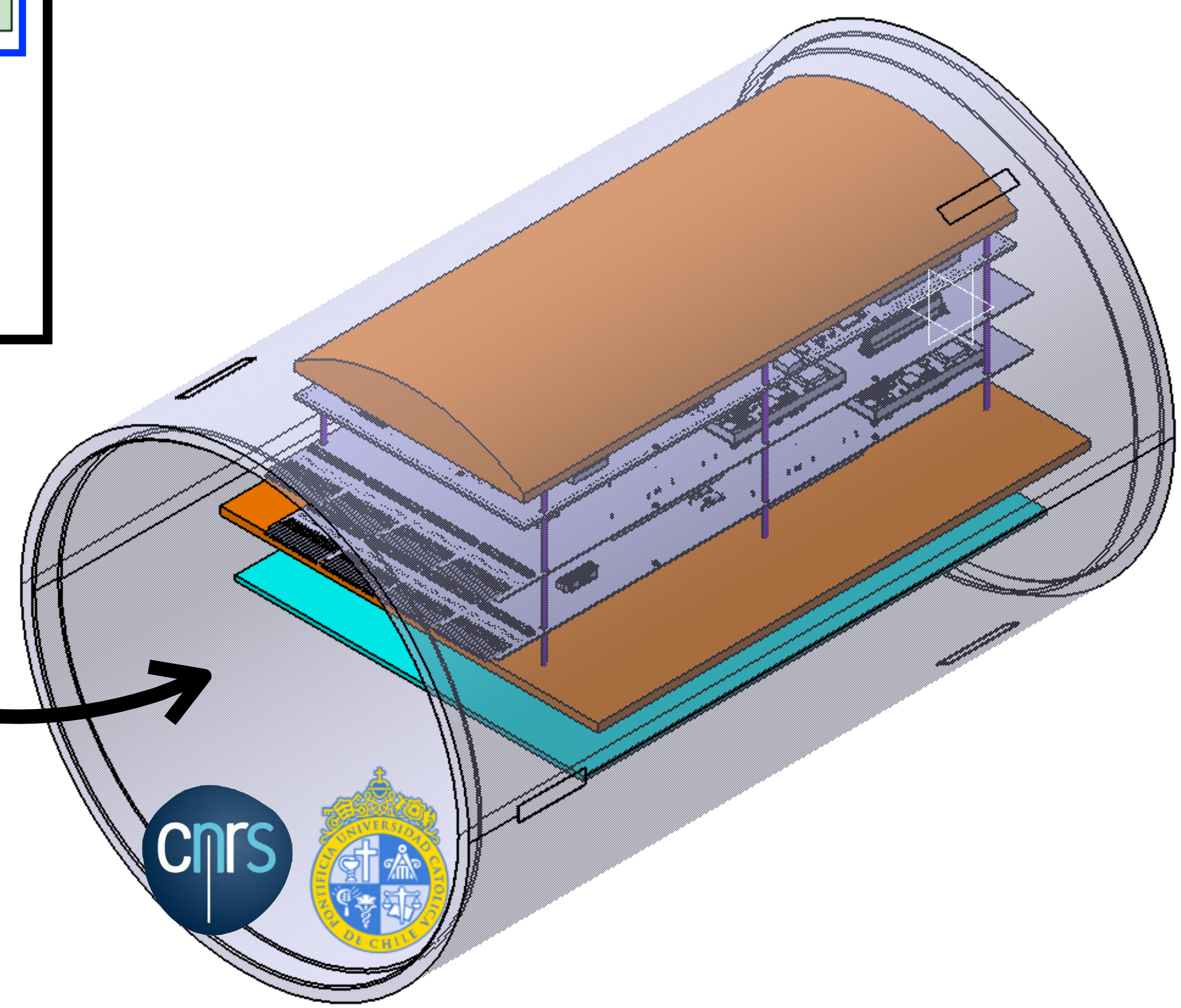


the readout goes (folded) under-water…



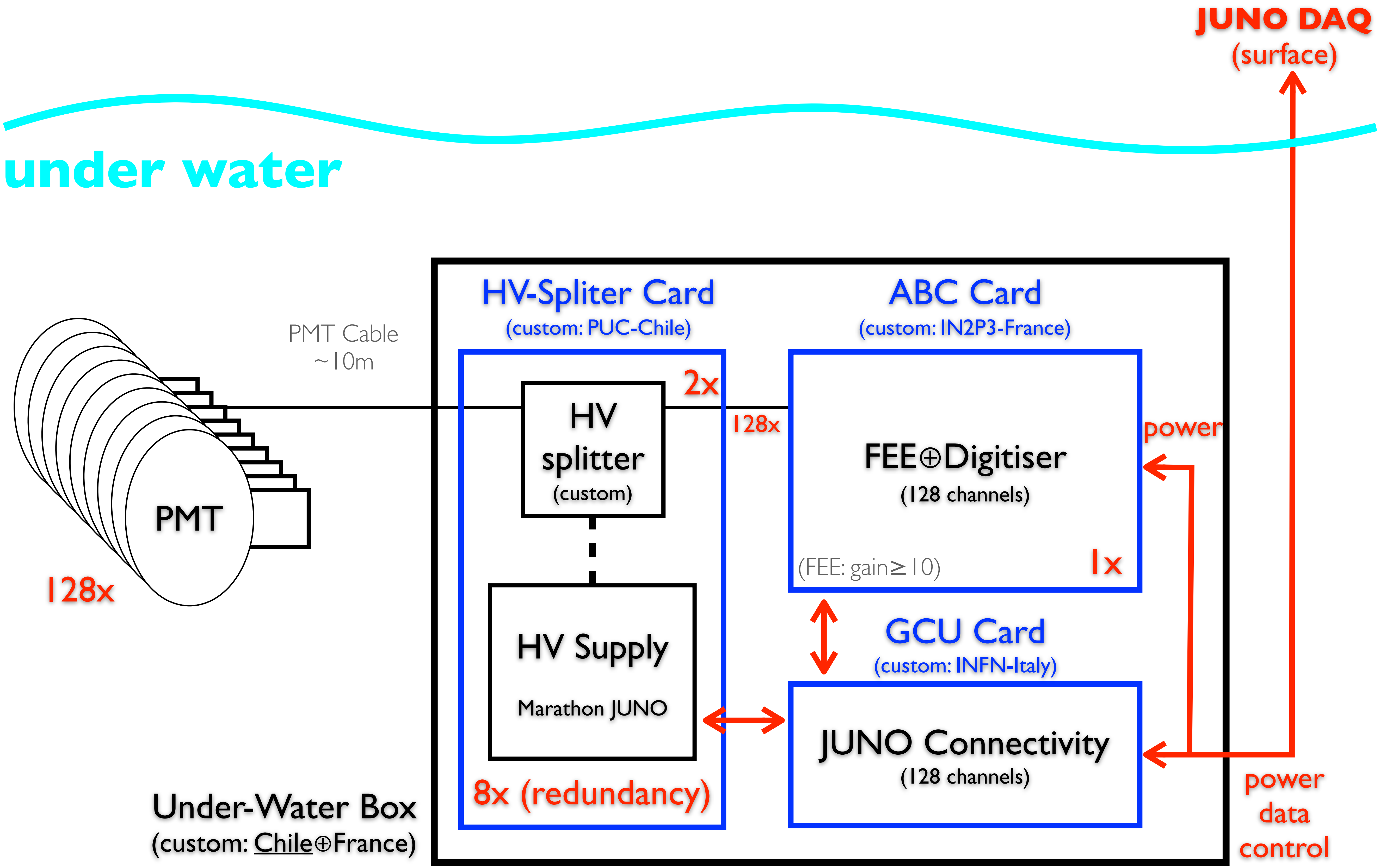
JUNO common
(SPMT⊕LPMT readout)

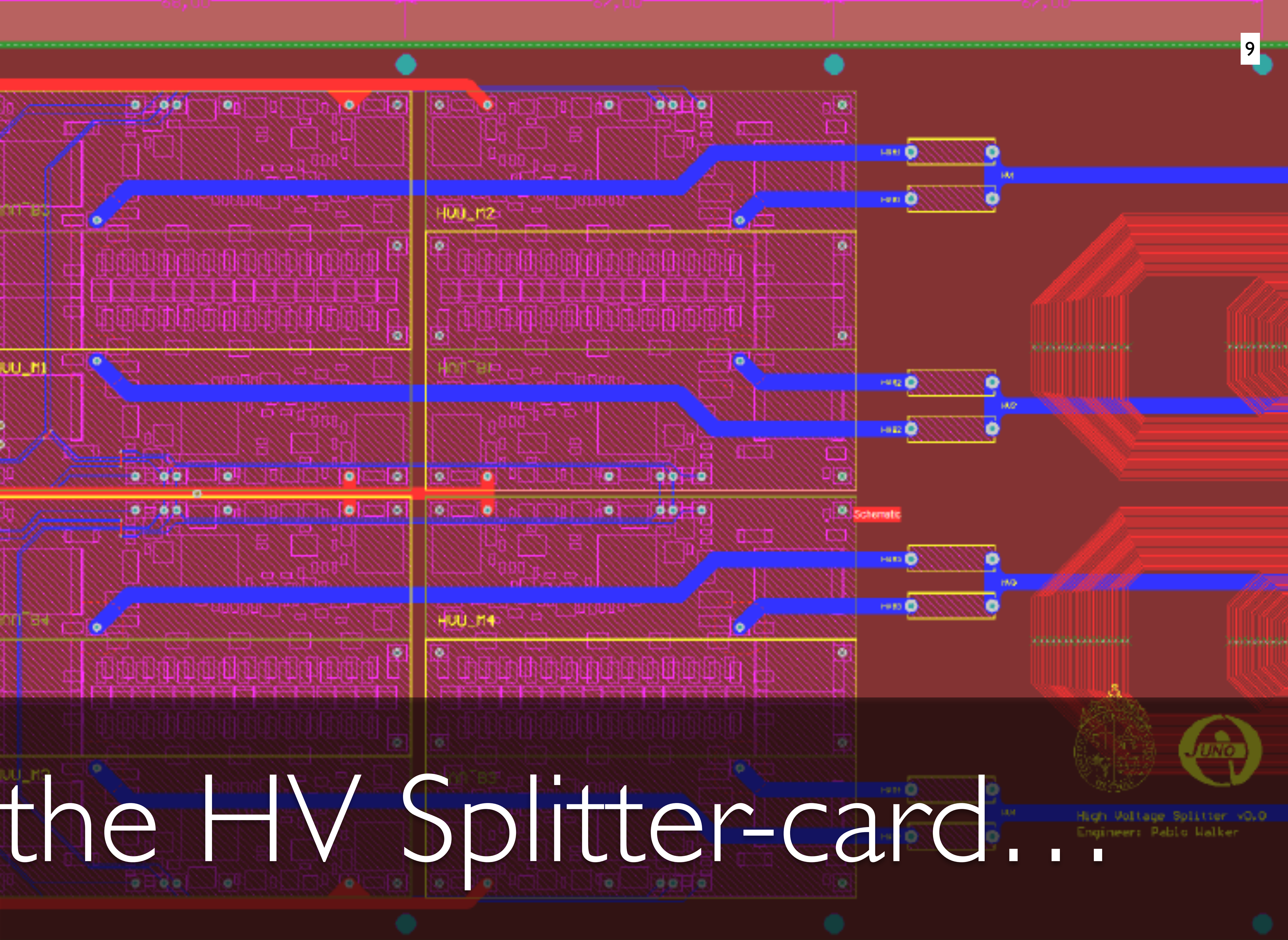
underwater box



Anatael Cabrera (CNRS-IN2P3 & APC)

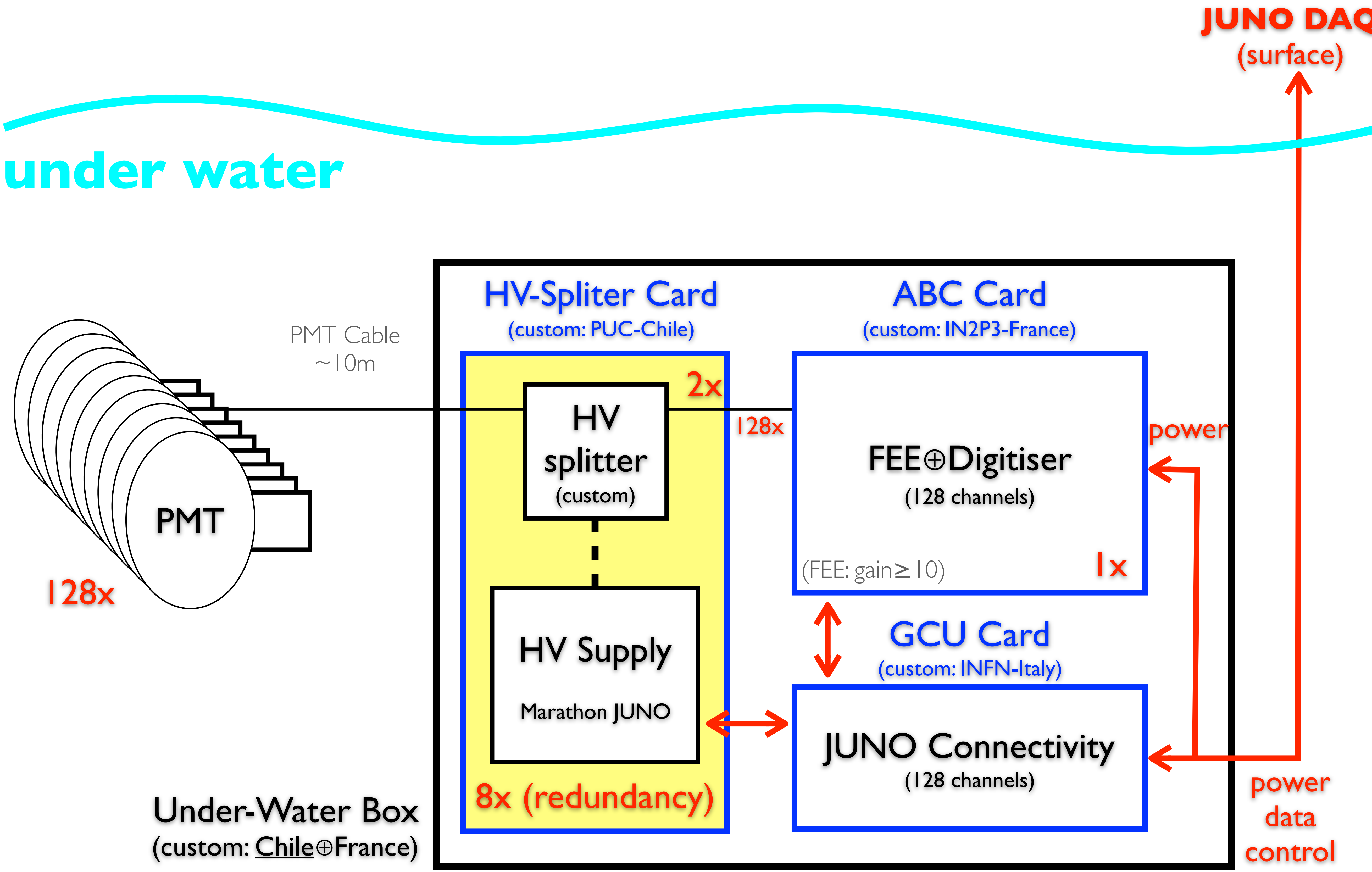
SPMT logic readout diagram…





the HV Splitter-card…

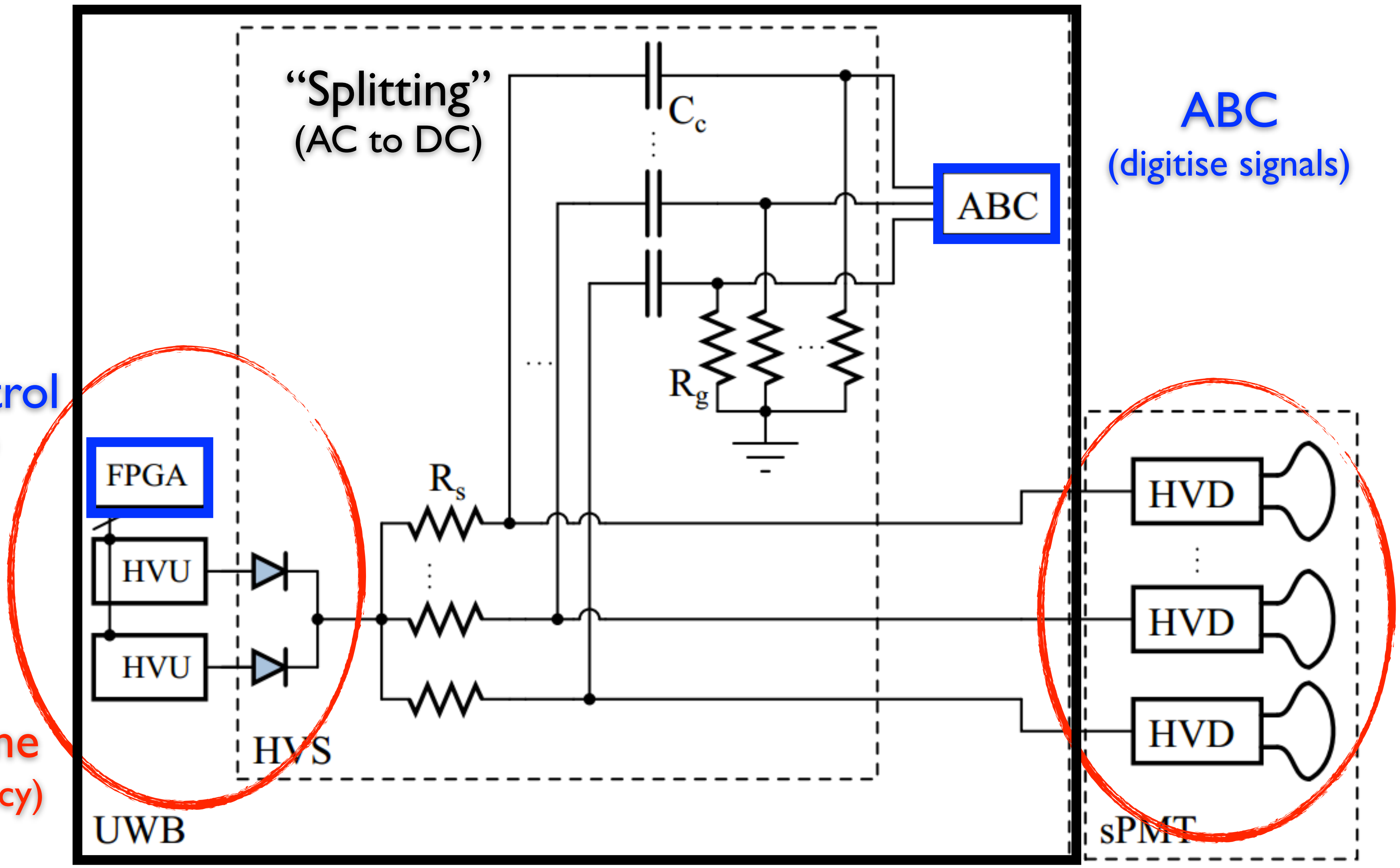
SPMT logic readout diagram…



card logic (3 channel example)…

GCU control
("FPGA")

2 HV per line
(cold redundancy)



ABC
(digitise signals)

Under-Water Box
(custom: Chile⊕France)

16 SPMTs
(per HVU)

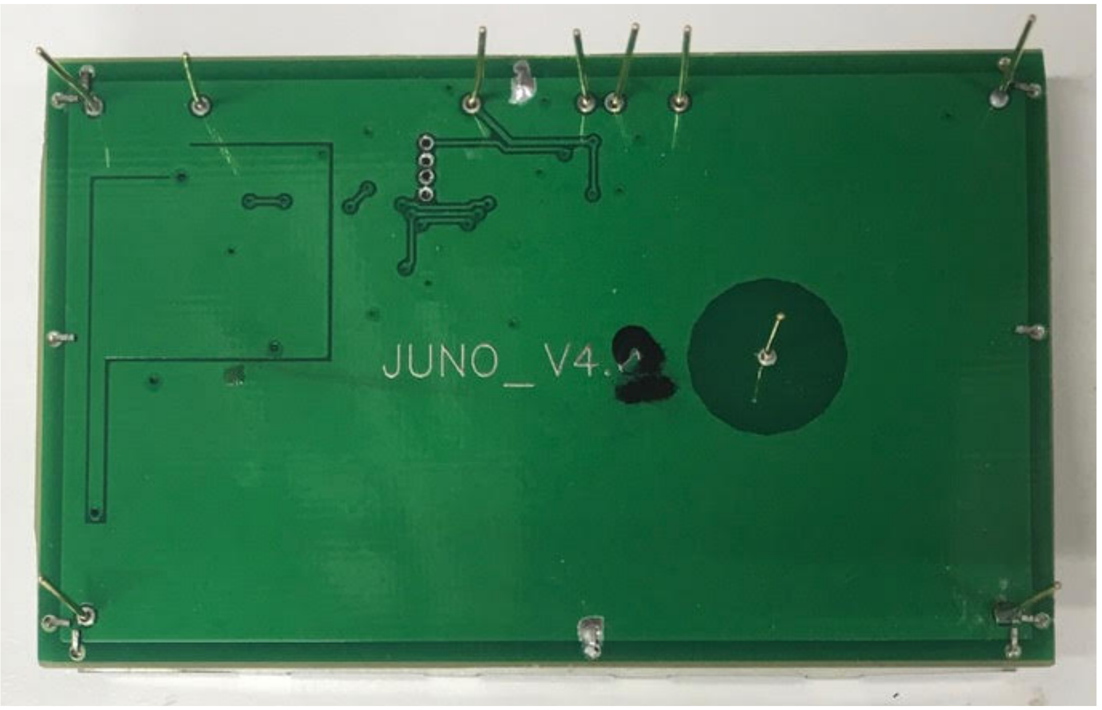
switch on/off
(under finalisation)

(test-bench with 3SPMTs)

packed PMTs based on their HV responses (similar gain)

the HV-unit (JINR+Moscow State University)…

HV-unit (same as LPMT): **generate HV** from low voltage (≤40V) **inside UWB**
(drive 16 3" PMT [current ≤10μA via voltage divider design])



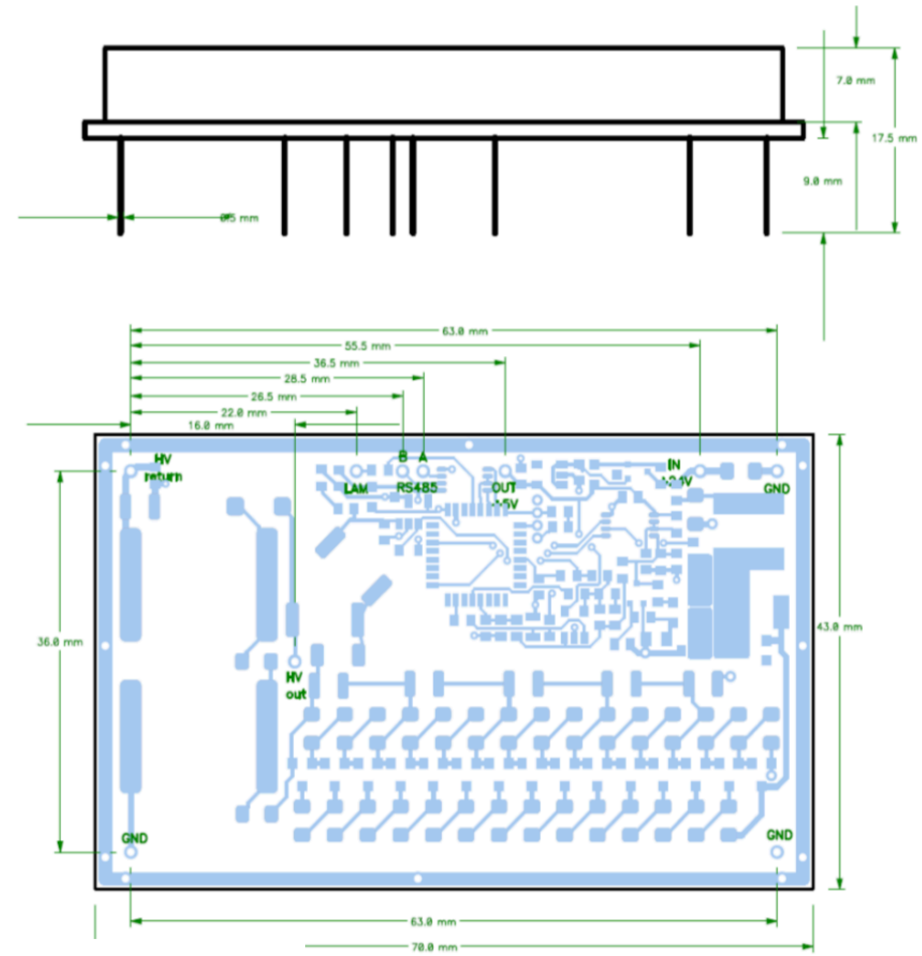
HV-unit going through special conditions in JUNO:

- **high reliability design** (components, pre-burning strategy, etc) [SPMT & LPMT]
- **cold redundancy switching** (2 HV-units per 16 3" PMTs)

intense testing ongoing & units being tested within LPMT+SPMT systems

HV-unit further details (MARATHON)…

The design and prototyping of HVU resulted in the following dimensions and input/output pin layout

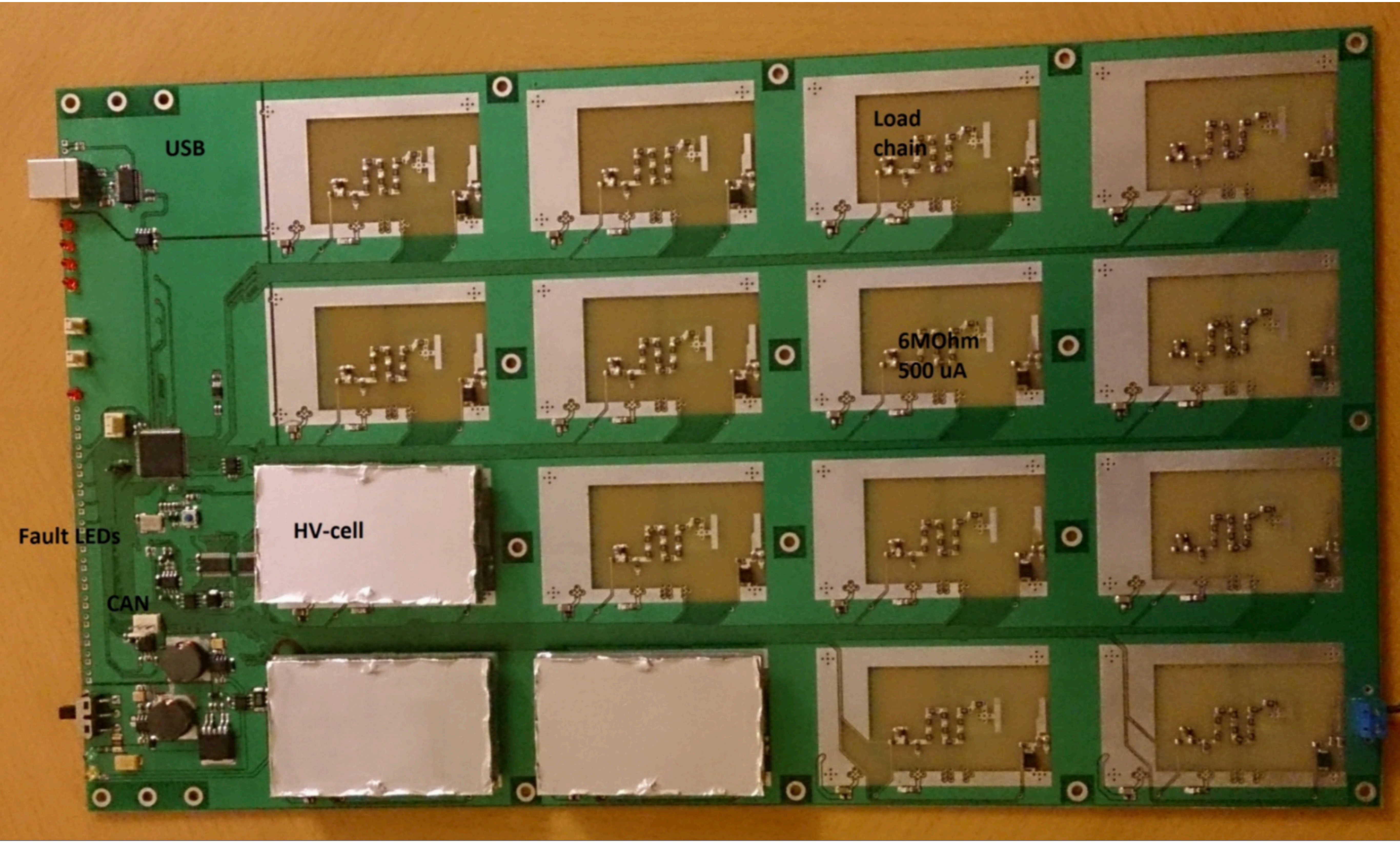


Pin Name	Pin Description
IN +24V	Power supply input pin (+24V/100 mA max)
OUT +5V	Auxilary power supply output pin (+5V/5 mA max)
GND	Power ground pins
HV out	HV output pin (Up to +3000 Vdc/300 mkA max)
HV return	HV output ground pin (Analog ground)
LAM	Look At Me signal
A RS-485	RS-485 transceiver Noninverting input/output
B RS-485	RS-485 transceiver inverting input/output

№	Parameter	Value
1	Polarity (grounded)	Positive (cathode)
2	Range of HV regulation (V)	1500-3000
3	Step of HV regulation (V)	0.5
4	Ripple (Vptp)	0.01
5	Systematic error of HV (%)	3
6	Stability of HV (%)	0.05
7	Temperature coefficient of HV (ppm/degree C)	100
8	Maximum output current (mkA)	300
9	Input voltage (V)	24
10	Remote interface	RS485 (half duplex)

At 2000V an Internal Power Consumption of HVU is ~0.3W, i.e., ~1W for the board with 3 HVU.

HV card units mass testing…



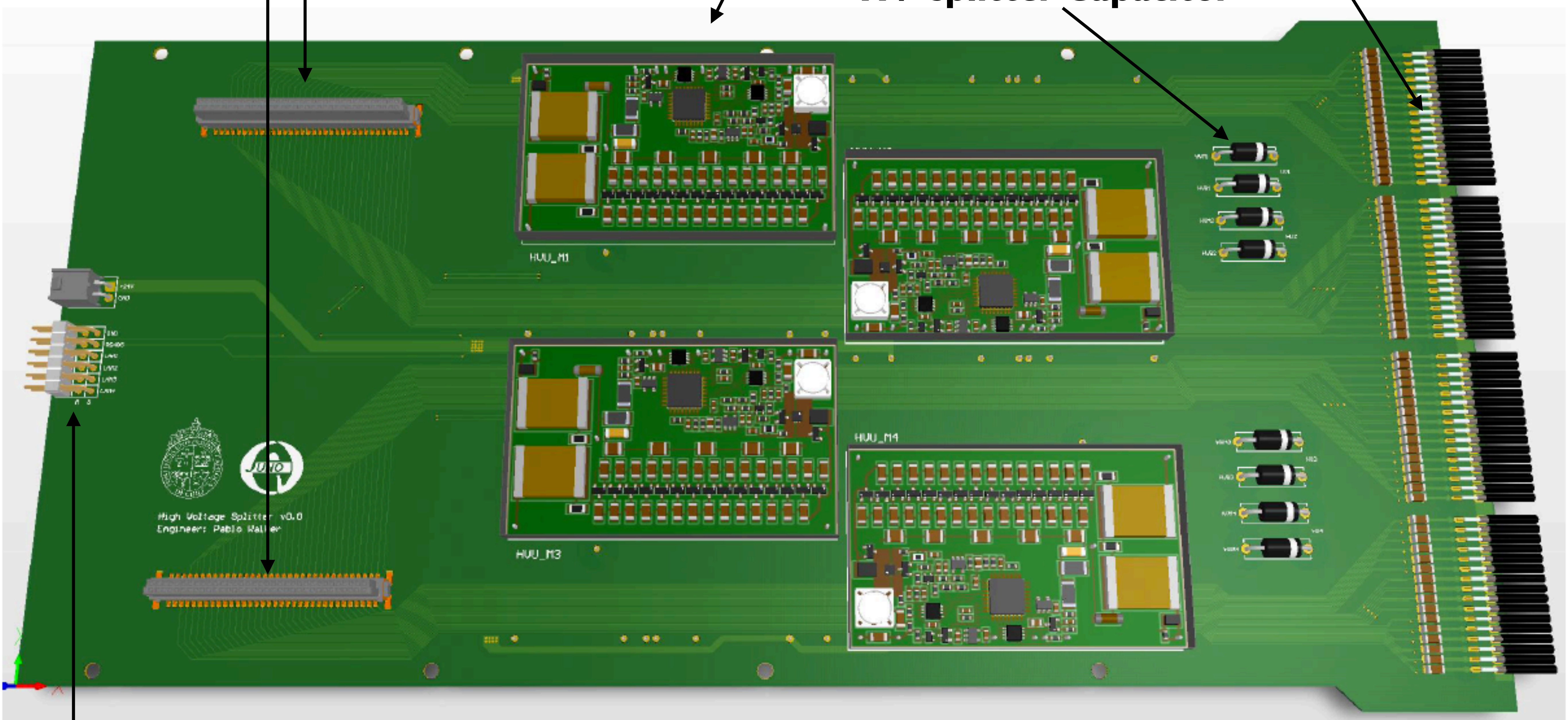
prototype design…

2 HV-units per 16 SPMT
(common HV ⊕ cold-redundancy)

32+32 output (signals→ABC)
(flat-cable ⊕ connector matched to ABC: SAMTEC)

input (HV⊕signal): 64PMTs

HV-splitter Capacitor



power supply (LPMT power-board)
(SPMT low power: ≤10μA per PMT)

same structure on verso
(8HV-units pairs = 64 channels)

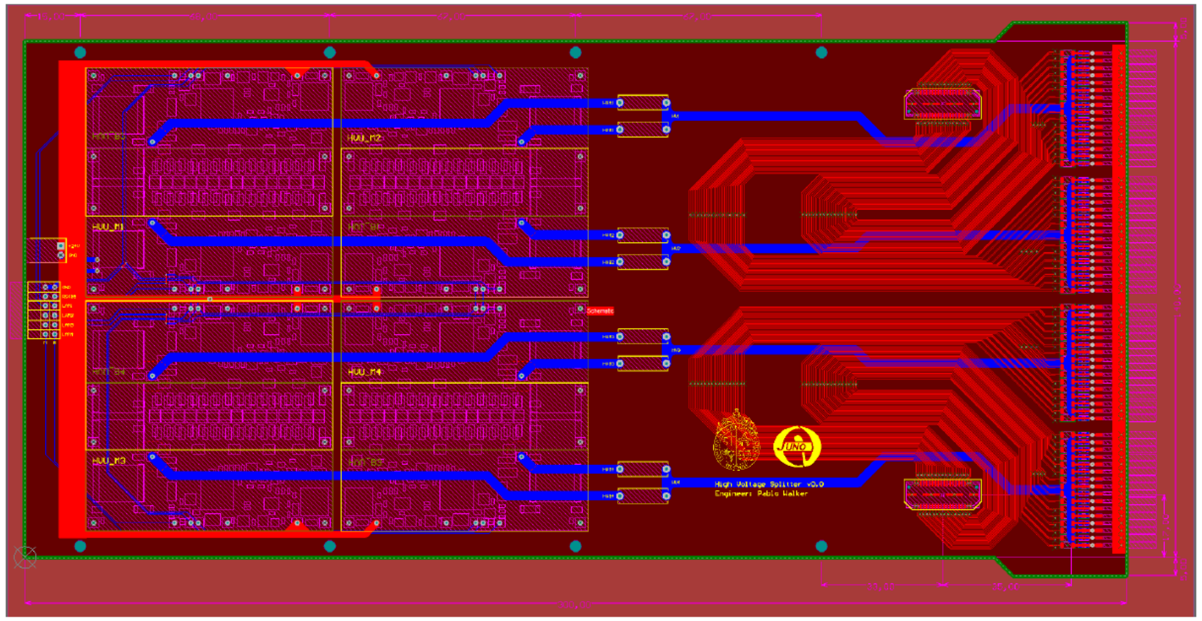
4-layers board (ground shielding: reduce analogue noise)

SPMT(many channels): HV-splitter battery (64 ch)

HVS system-level specs

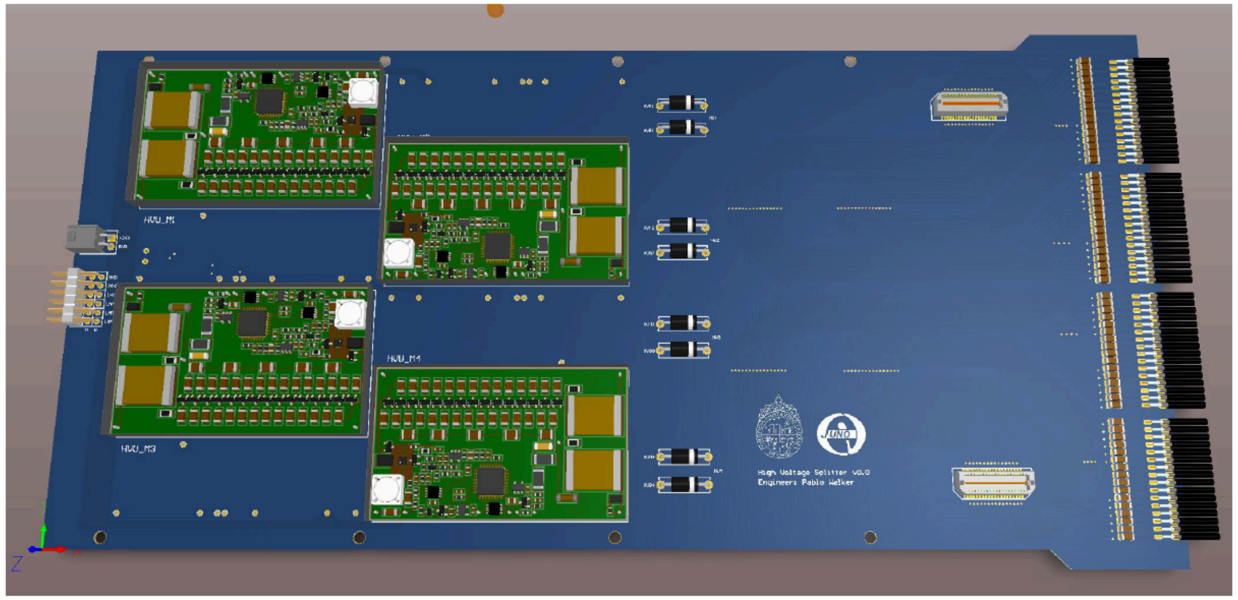
- Each UWB will power and read-out 128 sPMT's
- The current design of the HVS system consists of two board designs (A and B), **64 channels** each
  - Options for SAMTEC and ERNI connectors
- On each HVS board, **8 HVU's** will be mounted 4 for bias and 4 for redundancy
  - Each HVU will bias 16 sPMT channels
- The two HVS board, together with the ABC board and the HVU's form a **board stack** that is installed in the UWB

HVS_A v0.0 (Samtec): Layout

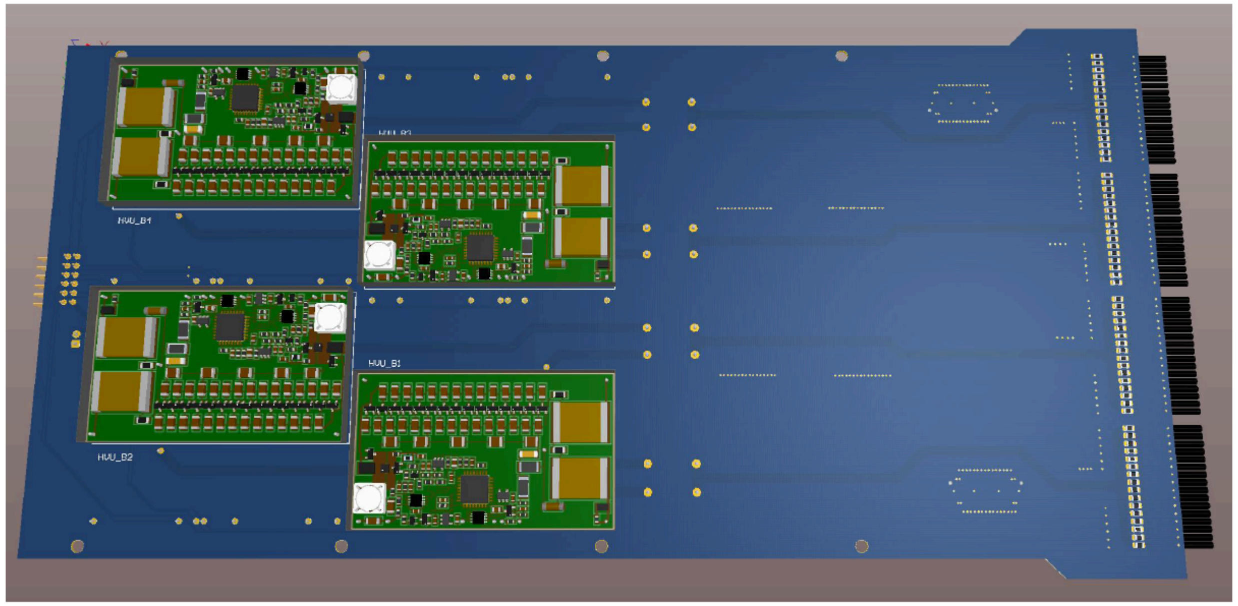


sPMT HV Splitter status 7

HVS_A v0.0 (Samtec): 3D Top view



HVS_A v0.0 (Samtec): 3D Bottom view



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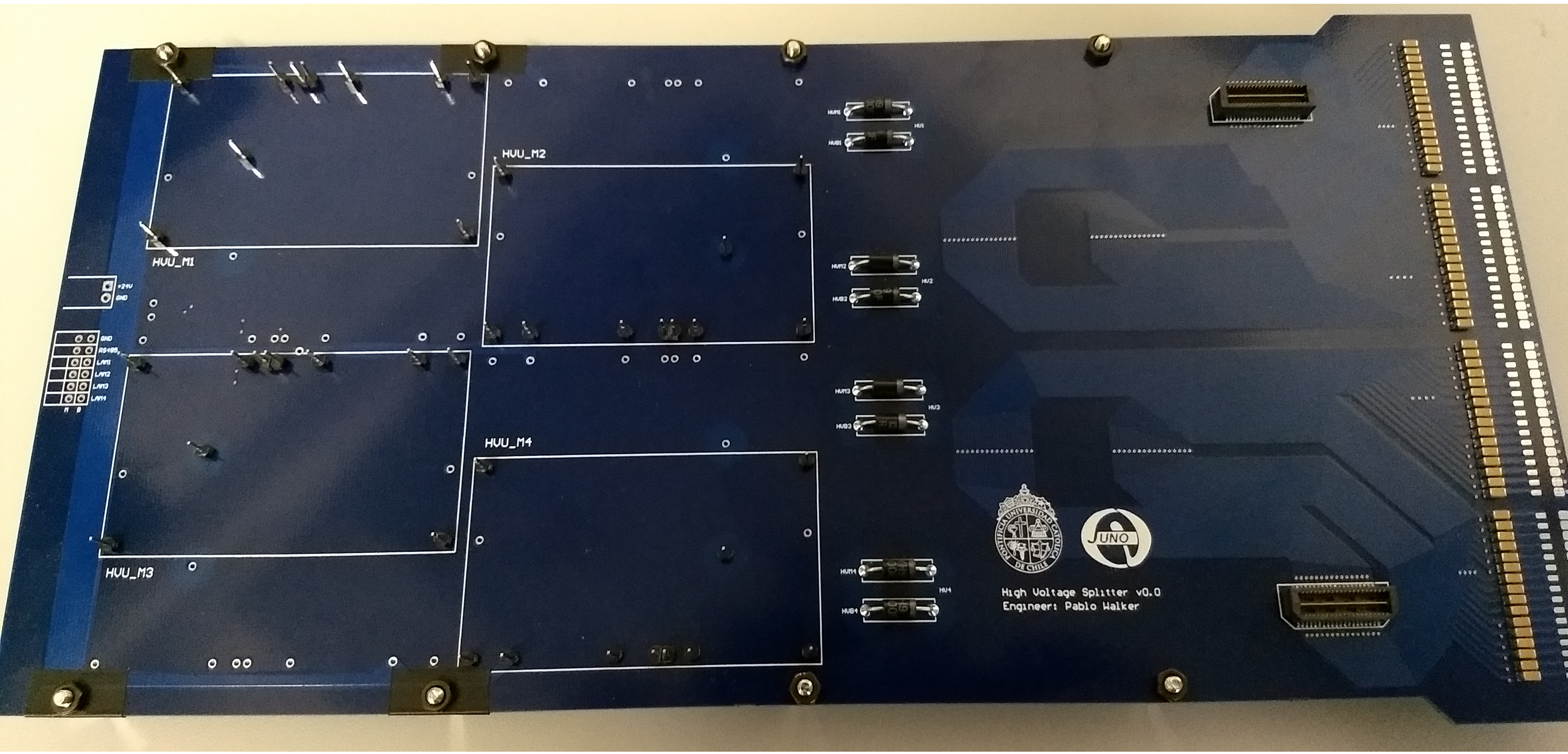
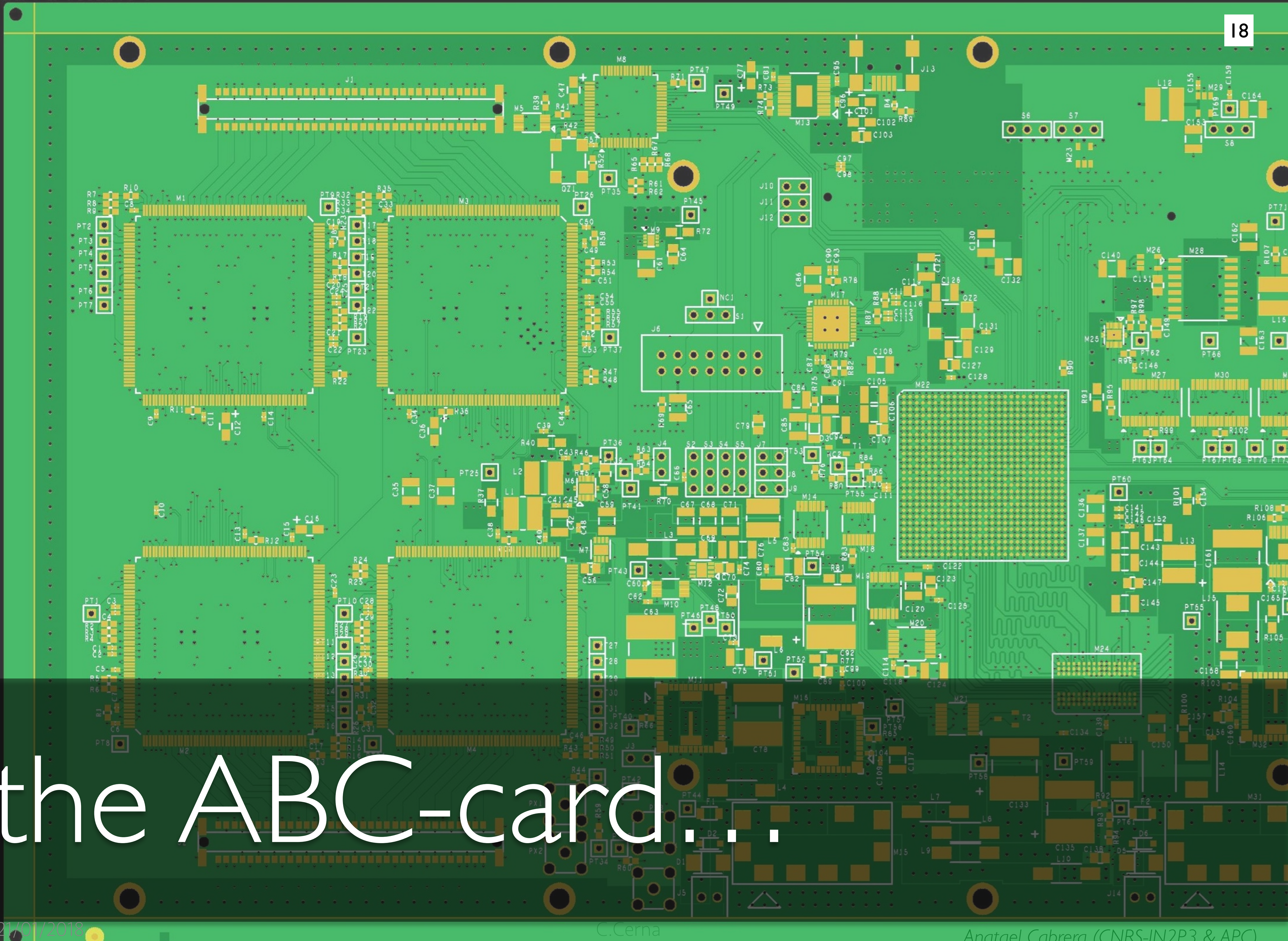
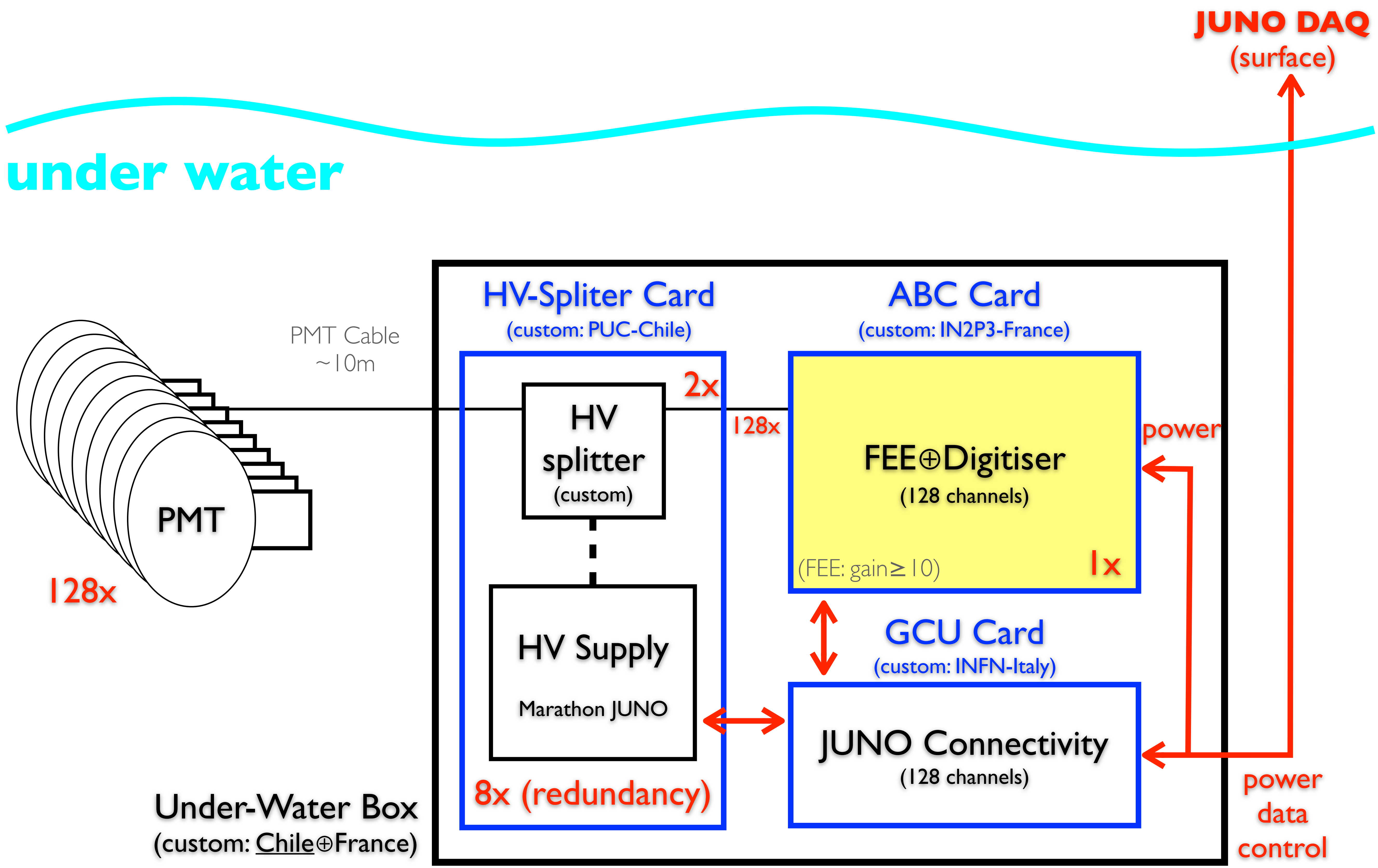
HV-Splitter card being ready for mounting…





the ABC-card…

SPMT logic readout diagram…



(most important) JUNO-SPMT specifications…

		goal	critical	comment
3" PMT	physical diameter	≤80mm	yes	light level (photon-counting tuning)
	SPE width	≤40%	yes	SPE discrimination efficiency
	dark count (@1/4 PE)	≤1.5k/s	yes	DAQ/readout rate (dominant)
	TTS (sigma)	≤1.5ns	yes	position reconstruction
	HV nominal (g=10^6)	[0.8,1.3]kV	no	signal size (discrimination for noise)
	QE@420nm (average)	≥25%	yes	light level (photon-counting tuning)
	non-linearity [0,5]PE	≤1%	yes	linearity in physics regime (redundancy)
	non-linearity [5,100]PE	≤10%	no	linearity above main physics
	current	≤10μA	yes	many PMTs on 1HV channel
CatiROC	time resolution	≤0.5ns	yes	negligible wrt PMT
	charge resolution	>1/10 PE	yes	negligible wrt PMT & SPE discrimination
	pre-amp gain	≥10	ok	compensate (channel-wise) PMT gain
	(non supernova) max rate	~10k/s	yes	non-supernova physics rate capability
	deadtime	≤10μs	ok	limits ADC maximal rate
	supernova max rate	10M event	yes	supernova physics rate capability

TESTING FOR ABC-V1 (≤2018)

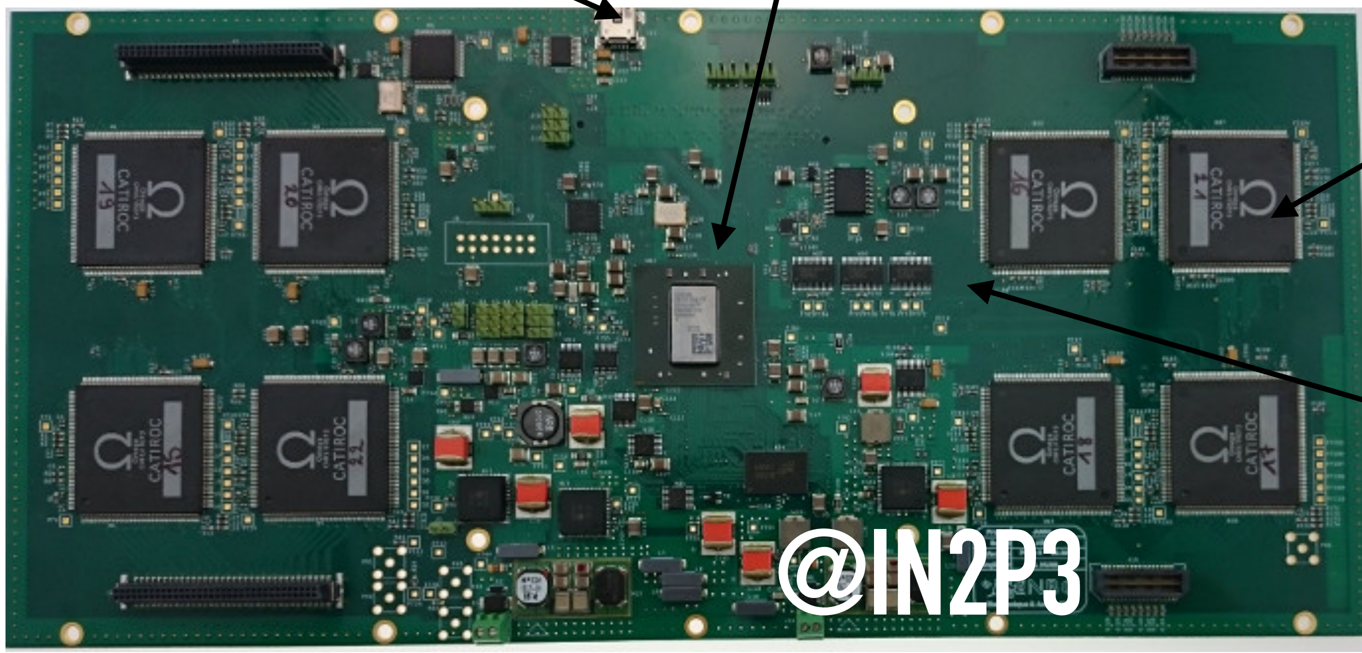
ABC-V0 Prototype

USB2

FPGA Kintex-7 (“FERRARI”)→ powerful digital handling

ABC TOP Side

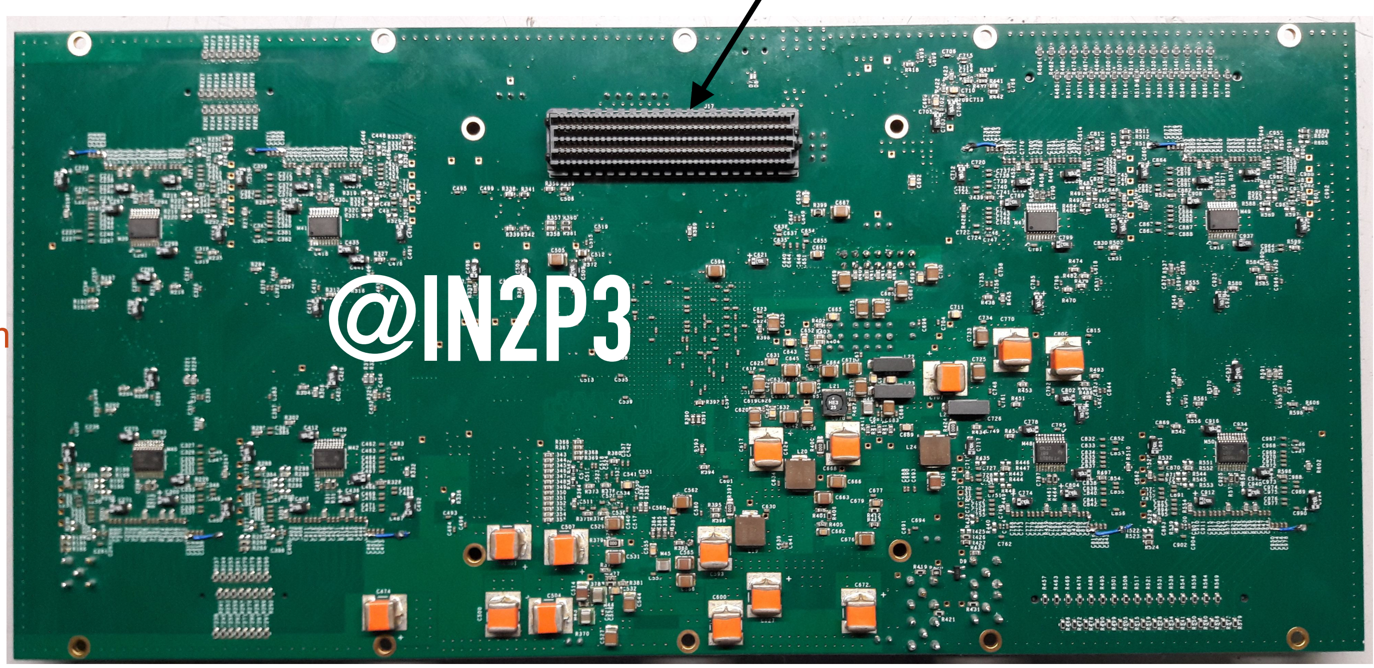
CatiROC



DDR3-RAM

FMC (interface to GCU)

ABC BOTTOM Side



14 cm

30 cm

ABC card

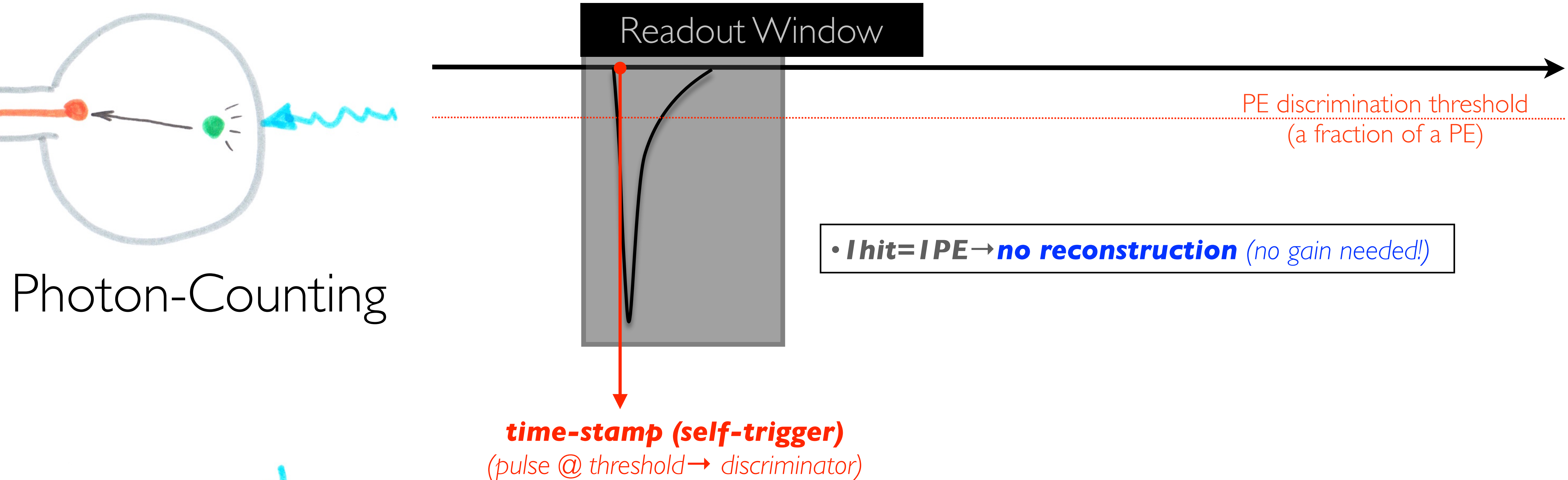
1. 8 x CATIROC (128 ch)
2. USB 2.0 compilant
3. 2 ERNI Connectors
4. 2 SAMTEC Connectors
5. 1 Xilinx Kintex 7 FPGA
6. DDR3 Memory (≤2GB)
7. Spi Flash Memory
8. FMC Compliant
9. 12V FPGA supply
10. 12V ASICs supply

INEXPENSIVE+HIGH DENSITY+COMPACT+MULTI-TRIGGER MODE

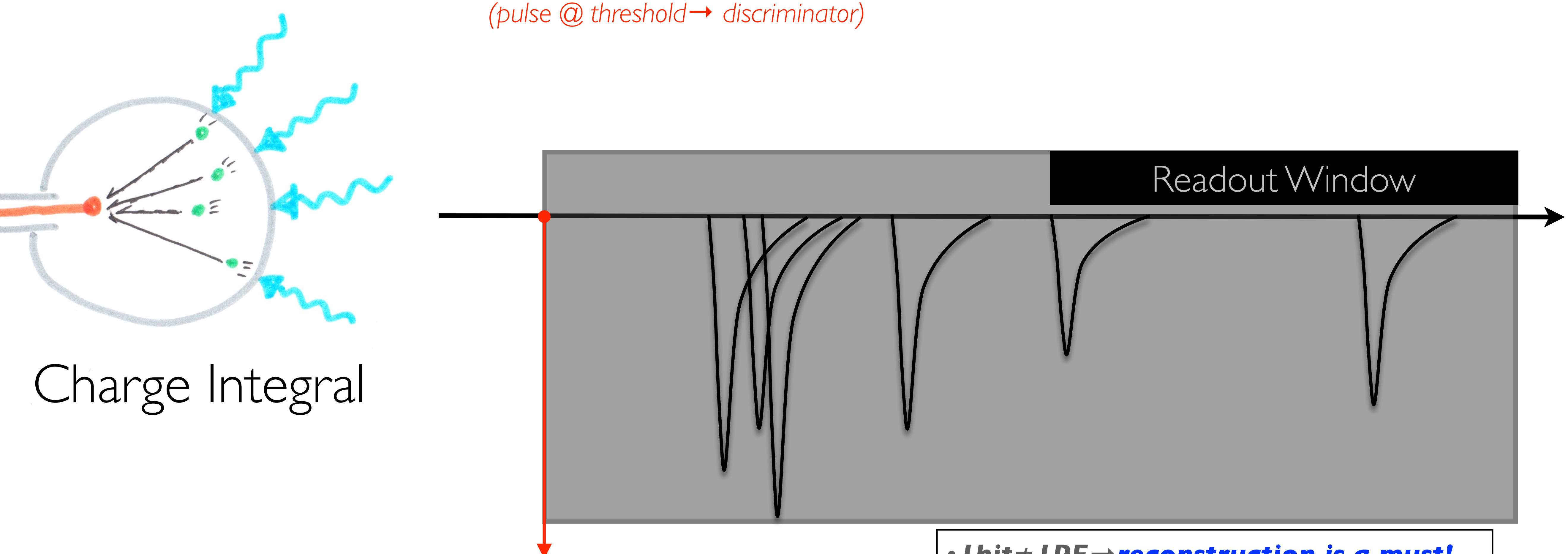
Ω's "ROC" (ReadOut Chip) family…

(**μ**-electronics @ IN2P3/CNRS, France)

Photon-Counting vs Charge-Integration…



• **1hit=1PE→no reconstruction** *(no gain needed!)*



• ***1hit≠1PE→reconstruction is a must! [calibration/reconstruction]***

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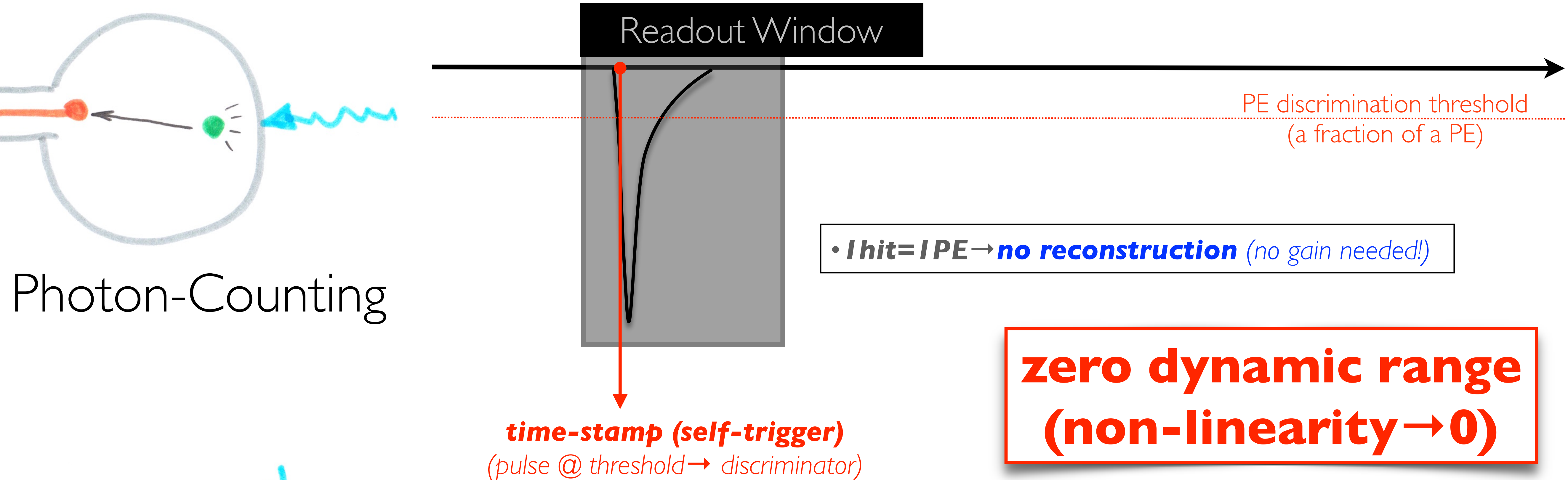
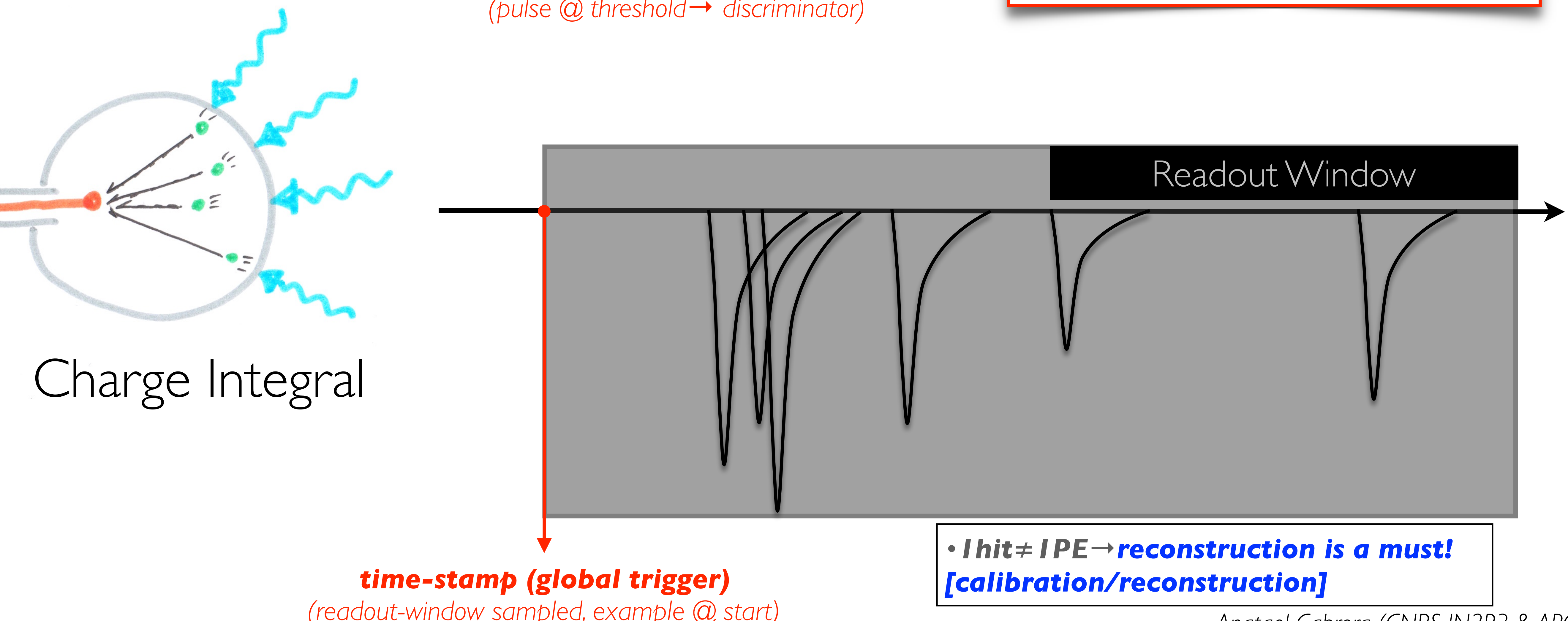


• 1hit=1PE→**no reconstruction** *(no gain needed!)*

zero dynamic range (non-linearity→0)



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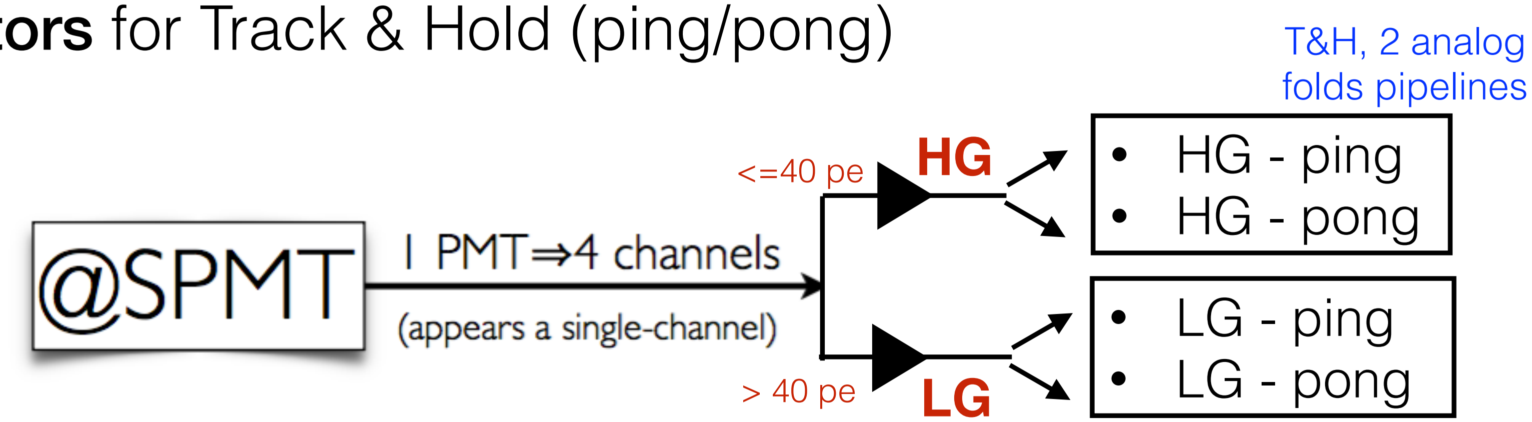
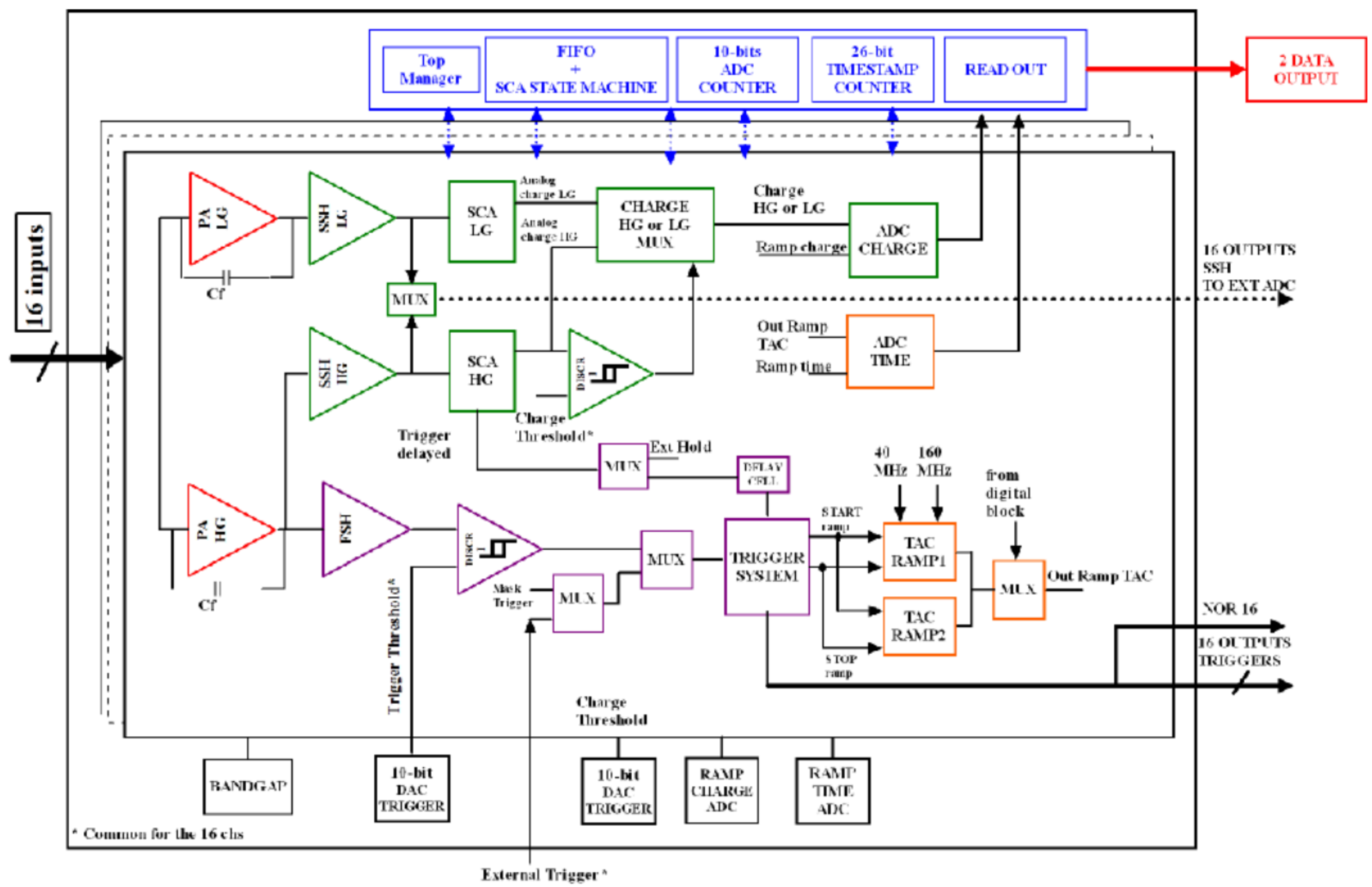
CATIROC DIAGRAM…

- **x2 pre-amplifiers** (**HG** if q <= 40 p.e., **LG** if q > 40 p.e.)
- **x2 capacitors** for Track & Hold (ping/pong)



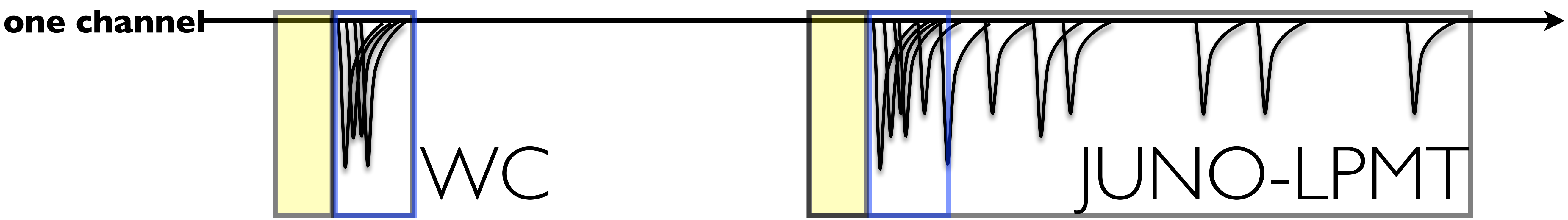
dead-time per circuit ~6μs

for detailed questions…



Δt(ToF)≤200ns (per channel)

designed for Water-Cherenkov…



Δt≤200ns? (per channel)

Δt≤1000ns (per channel)

CatiROC acceptance window ≤200ns (per channel) → truncate some scintillation light

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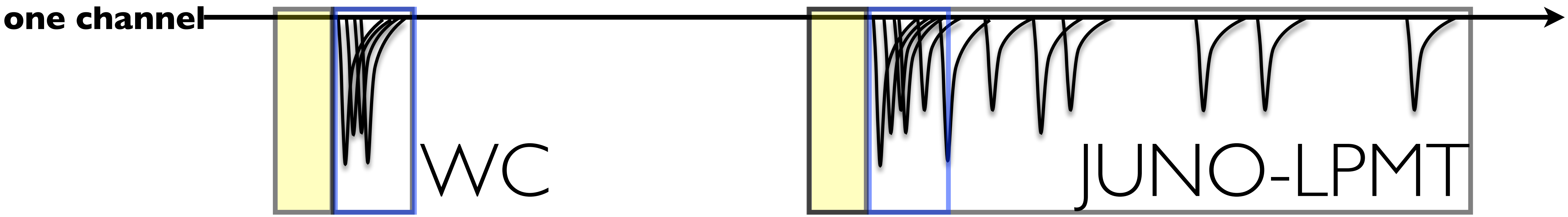

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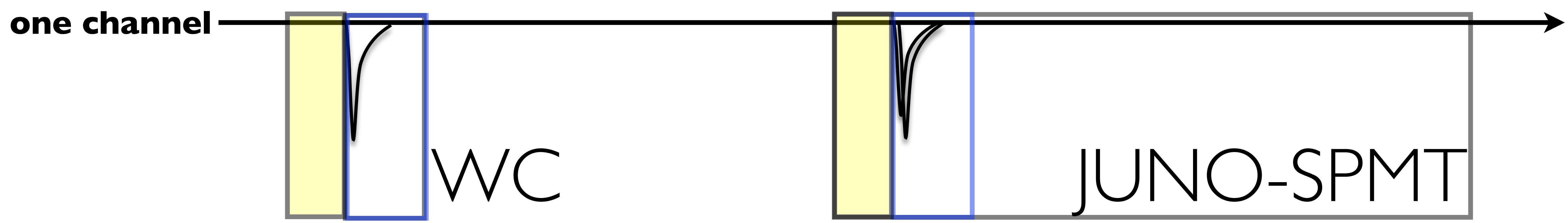
SPMT works in Photon-Statistics (low light level: 1PE per trigger)



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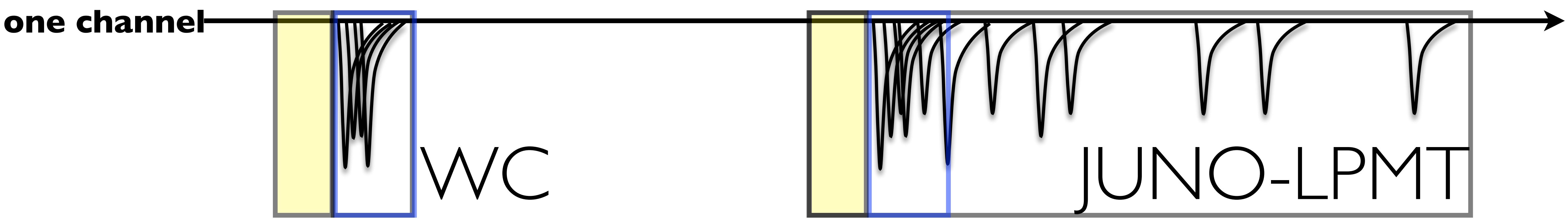

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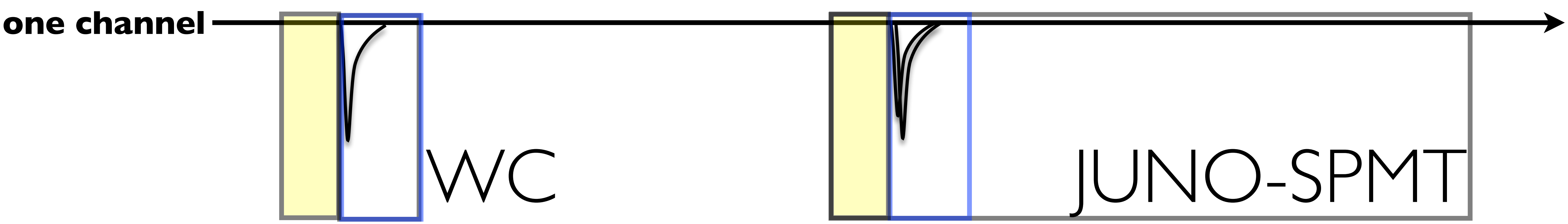


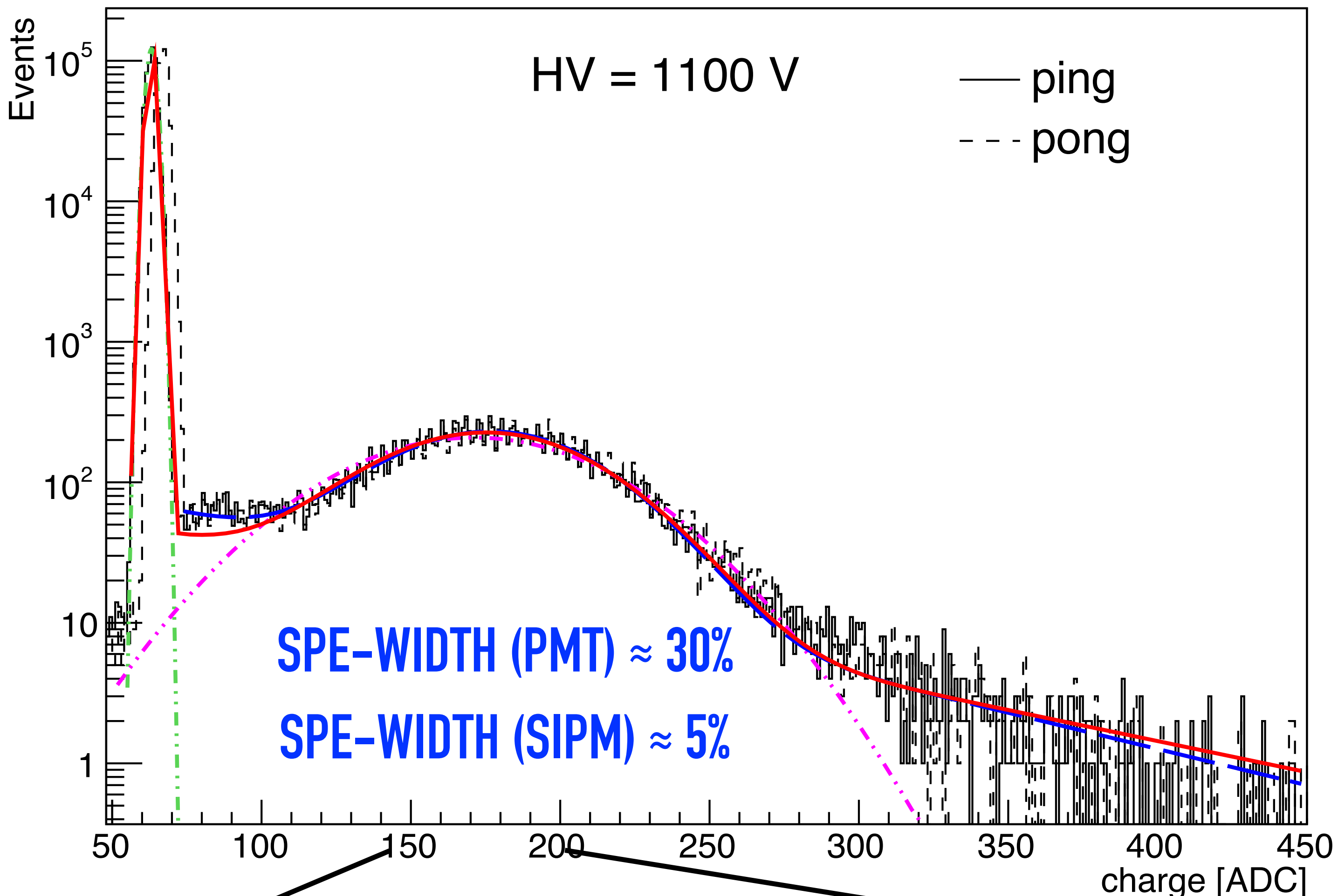
Δt≤50ns? (per channel)

Δt≤50ns? (per channel)

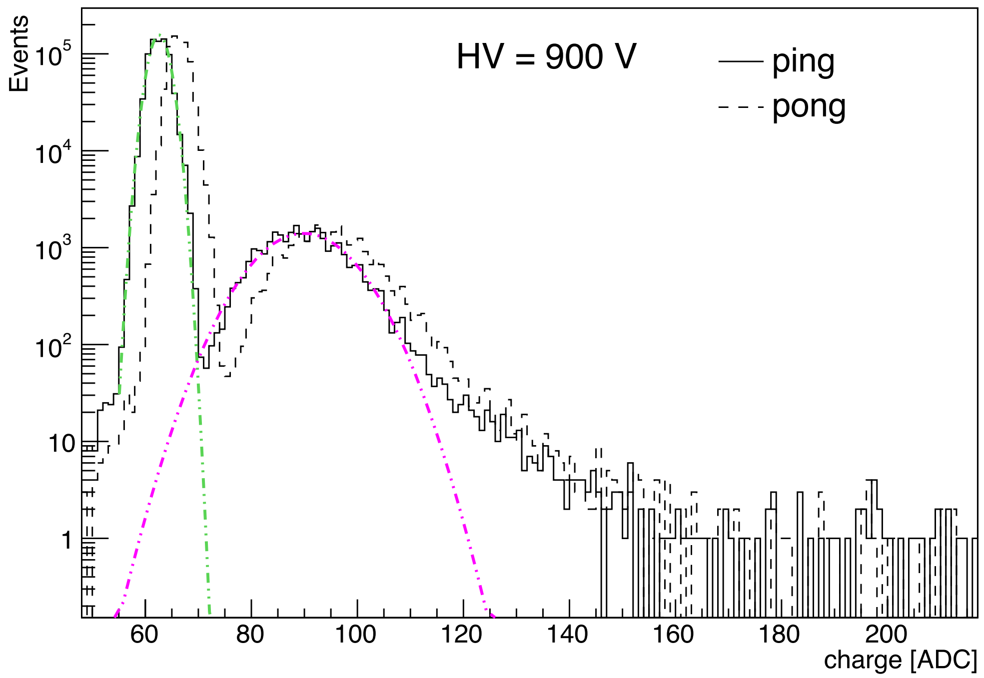
WC ≈ SPMT-JUNO

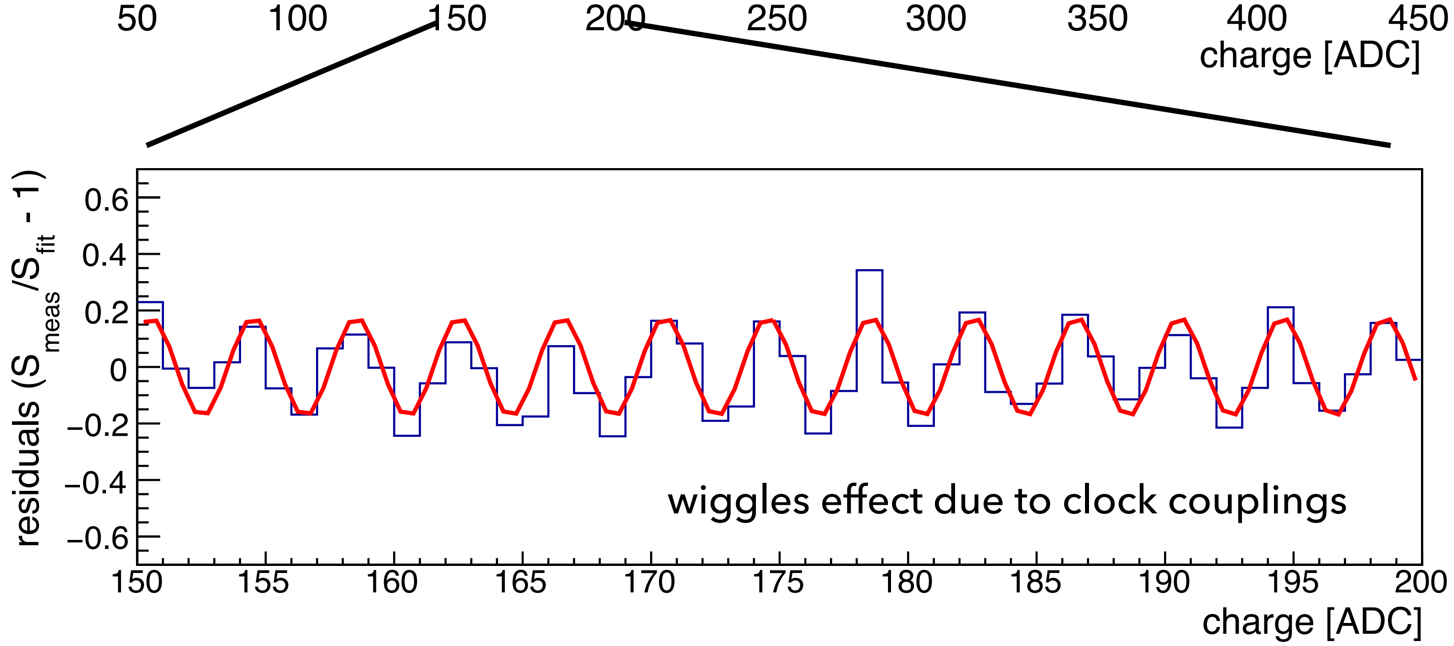
CHARGE PERFORMANCE…

PHOTO-ELECTRON SPECTRUM WITH CATIROC



ping-pong difference constant (for a given channel)





Wiggle effect fit with a function :

$$N_{meas} = N_{fit} \cdot A \cdot \sin(f x + \Phi)$$

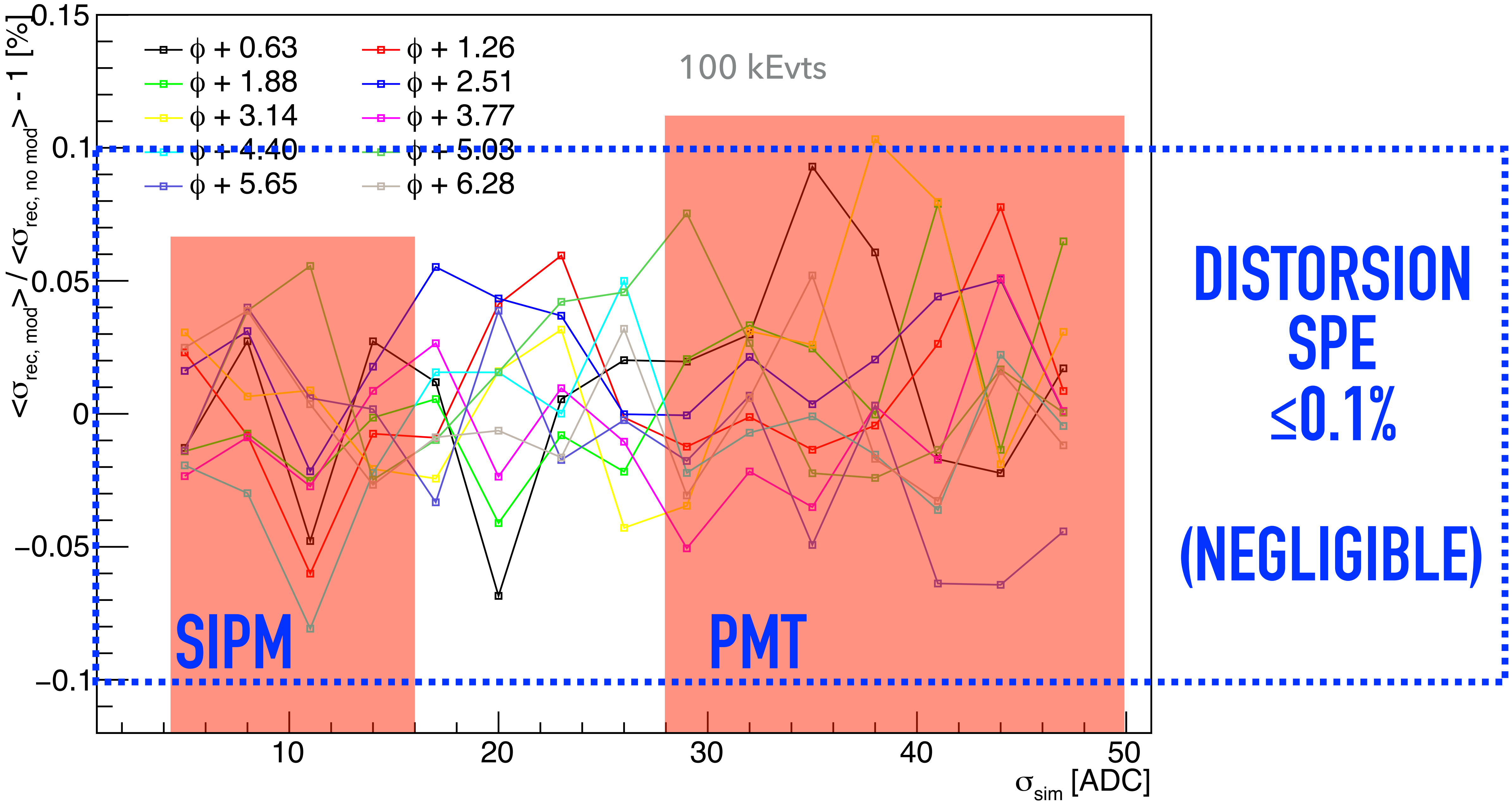
A = amplitude

f = frequency

Φ = phase

IMPACT OF THE WIGGLES ON THE P.E. MEASUREMENT

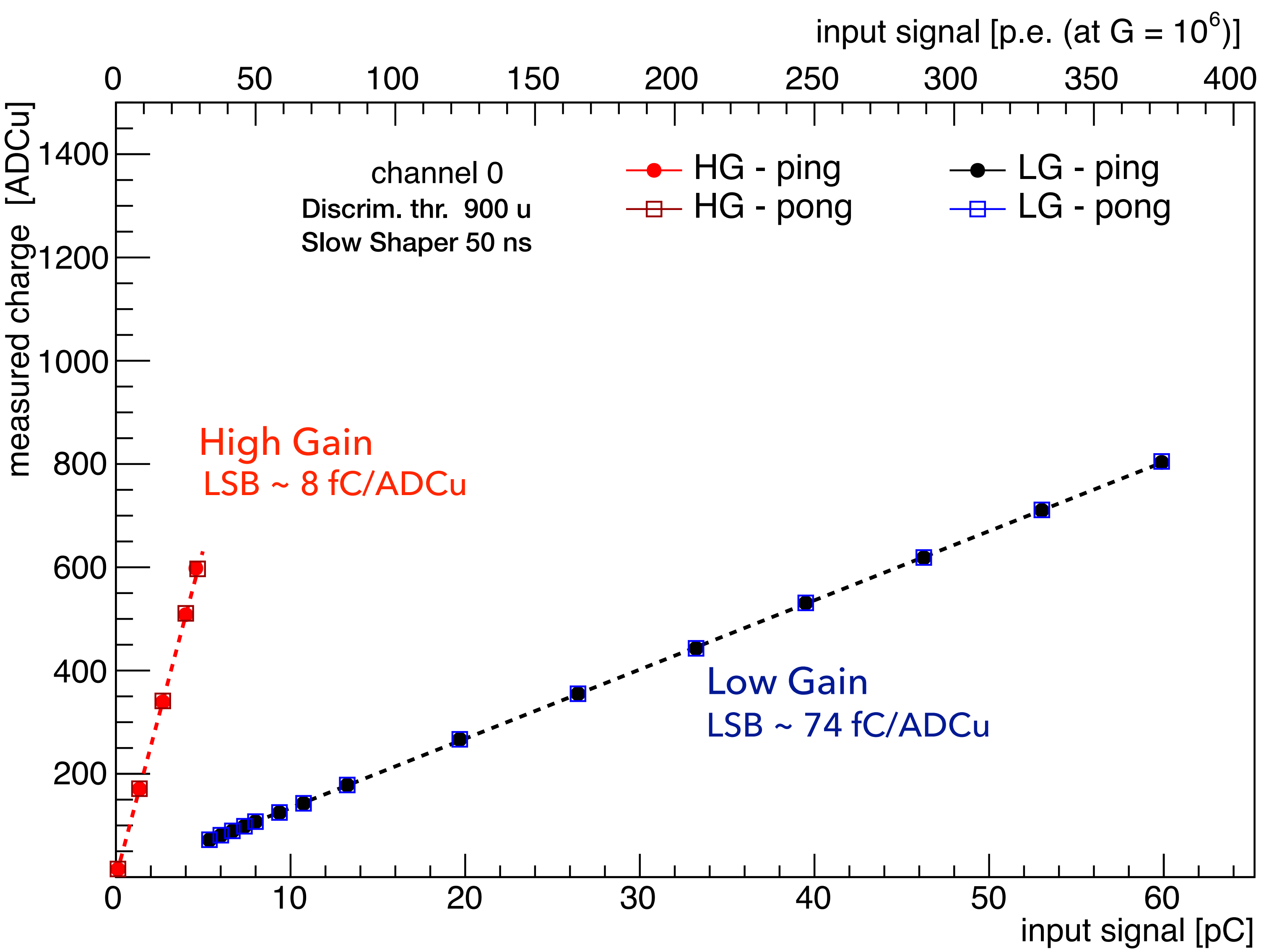
ToyMC to study the impact of the wiggle effect on the resolution and mean P.E. position for different width of the s.p.e distribution (~ 30-40% for PMTs, smaller for SiPMT), and for different Φ



Negligible effect on the reconstructed p.e. position.

LINEARITY AND CHARGE RESOLUTION

measurements done on two different test-boards, at Omega and Subatech



Range of operation :
1 - 400 p.e. (@ G=10^6)
(160 fC - 70 pC)

Saturation:
50 p.e. (HG), **500 p.e. (LG)**

Calibration for each channel,
T&H mode and HG/LG separately:
HG: ~ 8 fC/ADCu
LG: ~ 70 fC/ADCu
$Q_{ping}/Q_{pong} < 5\%$

Charge resolution:
2 ADCu (HG) ~ **0.1 p.e.**
1 ADCu (LG) ~ 1 p.e.

Note: For the SPMT we operate most of the time in HG mode

CONCLUSION

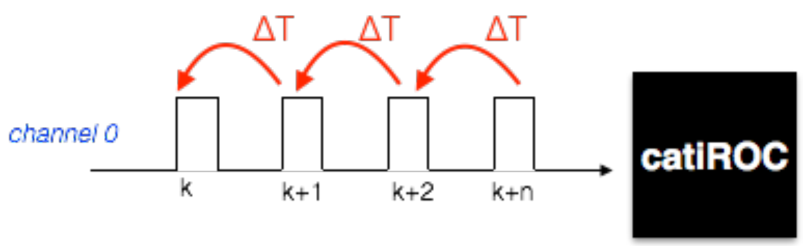
✓ CATIROC'S CHARGE PERFORMANCE

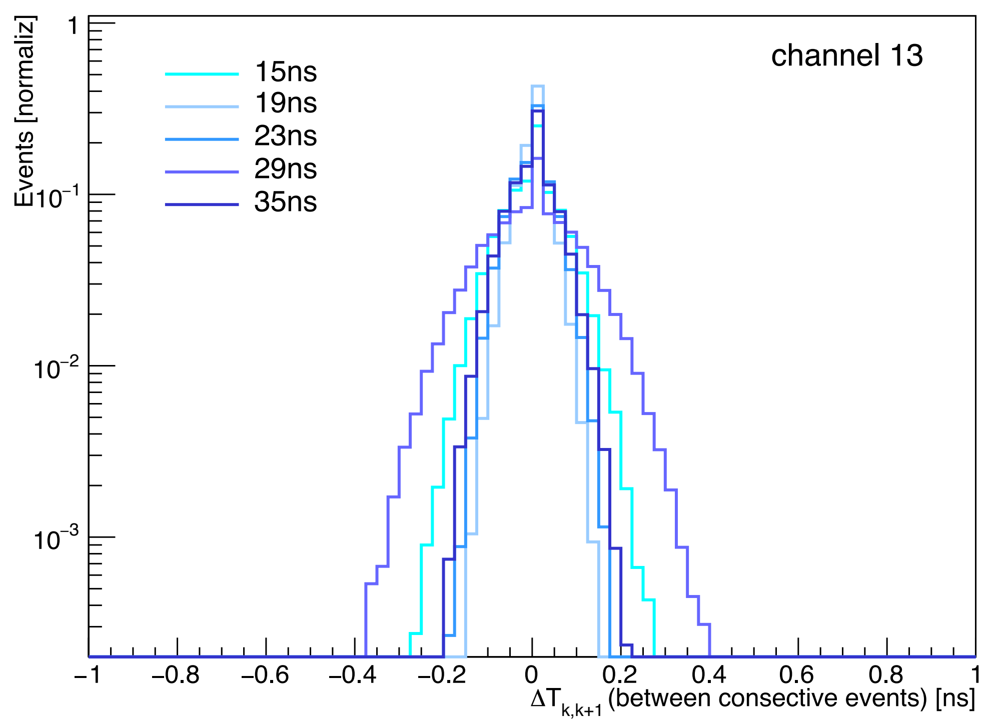
(JUNO AND BEYOND → SIPM?)

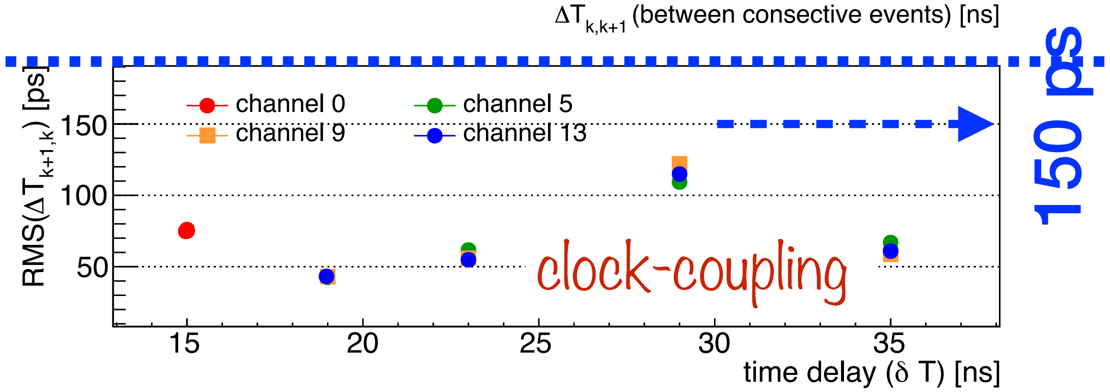
TIME PERFORMANCE…

TIME RESOLUTION

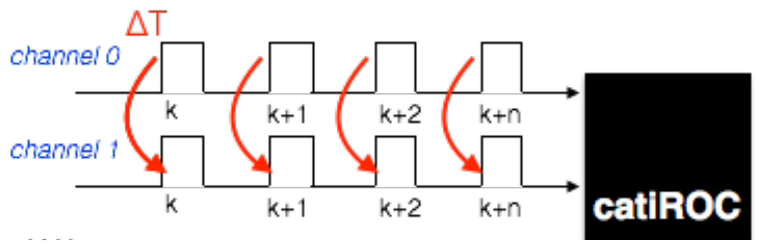
A) for each channel i, compare readouts k and k+1

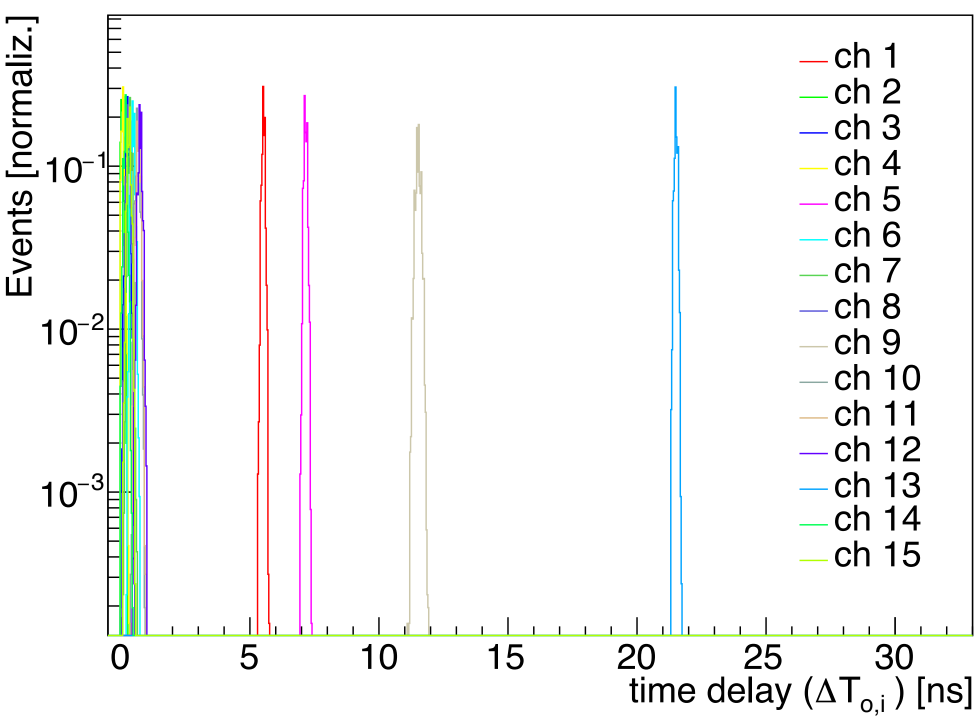


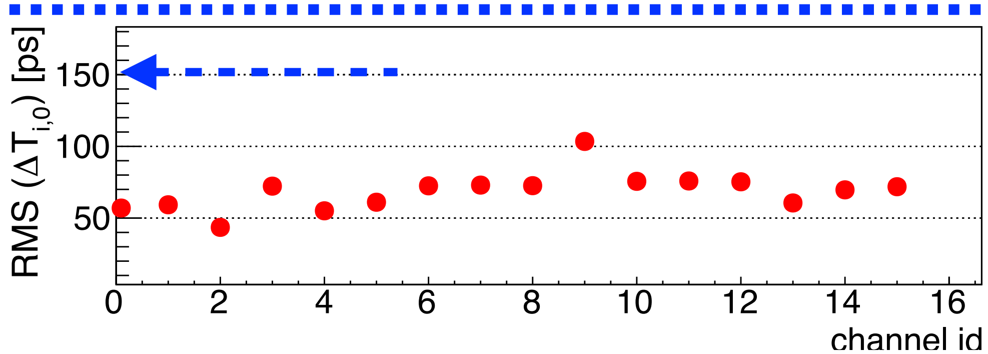




B) for each readout k, compare *i-th* channel and ch 0



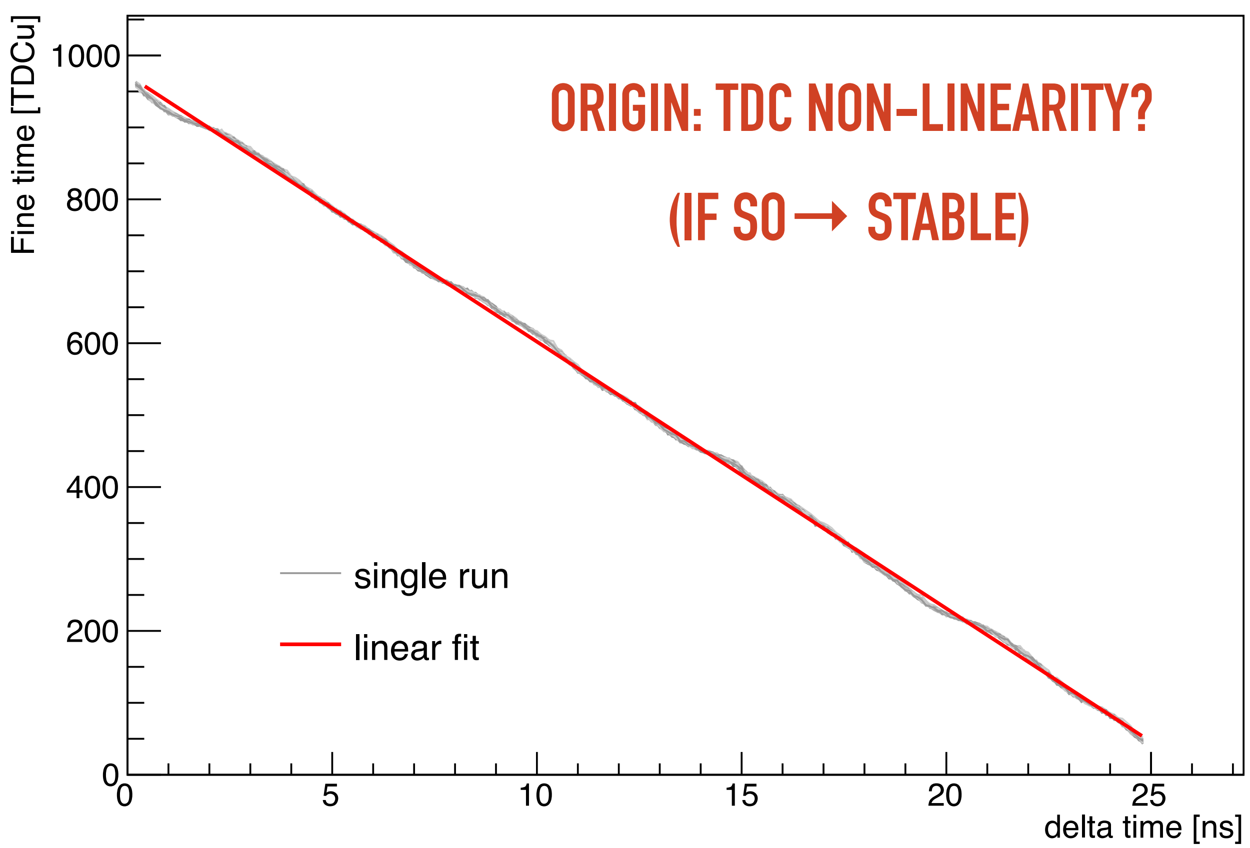




≤200PS RESOLUTION

TAC RECONSTRUCTION

TAC reconstruction measured several time (in continuous mode or after reset of catiro
100 runs are shown as gray lines (they overlap quite well).



The CatiROC behavior is quite well reproducible and may be corrected (not needed for JUNO, could be interesting for SiPMT)

<100PS RESOLUTION (PEAK-TO-PEAK) ⟹ ≈25PS RMS

CONCLUSION

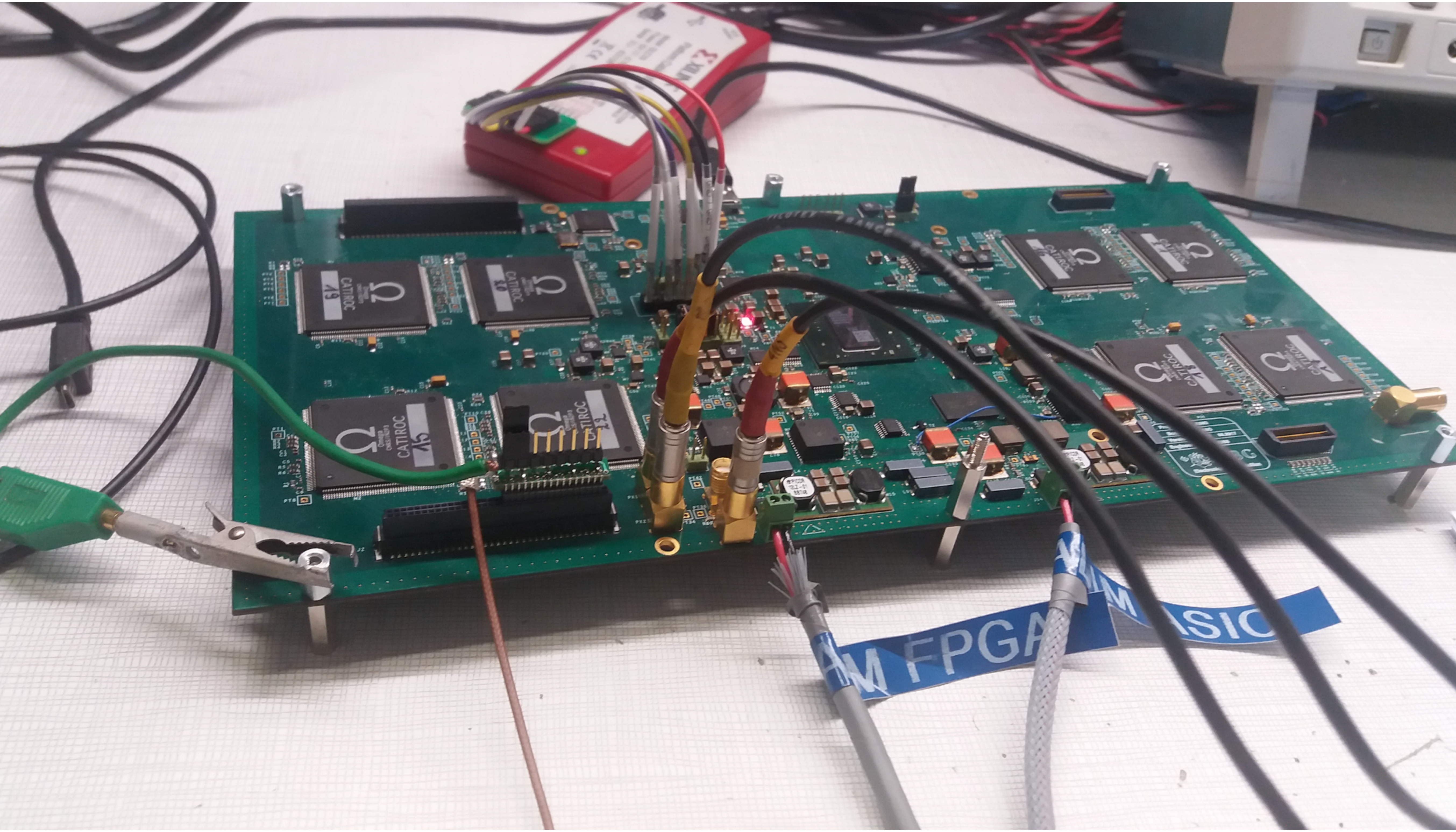
✓ CATIROC'S TIME PERFORMANCE

(JUNO AND BEYOND → SIPM?)

BEYOND CATIROC'S "DEATH"…

DUAL DATA STREAM (DDS)

UNIQUE JUNO VIA ABC-CARD

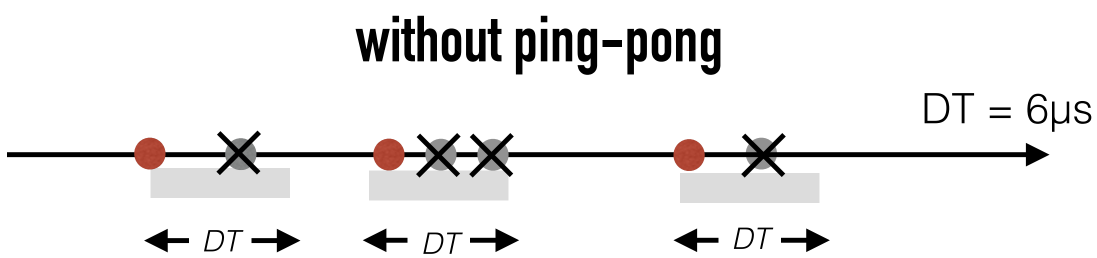


ABC-V0: EXERCISE CATIROC↔FPGA↔USB2 (SUCCESS)

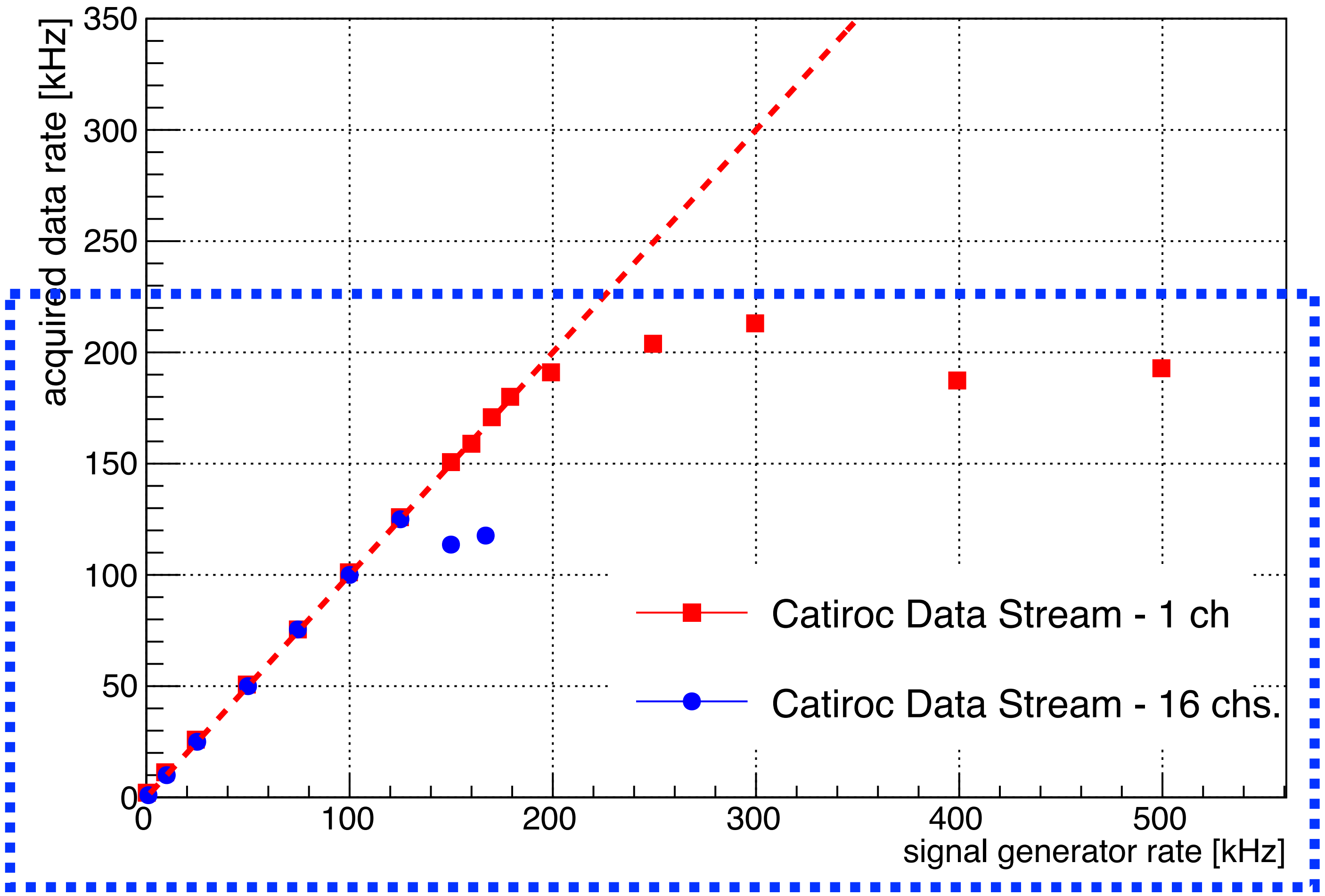
(STAND-ALONE READOUT→ JUNO INTEGRATION END 2018)

CATIROC DEAD TIME

The T&H system working in ping-pong mode reduces the dead time to 9 μs (6 μs for 1 channel only).



ADC READOUT: ≤200KHZ



preliminary

CATIROC DEAD TIME

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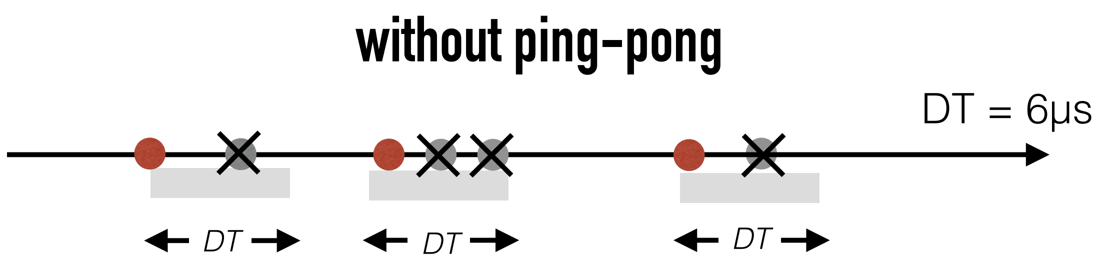
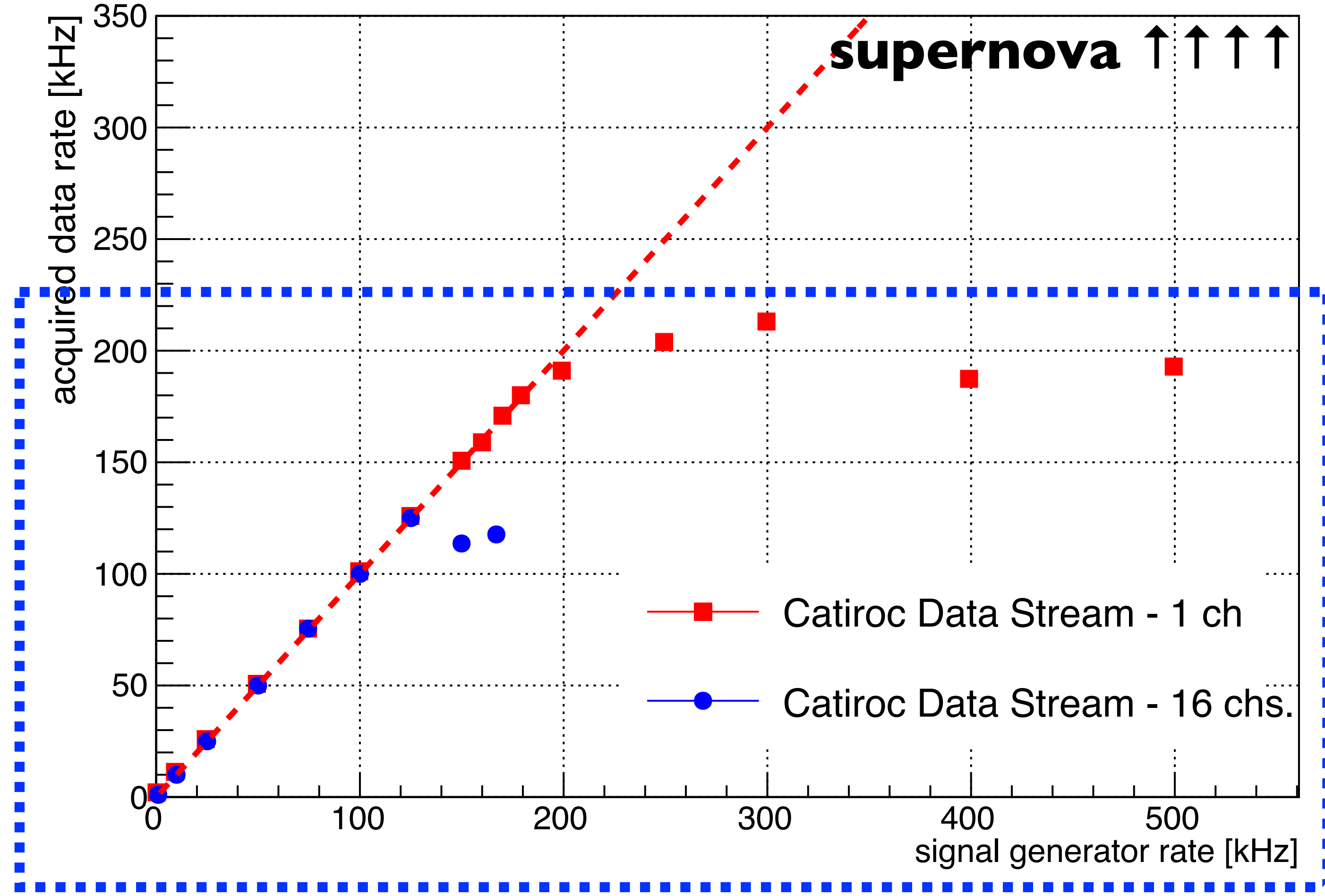


ADC READOUT: ≤200KHZ



preliminary

CATIROC DEAD TIME

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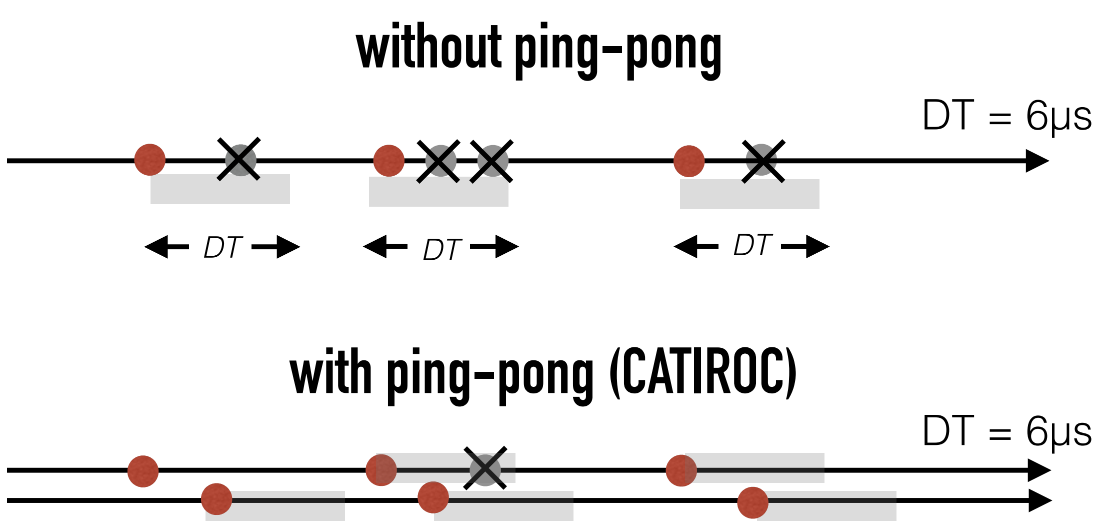
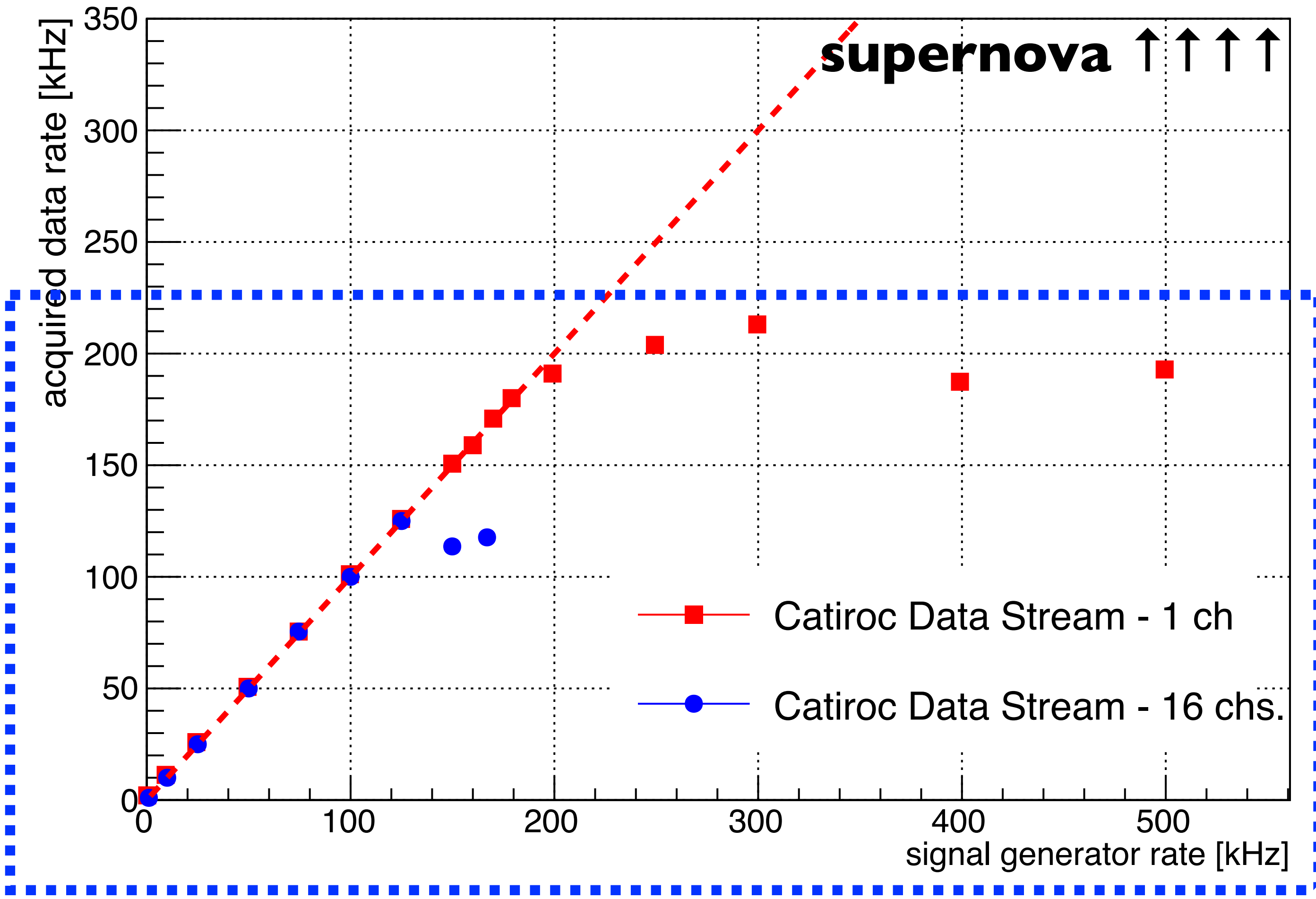
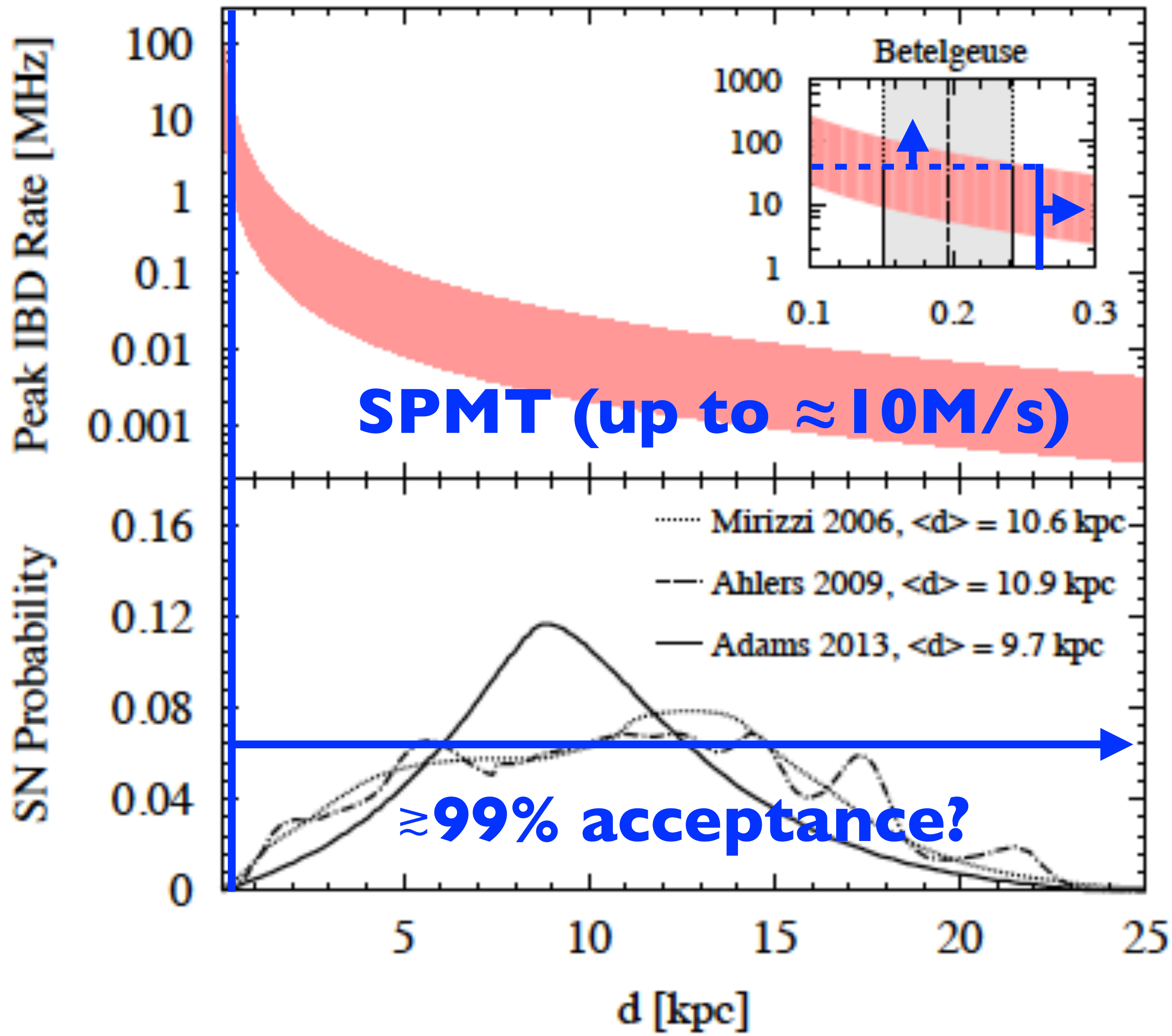


ADC READOUT: ≤200KHZ



preliminary

LET'S TRY TO GET IT ALL (OR ALMOST)



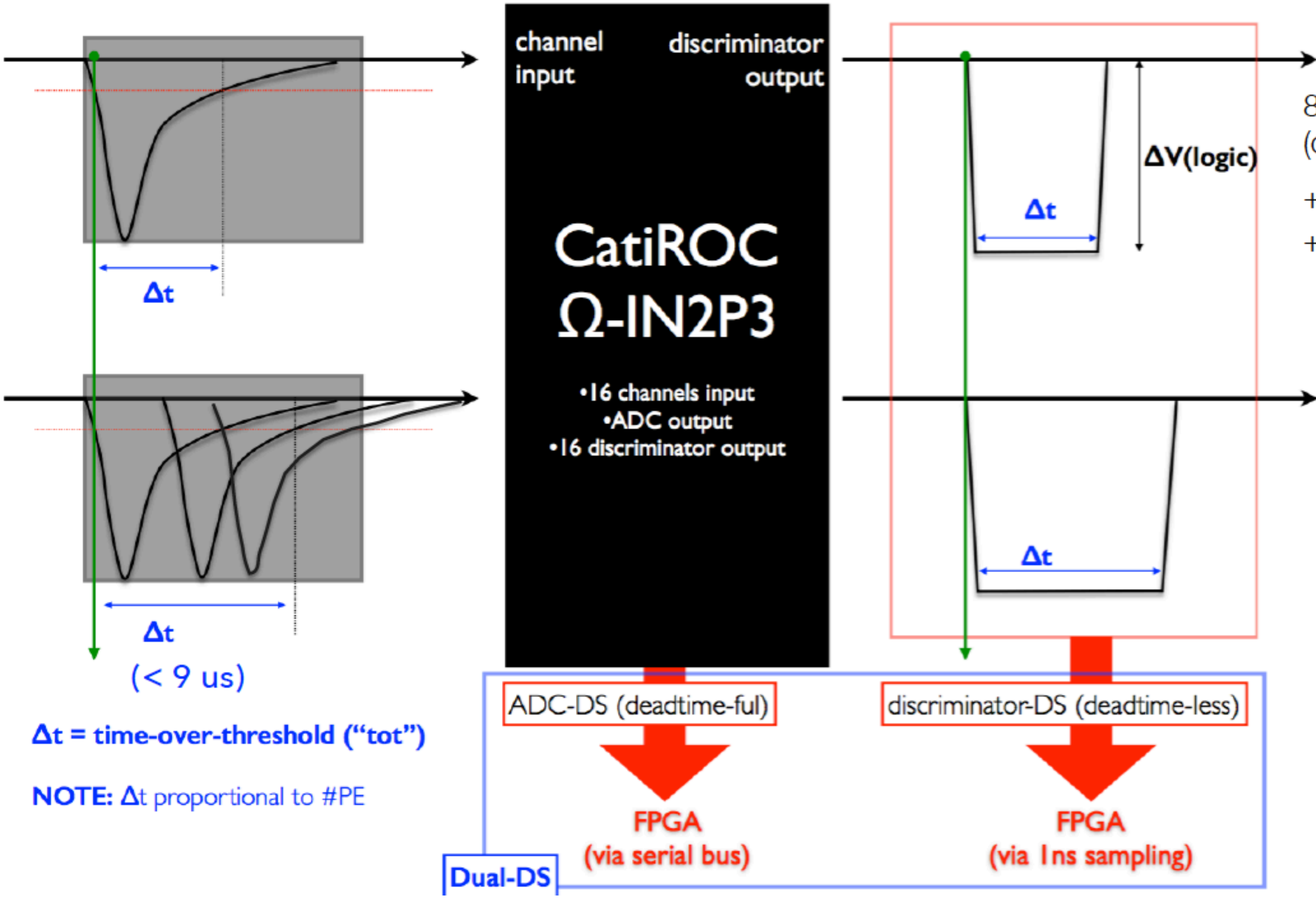
unbiased measurement

(high rate ⊕ deadtime monitor)

DUAL DATA STREAM RATIONALE…

Discriminator output does not suffer dead-time due to the signal digitisation part.

- Information preserved (in photon-counting regime) but worst resolution



DATA FLOW

80 bit: CATIROC output (charge, time)

+80 bit: Rising edge (DDS)

+80 bit: Fall edge (DDS)

1st evt:
80 bit: CATIROC output
+160 bits: DDS

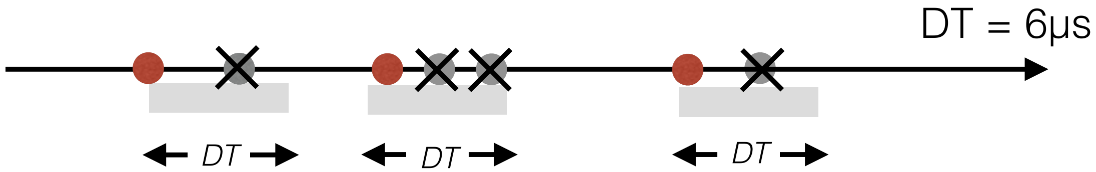
2nd evt (<9us)
80 bit: CATIROC output
+160 bits: DDS

3rd evt (<9us)
160 bit DDS
(no catiroc output)

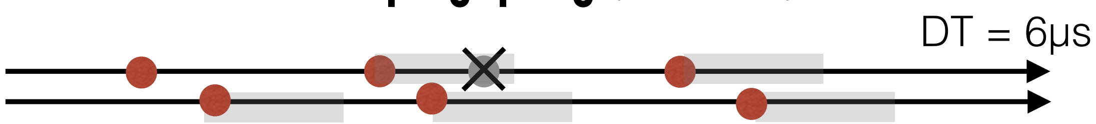
DUAL DATA STREAM : FIRST TESTS

The T&H system working in ping-pong mode reduces the dead time to 9 μs (6 μs for 1 channel only).
DDS has in principle no dead time : lost events recovered and redundant information for trigger rates < 110 kHz.

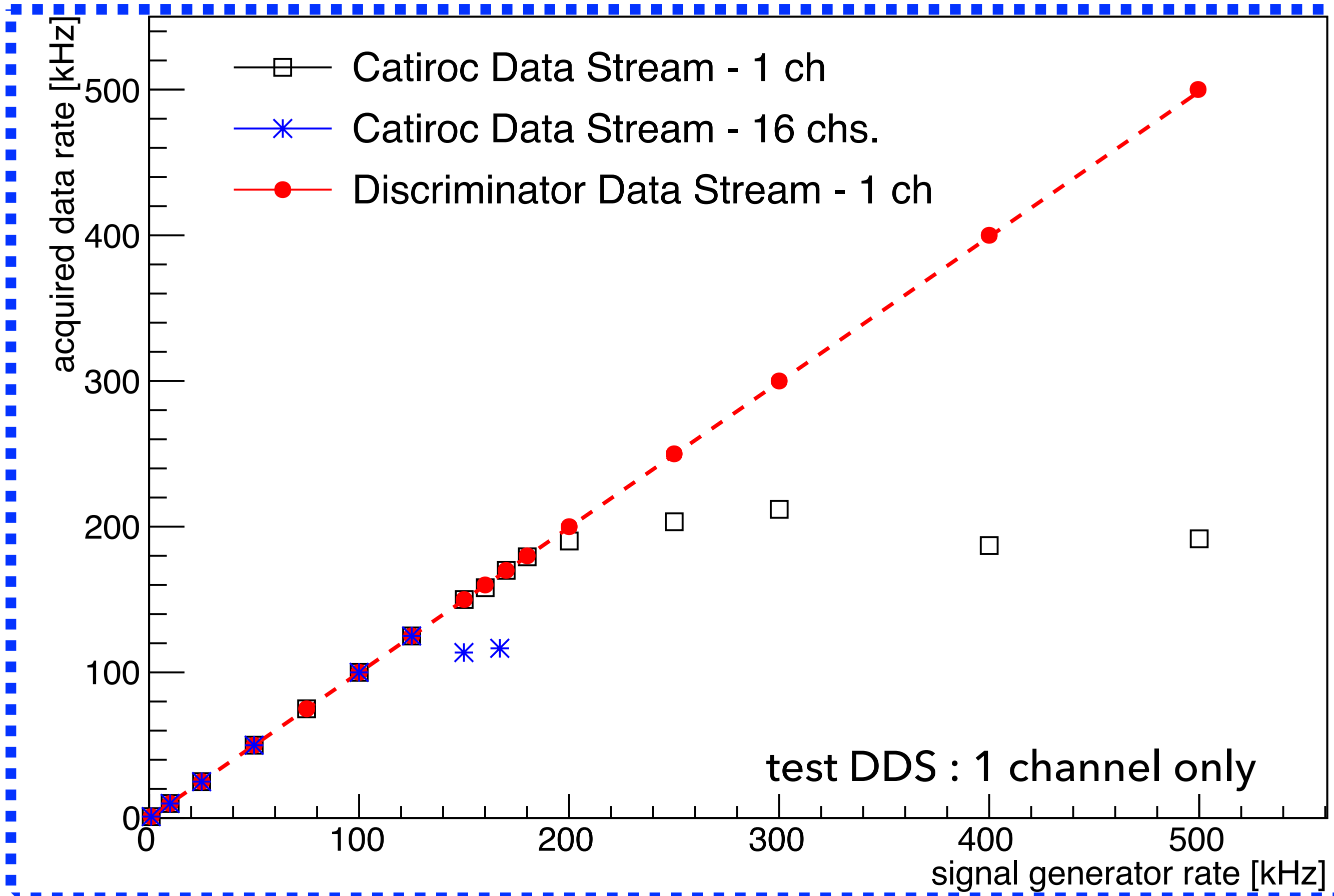
without ping-pong



with ping-pong (CATIROC)



DDS READOUT BEYOND ADC-DEADTIME



LIMITED BY USB (V0 PROTOTYPE)

ABC'S KINTEX7 FPGA(+)2GB-DDR: UP TO ~10M EVENTS (PRELIMINARY)

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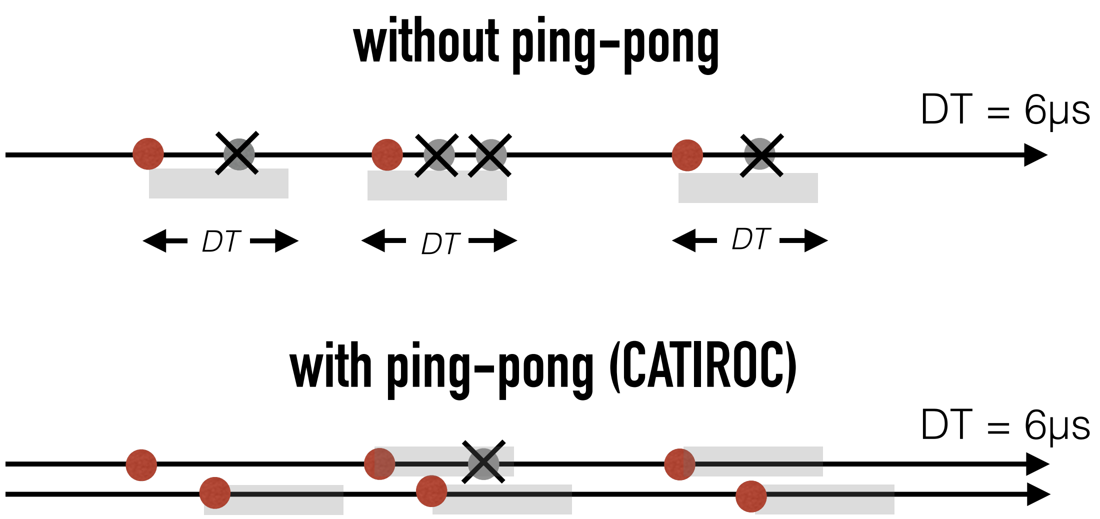
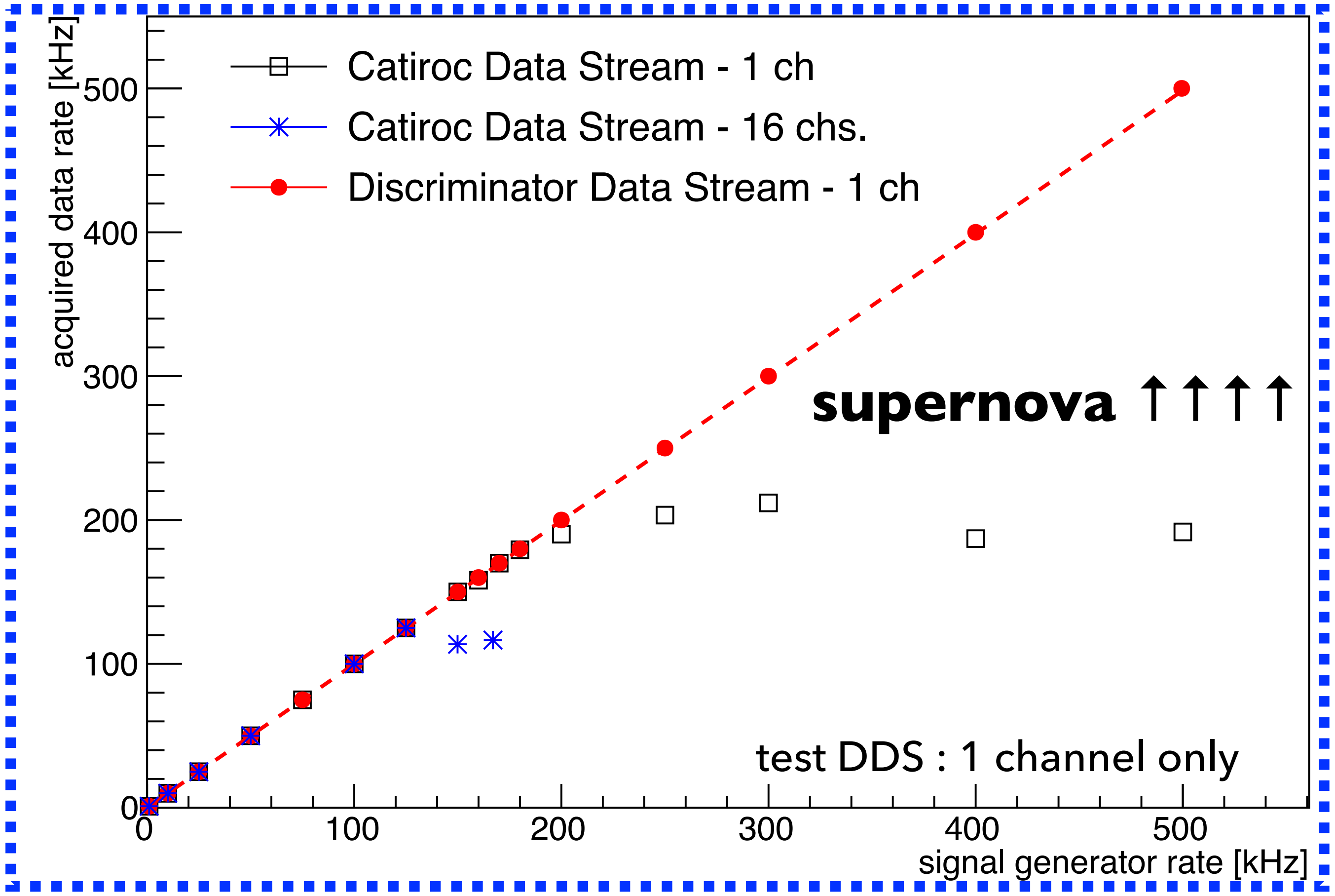


DDS READOUT BEYOND ADC-DEADTIME



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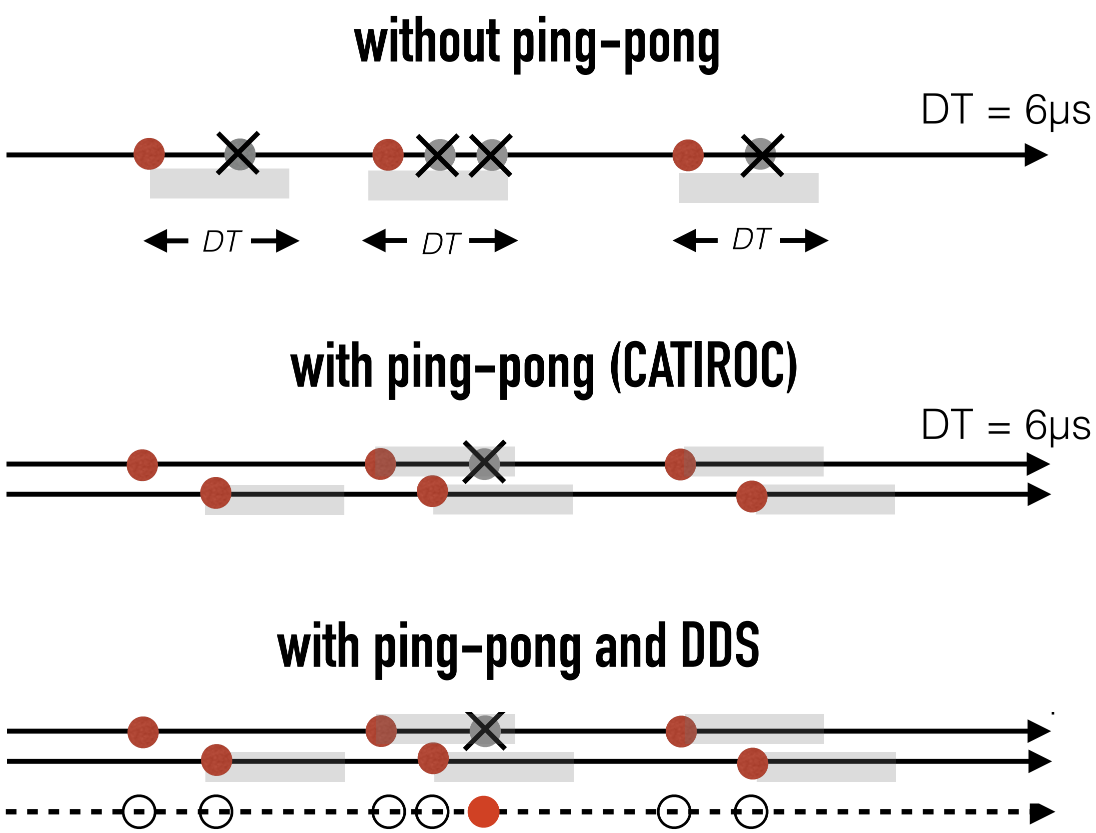
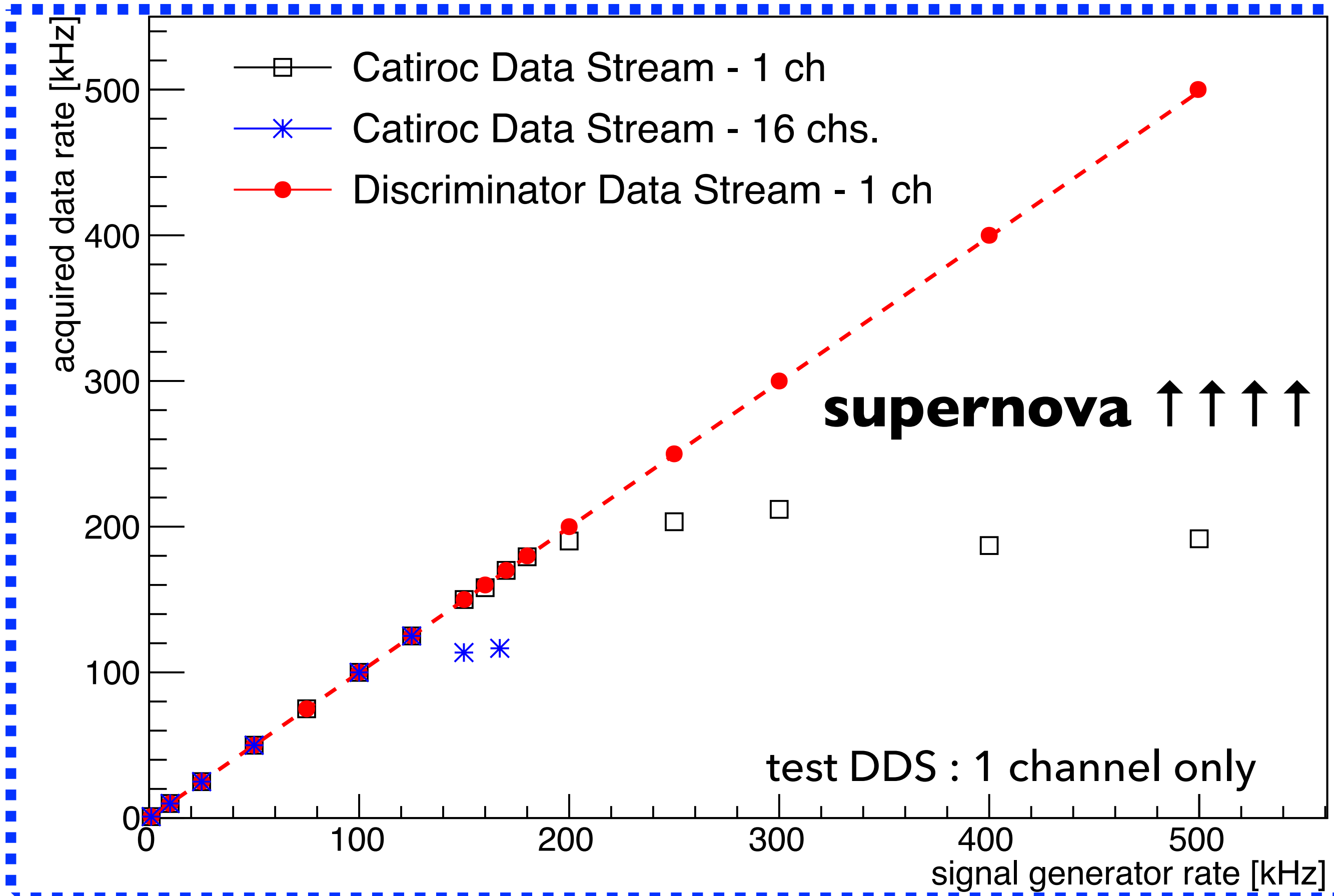


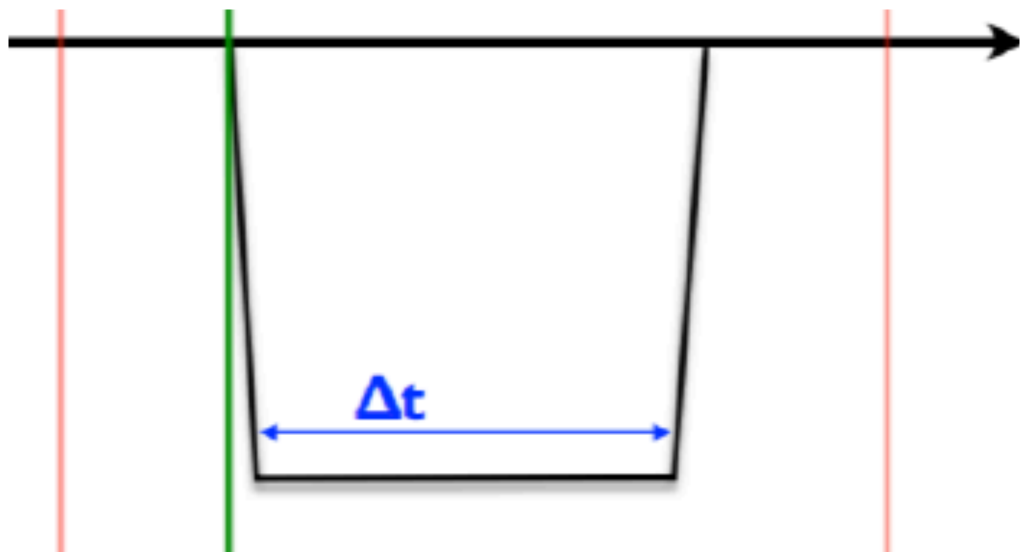
DDS READOUT BEYOND ADC-DEADTIME



LIMITED BY USB (V0 PROTOTYPE)

ABC'S KINTEX7 FPGA(+)2GB-DDR: UP TO ~10M EVENTS (PRELIMINARY)

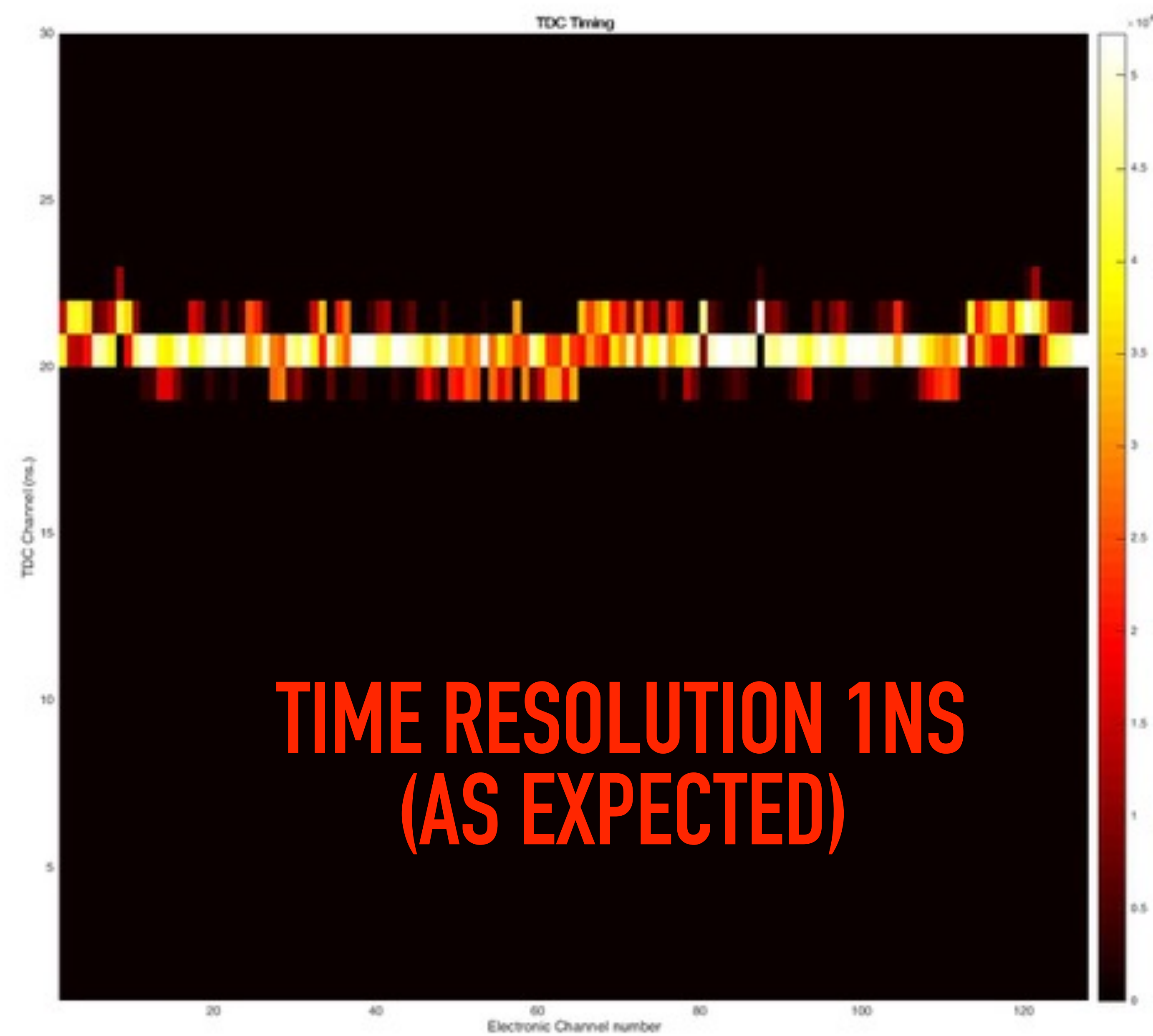
DISCRIMINATOR READOUT: DEMONSTRATION?



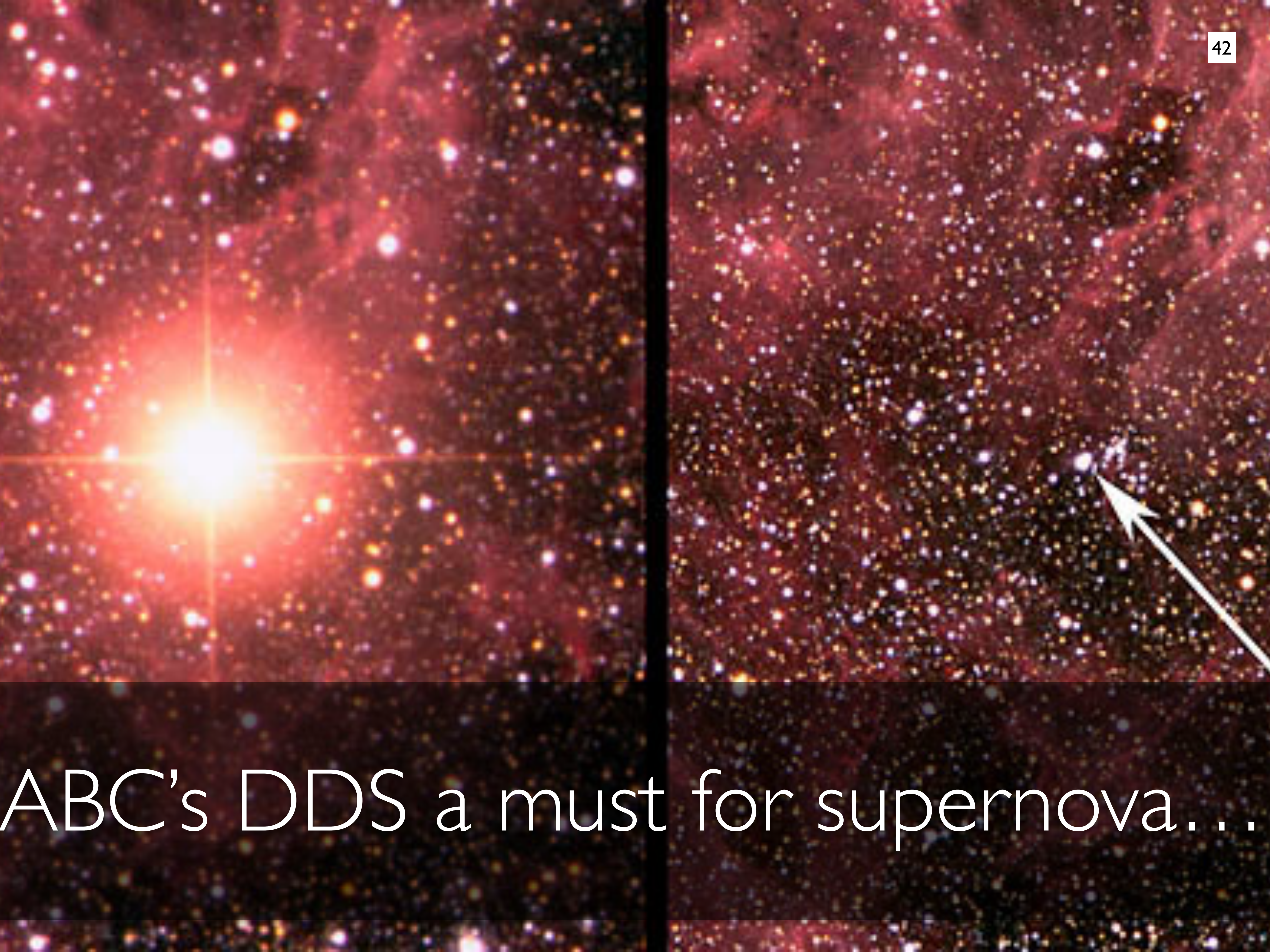
ΔT≈20NS

FPGA DIGITAL SAMPLING @ ~1GHZ

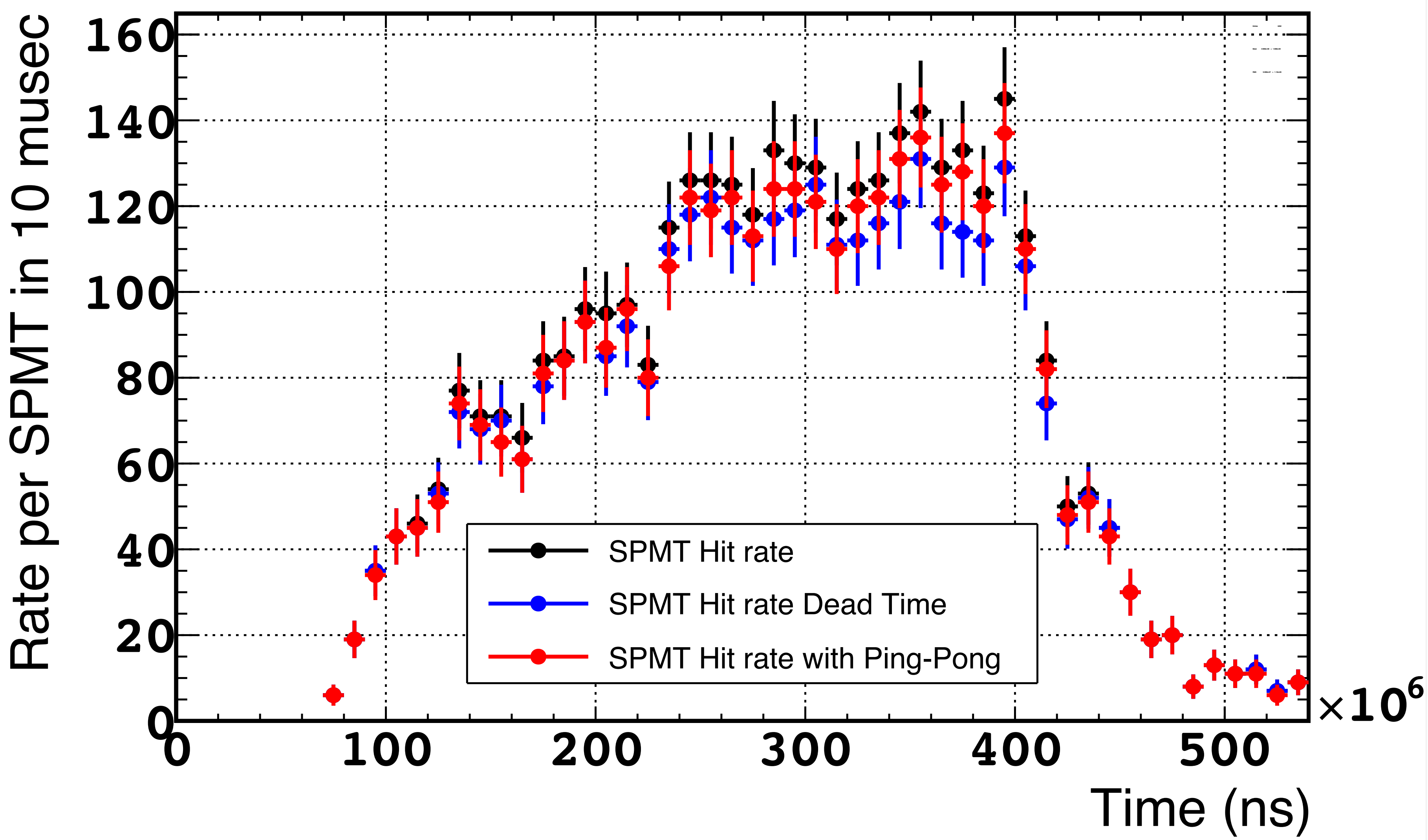
PRELIMINARY: TIME SPREAD CONSISTENT WITH JITTER



TIME RESOLUTION 1NS
(AS EXPECTED)


ABC's DDS a must for supernova…

IMPLICATIONS TO SUPERNOVA OBSERVATION



expected…

•readout DDS

•readout ADC-only

(ping-pong⊕no noise)

•readout ADC-only

(→noise deterioration)

to be demonstrated

(full readout behaviour needed!)

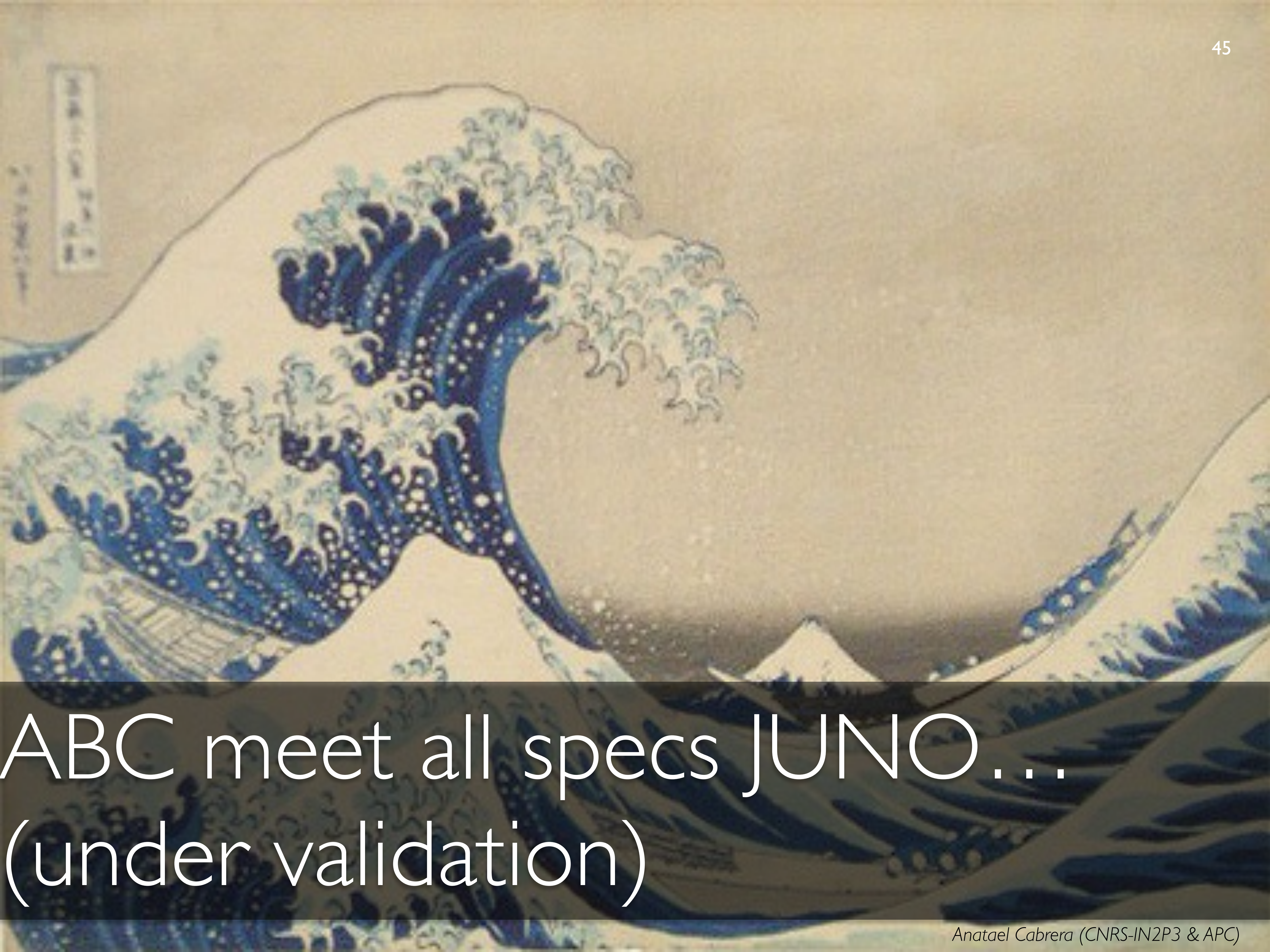
DDS IS A MUST FOR SUPERNOVA!

A FAST-PMT / SIPM READOUT

- DEADTIME-LESS (≤100K/S)

SUPERNOVA: 10M EVENT BURST CAPABILITY

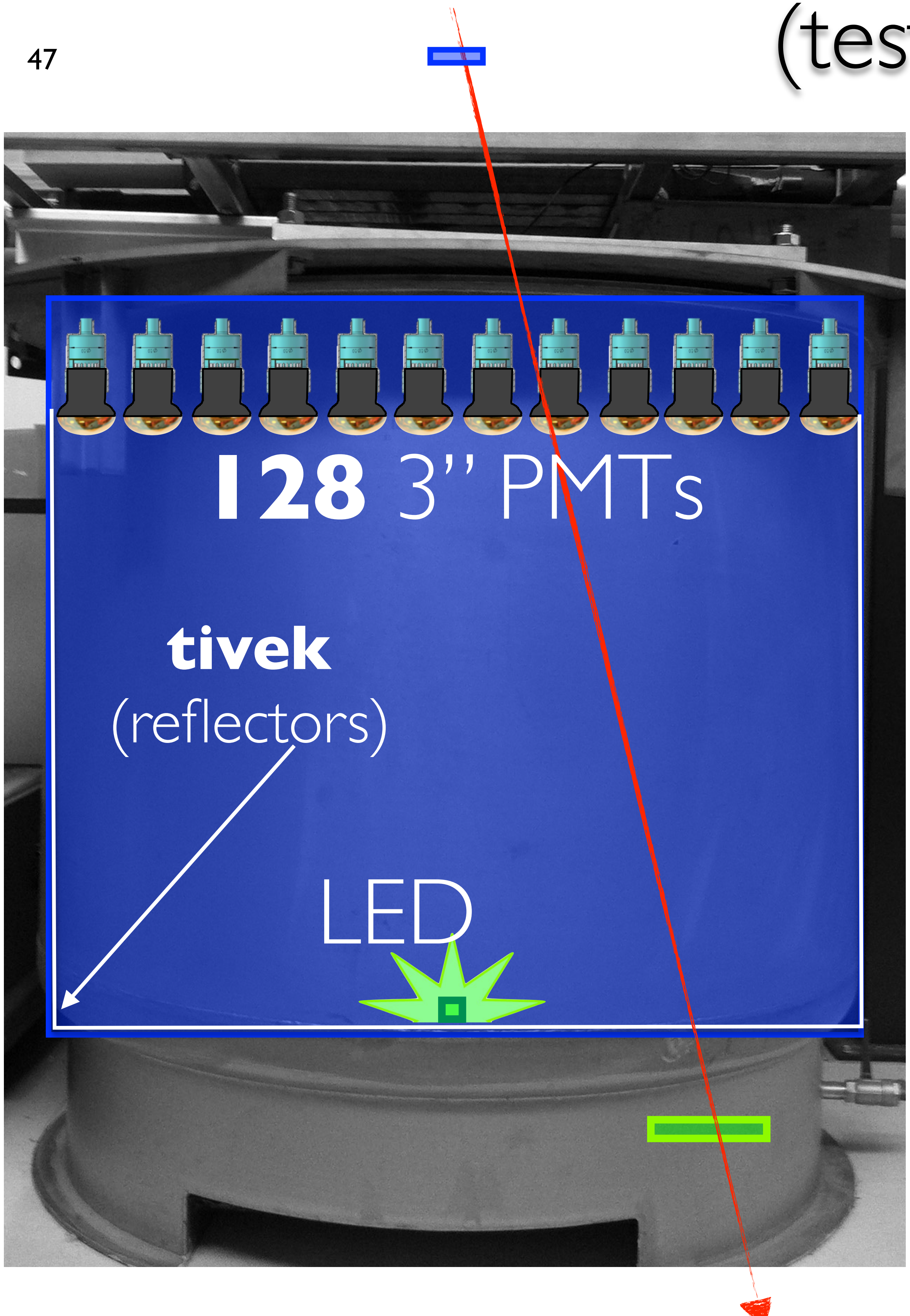
- TRIGGER-LESS (“PE-STREAMING”)
- LINEAR (≤400PE)
- FAST!! (~50PS TIME RESOLUTION)
- WATER-CHERENKOV OR SCINTILLATOR (LOW-MULTIPLICITY)



ABC meet all specs JUNO… (under validation)


ensure all works…

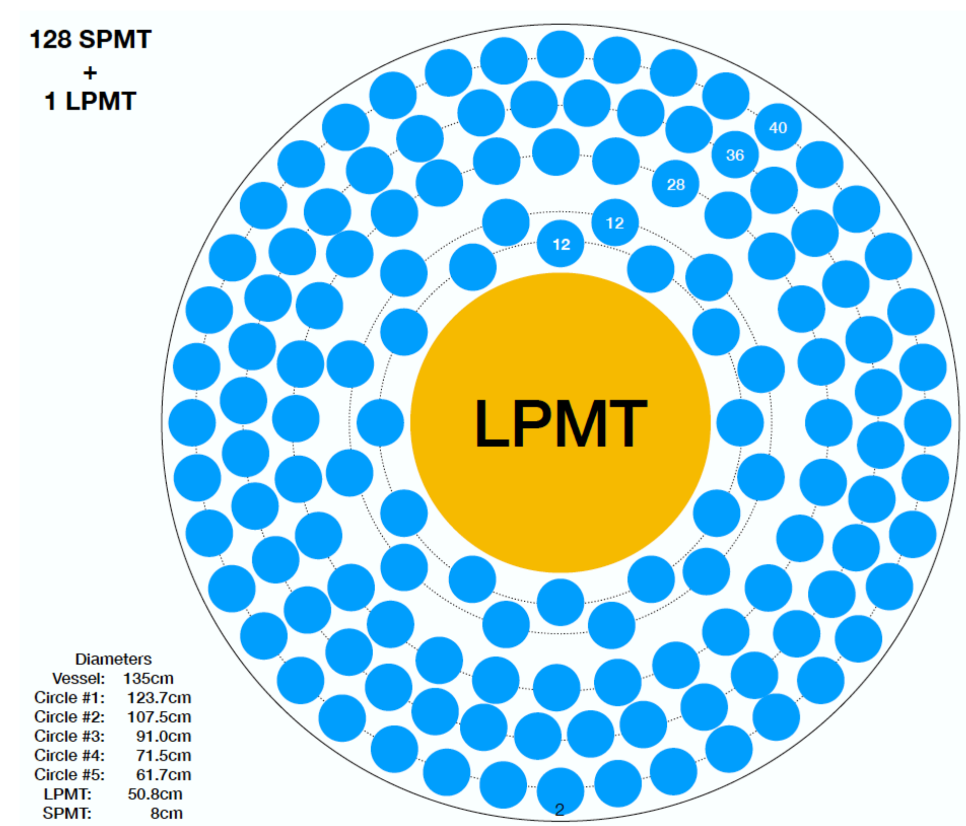
(test before) JINO @ IN2P3…



Φ=135cm M≤1.4tons

JINO (prototype) goals…

- **full system integration**
- **electronics/DAQ validation**
  - ABC card performance
  - multi-card synchronisation
- **supernova** high rate test/optimisation
- **stereo-calorimetry** data validation
- **pre-installation full system**



SPMT readout...

- √ fast timing PMT (resolution) & digitation [reactor-ν]
- √ trigger-less (PMT dark-noise) [new physics?]
- √ deadtime-less (DDS) [support supernova]
- √ full detector readout [water-Cherenkov ideal]

SiPM seem to be supported too (to be validated)

but JUNO less light (≲3%)!! [for stereo-calorimetry]

grazie...

thank you...

谢谢...