# TIMESPOT
## DAQ Hardware Development

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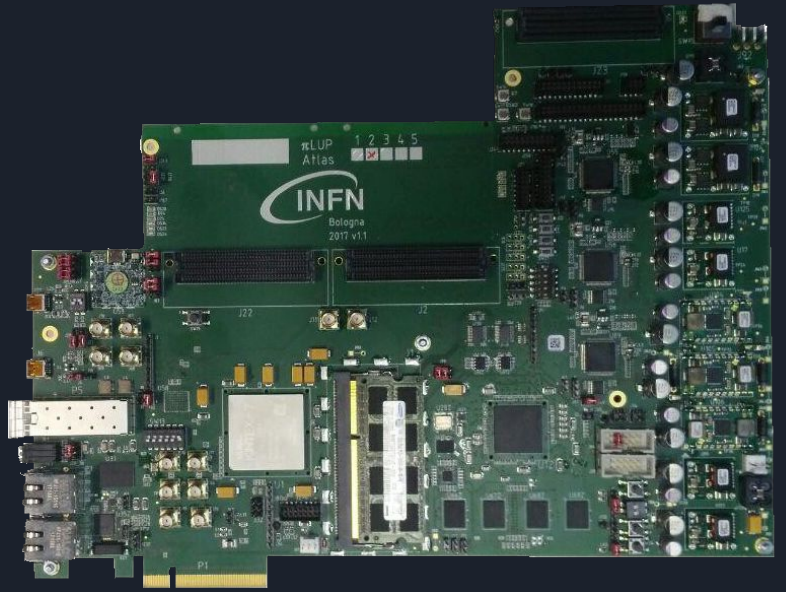
# *Reminder* - The **PiLUP** board

*Our proposal:* use the **PiLUP** board (developed internally for the ATLAS upgrade) for this setup:

- based on a XILINX **KINTEX FPGA** (easy to transpose their FW)
- already available in Bologna
- Very flexible, due to the presence of a XILINX **ZYNQ SoC** (FPGA + ARM dual core CPU)
- Zynq & Kintex in a standard Master/Slave configuration
- High number of output channels using multiple data transmission paradigms (PCIe, optical, ...)
- TIMESPOT emulator can be derived from the RD53A emulator (*N.Giangiacomi*)



# Previous (March18) ToDo List

Done:

- The proposed board, PiLUP, has been designed, developed, debugged and enhanced
- Every aspect of the board (electric parasites, connectivities, access to peripherals) have been tested with dedicated FW and SW
- **PetaLinux** has been implemented on the board, providing a reliable way to operate on the system
- A software framework (**PLUTO project**) for low-level operativity is being developed

ToDo (in the near future):

- We still lack the Neural Network FW implementation (INFN Milano/other ideas?)
- The emulator for a TIMESPOT-like data format is not ready yet

# TIMESPOT Emulator

- Nico (currently @ BNL) is working on a firmware implementation of the RD53A emulator on the PiLUP (and other XILINX-based systems as well)
- Nico provided us both the emulator code and various external "**handles**" to control the emulator via software
- The idea is to control various parameters of the emulator (data format, timing, etc.) at least partially from software using the **PetaLinux** system currently running on the XILINX ZYNQ SoC
- We are currently performing preliminary checks on the system, (the emulator is not implemented yet on the PiLUP)

Neural Network implementation

- No FW yet, as we (*Gabriele*, *Giuseppe*) are still studying possible implementations on the PiLUP.

# BACKUP

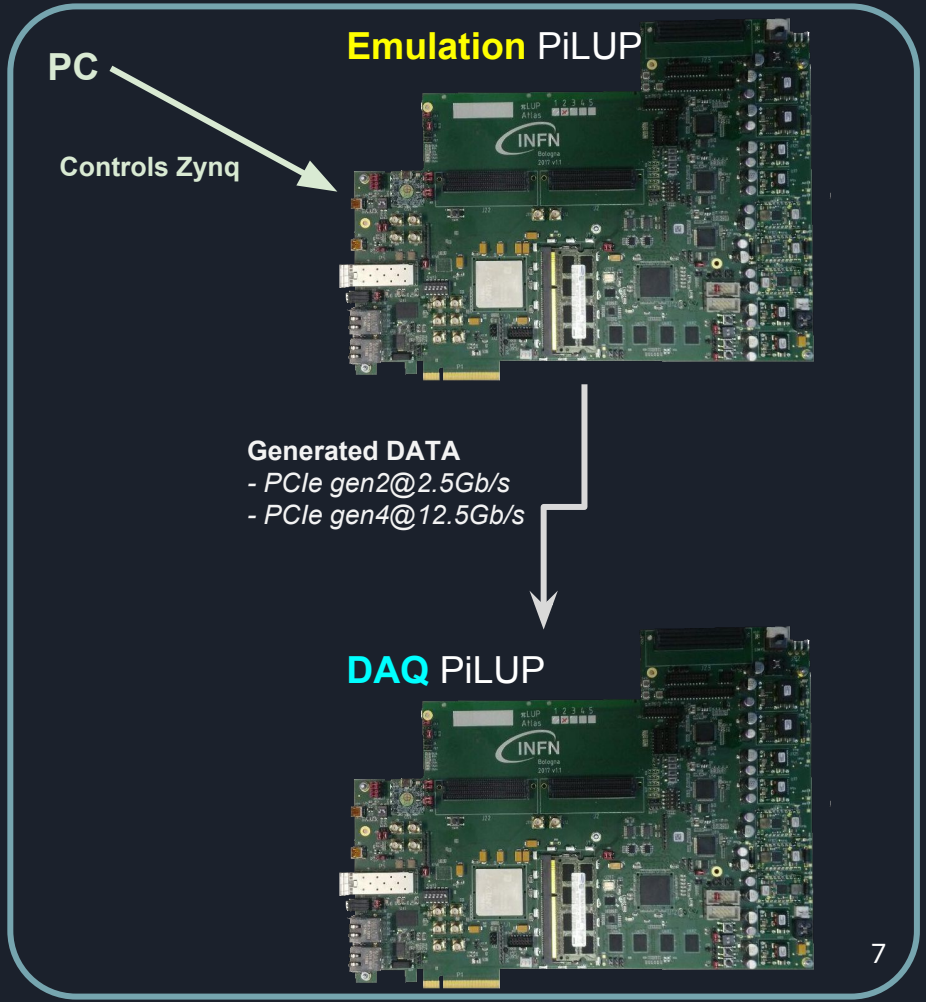
# Bologna WP Task

- As previously introduced, our WP is tied to the DAQ of the sensor
- As march 2018, the proposal for the data reconstruction algorithm is based on a **Retina-like Neural Network**
- INFN Milano has developed a firmware implementation (Kintex-FPGA based) of this algorithm
- We have to develop the **hardware to run** this Neural-Network
- Also, having an **emulator** of the proposed detector data output would help…

What if we put everything on the same system?

# Proposed Setup

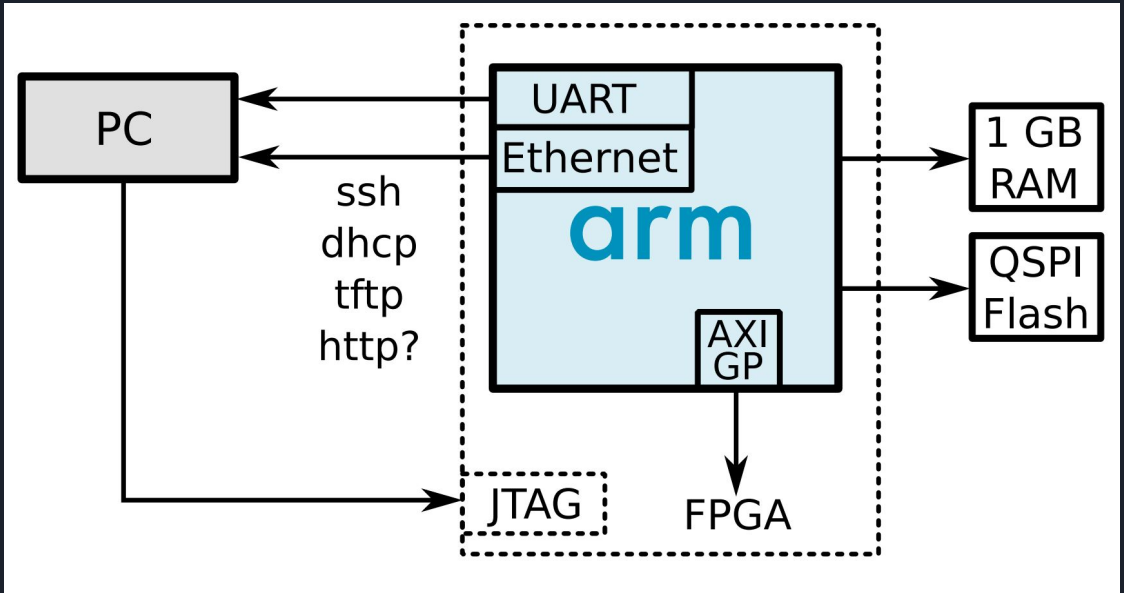
- Zynq on the **Emulation PiLUP (ePI)** receives commands from PC
- Using the internal bus, sends commands to the ePI Kintex to start emulation
- generated data is sent via PCIe to the **DAQ PiLUP (dPI)**
- dPI Kintex implements the Neural Network reconstruction



# Proposed Setup

# PetaLinux setup

***What is Petalinux?***
Petalinux is an SDK to automate building and deploying embedded linux system on Xilinx devices (Zynq SoC) (*implemented by G.Gebbia*).




- Communication with Zynq can be based on know non-fancy protocols (ssh, ...)
- Operativity of a full **Linux machine**
- Protocols, C/C++/whatever else code can be **implemented on the fly**

# PetaLinux setup - Chip2Chip

- Master/Slave configuration lets us exploit the **AXI Chip2Chip** paradigm
- Kintex becomes an extension of the Zynq
- Operations on Kintex can be driven by Linux too