INFN

# Silicon Pixel Trackers

VI Seminario Nazionale Rivelatori Innovativi
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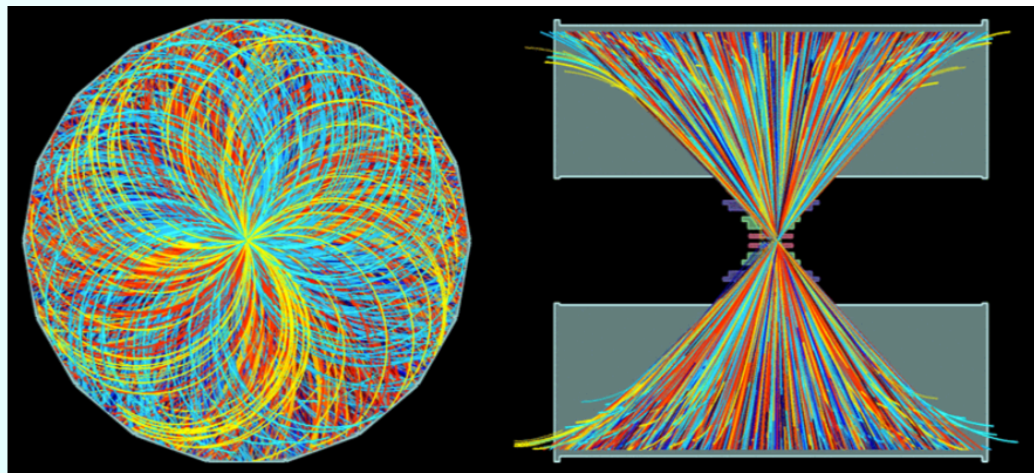
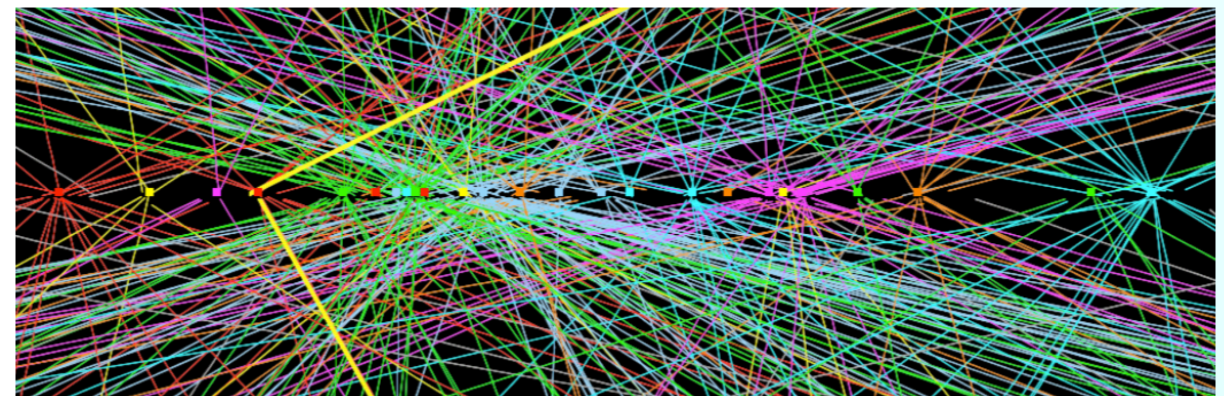
C. Sbarra, A.Cervelli

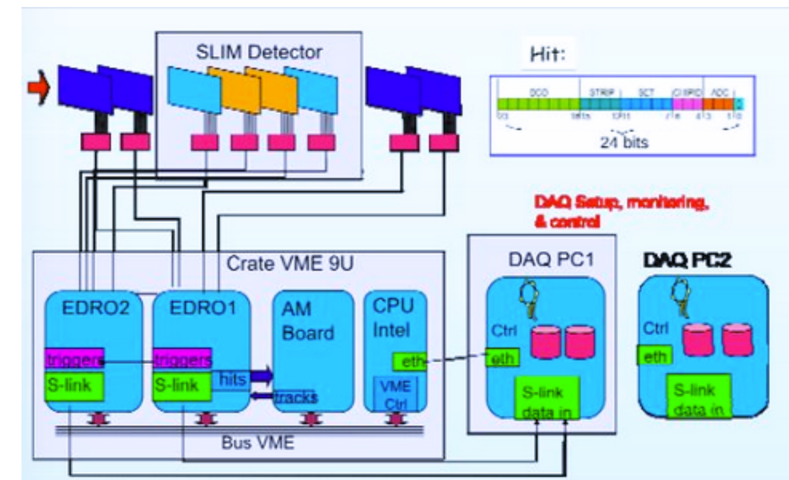


Pb-Pb event (ALICE, 2011)



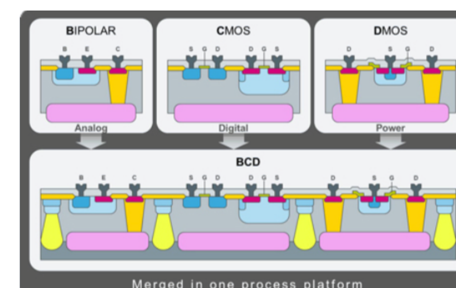
Candidate Z—> μ+μ- event among 25 reconstructed vertices (ATLAS, 2012)

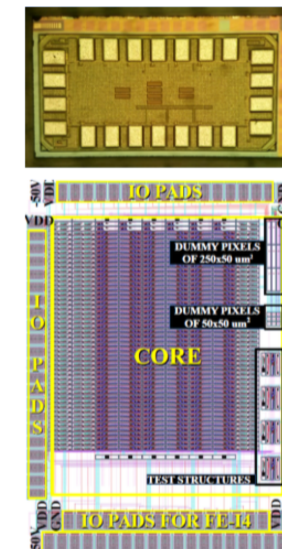
# Bologna activities

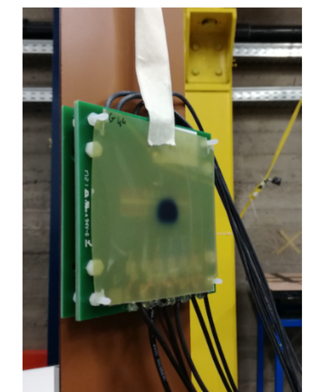


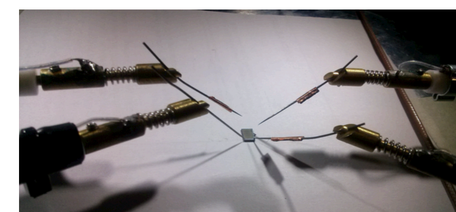

## Slim5 (2006-2008) & Vipix (2009-2011)

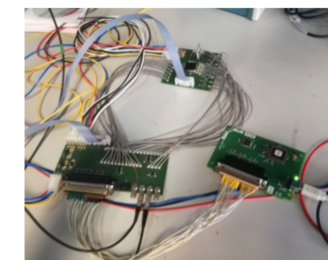
- **Ultra-thin** silicon detectors (Monolithic Active Pixel) and vertical integration technologies for hybrids
- Mainly targeted to **SuperB-like** environment & needs
- Bologna responsible for beam-test off-detector electronics & SW + digital readout architecture for MAPs and hybrid readout chip







## HVR-CCPD (2015-2017)

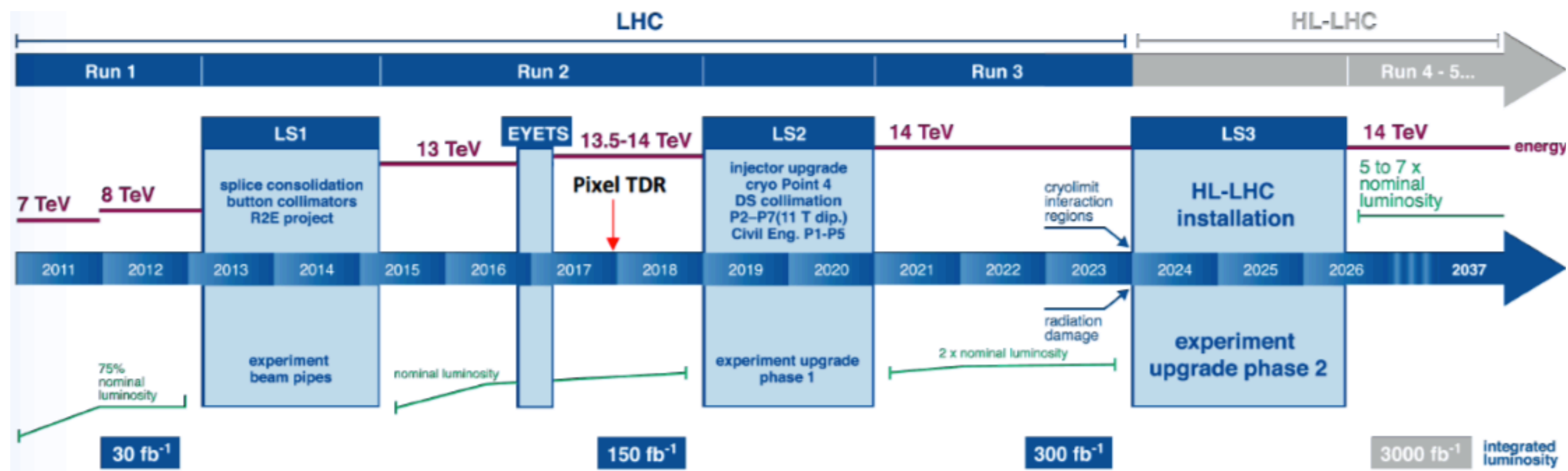
- High Resistivity, High Voltage **CMOS** detector in BCD8 technology (STMicroelectronic) Capacitively Coupled to a Readout ASIC
- Targeted to **HL-LHC** trackers and X-FEL imaging detectors
- Bologna responsible for test board + contributions in technology qualification

## Atlas ITK (HL-LHC)

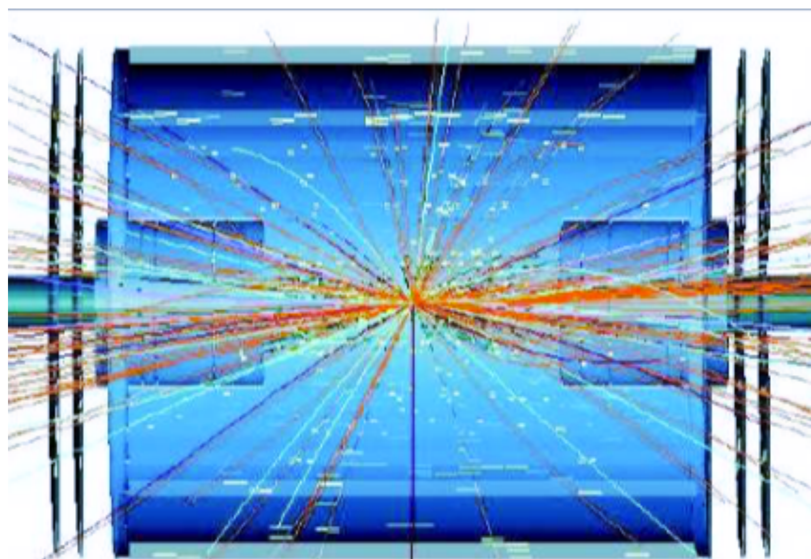
- Quality Check of pixel modules during production

**Focus on silicon pixel trackers for future hadron colliders**

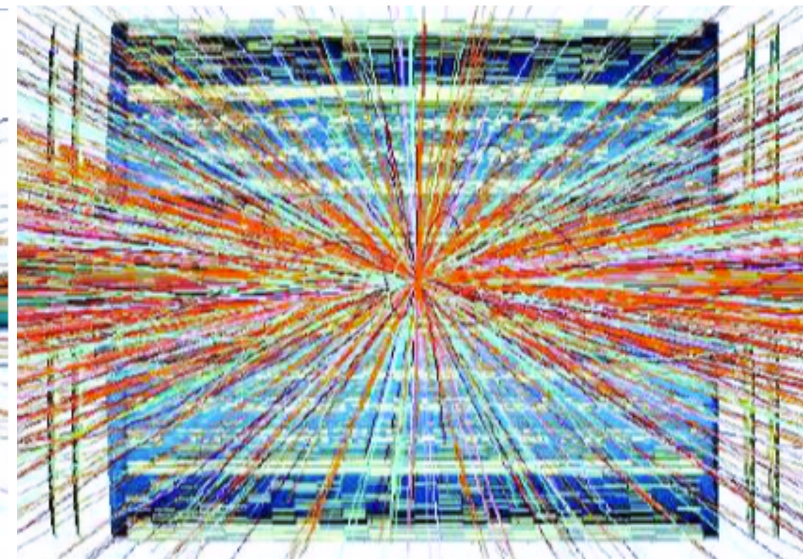
# High Luminosity LHC




A factor ~10 increase in integrated Luminosity with respect to LHC:
radiation hard sensors and new readout electronics

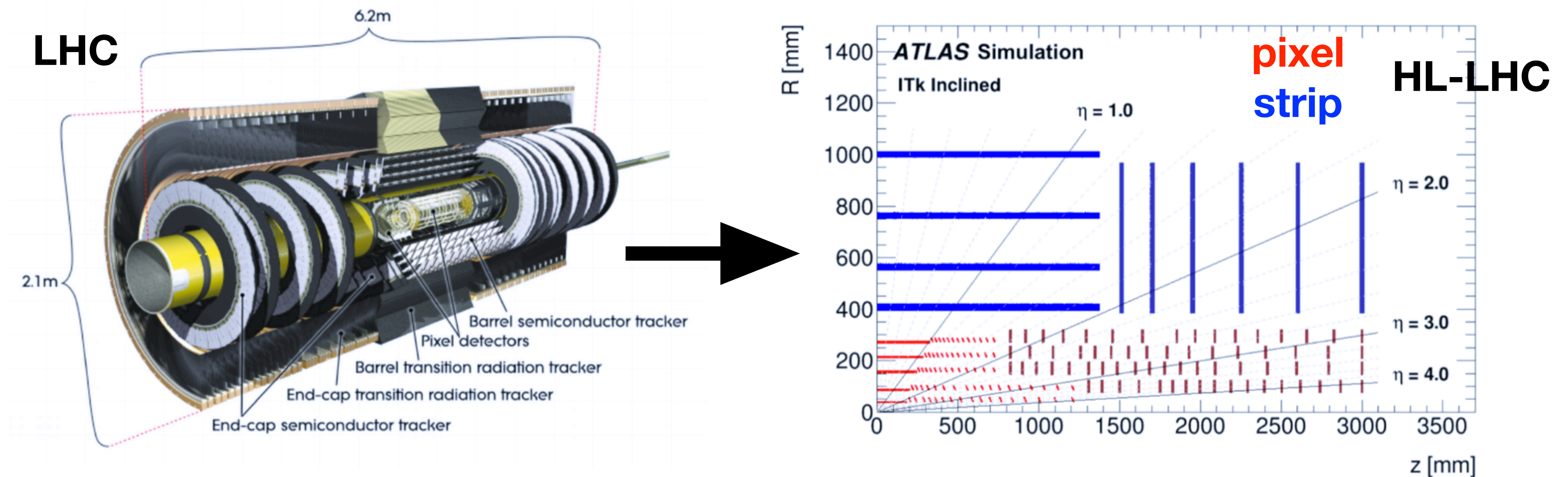


**LHC in 2011**
**pileup ~ 25**



**HL_LHC**
**average pileup ~ 200**

# ATLAS Inner TracKer




- All silicon: strip surface ~150 $m^2$, pixel ~12 $m^2$
- Fluencies from 2-3·$10^{16}$ 1 MeV $n_{eq}/cm^2$ (innermost layer) to 2·$10^{15}$ 1 MeV $n_{eq}/cm^2$ (outermost pixel layer)
- Pixel area 50x50 or 25x100 $\mu m^2$ to keep ‰ occupancy
- **Hybrid Pixel Detector** with improved radiation hardness, granularity, production yield
- High hit-rate —>New RO ASIC in 65 nm CMOS technology for both ATLAS and CMS (RD53)

# Hybrid Pixel Detector fundamentals

- pn junction between moderately (~$10^{12}$ cm$^{-3}$) doped silicon bulk (high resistivity, 100-500 µm thick) and heavily doped (~$10^{14}$ to $10^{16}$ cm$^{-3}$) pixel implants
- reverse bias to depleted bulk
- pixel implants electrically connected to a ReadOut chip (low resistivity custom CMOS ASIC), with channels *matching* sensor pitches, via solder bump-bonds
- Each channel in the RO-ASIC typically hosts preamplifier(s), shaper and a comparator (few 100 transistors in current LHC experiments)

**Silicon facts:**

$$n_i^2(T = 300\ K) \simeq 10^9$$

$$\mu_e = 1350\ \mathrm{cm}^2/\mathrm{Vs}$$

$$\mu_h = 480\ \mathrm{cm}^2/\mathrm{Vs}$$

MIP release ~ 80 eh pairs/µm (MPV)

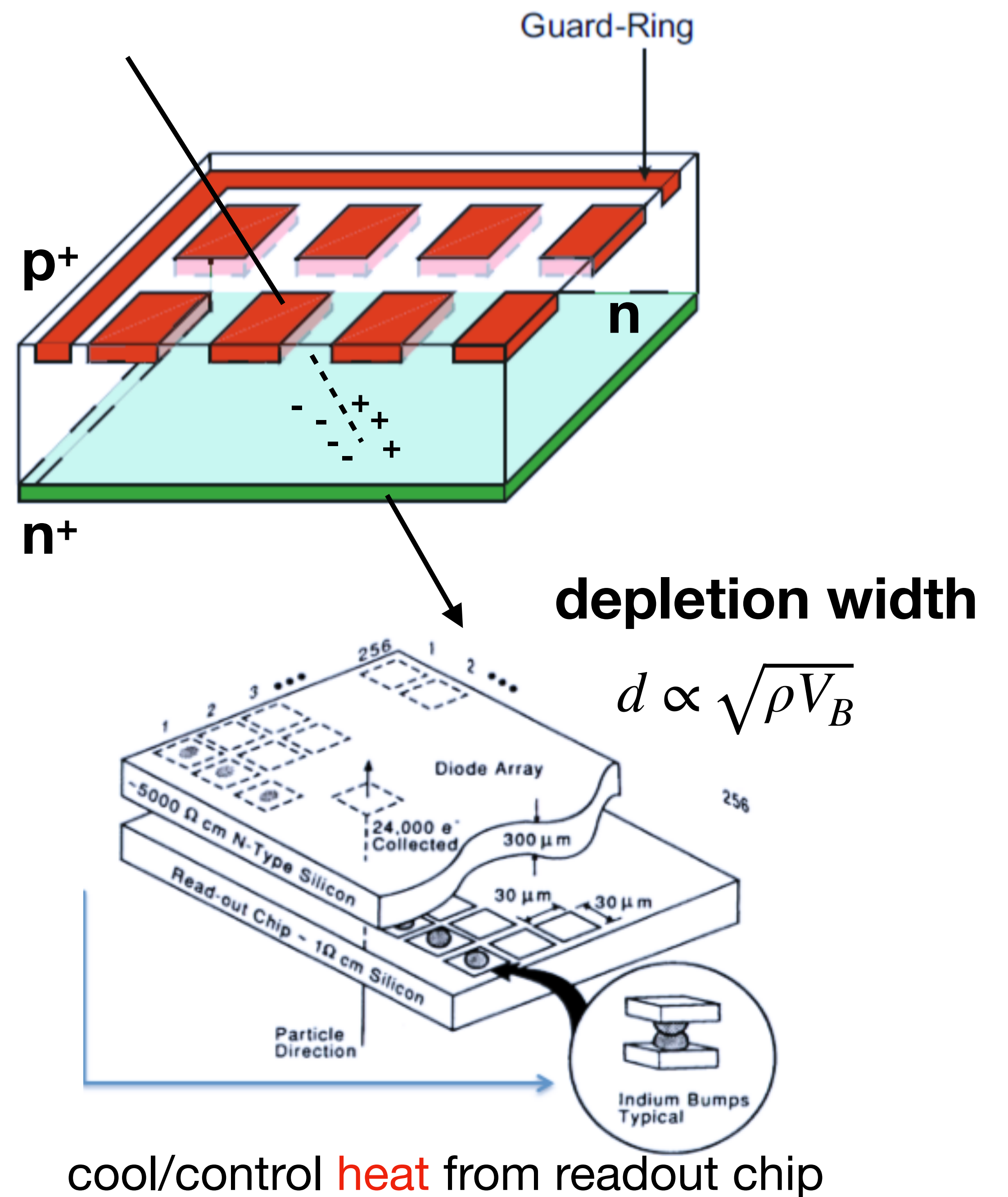
**Collection time**

$$t = \frac{d}{\mu E} = \frac{d^2}{\mu V_B}$$

**leakage current**

$$I_{leak} = \frac{e n_i(T) V}{2\tau}$$

$$I_{leak} \propto T^{3/2} e^{-\frac{E_g}{kT}}$$




$$d \propto \sqrt{\rho V_B}$$

cool/control heat from readout chip

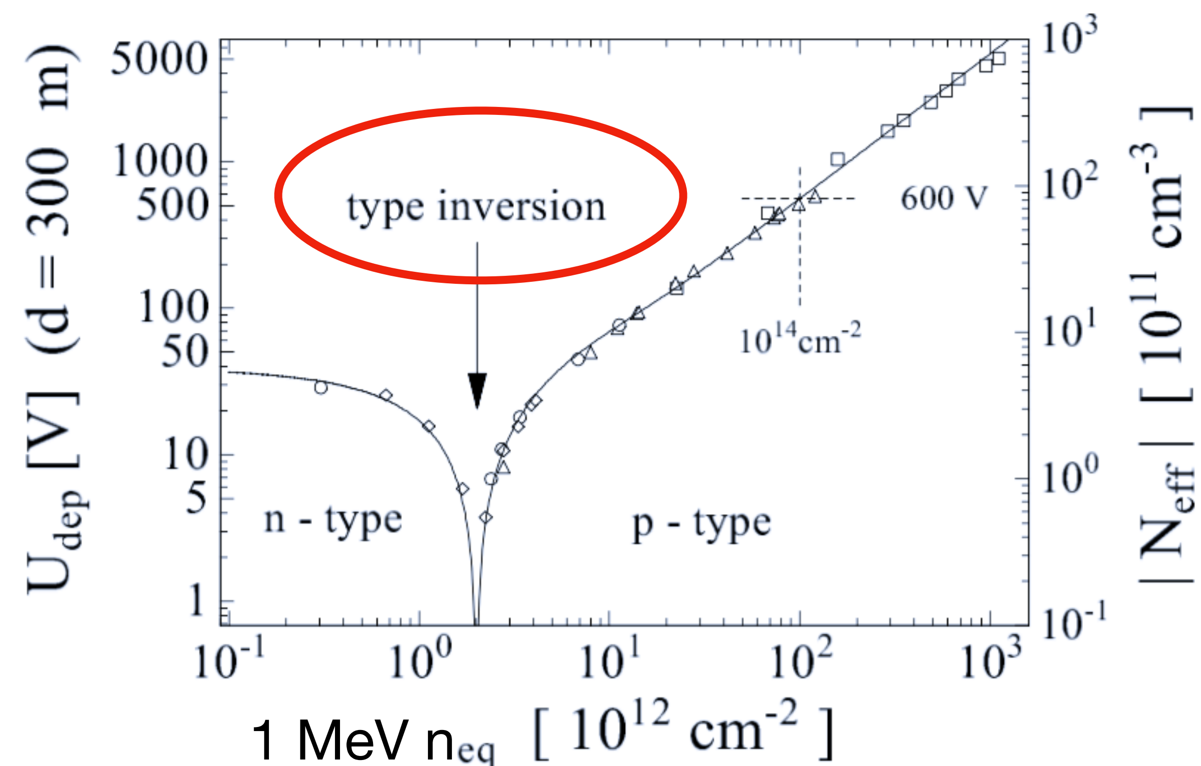
# Radiation effects in silicon

Different radiation type produce different damages (vacancies, intestitials, displacements)—> scale Non Ionising Energy Loss (NIEL) to damage caused by fluence of 1MeV neutrons ($\Phi_{eq}$ or $n_{eq}$ $cm^{-2}$)

## Bulk

$$I_{leak} = I_{leak}^{unirr} + \alpha \Phi_{eq} d A$$

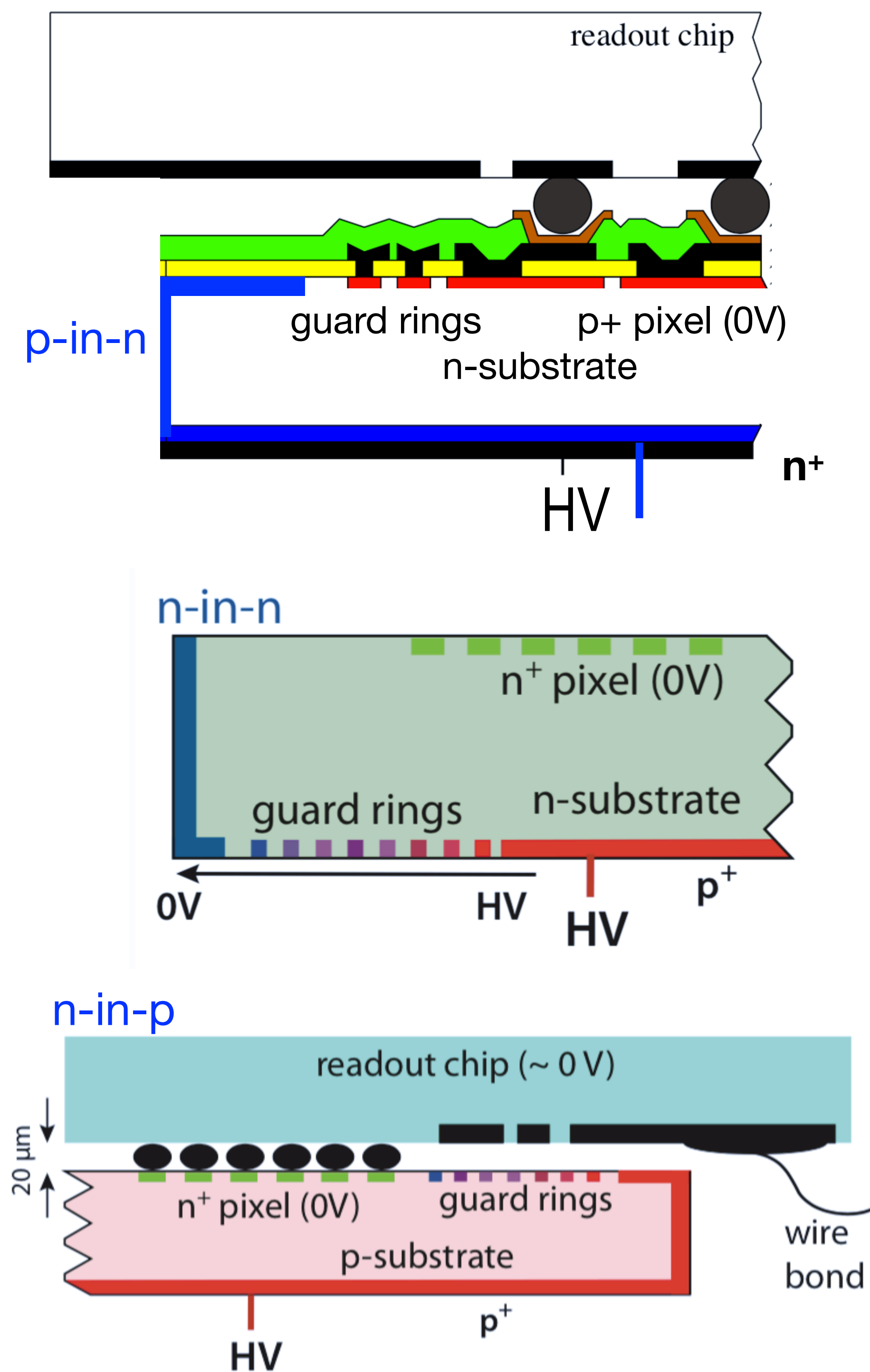
- Increase of leakage current
- Change of full depletion voltage and effective doping ($N_{eff}$)
- Creation of trapping centres




## Surface

- Positive charge on silicon oxide —> compensating electrons accumulation in n-type silicon, depletion layer in p-type
- Surface current area not covered by pixels implants contributing to dark current

# Planar Sensor Radiation hardness




## First generation - p-in-n

- Single side, 1-2 guard rings (gradual voltage drop)
- Edge/RO-chip distance uncritical ($V_{depl}$ < 100 V)
- pn junction initially on structured side, then on backside

suitable before type-inversion

## LHC standard ($5{\cdot}10^{15}\ n_{eq}cm^{-2}$) n-in-n

- Double-side process (twice in cost, lower yield)
- pn junction initially on backside, then on pixel side
- pixel isolation via p-stop/p-spray
- No sensor edge/RO chip problems (both at ground)

expensive

## HL-LHC ($2{\cdot}10^{16}\ n_{eq}cm^{-2}$) p-in-n

- Single side (cheaper than n-in-n)
- Thin (~150 µm)
- Sensor edge close to RO chip needs protection ($V_B$<600-700 V)

Cost effective

# The ReadOut ASIC

**Analogue block**

- the charge collected in each pixel is amplified, shaped, and compared to a programmable threshold

**Digital part**

- Calculates and transfer the Time Over Threshold to che chip periphery, together with a hit pixel address and a time stamp

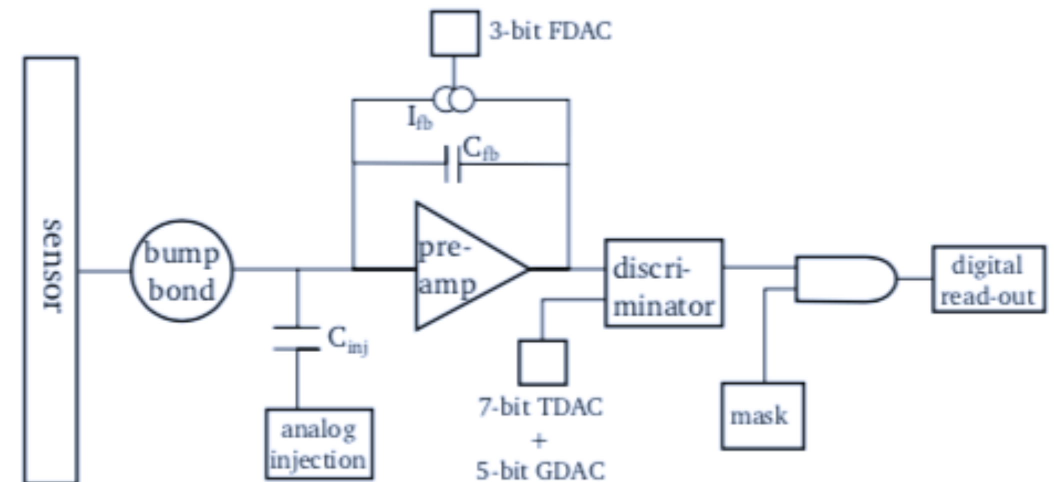
- timing anf triggering

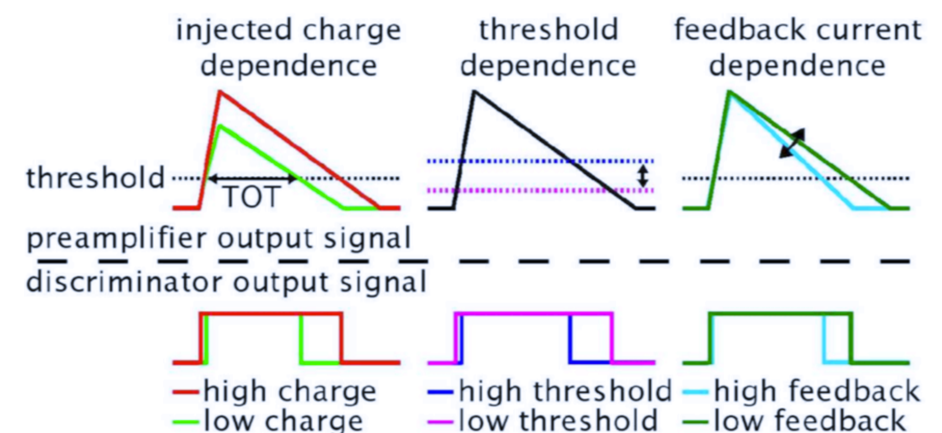
**Radiation Hardness**

- Bulk damage negligible (doping concentration much larger than in the senso)

- Surface damage in $SiO_2$-Si interface depends on Total Ionizing Dose and affects transistors behaviour

- Transient effects SEU

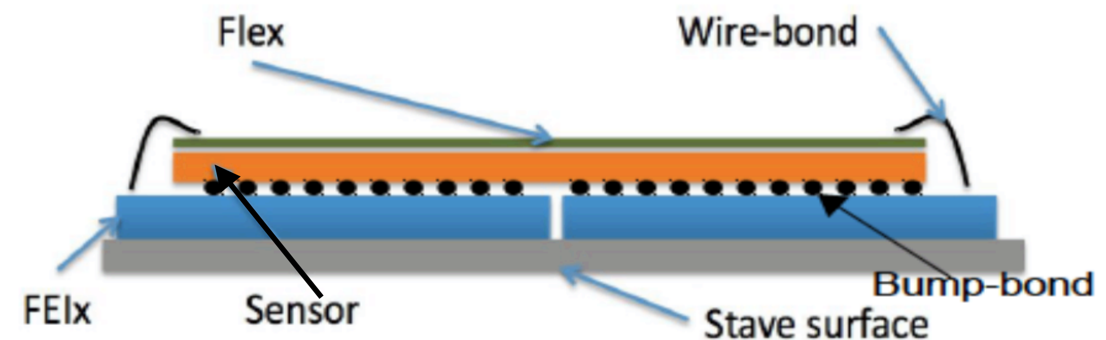


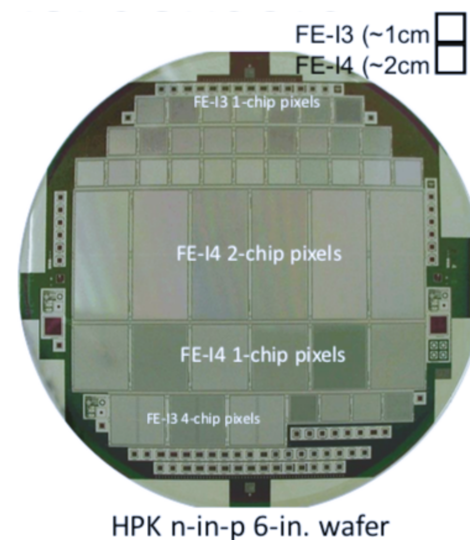



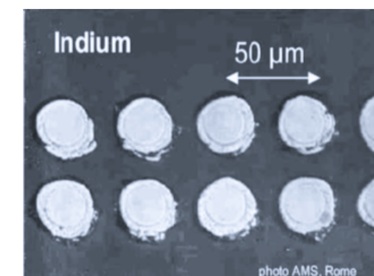

**Pixel thresholds and ToT must be equalised before use**

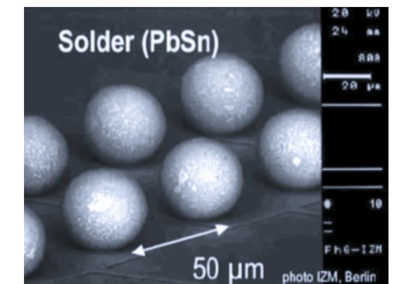
# Hybrid Module Production Chain

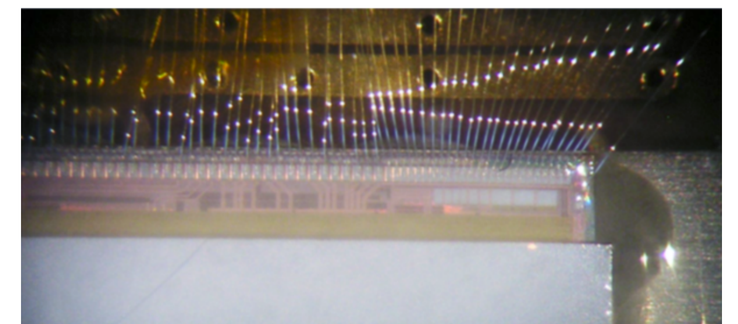
- Wafer production (4” or 6” diameter, specialised foundries)
- Bare wafer testing (IV and CV diode characteristics to check for quality and determine $V_{depl}$, $V_{break}$)
- Bump deposition (specialised foundries), wafer cut, and flip-chip
- Bare module glueing to flex/ support PCB
- Wire bonding (HV to sensor, LV to readout chip, I/O lines)
- Electrical, mechanical (thermal stress) and functional tests (both of sensor, ReadOut ASIC and interconnections) before loading



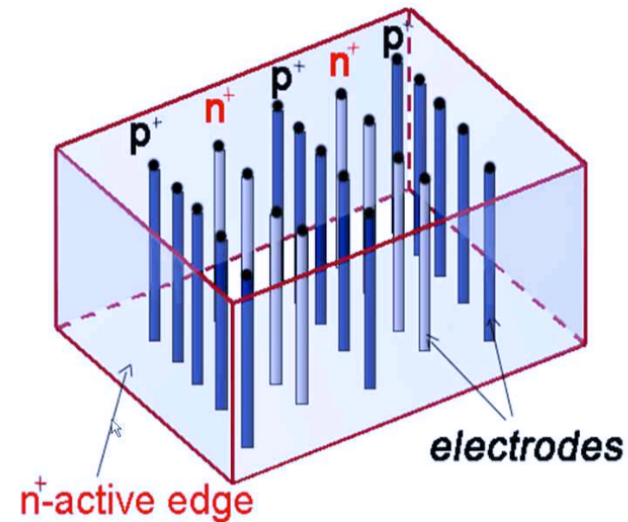



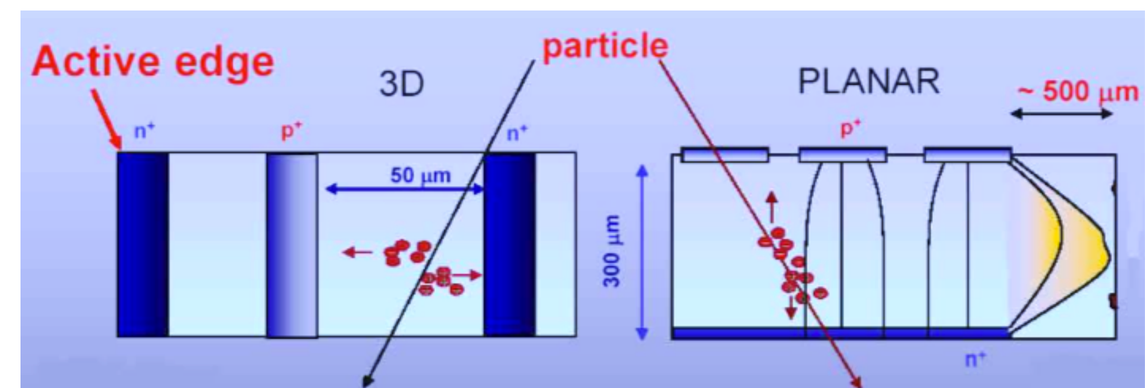



# 3D sensors

- Pillar shape electrodes penetrating sensor bulk orthogonally to surface
- Drift distance decoupled from depletion width
- PROs:
  - Radiation hard (less trapping)
  - High $\vec{E}$, saturation of drift velocity
  - Reduced operational $V_{Bias}$
  - Large active area (active edge)
- CONs:
  - Few foundries (difficult process)
  - Lower yield, higher cost
  - Larger capacitance




Already used in **ATLAS IBL & AFP** Both single and double-side processes exist



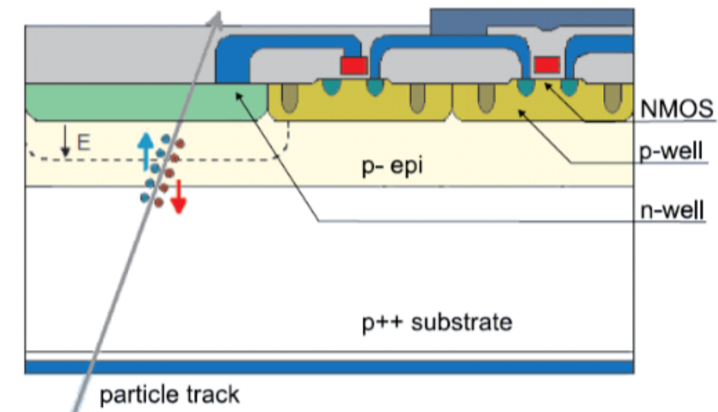

**Selected for innermost layer of ATLAS ITK**

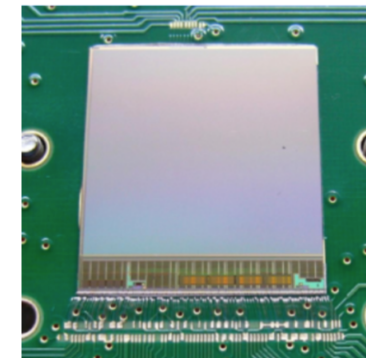
# MAPS & DMAPS

### Monolithic Active Pixel

- pn junction between CMOS n-well (ρ<1 Ωcm) and p-epitaxial layer (ρ~10 Ωcm)
- everything in one substrate (sensor + readout)
- Depletion depth in epitaxial layer < 1 μm
- Charge collected by diffusion: slow, not rad-hard
- Thin, high granularity
- Commercial CMOS processing (many foundries)
- Large wafer 8” or 12”

$$d \propto \sqrt{\rho V_B}$$



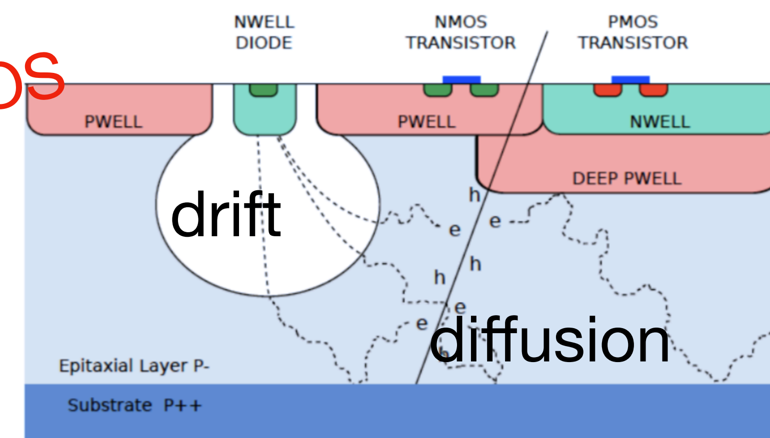
MAPS for STAR upgrade
Readout time 190 μs
TID 150 krad
NIEL few $10^{12}$

### Depleted Monolithic Active Pixel

- Profit of industry developments for phone cameras
- High resistivity epitaxial layer—> depl. depth to few μm
- High Voltage ( adds-on from automotive industry) > depletion depth in 10-30 μm range
- Existing DMAPS withstand up to O($10^{14}$) $n_{eq}/cm^2$
- Developments to full depletion and rad-hardness to O($10^{15}$) $n_{eq}/cm^2$

HR-CMOS

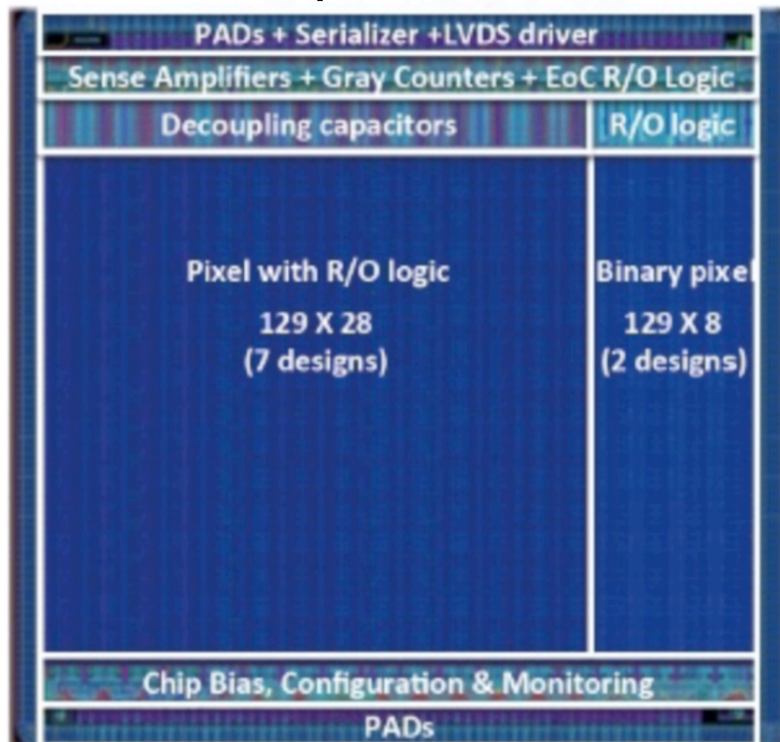
HV-CMOS



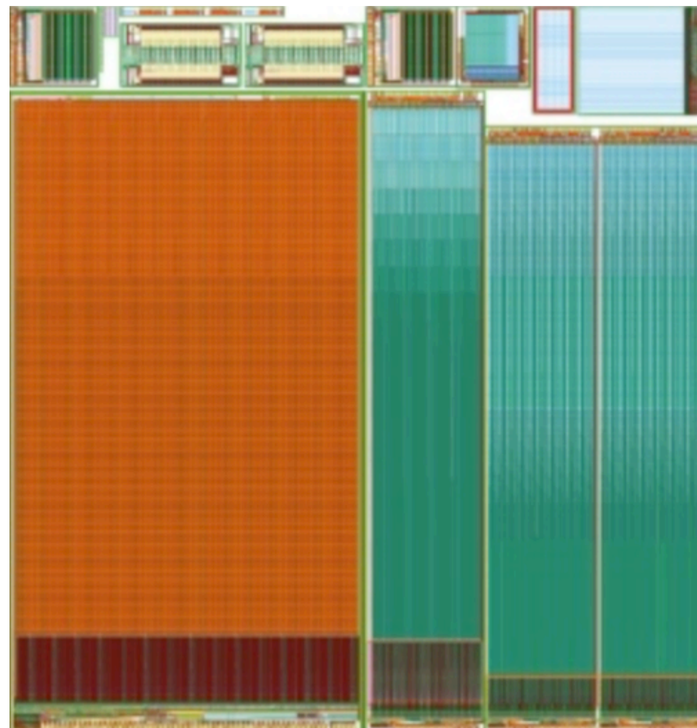

Schematic cross-section of CMOS pixel sensor (*ALICE ITS Upgrade TDR*)

# DMAPS studies for ITK

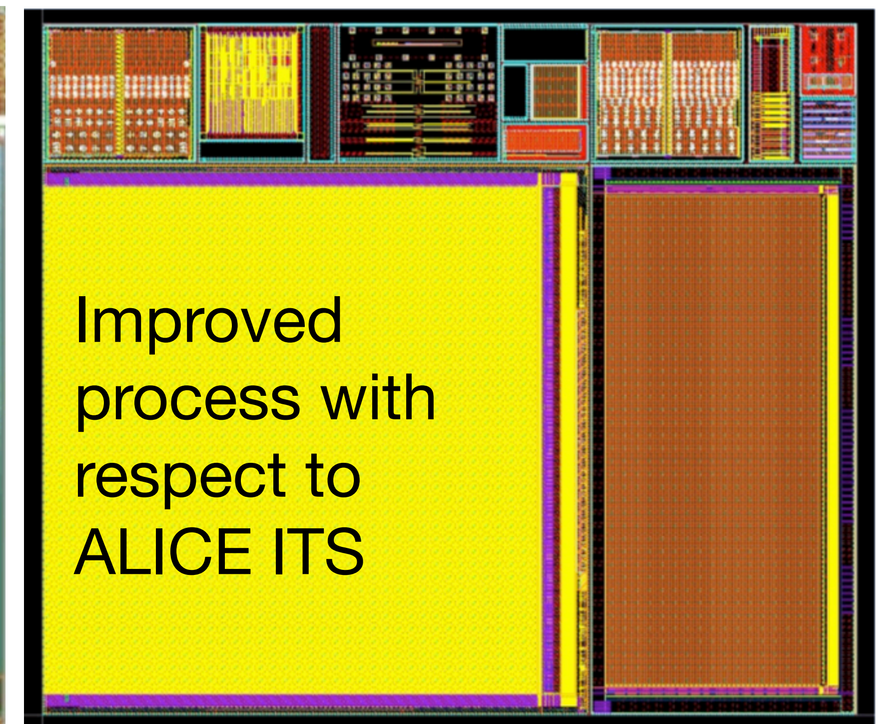
**LFoundry** 150 nm
substrate ρ > 2 kΩcm



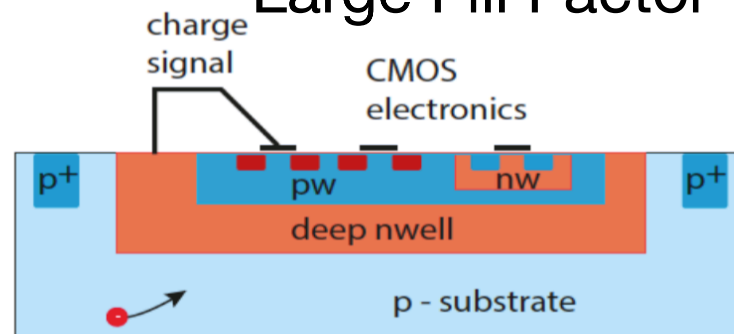

**AMS** 180 nm
substrate ρ ~ 1 kΩcm



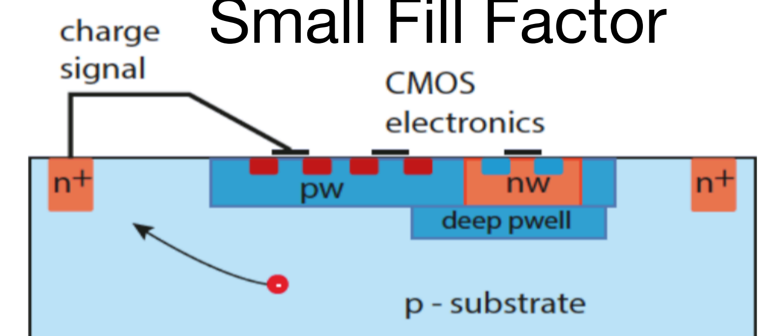
**TowerJazz** 180 nm
substrate ρ > kΩcm




Large Fill Factor




Small Fill Factor




**Still an option for outermost layer of ATLAS ITK**

# Hands-on

- Look at prototype chips with a microscope and check for defects and broken wire-bonds (get a feeling of field complexity, needed instrumentation and infrastructures for development and testing)

- Tune the readout chip of a planar pixel module, bias the sensor, compare noise with and without bias, check rensponse to radioactive source

- Perform IV scans on different kind of sensors inside a climate chamber to identify $V_{dep}$ and $V_{breakdown}$, check sensor quality and T dependence:

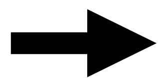
  - ATLAS IBL-like planar module
  - ATLAS IBL-like 3D module
  - LFCPIX chip (LFoundry, HR/HV-CMOS)

**more detailed instructions in the lab**

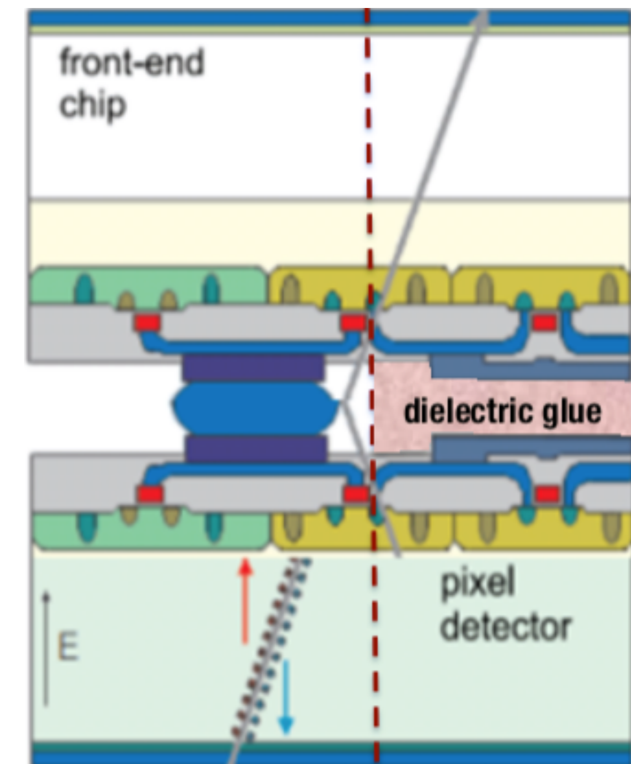
# further material

# Capacitive Coupling

Bump-bonding cost for hybrids similar to sensitive part, limited yield



- Exploit depleted HR/HV-CMOS:
  - avoid trapping after irradiation
  - keep in time (25 ns for HL-LHC)
  - first stage of amplification in sensor




- Use capacitive coupling between CMOS sensors and ReadOut chip
  - less elaborate assembly, cost effective, larger yield
  - Fast turn-around production for large volumes
  - Pixel size of 50x50 $\mu m^2$ and smaller (25x25 $\mu m^2$ feasible)
  - Glue uniformity obtained with use of pillar spacers
  - Separate functionalities of smart sensor and readout chip to exploit best technology on each side

studies in Genova & Geneva Univ.