Status of the PADME Mimosa and Timepix3 detectors Beam Monitor

- 1. Introduction
- 2. Pixels for PADME beam monitoring
- 3. The Mimosa pixel sensors for PADME beam monitor
- 2. The Timepix3 sensors PADME beam monitor
- 3. Conclusions

### **PADME beam diagnostic**

Mimosa pixel sensor based beam monitor ( in vacuum )

> Timepix3 pixel sensor based beam monitor ( NOT in vacuum )

- Knowledge of the beam parameters is a key in the PADME experimental technique:  $M_{miss}^2 = (P_{e^-}^4 + P_{beam}^4 - P_{\gamma}^4)^2$ 

- PADME needs to measure beam divergence and beam spot to very high precision to obtain a good estimate of P<sup>4</sup><sub>Beam</sub>

- Due to the very this target upstream mimosa monitors cannot be operated during data taking

## **PADME beam monitor**



M28 (Ultimate) sensor glued and
bonded on the hole of the PCB
(2x2 cm area, thickness 50 μm)



# PADME Mimosa beam monitor (where we are) Ultimate boards



## **PADME Mimosa beam monitor**

## (where we are)





# **PADME Mimosa beam monitor**

### (where we are)

### Altera SoC readout board (ethernet output)



Ultimate final board ( housing one M28 pixel sensor )

# PADME Mimosa beam monitor (where we are)

#### All needed cards produced at G&A engineering company.

![](_page_7_Picture_2.jpeg)

![](_page_8_Picture_1.jpeg)

![](_page_9_Picture_1.jpeg)

![](_page_10_Figure_1.jpeg)

#### **Discussion at Advacam company.**

![](_page_10_Figure_3.jpeg)

#### INFN - LNF visit in Prague on 16/02/2018

Friday, 16 February 2018 09:15

#### Mechanics:

Share step file of the mechanical design, even the preliminary for simulation

#### **Electronics:**

Experiment uses 40MHz clock - it should be used also for our device, provided externally

Input to our device is LVDS unterminated, so it could be terminated extra or in our detector

There could be an external sync device that will provide clock to all modules (red version in the image).

So the clock will be the same in all device. In addition, there will be a sync signal that will reset all counters to zero.

INFN system provides LVDS type signals.

"Shutter signal" will be provided (start measurement)

Then there will be "trigger signal" that resets the counters. It must also reset

shutter to reset the fine time counters in pixels

The experiment will run at 50 Hz repetition rate.

INFN will have a Trigger box whether they can decide whether only global counter will be reset or also shutter will be reopen.

Shutter signal has to be at least ~300 to 400ns send earlier to have time to open th shutter. This delay is always precisely the same for each shutter signal.

The timing information is essential for this experiment => all needs to be precisely synchronized with known (constant) delays between modules.

Connectors - all should be LVDS (so no BNC!), connectors RJ45 (internet)

Particles arrive every 20ms and the pulse is 200 ns wide.

"Trigger signal" = reset of global time counter

"Shutter signal" resets the fine time counters in pixels

### Discussion at Advacam company: conclusions.

Signals need to be synchronous at level of 1 ns or better (probably will be 75 ps). Our FPGA should mangle the signals in no way to make it easier debugging. Any extra delays will be done by INFN in their signal.

We will provide busy signal, one signal for the whole device.

Provide timing drawing in the datasheet

Data stream: single TCP/IP connection 1Gb/s.

Starting form mid March we could do tests with beam at INFN for synchronization testing, April might not be available due to maintenance of the accelerator => best time slot might be the end of March and then even better the end of April.

#### Lead time:

Summer (end of June) is currently achievable

The worst scenario is September (INFN shuts down for July and August)

### PADME Mimosa and Timepix3 detectors Beam Monitor status

- Mimosa sensor boards produced.
- Mechanics in vacuum for Mimosa built.
- Flanges (2 flanges housing 50 pins DB50 connectors each ordered (still to be delivered)
- New FPGA readout code designed
  - tested in lab ( phase synchronization working)
- Test of all the board to be done (FPGA code for pedestal to be designed)
- Cooling system (Peltier and fan) available and tested
- Interlock boards to be designed
- Assembly and test of entire system in vacuum to be done
- Timepix3 system definition finalized (trip to Advacam february the 16th)
- Timepix3 cable test at Advacam succesfull
- First mechanical descriprion defined
- Formal quotation request to Advacam today or tomorrow
- Advacam consider viable second or third quarter 2018 as delivery time