SiPM readout circuits for Fast Timing

D. Gascon on behalf ICCUB-TECH instrumentation section and CIEMAT and CERN collaborators

Picosecond Timing Workshop
18/05/2018
I. Introduction
II. SiPM model
III. FE circuits
IV. ASICs for PET
V. Avenues to fast timing
I. Introduction

- Many different ASICs
  - Many possible classifications as well!
- According the input impedance
  - Current mode versus voltage mode
- According the complexity / functionality
  - Pure analogue front-end
    - Section III
  - Mixed-mode including digitization and readout
    - Section IV
- According the application
  - Many applications: PET, LIDAR, vision, life-sciences, particle physics, astrophysics, etc
  - Fast timing is a must in many of them, e.g. TOFPET
I. Introduction
II. SiPM model
III. FE circuits
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V. Avenues to fast timing
II. SiPM model

Vacuum Photomultipliers
\[ G = 10^5 - 10^7 \]
Cd \( \sim \) 10 pF
L \( \sim \) 10 nH

Silicon Photomultipliers
\[ G = 10^5 - 10^7 \]
C = 10 - 400 pF
L = 1 – 10 nH

\[ \text{Rs} = 50 \, \Omega \]

C. De La Taille, Photodet conference, 2012
II. SiPM model

1) Peak V/I signal goes with $C^{-1}$

2) Peak I signal goes with $R^{-1}$ increasing with $R_q$ and $1/R_{load}$ (and $C_q$ of course)

3) Fast vs slow component

Increasing $C_q/C_d$ or/and $R_q/R_{load}$

→ spike enhancement

→ better timing
II. SiPM model

- Front end electronics for SiPM is needed to:
  - Preamplify for SNR optimization
    - Even if “nominal” gain is in the order of $10^6$ only a fraction of the charge is used for fast read-out systems
    - The “effective” gain for a fast system can be between 2 and 10 times lower than the nominal gain

\[
V(t) \approx \frac{Q}{C_q + C_d} \left( \frac{C_q}{C_{tot}} e^{-\frac{t}{\tau_{fast}}} + \frac{R_{load}}{R_q} \frac{C_d}{C_q + C_d} e^{-\frac{t}{\tau_{slow}}} \right)
\]

- Pulse shape
  - Charge ratio: $Q_{fast} / Q_{slow}$
  - Peak height ratio: $V_{fast}^{max} / V_{slow}^{max}$
  - Increasing with $R_q$ and $1/R_{load}$ (and $C_q$ of course)
  - Increasing $C_q / C_d$ or $R_q / R_{load}$
  - Spike enhancement → better timing
I. Introduction
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III. FE circuits: Pole-Zero cancellation

- Pole-Zero (PZ) cancellation of the SiPM recovery long time constant ($\tau_{\text{slow}}$)
- The PZ shaping has an effect in the signal to noise ratio (SNR)
  - A SNR>5 is required for photopeak identification
  - Can be seen in 2 different ways:
    1) Attenuation of slow frequency components of the signal
    2) Increase of the input referred noise (ENC=Equivalent Noise Charge)

![Graph showing response to 50 um 6x6 mm^2 SiPM single cell pulse](image)

Simulation with a model obtained from 3x3 mm device
• Front end electronics for SiPM is needed to:
  
  – Low noise front end is required for large SiPMs
  
  SiPM capacitances range from 10s pF to more than several nF

**Equivalent Noise Charge**

- Series noise < 2 nV/sqrt(Hz)
- Parallel noise < 20 pA/sqrt(Hz)

ENC\text{max} for SNR>5 @ 2\times10^6 nominal gain

ENC\text{max} for SNR>5 @ 1\times10^6 nominal gain
III. FE circuits: current versus voltage mode

• Typical photo-sensor front end circuit configurations:

- Charge preamplifier
  - E.g. common-emitter/source configuration
  - Large $Z_{in}$ // Large $Z_{out}$
  - Current conversion with $R_{in}$
  - High power budget for high speed systems
  - But can exploit RF technologies

- Voltage preamplifier
  - E.g. (super) common-base/gate
  - Low $Z_{in}$ // Large $Z_{out}$
  - Current conversion with $R_{in}$
  - Potential stability issues
  - Best for high rate applications
  - Good power/BW trade-off

- Current preamplifier
  - E.g. common-emitter/source configuration
  - Large $Z_{in}$ // Large $Z_{out}$
  - Current conversion with $R_{in}$
  - High power budget for high speed systems
  - But can exploit RF technologies

III. FE circuits: NINO

- **NINO**: current mode, binary and quite generic
- Chip designed by CERN group for ALICE TOF RPCs but quite used for SiPM read-out
  - 8 channels amplifier and discriminator
  - Common grid current conveyor, high speed differential discriminator
  - High speed time measurement (10 ps),
  - \( P_d = 25 \text{ mW/ch}, \) Manufactured in IBM 0.25 um

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**Diagram:**

III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- Active summation to build large area detectors

- Why active summation?
  - Total noise for active and passive summation can be similar
  - But signal (peak) is much higher!
    - Provided that BW of summation is wide enough

7 x SIPM 6x6 mm$^2$ each
1 x PMT 18 mm diameter

*7x7mm$^2$ and some custom larger SiPMs exist

Series noise < 2 nV/sqrt(Hz)
Parallel noise < 20 pA/sqrt(Hz)

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III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- MUSIC: current mode, analog (binary) and designed for astroparticle (CTA) but multipurpose
  - Amplification / impedance adaptation
  - Pole zero cancellation
  - Summation
  - Discrimination

- Current mode input stage for SiPM anode readout
- Gain control
- Anode voltage control
- Sensor switch off

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III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- Possible to disable each input reducing overvoltage by 4V
- Double feedback loop
  - Low input impedance
  - Anode voltage control
- High bandwidth

Series noise < 2 nV/\sqrt{\text{Hz}}
Parallel noise < 20 pA/\sqrt{\text{Hz}}
III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- MUSIC 8 ch ASIC integrates all those functionalities

Individual channel amplification with adjustable pole-zero cancellation (analog)
III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- Output for a LCT4 MPPC (3x3 mm²)

No Pole Zero
FWHM = 100 ns

Pole Zero
FWHM ≈ 6 ns
III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- Charge spectrum for a LCT4 MPPC (3x3 mm²)
- Pole-zero cancellation
- Excellent resolution with FWHM of 5 ns
**III. FE circuits: MUSIC: Multipurpose SiPM RO chip**

- **MUSIC 8 ch ASIC integrates all those functionalities**

**Summation of 1 to 8 channels with double gain (high dynamic range) and tunable pole-zero cancellation**

- CURRENT mode input stage for SiPM anode readout
- Gain control
- Anode voltage control
- Sensor switch off

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III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- MUSIC configuration: the adder takes only 1 channel
  - Pole-zero cancellation: trade-off between resolution and speed
  - High transimpedance gain (MUSIC)

**S13360-6050 SiPM**
- 6x6 mm², 50 um cell
- 1.2 nF capacitance
- 7 V overvoltage

![Charge vs Counts](image)

Qc calculation for V = 59.0

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III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- MUSIC configuration: the adder takes 7 channels
  - Noise is much higher (sqrt(7))
  - But pe (cell) peaks can still be identified
  - Channels have been equalized by MUSIC anode ctrl voltage

\[
\text{S13360-6050 SiPM} \\
\text{6x6 mm}^2, \text{50 um cell} \\
\text{1.2 nF capacitance} \\
\text{7 V overvoltage}
\]

\[
\text{1 x PMT} \\
\text{18 mm diameter} \\
\approx \text{7 x SIPM} \\
\text{6x6 mm}^2 \text{ each}
\]
I. Introduction
II. SiPM model
III. FE circuits
**IV. ASICs for PET**
V. Avenues to fast timing
IV. ASICs for PET: PETIROC

- **PETIROC2:**
  - Voltage mode,
  - Configurable: analogue, binary or digital
    - S&H + Wilkinson ADC
  - For medical imaging (PET)
  - Versatile: analog or digital
  - But shaping time > 10 ns
  - Max ev. rate is 40 KHz in digital mode
  - Power:

https://www.weeroc.com/fr/products/petiroc-2a

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**Detector Read-Out:** SiPM, SiPM array

**Number of Channels:** 32

**Signal Polarity:** Positive or Negative

**Sensitivity:** Trigger on first photo-electron

**Timing Resolution:** ~ 35 ps FWHM in analogue mode (2pe injected) - ~ 100 ps FWHM with internal TDC

**Dynamic Range:** 3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2500 ph-e

**Packaging & Dimension:** TQFP208 – TFBGA353
IV. ASICs for PET: TOFPET

- **TOFPET2**: current mode, digital (linear ToT) and for medical imaging (PET)
  - Power: 8 mW/ch
  - Max rate 200 KHz/ch

- Pre-amplifier: low input impedance current conveyor
- Two post-amplifiers (TIA) for time and energy measurements
- Three leading edge discriminators;
  - Very low threshold (1-5 p.e.) for optimum PET time resolution
  - Multi-level event rejection

- **Time to Amplitude Converter (TAC)**
- **Charge Integrator (CI)**
  - Configurable integration windows
  - Linear amplitude measurement
  - TAC and Charge Integrator are quad-buffered
    - No dead-time due to Poisson fluctuations

- Two 10-bit ADCs per channel
  - Time and amplitude measurements
  - Optionally: Time-over-Threshold

J. Varela, “New results with TOFPET2”, FAST, Ljubljana, Jan 2018
IV. ASICs for PET: STiC

- STiC: current mode, digital (linear ToT) and for medical imaging (PET)

Features:

- STiC 2.1: 16 channels
- STiC 3.0: 64 channels

- Differential and single-ended readout ...
- Integrated TDC [ZITI, Fischer et al.] and digital data processing ...
- Timing and ToT-based linearized energy measurement ...
  [SPTR: 180 ps; MPPC S10362-11-100]
- SiPM bias tuning ...
  [Tuning range: ~ 500 mV]
- Serial interface for data transmission and configuration ...

STiC — a mixed mode silicon photomultiplier readout ASIC for time-of-flight applications
T. Harion et alt., 2014 JINST 9 C02003
IV. ASICs for PET: FlexToT: linearized ToT RO chip

- Joint project with CIEMAT to develop a time-over-threshold ASIC for SiPM based PET
  - ICCUB: expertise on electronics and microelectronics design for detector FE
  - CIEMAT: expertise on PET and medical imaging instrumentation

**FlexToT**
- 16 channel
- SiGe BiCMOS 0.35um
- Aaustriamicrosystem
- 10 mm²
- 3.3 V (10 mW/ch)
- QFN 64
IV. ASICs for PET: FlexToT: linearized ToT RO chip

- A Flexible ASIC for SiPM RO (PET, SPECT, Compton)
  - Novel current mode input stage
  - Time resolution for ToF
  - Time over Threshold RO
    - No ADC
IV. ASICs for PET: FlexToT: linearized ToT RO chip

- **Good linearity and uniformity**
  - With only comparator threshold offset equalization
- **Different operating ranges can be covered**
IV. ASICs for PET: FlexToT: linearized ToT RO chip

• Measured @ CERN:
  – Single Photon Time resolution (SPTR)
  – Coincidence Time Resolution (CTR)
  – Supported by FAST COST ACTION
    ▪ Many thanks to E. Auffray and S. Gundacker
  – Similar results as for NINO but 3 times lower power consumption

SPTR=90ps

Jitter floor: 7 ps rms
IV. ASICs for PET: FlexToT: linearized ToT RO chip

- Pisa University has developed a FPGA based TDC readout for FlexToT
  - Based on Arria 10 FPGA
    - TDC: 38 ps resolution
  - System CTR: 116 ps FWHM!
  - Energy resolution: 8 % FWHM @ 511 KeV
  - Dead time < 5ns: event rate > 1 MHz!
IV. ASICs for PET: HRFlexToT: linearized ToT RO chip

- A new version of the FlexToT has been recently developed.
  - A linear Time over Threshold with higher resolution (>8bits)
  - Lower power consumption (about 3.5 mW/ch)
  - Different trigger levels and cluster trigger for monolithic crystals.
  - Different scintillator time constants.

HRFlexToT
180 nm CMOS

Characterization during Q1 2018

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IV. ASICs for PET: HRFlexToT: linearized ToT RO chip

- Preliminary results
Outlook

I. Introduction
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V. Avenues to fast timing
V. Avenues for fast timing

• Disclaimer: I will not talk about “digital SiPMs”
• In the analog domain the FE circuit seems not to be the limitation for large area SiPMs (> 2x2 mm\(^2\))
  – Best FE chips (PETIROC2A, TOFPET2, STIC, FlexToT and HRFlexToT) show similar results
    ▪ SPTR for small SiPMs (1x1 mm\(^2\)): 40 ps sigma / 100 ps FWHM
    ▪ SPTR for large SiPMs (3x3 mm\(^2\)): 85 ps sigma / 200 ps FWHM
    ▪ CTR for small crystals (2x2x3 mm) around 100 ps FWHM
    ▪ CTR for large (realistic) crystals (2x2x20 mm) around 200 ps FWHM

• These are results for pure analog chip/mode
  – Degradation when using on-chip TDCs
    ▪ Limited resolution of the TDCs (>30 ps) due to power constraints
    ▪ Noise coupled to the sensitive analog FEs
V. Avenues for fast timing

- These results are for the best SiPMs
  - Some dependence on the SiPMs
  - But general conclusion remains…

Single photon time resolution of state of the art SiPMs
JINST, published: October 21, 2016
M.V. Nemallapudi, S. Gundacker, P. Lecoq and E. Auffray
doi:10.1088/1748-0221/11/10/P10016
V. Avenues for fast timing

• In order to improve CTR we need to progress in
  – Crystals: prompt light emission
  – Sensors: SPTR
    ▪ In the the limit, the single SPAD SPTR: 20 ps FWHM?

• A cost/power effective mixed-mode approach:
  – Use small SiPMs
    ▪ Better SPTR
  – Low power input stage
    ▪ Demonstrated with HRFlexToT chip
  – Fast analog summation
    ▪ Demonstrated with MUSIC chip
  – Multi threshold comparators
    ▪ Provides estimation of the time of arrival of several photons
  – High performance TDCs and synchronization
    ▪ < 10 ps timing resolution demonstrated in 130 nm technology
V. Avenues for fast timing

- New ASIC in 65 nm being developed by ICCUB and CERN (FastIC)
  - Fast (2 GHz) and low power (< 1mW/input) summation
  - Compatible with picoTDC (3 ps time resolution)
Thanks a lot for your attention !!!

Questions ?

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Barcelona Techno Week

Barcelona Techno weeks are a series of meeting point events around a technological topic of interest for both academia and industry. They include comprehensive multidisciplinary keynote presentations by world experts that are combined with networking activities to foster collaboration among participants.
III. FE circuits: NINO

• NINO: current mode, binary and quite generic
• Binary: usually connected to TDC for Time-Over-Threshold (ToT) energy
  – Simple discriminator: ToT is not linear
• Differential connection to the SiPM

III. FE circuits: NINO

- Classical ToT is non-linear

- It has an impact on energy resolution
  - Calibration is possible
  - But not perfect…

E. Orita, NIMA 648, S24-27, 2011

Graphs showing non-linear and linear ToT.
III. FE circuits: CITIROC

- CITIROC: voltage mode, analogue and for CTA SSTs ASTRI camera
- Part of Omega/Weeroc family: CITIROC, PETIROC, PETIROC2, TRIROC, etc

- General ASIC
  - 32 channel, charge and trigger outputting
  - 6.26mW/Ch. Power pulsed

- Front-end
  - Trigger
    - Fast shaper connected to either low or high gain preamp
  - Two discriminator: one for timing, one for event validation on energy

- Energy measurement
  - 2 voltage preamplifier (10x gain difference) followed by shaper
  - Analogue memory: track and hold or peak detector
  - Analogue multiplexer
  - **Peaking time between 12.5 and 100 ns**
  - **Valid only for SSTs**

https://www.weeroc.com/fr/products/citiroc-1a
III. FE circuits: MUSIC: Multipurpose SiPM RO chip

**MUSIC 8 ch ASIC integrates all those functionalities**

- Individual channel amplification with adjustable pole-zero cancellation (discriminated)
- Current mode input stage for SiPM anode readout
  - Gain control
  - Anode voltage control
  - Sensor switch off

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III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- Output for a LCT4 HPKK MPPC (3x3 mm²)
  - Picosecond laser
  - Pole-zero cancellation
  - Single Photon Time Resolution about 100 ps (@ 5V OV)

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III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- SHIP experiment is a new general-purpose beam dump facility at the SPS (CERN) to search for hidden particles
  - Predicted by a very large number of recently elaborated models of Hidden
  - Dark matter, neutrino oscillations, and the origin of the full baryon asymmetry

- Reconstruction of the HNL decays in the final states: $\mu^-\pi^+$, $\mu^-\rho^+$ & $e^-\pi^+$

  Requires long decay volume, magnetic spectrometer, muon detector and electromagnetic calorimeter, preferably in surface building

- Long vacuum vessel, 5 m diameter, 50 m length
  Background from active neutrino interactions becomes negligible at 0.01 mbar

- 10 m long magnetic spectrometer with 0.5 Tm dipole magnet and 4 low material tracking chambers
III. FE circuits: MUSIC: Multipurpose SiPM RO chip

Timing Detector in SHiP

- For the TD of size 5 m x 10 m with a bar
  100 cm x 6 cm x 1 cm
  - 5 col x 182 row = 910 bars =>
  - 910 bars x 2 = 1820 ch =>
  - 1820 x 8 = 14560 SiPMs

- The resolution at 50 cm is ~140 ps => we can use with 1 m bar and 2-side readout to be within 100 ps.
III. FE circuits: MUSIC: Multipurpose SiPM RO chip

Bar and sensors for ToF/ND280

- Bar: 230 cm x 6 cm x 1 cm
- Plastic material:
  - EJ200 (BC408) or EJ208(BC412)
  - Attenuation length ~4 m
  - 1.42 kg/bar
- Readout from both ends
  - 8 sensors of 6 mm x 6 mm
  - Example: S13360-6050PE
III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- Timing sub-detector test beam with MUSIC chip
  - By Univ. Geneva & Univ. Zurich
  - MUSIC in summation mode (8 6x6 mm² SiPMs)
    - Bar read-out at both ends
  - 2.5 GeV/c muon beam at the CERN PS
  - Readout with Wavecatcher
    - Fast analog memory (LAL & IRFU/CEA)

- Measurements with the 150 cm x 6 cm x 1 cm bar.
- Time resolution as measured by the SiPM arrays at both ends of the bar as a function of the interaction point along the bar.

© A. Kornezev (Univ. Geneva)
III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- Studying the possibility to develop a beam loss monitoring system based on scintillating fibers
  - Collaboration with Alba synchrotron General idea:
  - Fiber along the beam pipe or in selected regions
  - Losses are detected by a rate increase
  - With timing information, additional position information
    - Preliminary results: 20 cm resolution for a 2 m fiber of 1 mm diameter

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Thanks to C. Joram (CERN) for providing SciFibers
IV. ASICs for PET: FlexToT: linearized ToT RO chip

- **Spectroscopy with linear ToT**

![Image of a circuit board with a chip]

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**Sources spectra**

- Na
- Na$_{ht}$
- Cs
- Cs$_{ht}$
- Cd
- Co$_{ht}$

**Repetitions**

![Graph showing spectroscopy data with labeled peaks for Na, Cs, and Co isotopes]
I. Introduction
II. SiPM model
III. FE circuits
IV. Digitization
V. System-On-Chip (SoC)
VI. Emerging technologies
III. Digitization: basic options

1) “Classical” signal processing chain
   - Requires complex analogue processing
   - Not so flexible
   - Optimal in power for specific app.

2) Digital signal processing
   - Waveform sampling and digital signal processing
   - Ideally one should sample at $f_s > 2 \times$ signal BW (x5)

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III. Digitization: waveform sampling

- Very demanding sampling specs for IACTs
  - Dynamic range of about 12 bits (with several gains)
  - Analog BW > 300 MHz requires 1-2 GS/s
    - Power consumption and ADC cost!
    - Alternative: FlashCAM digitizes at much lower speed and tries to extract signal parameters by signal processing
      - But NSB will be there anyway, so energy threshold will be degraded...

- Many projects have been using Switch Capacitor Arrays (SCAs) to perform analog sampling

III. Digitization: waveform sampling

- SCAs sample the signal which is digitized at a lower speed

**Switched Capacitor Array (Analog Memory)**

- Inverter “Domino” ring chain
- Clock
- Shift Register
- Waveform stored
- 0.2-2 ns
- 10-100 mW
- FADC 33 MHz
- “Time stretcher”
  GHz → MHz

S. Ritt
III. Digitization: waveform sampling

G. Varner, Univ. Hawaii

TARGET
CTA SCT and SST
Many chips for different projects
Buffered and unbuffered
Very deep arrays
ADC on chip.
Philosophy => pushing the limit of the SCA technology

Straw3  Labrador  Labrador3  Target  BLAB family

H. Frisch et al., Univ. Chicago

Goal: reach a 1ps precision!
Pioneering R&D work
130nm IBM
18 GSPS, 256 samples, 6ch
ADC on chip

Initiator of a networking activity on SCAs and ps-timing

S. Ritt, R. Dinapoli, PSI

Universal chip for many applications
8 + 1 channels 1024 cells
5GSPS, 950 MHz BW
Low power consumption
Short readout time
Several possible modes of operation

DRS1  DRS2  DRS3  DRS4

NECTAr
CTA MST
NECTArCAM

D. Breton, IN2P3/LAL
E. Delagnes, CEA/Saclay

More than 120,000 SCAs operating worldwide
Buffered (f_{3dB} 400-500MHz) 3.2GSPS
High dynamic range
Robust (minimum calibration or ext. control)
Conservative technologies
Moderate depth 256-1024 cells/2ch
On-chip ADC in the last chip

NECTArCAM


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III. Digitization: waveform sampling

**SAMPIC Waveform TDC**

- **One Common 12-bit Gray Counter** (FClk up to 160MHz) for Coarse Timestamping
- **One Common servo-controlled DLL** (from 1.6 to 10.2 GHz) used for medium precision timing & analog sampling
  - 16 independent WTDC channels each with:
    - 1 discriminator for self triggering
    - Registers to store the timestamps
    - 64-cell deep SCA analog memory
    - One 11-bit ADC/ cell
      (Total: 64 x 16 = 1024 on-chip ADCs)
- **One common 1.3 GHz oscillator + counter used as timebase for all the Wilkinson A to D converters.**

Global time = counter (~10ns) + DLL (~100ps) + waveform (~ps)

Waveform is available for extraction of other parameters (Q, A)

D. Breton, 4th FAST WG3/4/5 Meeting, Ljubljana, January 7/8 2018
III. Digitization: waveform sampling

SAMPI_C V1 PERFORMANCES

- Power consumption: **10 mW/channel**
- 3dB bandwidth > **1 GHz**
- Discriminator noise ~ **2 mV rms**
- Counting rate > **2 Mevts/s** (full chip, full waveform), up to > **10 Mevts/s** with Region Of Interest (ROI)

- Wilkinson ADC works with internal **1.3 GHz** clock
  - Dynamic range of **1V**
  - Gain dispersion between cells ~ **1% rms**
  - Non linearity < **1.4 %** peak to peak
  - After correction of each cell (linear fit):
    - noise = **0.95 mV rms**

- Time Difference Resolution (TDR):
  - Raw non-gaussian sampling time distribution due to DLL non-uniformities (TINL)
  - Easily calibrated & corrected (with our sinewave crossing segments method [D. Breton & al, TWEPP 2009, p149])

D. Breton, 4th FAST WG3/4/5 Meeting, Ljubljana, January 7/8 2018
III. Digitization: waveform sampling

- CHEC camera is an interesting example of compact readout

CTA Application for TARGET

2,048 readout channels/camera

CHEC design for CTA

III. Digitization: waveform sampling

- Several iterations to have a functional chip: TARGET7

Outlook

I. Introduction
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V. System-On-Chip (SoC)
VI. Emerging technologies
IV. ASICs for PET: PETA

- PETA: current mode, charge (ADC) and time (TDC), for PET
  - Choice between Differential FE (both polarities, MRT immune) and Single Ended FE (low Zin, DC bias adjustment, no external coupling parts)
  - Readout rates >200 kHz per channel (in all channels)
  - Power consumption ~30mW / channel

P. Fischer, Heidelberg University, The PETA Chip Family FAST Workshop, FBK 2016
IV. ASICs for PET: BASIC64

- BASIC64: current mode, digital (peak detector + ADC) and for PET
  - Power: 10 mW/ch
  - Max rate: 75 KHz/ch
  - No TDC for timing

C. Marzocca et al., "BASIC64: A new mixed-signal front-end ASIC for SiPM detectors," NSS 2016
IV. ASICs for PET: PACIFIC

- PACIFIC: A 64 ch ASIC for Scintillating Fiber Tracking in LHCb Upgrade

  Collaboration: ICCUB, Heidelberg, LPC-Clermont, IFIC-Valencia

- Similar input current conveyor as in FlexToT
- Current conveyor with very low impedance input (≈ 30Ω)
  - Adjustable gain / dynamic range
  - Input voltage adjustment
- Fast tunable shaper
  - Pole-zero cancellation to cancel slow SIPM time constant
  - A FWHM of 5 ns is achieved for single-cell signal
- Dual interleaved 25ns gated integrator
  - Almost no dead time
  - Average photo-statistical fluctuations
  - Maximize charge collection (25 ns integration)
- 2 bits 40MS/s flash non-linear ADC
- Power consumption < 8mW/channel @ 1.2 V

130 nm CMOS technology
IV. ASICs for PET: FlexToT: linearized ToT RO chip

- Why FlexToT is flexible?
  - Different scintillator time constants
  - Trading-off resolution versus rate
  - Accurate analog processing directly connected to FPGA
    - TDCs and signal processing are in FPGA: reconfigurable!
IV. ASICs for PET: FlexToT: linearized ToT RO chip

- No linear ToT may degrade resolution
- Linear ToT is possible
  - Used in Medipix, Timepix, Dosepix ASICs family
  - Also proposed for PET
  - Tuneable feedback current (IFB)
    - Rate vs resolution

\[
T_{ToT} = \frac{Q}{I_{FB}} - \frac{V_{th}C_{FB}}{I_{FB}} - (I_{FB}/C_{FB}) \cdot t
\]

- Orita, NIMA 648, S24-27, 2011
IV. ASICs for PET: HRFlexToT: linearized ToT RO chip

- Preliminary results

![Graph showing input signal, shaper output, timing-OR, and channel output time](image)

Input signal
Shaper Output
Timing-OR
Ch Out: time
IV. ASICs for PET: HRFlexToT: linearized ToT RO chip

- Preliminary results

![Graph showing input signal, shaper output, timing-OR, and channel output: energy.](image)
IV. ASICs for PET: HRFlexToT: linearized ToT RO chip

- Preliminary results

![Graph showing input signal, shaper output, timing-OR, and channel output.]

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