The ATLAS High-Granularity Timing Detector

Sabrina Sacerdoti
on behalf of the HGTD group

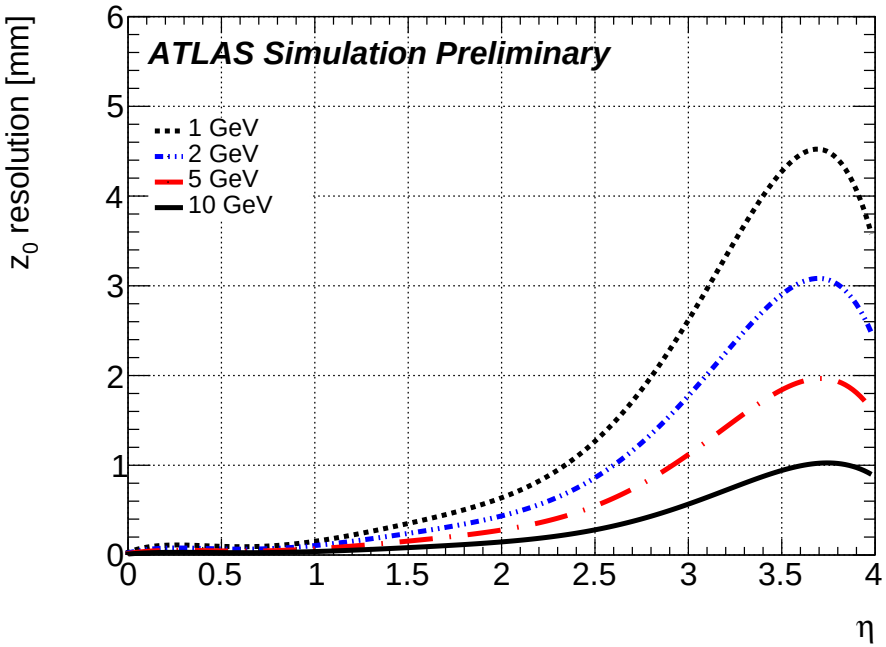
Laboratoire de l'Accelerateur Lineaire

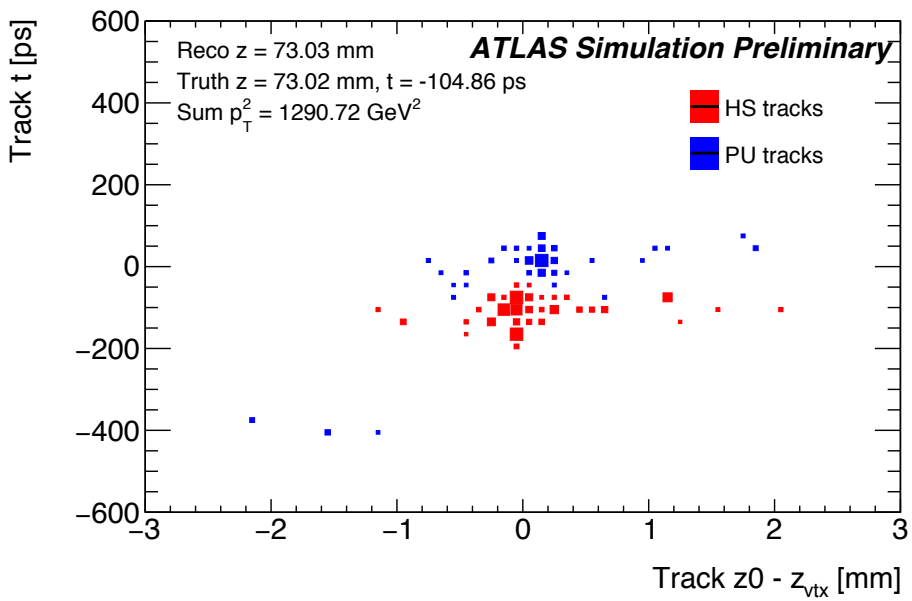
11th Workshop on Picosecond-timing Detectors
for Physics and Medical Applications
Torino, May 17th

Contents

Motivation

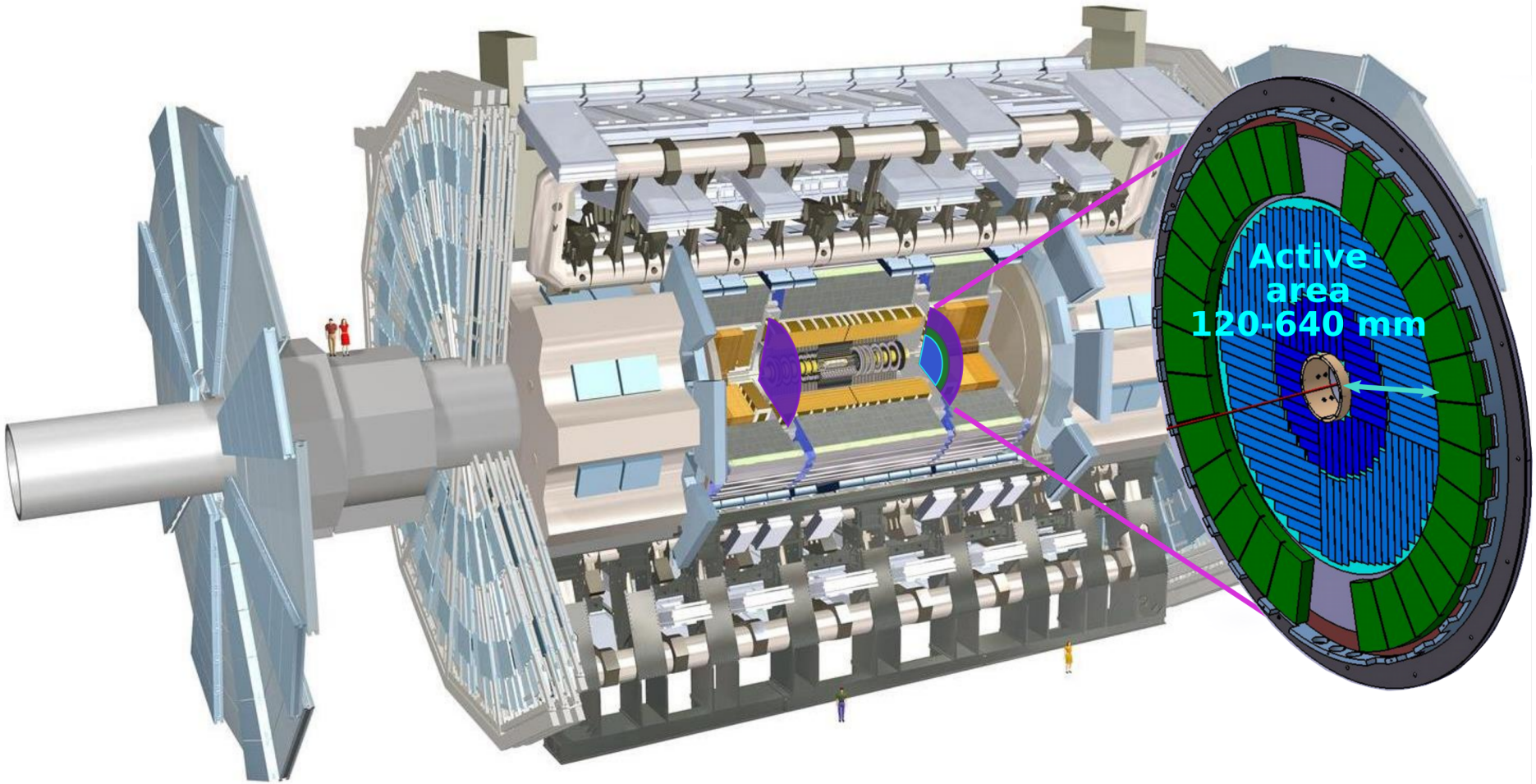
- Increased luminosity at the HL-LHC:
  - expected $\langle\mu\rangle = 200$
  - average interaction density $\sim$ 1.8 vtx/mm
- With the design z_0 resolution, several vertexes could be merged
- Adding an additional dimension (4D) to existing detectors can provide a new handle on increased interactions per mm





The High-Granularity Timing Detector

The HGTD will provide time measurements for objects in the forward regions of the ATLAS detector



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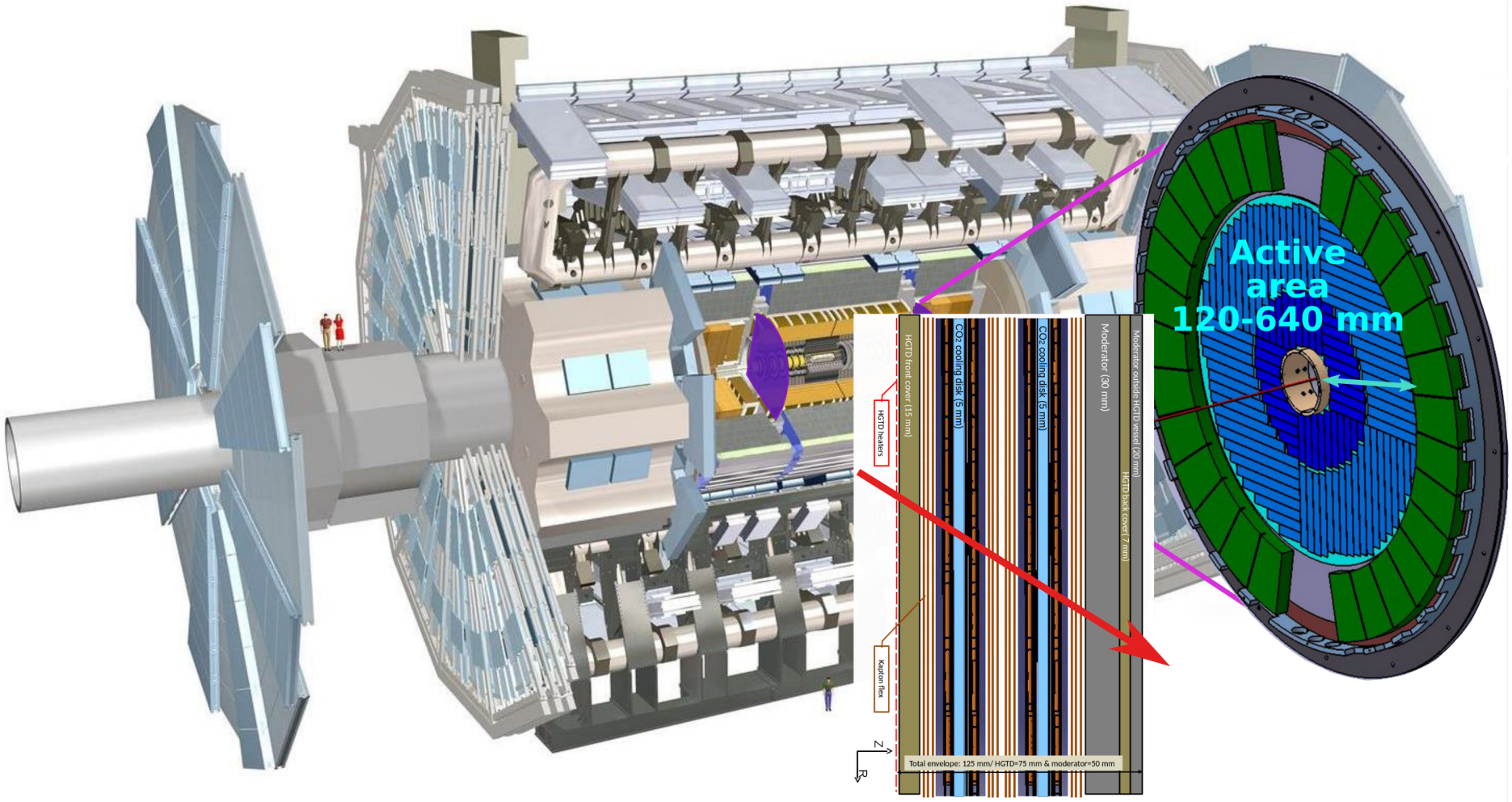

The HGTD: timing in ATLAS

General parameters:

- $2.4 < |\eta| < 4.0$
- Active area 6.3 m^2 (total)
- Design based on $1.3 \times 1.3\,\mathrm{mm}^2$ silicon pixels ($2 \times 2\,\mathrm{cm}^2$ sensors)
- Radiation hardness up to 4.5 10^{15} n_{eq}/cm^2 and 4.5 MGy
- Number of hits per track:
  - 2 in $2.4 < |\eta| < 3.1$
  - 3 in $3.1 < |\eta| < 4.0$

Goal:

- Provide minimum bias trigger
- Instantaneous and unbiased luminosity measurement
- Resolve close by vertices
  - small timing resolution ($\sim$few 10s of picoseconds).

Time Resolution

Contributions to the timing resolution:

$$\sigma_T^2 = \sigma_L^2 + \sigma_{TW}^2 + \sigma_{jitter}^2 + \sigma_{clock}^2$$

- σ_L Landau fluctuations in the deposited charge in the sensors

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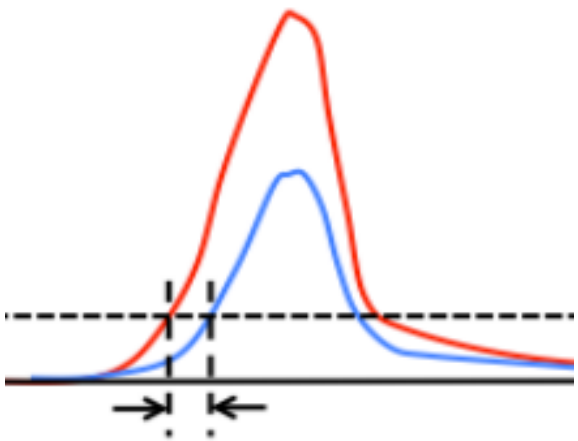
- $\sigma_{TW}^2 = [\frac{V_{th}}{S/t_{rise}}]_{RMS} \propto [\frac{N}{dV/dt}]_{RMS}$



- Variations due to differences in the amplitude of the signal.
- Expected to be negligible after applying an offline correction based on measuring the TOT.

Time Resolution

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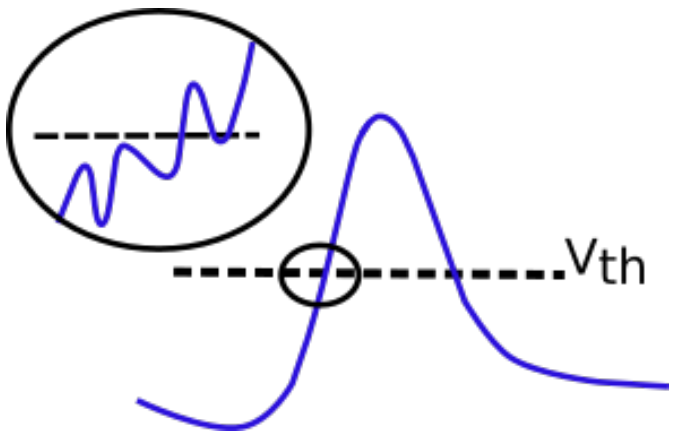
- $\sigma_{jitter}^2 = \frac{N}{dV/dt} \sim \frac{t_{rise}}{S/N}$



Variations due to noise in the signal

Time Resolution

Contributions to the timing resolution:

$$\sigma_T^2 = \sigma_L^2 + \sigma_{TW}^2 + \sigma_{jitter}^2 + \sigma_{clock}^2$$

- σ_L Landau fluctuations in the deposited charge in the sensors
- $\sigma_{TW}^2 = [\frac{V_{th}}{S/t_{rise}}]_{RMS} \propto [\frac{N}{dV/dt}]_{RMS}$
- $\sigma_{jitter}^2 = \frac{N}{dV/dt} \sim \frac{t_{rise}}{S/N}$
- σ_{clock}^2 contribution from the clock distribution
  - High Frequency: bunch to neighbouring bunch
  - Low frequency: drift (over periods of $\sim$ 1ms)
  - Expected to be below 10 ps

Time Resolution

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- σ_L Landau fluctuations in the deposited charge in the sensors
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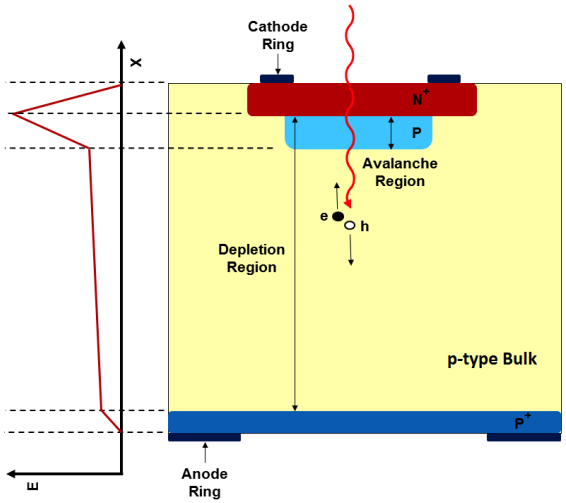
- $\sigma_{jitter}^2 = \frac{N}{dV/dt} \sim \frac{t_{rise}}{S/N}$
- σ_{clock}^2 contribution from the clock distribution < 10 ps

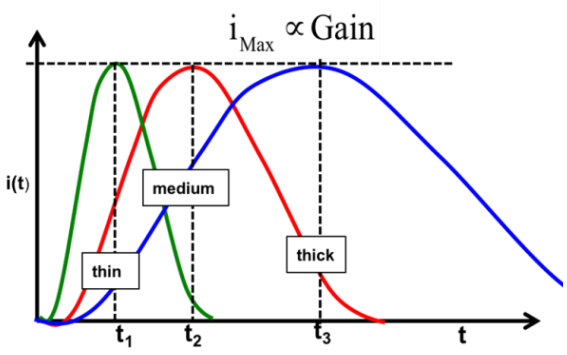
Additional contributions from TDC and t_0 calibration are expected to be negligible.

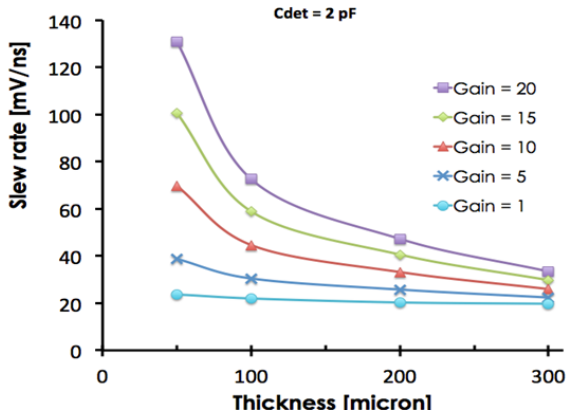
Low Gain Avalanche Diode

LGADs are n-on-p planar silicon detectors:

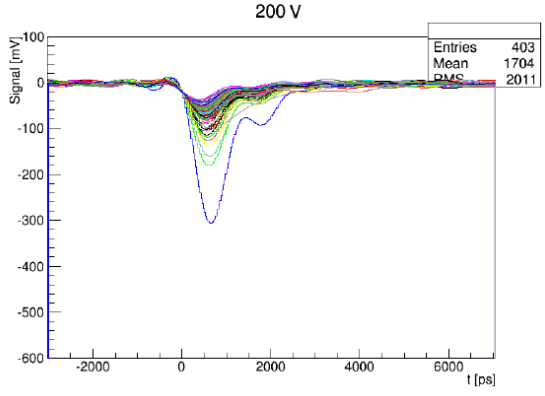
- low internal gain (lower noise amplification)
- radiation hardness
- excellent timing resolution







- Gain is independent of the thickness
- Thinner pads/larger gain give smaller rise times
- 50μm is baseline and 35μm under study
- Radiation damage can be controlled with cooling (-30 ℃)

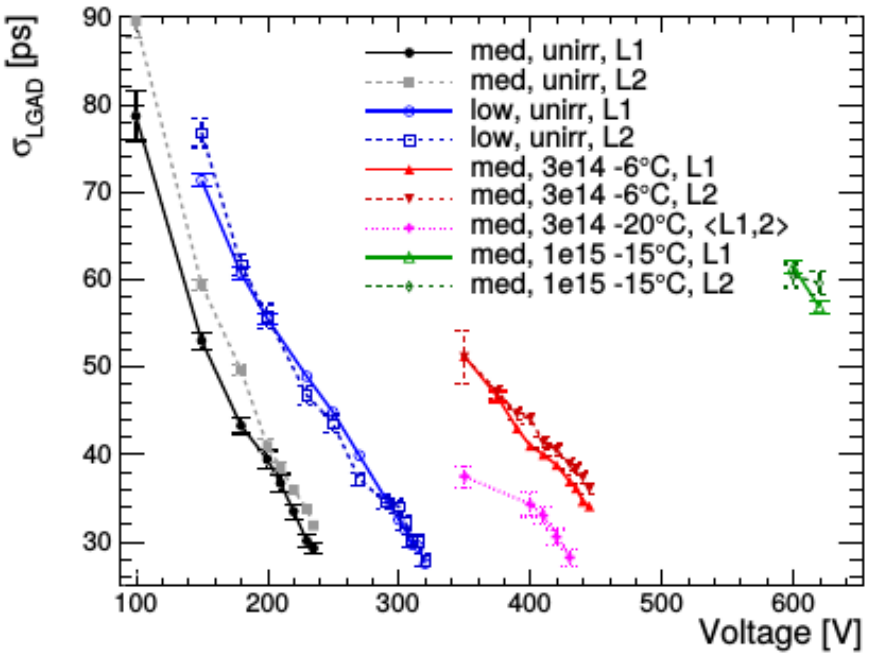


Overview of test beam results

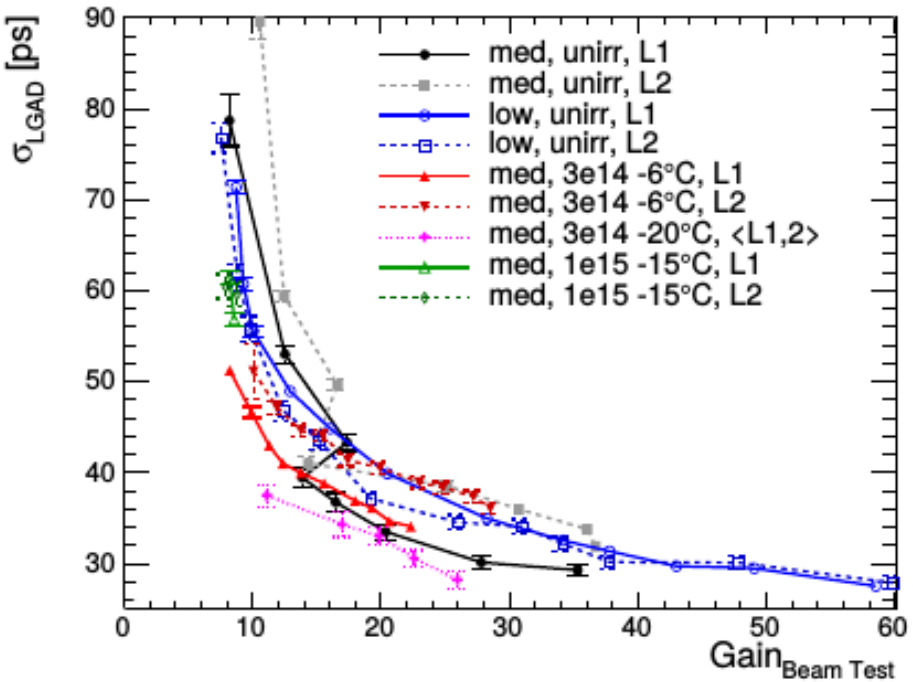
- Several test beam campaigns since 2016 (sensors from CNM and HPK).
- Achieved time resolution below 30 ps

CNM - 45 μm thick single pads[1]

σ_t vs V_{bias}



σ_t vs gain



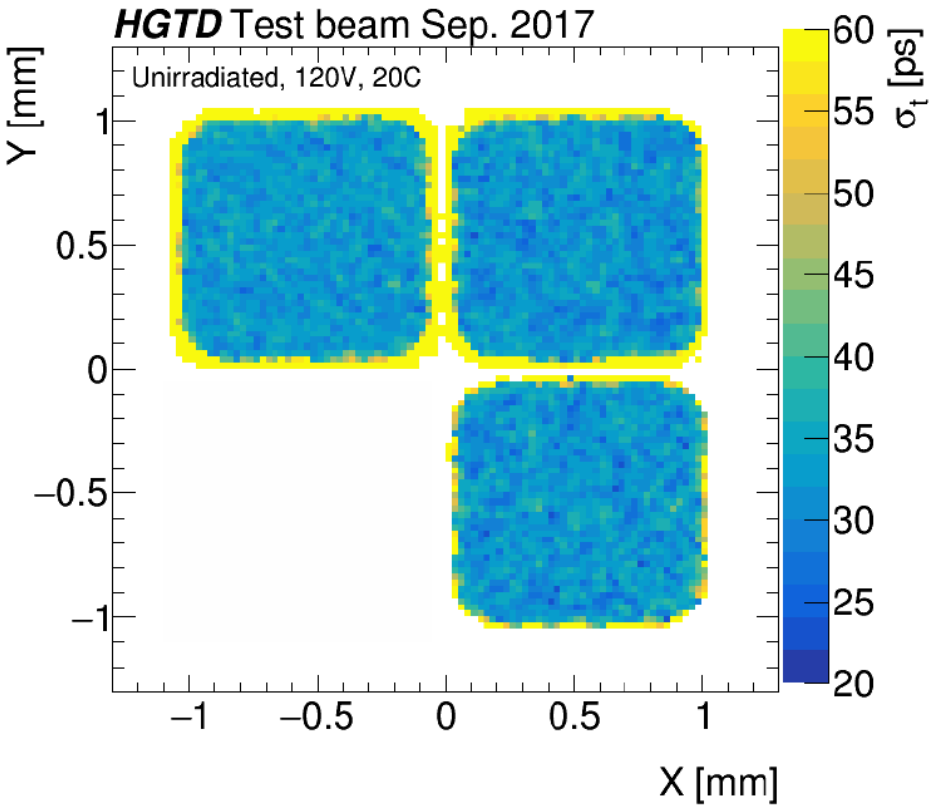
- Strong decrease of σ_t with V_{bias} ($\sigma_t < 30$ps at 235/320 V in non-irrad. sensors)
- Irradiated sensors tested at different temperatures.
- Decrease of σ_t with gain. Studies point to a safe gain of 10-20.

[1] results from J. Lange et al.; similar results in sensors from FBK

Overview of test beam results: time resolution

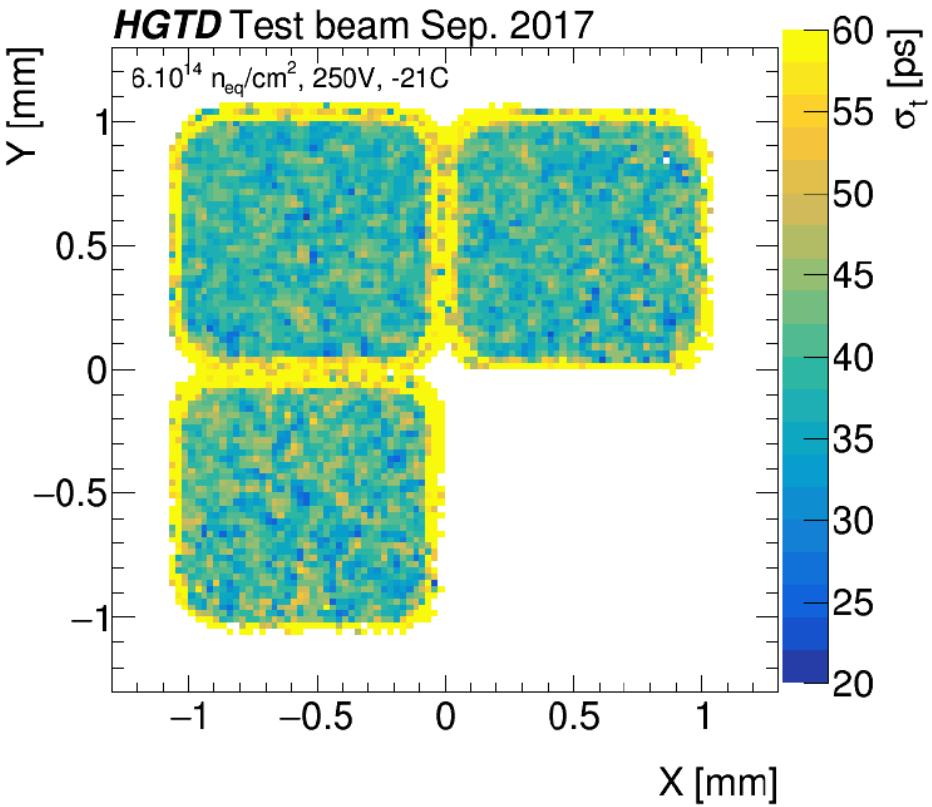
- September 2017 test beam with 120 GeV pions at CERN-SPS
- CNM 2×2 arrays, each pad $1.063 \times 1.063\,\mathrm{mm}^2$
- Test-beam 2016 paper available in in arxiv

Non-irradiated



Average $\sigma_t \sim 30$ ps

$6 \times 10^{14} \mathrm{n}_{eq}/\mathrm{cm}^2$

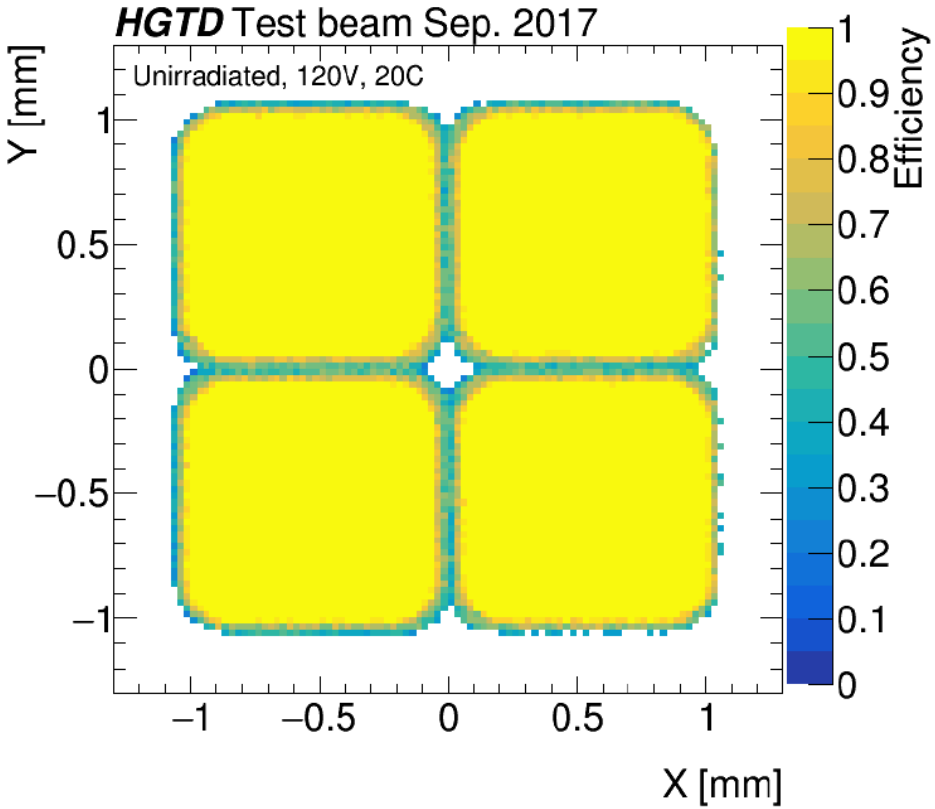


Average $\sigma_t \sim 40$ ps

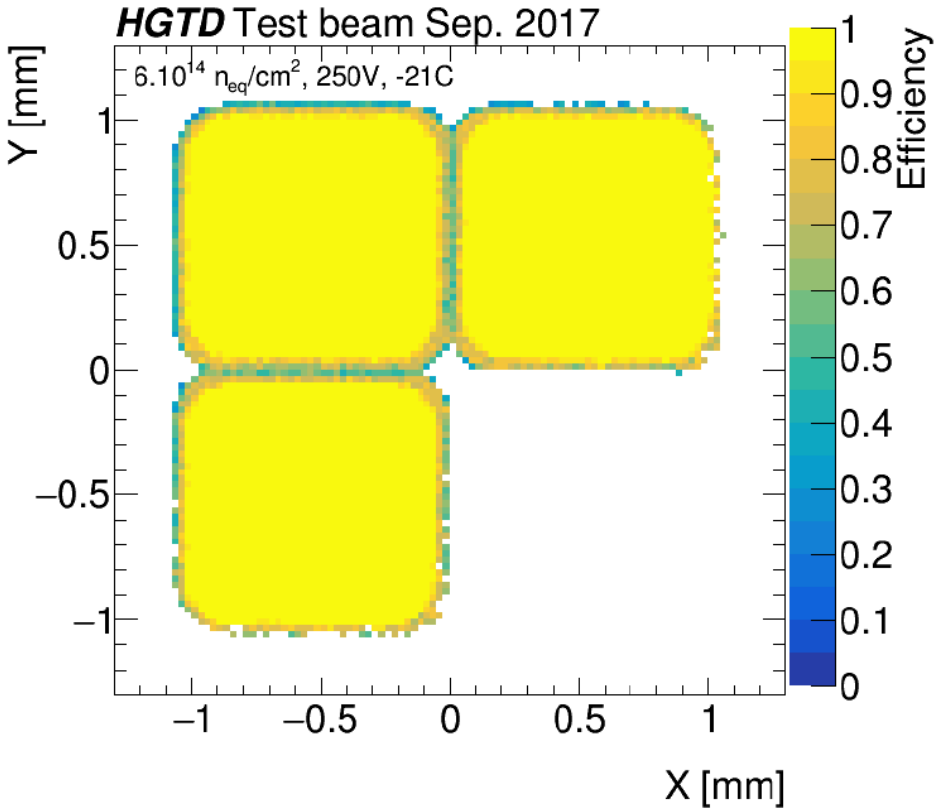
Overview of test beam results: efficiency

- CNM 2×2 arrays, each pad $1.063 \times 1.063\,\mathrm{mm}^2$
- September 2017 test beam with 120 GeV pions at CERN-SPS

Non-irradiated

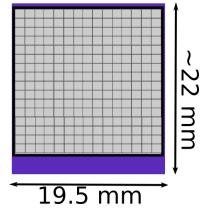


$6 \times 10^{14} \mathrm{n}_{eq}/\mathrm{cm}^2$

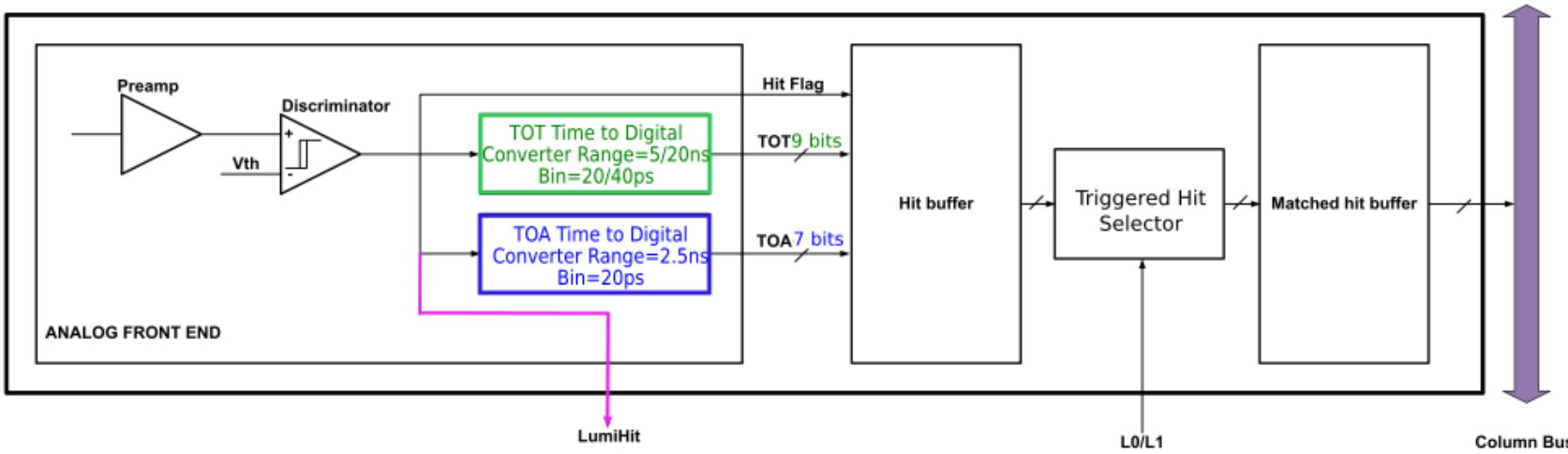


- Negligible inefficiency in the centre of the pads.
- Interpad area is not a dead region
- Also: cross-talk mostly negligible/$\sim$ 5% in irradiated sensors

ALTIROC ASIC

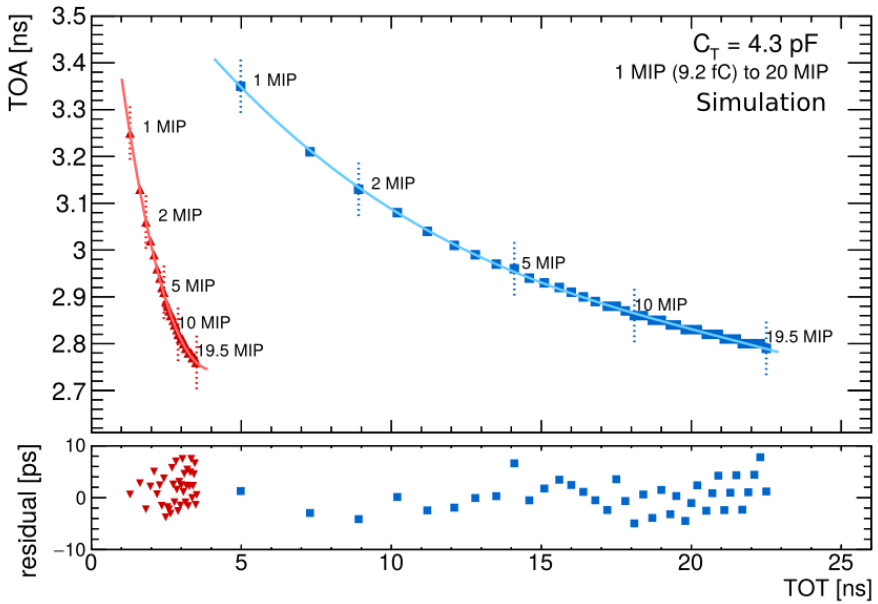


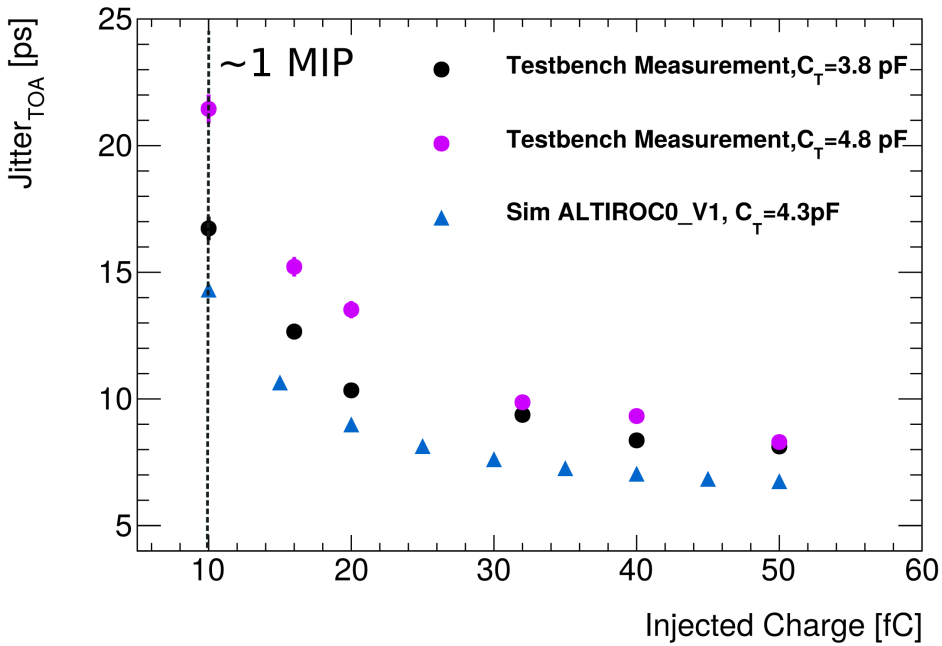
- HGTD design is to have sensors of 225 pixels ($1.3 \times 1.3\,\mathrm{mm}^2$)
- Will be read out by an ASIC, bump-bonded to the sensor
  - Should keep the excellent time resolution of the LGADs, $\sigma_{el} < 25$ ps
  - Power consumption constrained by cooling power (sensors at -30 ℃)
  - Current status:
    - ALTIROC0_v1: analog single pixel
    - ALTIROC0_v2: test bench studies are starting
    - layout of single channel readout is finished, post-layout simulations ongoing
    - off-pixel design is ongoing (mainly phase-shifter and luminosity data formatting unit)
    - will submit a 5×5 version (ALTIROC1) in June



Single channel: preamplifier + discriminator

- Rise time optimised to match drift time of sensor ($\sim 0.5 - 1$ns) to minimise jitter
- Voltage/VPA and transimpedance/TZ have been implemented in simulation
- TOT excursion of the TZ is much shorter, and jitter is higher
- Simulated/measured jitter in VPA below 15/25 ps for 1 MIP

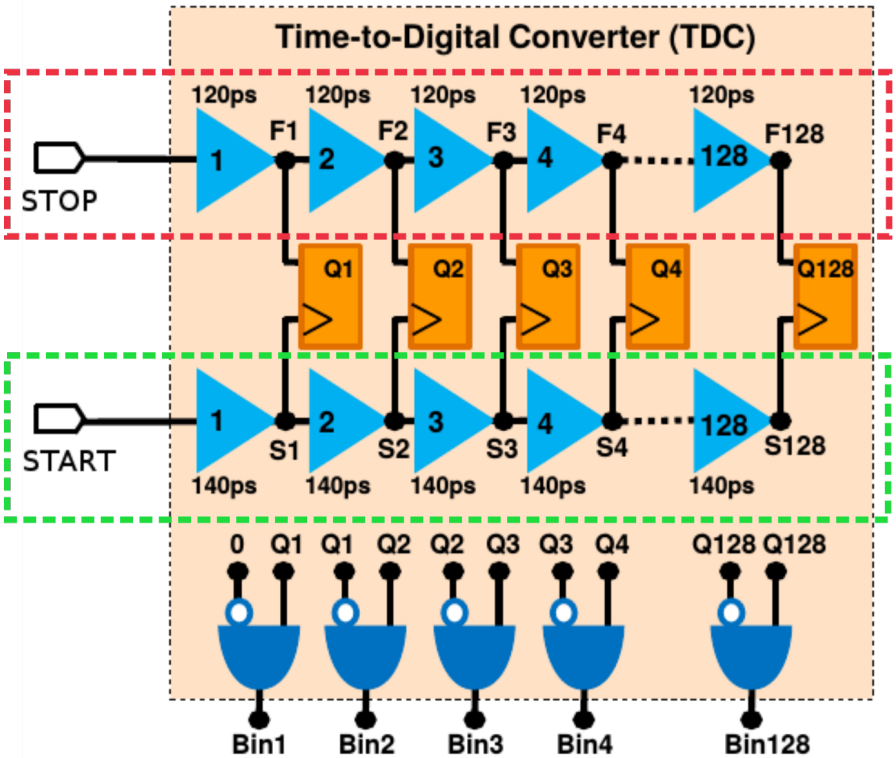


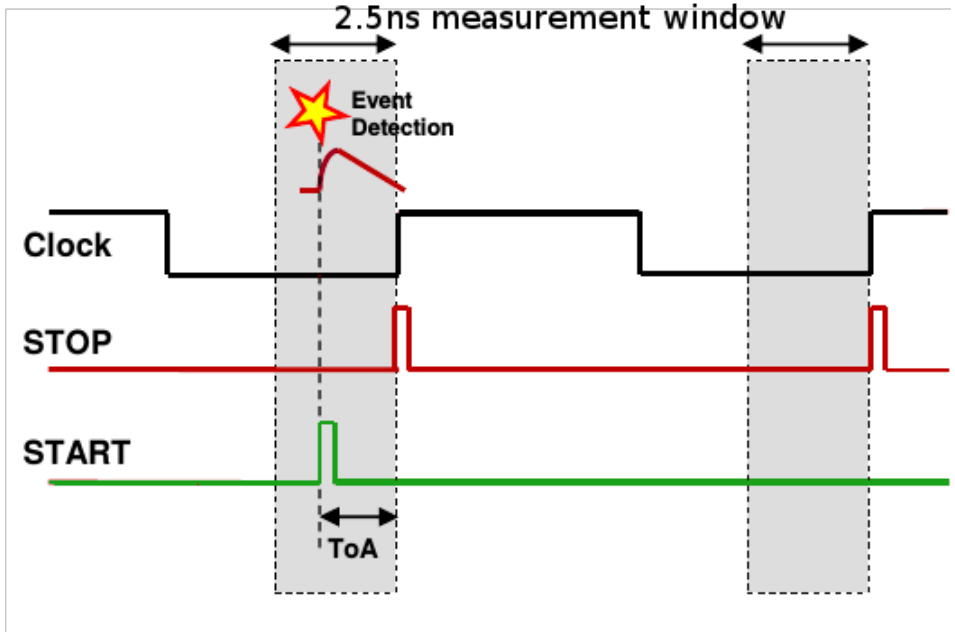


A fixed threshold discriminator will be used to measure the TOA.
Time walk will be corrected through the measurement of the TOT.

Single pixel TDC

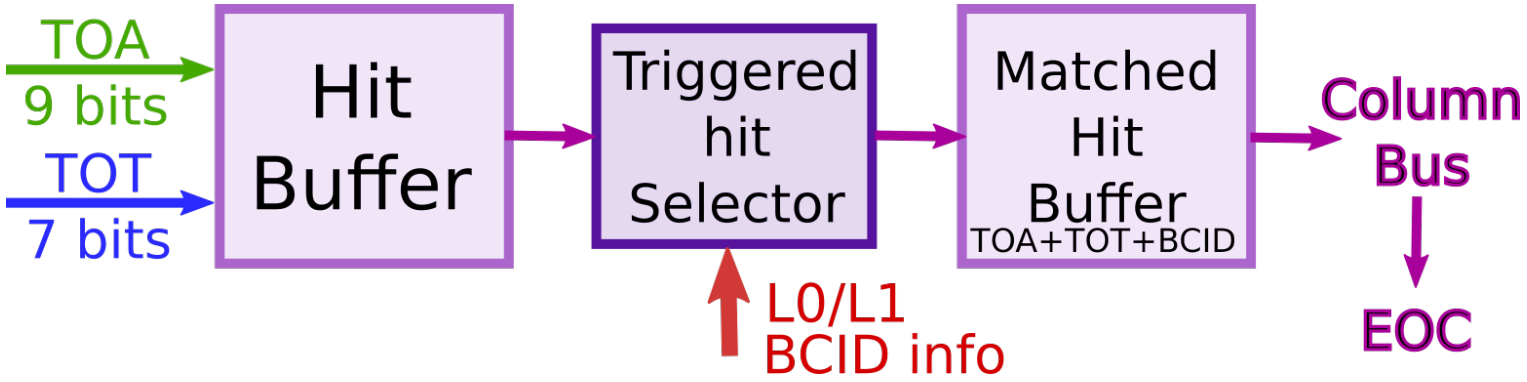
- Vernier delay line configuration with a reverse START-STOP scheme for power saving
- TOA-TDC: 2.5 ns range, 20 ps bin
- TOT-TDC: 5/20 ns range, 20/40 ps bin (TZ/VPA)
- Maximum conversion time of 25/28 ns for the TOA/TOT TDCs (preliminary sim.).





Single pixel memory

Temporarily store hit data and select hits associated to a trigger.

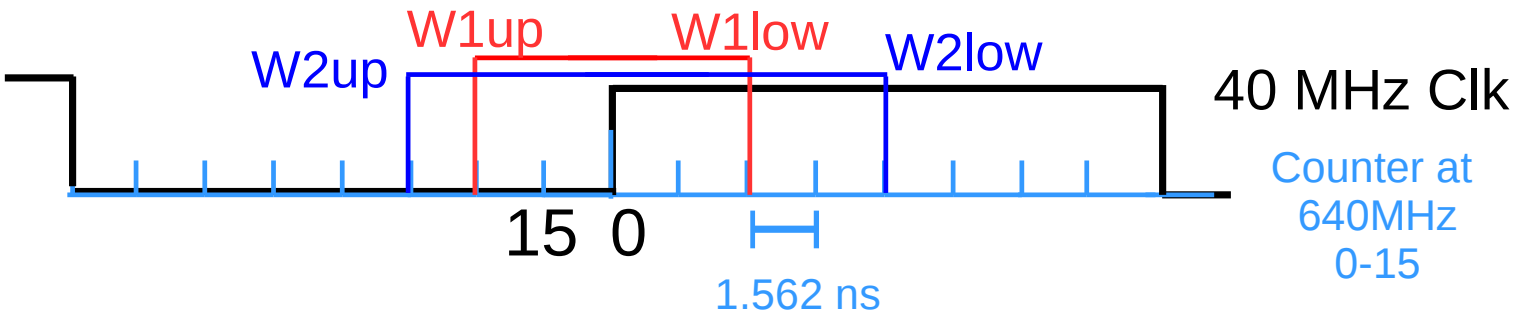


Baseline design is to use full buffering, storing TOA+TOT/hit flag:

- Handle 10/35μs latency for L0/L1 trigger
- 1 memory position per BC: 1400 $\times$ 17 bits depth
- Simulation of 400 $\times$ 17 SRAM, assuming 10% occupancy gives a power consumption of 57.2μW
- A 1400 depth memory would need to be split in several banks, yielding a power consumption 1.5/2 times larger

Off-pixel electronics - Luminosity

- $\mathcal{L}$ is linearly proportional to N_{hits}
- Non-linearities arise from:
  - double hits $\rightarrow$ low occupancy
  - background noise (*afterglow*)$\rightarrow$ compare N_{hits} in a smaller and wider time window around the BC



- Two time windows, W2>W1
- Rising and falling edges of both windows are tunable
- Transmit the sum of hits per ASIC for each BC
- Only for ASICs at $R > 320$ mm
- The sum over ASICs is computed in 64 regions and saved.

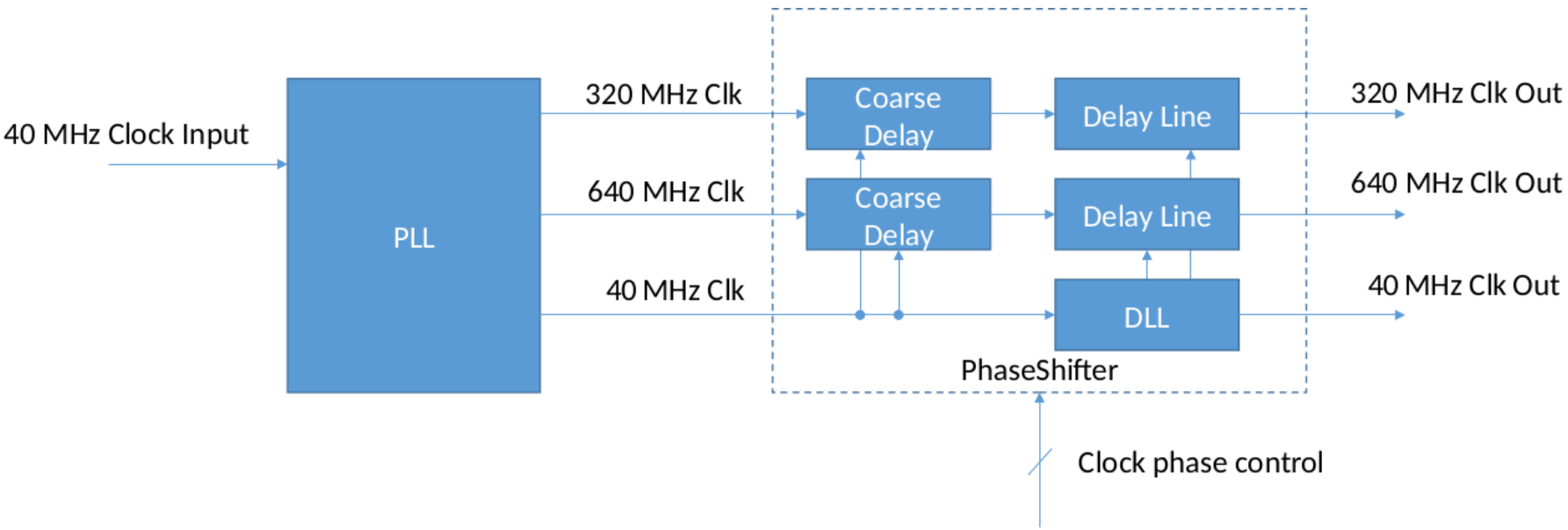
Off-pixel electronics - Phase shifter

The inner clocks of the ASIC have to be in phase, with an accuracy $\sim$ 100ps, in order to:

- ensure the correct time conversion of the TDC
- correctly adjust the time windows necessary to measure the luminosity

Characteristics:

- Receives clocks at 40, 320 and 640 MHz from the PLL
- Output phase adjusted to a step smaller than 100 ps
- Additional jitter below 5 ps
- Estimated power consumption around 10 mW
- Design is ongoing



Summary

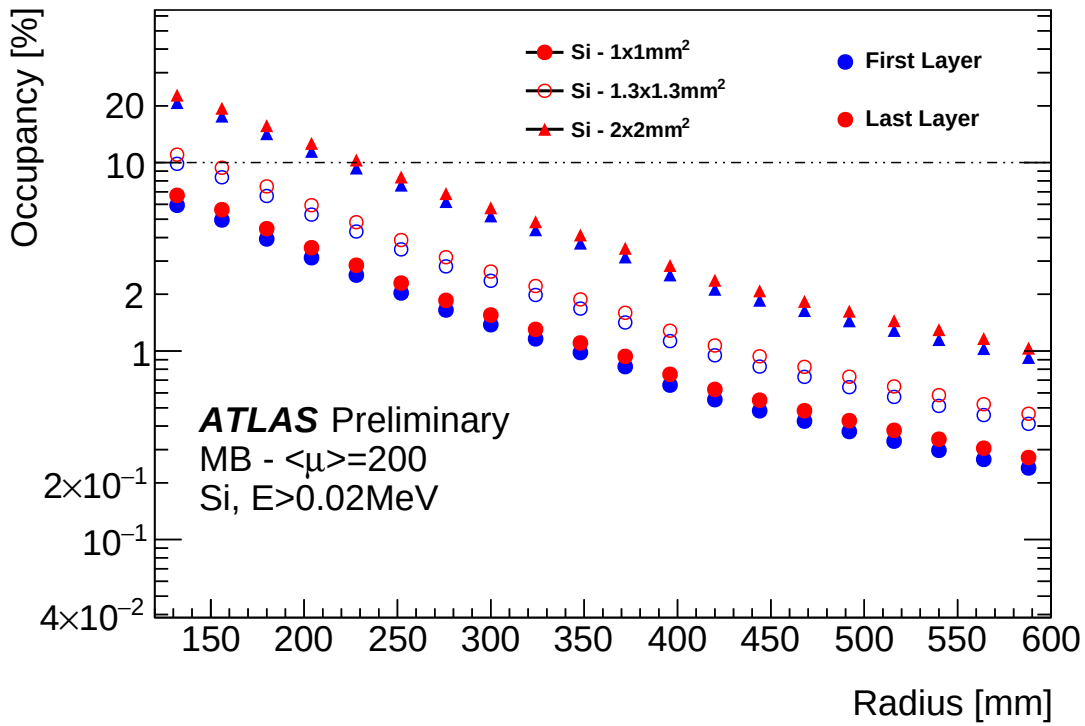
- The HGTD is a Phase-II upgrade ATLAS project that will provide timing capability in the forward region.
- The detector layout has converged to a compromise between spatial/monetary constrains and the goal to guarantee 3 hits per track for smaller radius (high η).
- Next steps:
  - Tests of single pixel readout will continue this year with sensors+ALTIROC0_v2 (2x2 pads)
  - Testing different methods to improve radiation hardness in sensors
  - Arrays of 5×5 pixels will be ready in summer 2018
  - Submission of ALTIROC1 foreseen in June 2018
  - Extensive testing to be done through Q4 2018/Q1 2019, including test bench measurements of the sensor bump bonded to the ASIC
- Approval status:
  - technical proposal approved internally by ATLAS in April
  - approval by LHCC is expected in summer
  - delivery of TDR should be in Q1 2019

BACK UP

Pixel Size

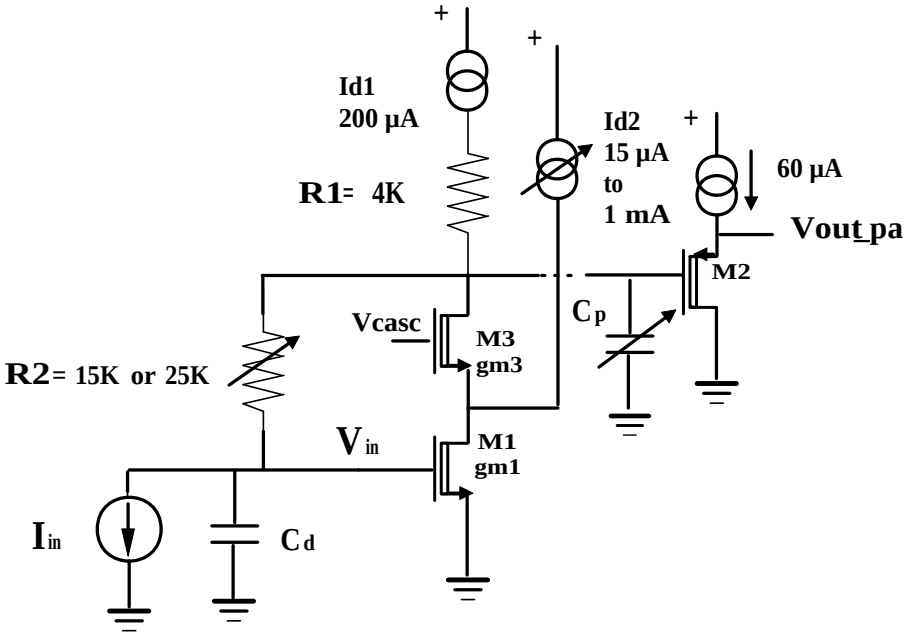
The definition of the size of the pixel is a result of several considerations, mainly:

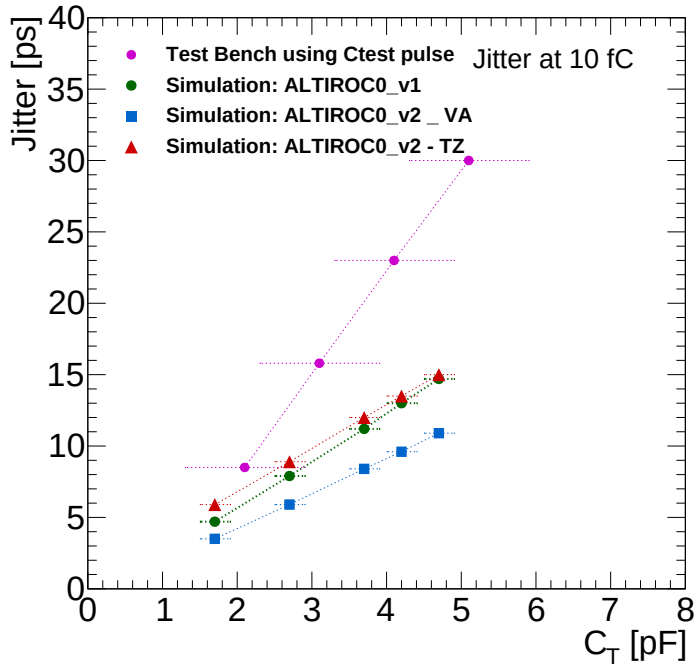
- The need to keep occupancy low (below 10%)
- A small detector capacitance reduces noise, $C = \epsilon_r \epsilon_0 A/w$



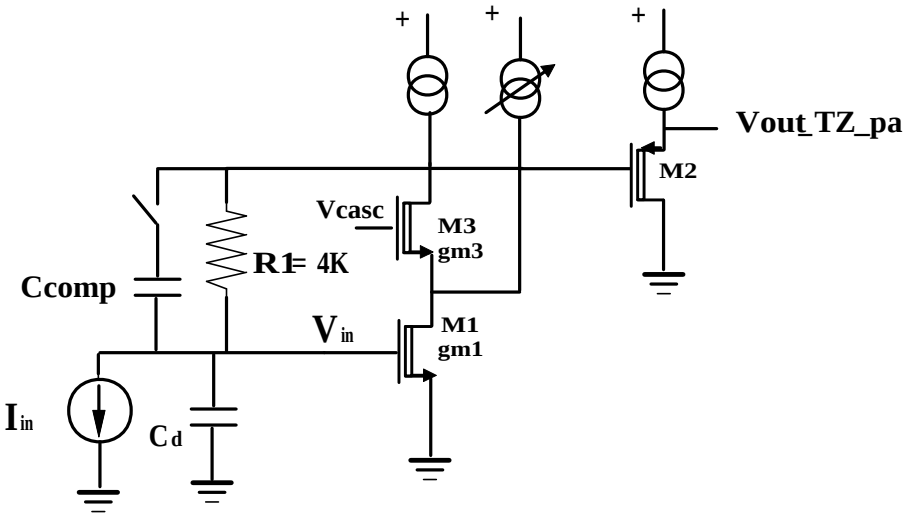
Voltage/Transimpedance preamplifier: schematics

Voltage Preamplifier



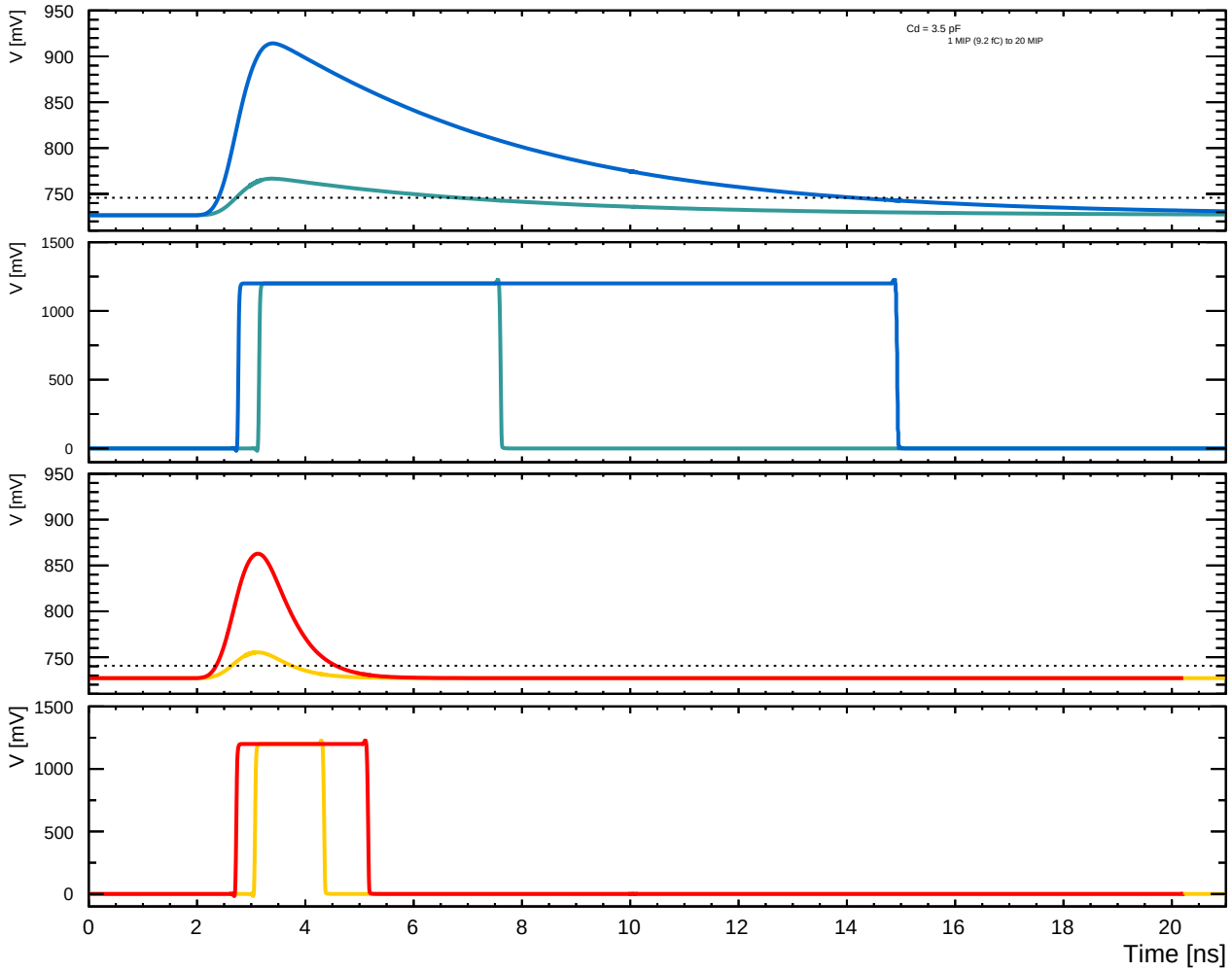


Transimpedance Preamplifier



- Difference btw measurement and simulated jitter attributed to different noise
- Lower jitter in v2
- Jitter in TZ larger than in VPA

Voltage/Transimpedance preamplifier: pulse simulation



- TZ preamplifier gives a faster, lower amplitude pulse than VPA.

ALTIROC ASIC schematic