

Front-End electronics optimization for time tagging with Ultra-Fast Silicon Detectors

Workshop on pico-second timing detectors for high energy physics and applications

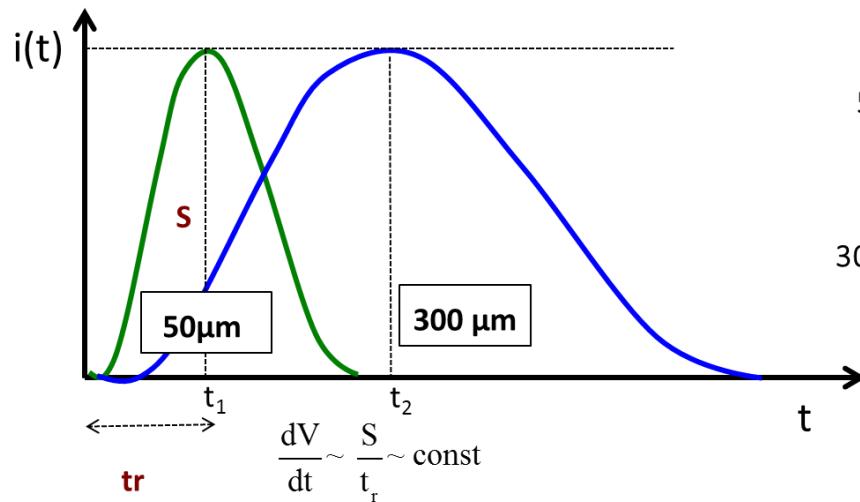
Turin,
May 16th 2018

Federico Fausti
On behalf of the **UfSD** collaboration

Outline

- ❖ Introduction
 - Ultra-Fast Silicon Sensors
 - Front-end electronics for timing applications
- ❖ Preamplifier choice
- ❖ Fast TIAs for UFSD coupling
- ❖ The TOFFEE example
 - Limits
 - Possible improvements
- ❖ FE optimization approach
- ❖ Summary

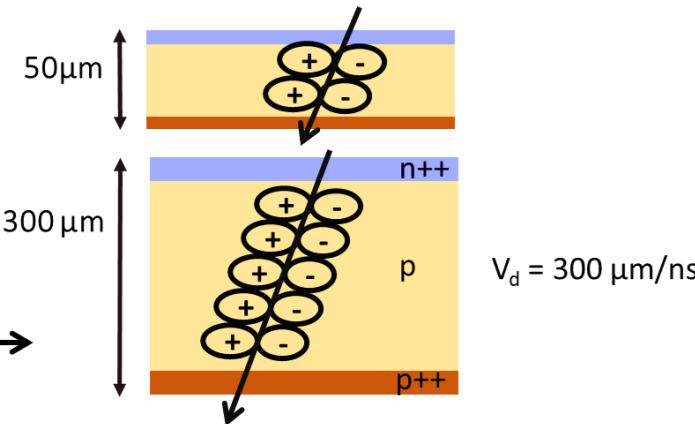
Introduction: Ultra-Fast Silicon Sensors



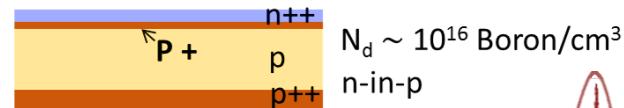
**The maximum value depends
only on the gain value**

**The rise time depends only on
the sensor thickness $\sim 1/d$**

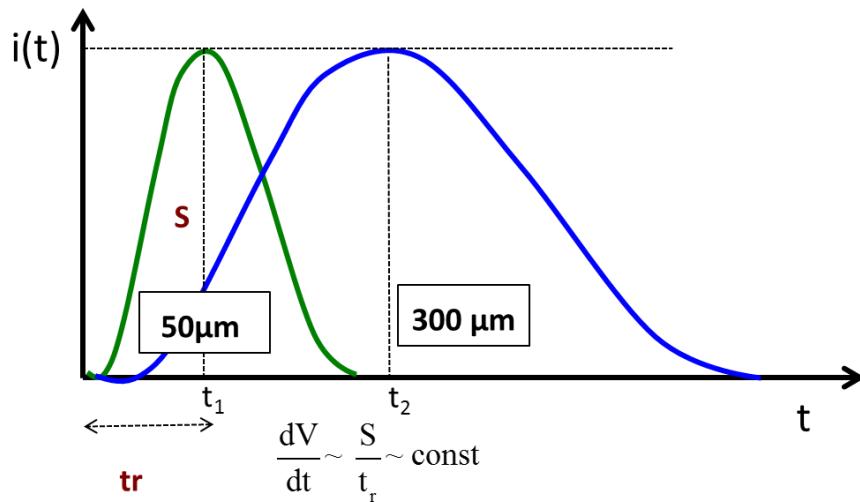
$$\frac{dV}{dt} \propto \frac{G}{d}$$



Thick detectors have longer signals, not higher signals



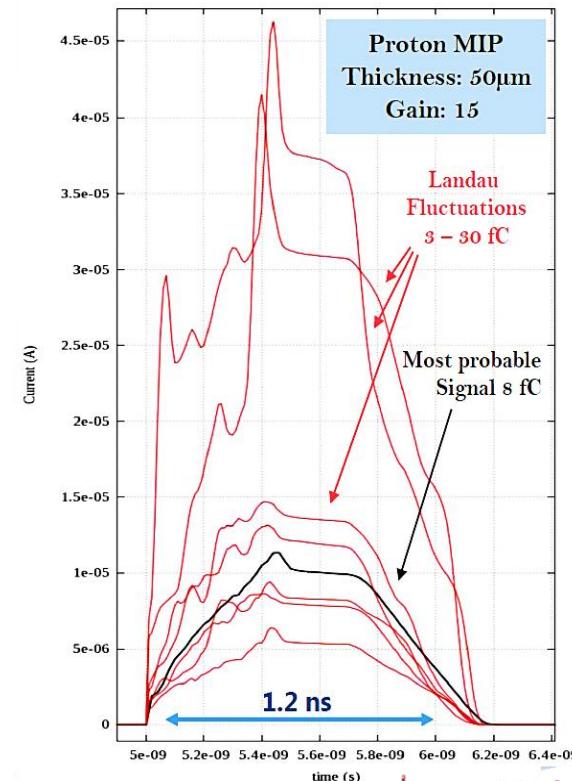
Introduction: Ultra-Fast Silicon Sensors



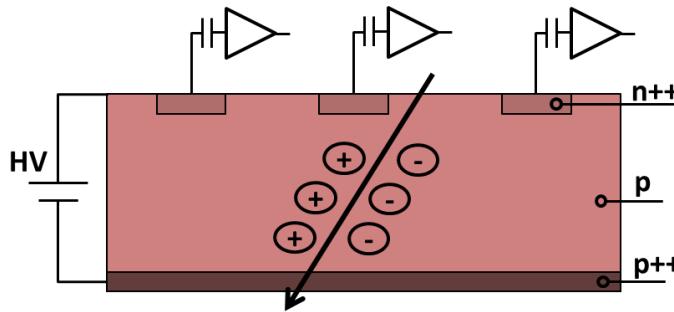
The maximum value depends
only on the gain value

$$\frac{dV}{dt} \propto \frac{G}{d}$$

The rise time depends only on
the sensor thickness $\sim 1/d$



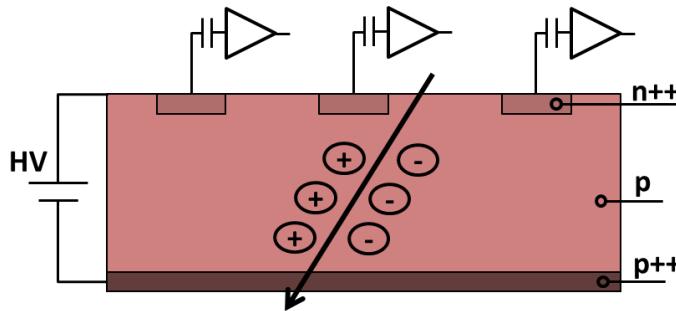
Introduction: Front-end electronics for timing applications



This intrinsic Landau noise sets a pre-front-end limit: $\sigma_{Landau\ Noise} \sim 20\ ps$.

The electronics design goal is then fixed by this number.

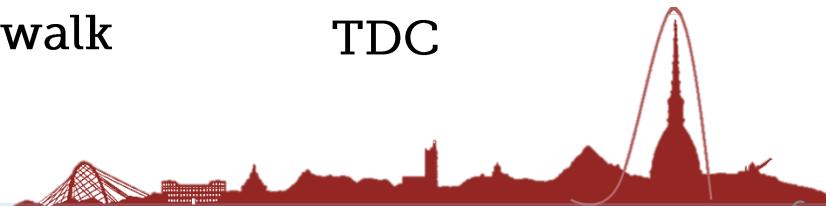
Introduction: Front-end electronics for timing applications



This intrinsic Landau noise sets a pre-front-end limit: $\sigma_{Landau\ Noise} \sim 20\ ps$.
The electronics design goal is then fixed by this number.

$$\sigma_t^2 = \left(\frac{t_{rise}}{S/N} \right)^2 + \left(\left[\frac{t_{rise} V_{th}}{S} \right]_{RMS} \right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}} \right)^2$$

jitter time walk TDC



Introduction: Front-end electronics for timing applications

$$\sigma_t^2 = \left(\frac{t_{rise}}{S/N} \right)^2 + \left(\left[\frac{t_{rise}V_{th}}{S} \right]_{RMS} \right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}} \right)^2$$

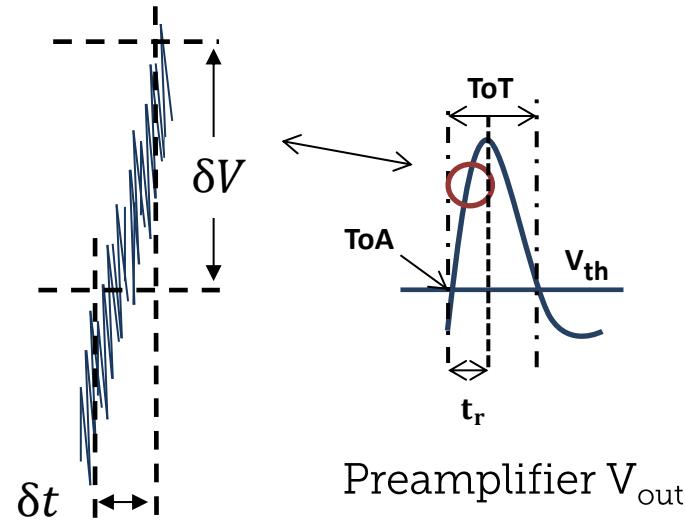
jitter time walk TDC

Introduction: Front-end electronics for timing applications

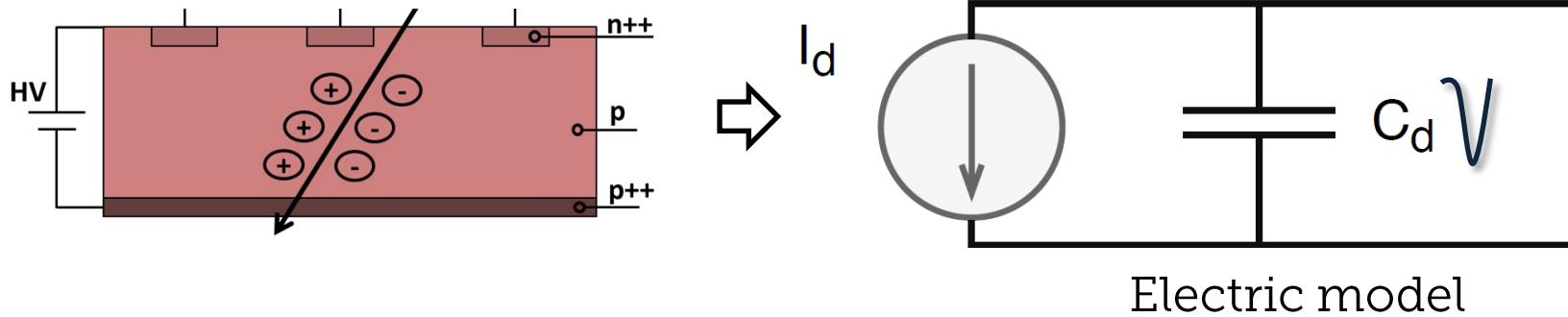
$$\left(\frac{t_{rise}}{S/N} \right)^2$$

jitter

$$\sigma_t^j = \frac{N}{dV/dt} = \frac{t_r}{S/N}$$



Fast TIA for UFSD coupling



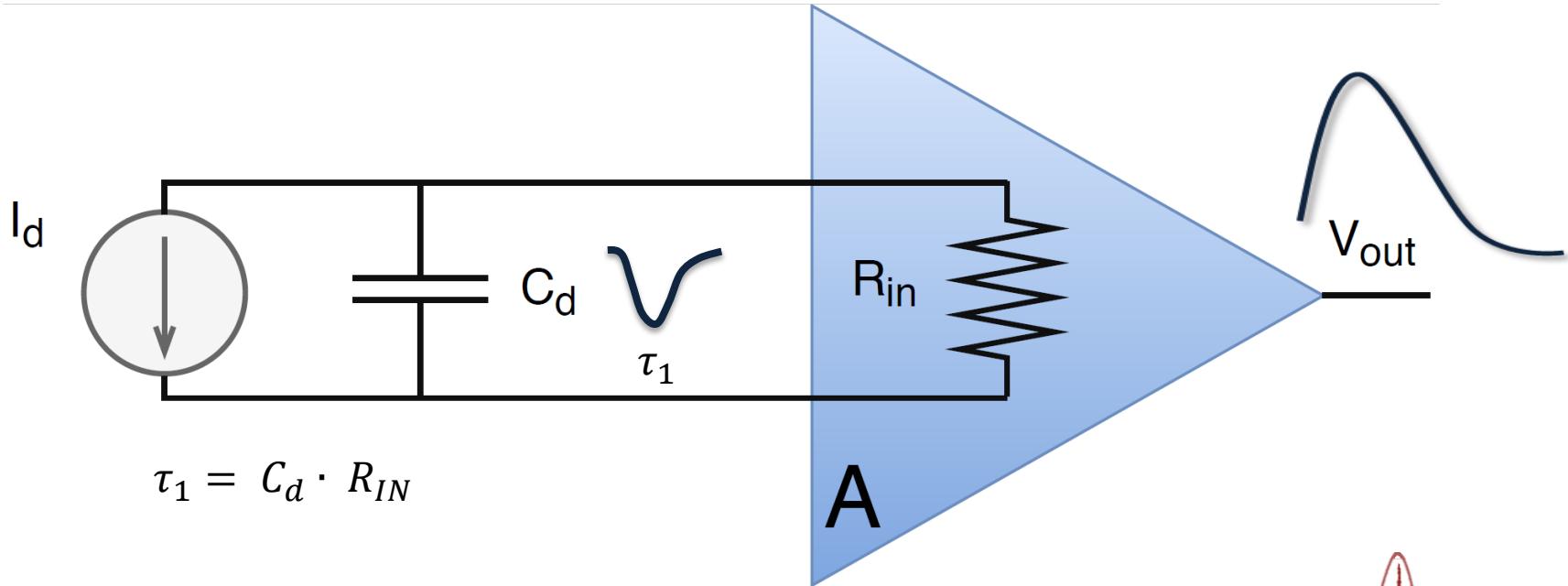
Fast TIA for UFSD coupling

Input	Output	Gain	Type
v_i	v_o	$A_v = v_o/v_i$	Voltage
i_i	i_o	$A_i = i_o/i_i$	Current
v_i	i_o	$A_g = i_o/v_i$	Transconductance
i_i	v_o	$A_r = v_i/i_o$	Transimpedance

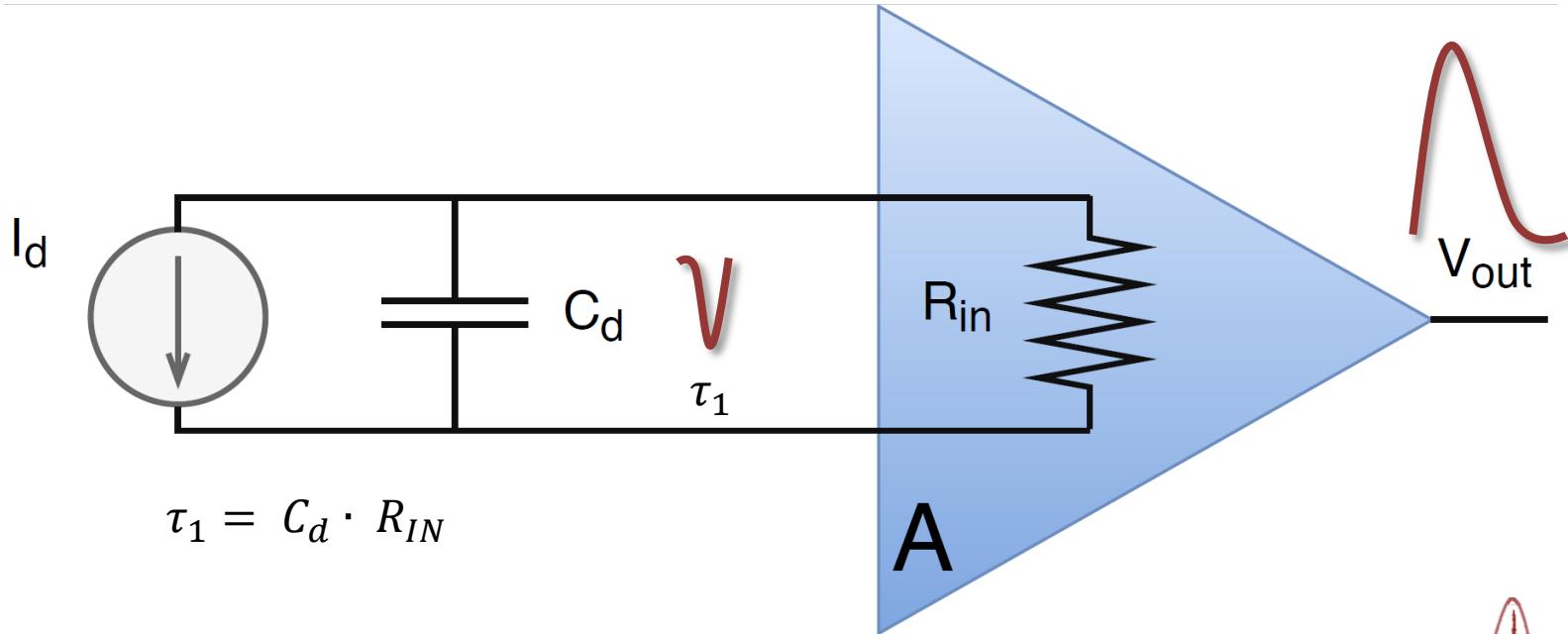
Fast TIA for UFSD coupling

Input	Output	Gain	Type
v_i	v_o	$A_v = v_o/v_i$	Voltage
i_i	i_o	$A_i = i_o/i_i$	Current
v_i	i_o	$A_g = i_o/v_i$	Transconductance
i_i	v_o	$A_r = v_i/i_o$	Transimpedance

Fast TIA for UFSD coupling



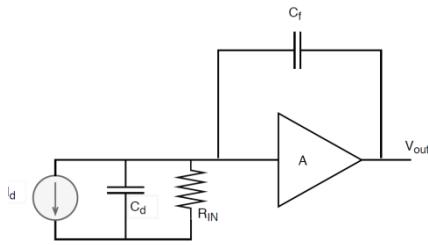
Fast TIA for UFSD coupling



Fast TIA for UFSD coupling

Capacitive feedback.

CSA

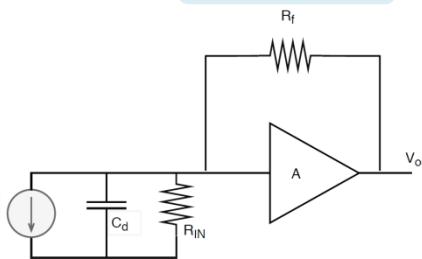


$$V_{out} = -1/C_f \int i(t)dt$$

= Charge sensitive

Resistive feedback

R_f -TIA

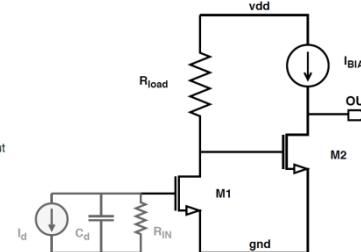


$$V_{out} = -R_f i(t)$$

$$V_{out} = -(Z_{IN} i(t)) g_{m1} R_{load}$$

Broad-Band

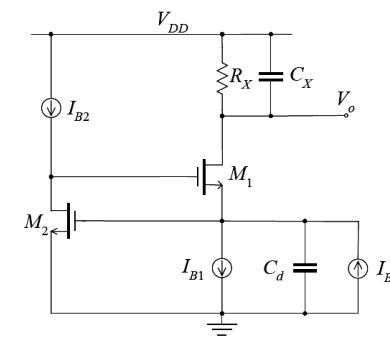
BB



= Current sensitive

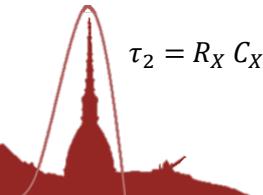
Regulated Common Gate

RCG



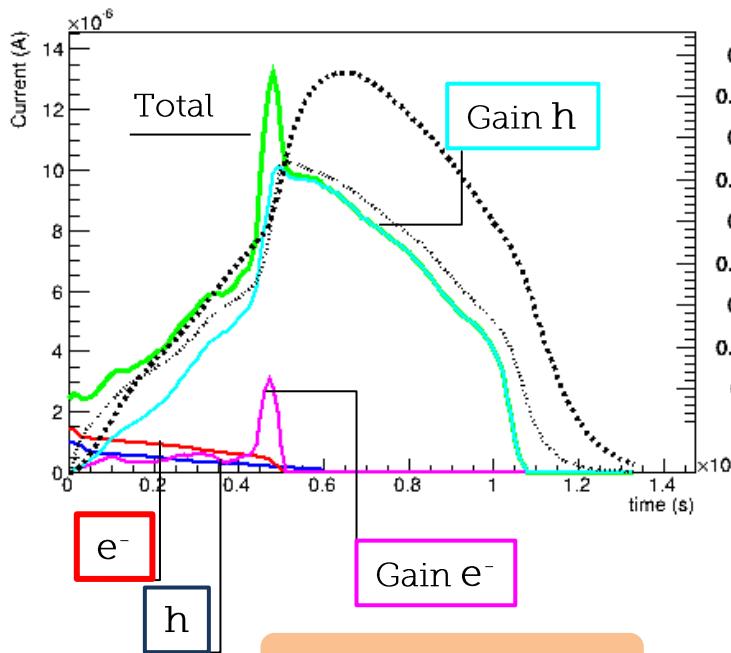
$$V_{out}(t) = \frac{Q_{in}}{C_f} \frac{\tau_1}{\tau_1 - \tau_2} \left(e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}} \right)$$

$$\tau_1 = \frac{C_d}{g_{m1} A}$$



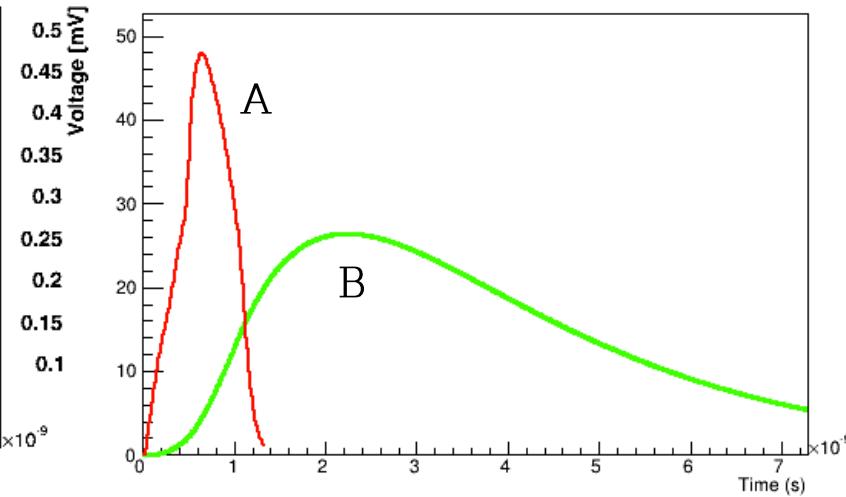
Introduction: Front-end electronics for timing applications

Current signal in a $50 \mu\text{m}$ sensor



N. Cartiglia's talk

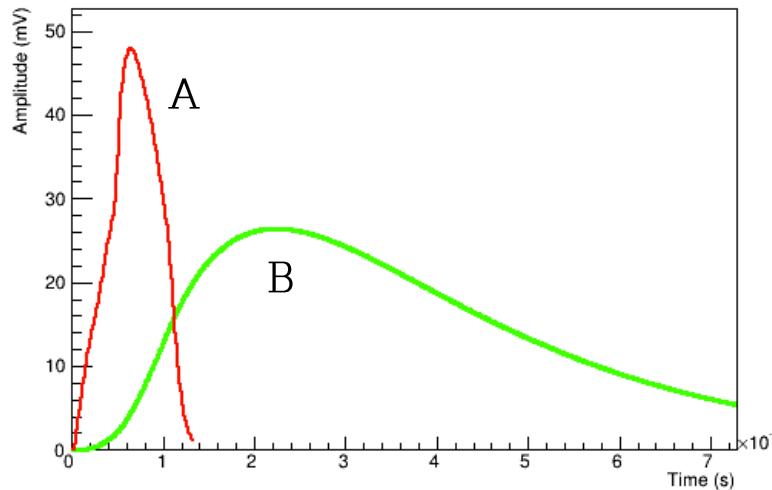
Front-end amplifier response



Current sensitive (A) \rightarrow BB
Charge sensitive (B) \rightarrow CSA

Introduction: Front-end electronics for timing applications

Front-end amplifier response



Current sensitive (A) → BB

Charge sensitive (B) → CSA

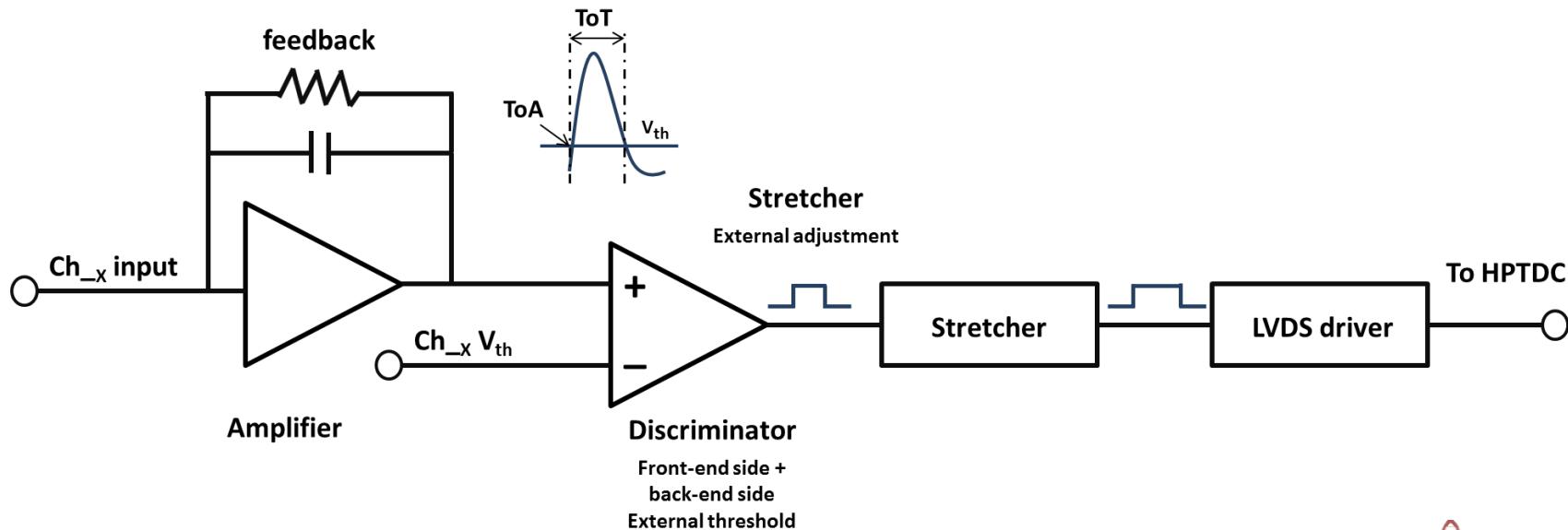
CSA

- $V_{\text{out}}/I_{\text{in}} = -1/j\omega C_f$
- Fine integration : $V_{\text{out}} = -Q/C_f$
- Lowest noise configuration
- Need R_f to discharge C_f

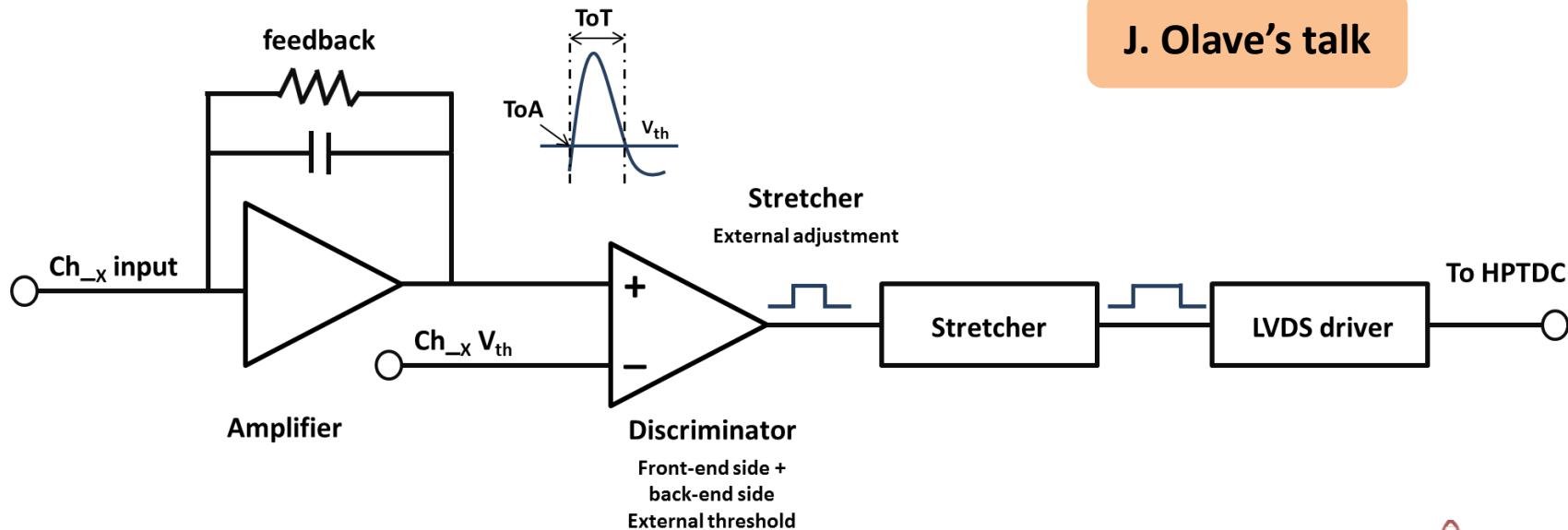
BB

- $V_{\text{out}}/I_{\text{in}} = -R_f$
- V_{out} profile follows I_{in}
- Sensitive to Landau bumps
- Need C_f for stability

The TOFFEE Example



The TOFFEE Example



The TOFFEE Example: simulation outcomes

	BLOCK	JITTER [ps]			
CURRENT [mA]		2		12	
CHARGE [fC]		3	8	3	8
 LAYOUT	Preamp	120	46	104	40
	Discriminator 1	132	47	106	39
	Discriminator 2	131	47	110	40
	Delay line	131	47	111	40
	LVDS	131	47	111	40
	Preamp	42	16	42	11
	Discriminator 1	52	17	53	12
	Discriminator 2	46	16	43	12
	Delay line	47	15	43	12
	LVDS	47	16	43	13

The TOFFEE Example: simulation outcomes

	BLOCK	JITTER [ps]			
CURRENT [mA]		2		12	
CHARGE [fC]		3	8	3	8
 LAYOUT	Preamp	120	46	104	40
	Discriminator 1	132	47	106	39
	Discriminator 2	131	47	110	40
	Delay line	131	47	111	40
	LVDS	131	47	111	40
	Preamp	42	16	42	11
	Discriminator 1	52	17	53	12
	Discriminator 2	46	16	43	12
	Delay line	47	15	43	12
	LVDS	47	16	43	13

Front-end electronics optimization

Looking for a low-power, 20 ps Jitter VFE:

- Parasitics control → layout techniques

Front-end electronics optimization

Looking for a low-power, 20 ps Jitter VFE:

- Parasitics control → layout techniques
- Light architectures → minimum number of MOSFETs

Front-end electronics optimization

Looking for a low-power, 20 ps Jitter VFE:

- Parasitics control → layout techniques
- Light architectures → minimum number of MOSFETs
- Low power → small MOSFETs → less parasitics → faster transients

$$\text{Area} \propto I_{bias}$$

Front-end electronics optimization

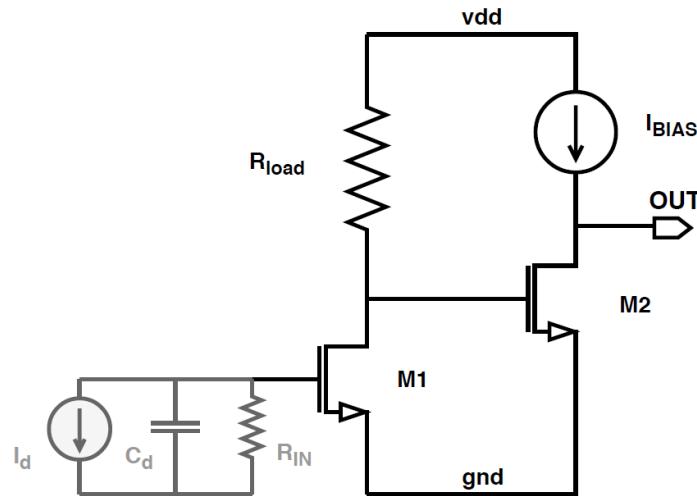
Looking for a low-power, 20 ps Jitter VFE:

- Parasitics control → layout techniques
- Light architectures → minimum number of MOSFETs
- Low power → small MOSFETs → less parasitics → faster transients
- S/N optimization → larger g_m

Front-end electronics optimization

- S/N optimization → larger g_m

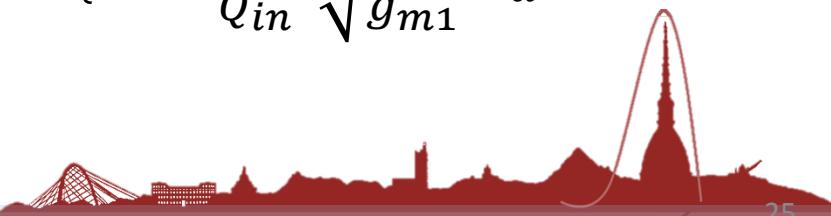
Example: the Broad-Band



$$V_{out} = -(Z_{IN} i(t)) g_{m1} R_{load}$$

$$\sigma_J^J t = \frac{t_r}{V_{out}/N}$$

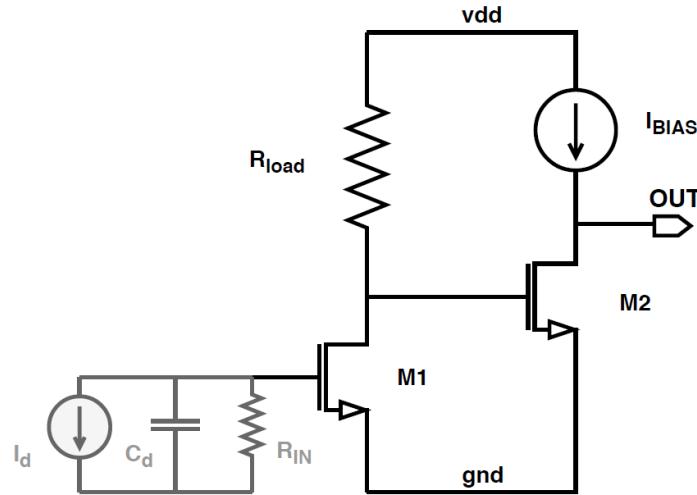
$$\sigma_J^J t = \frac{C_d}{Q_{in}} \sqrt{\frac{2KT}{g_{m1}}} t_d$$



Front-end electronics optimization

- S/N optimization → larger g_m

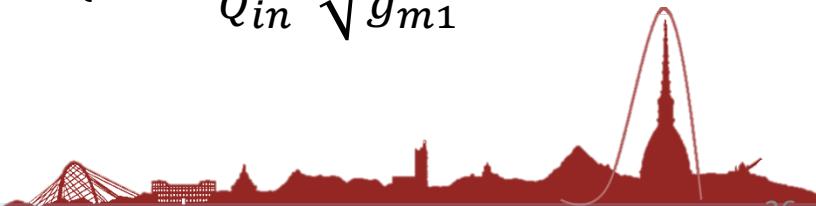
Example: the Broad-Band



$$V_{out} = -(Z_{IN} i(t)) g_{m1} R_{load}$$

$$\sigma_t^J = \frac{t_r}{V_{out}/N}$$

$$\sigma_t^J = \frac{C_d}{Q_{in}} \sqrt{\frac{2KT}{g_{m1}}} t_d$$



Front-end electronics optimization

Looking for a low-power, 20 ps Jitter VFE:

- Parasitics control → layout techniques
- Light architectures → minimum number of MOSFETs
- Low power → small MOSFETs → less parasitics → faster transients
- S/N optimization → larger g_m
- Different technology nodes comparison → g_m scaling effect

Front-end electronics optimization

Looking for a low-power, 20 ps Jitter VFE:

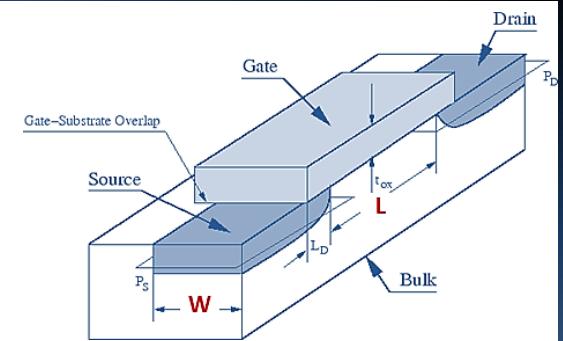
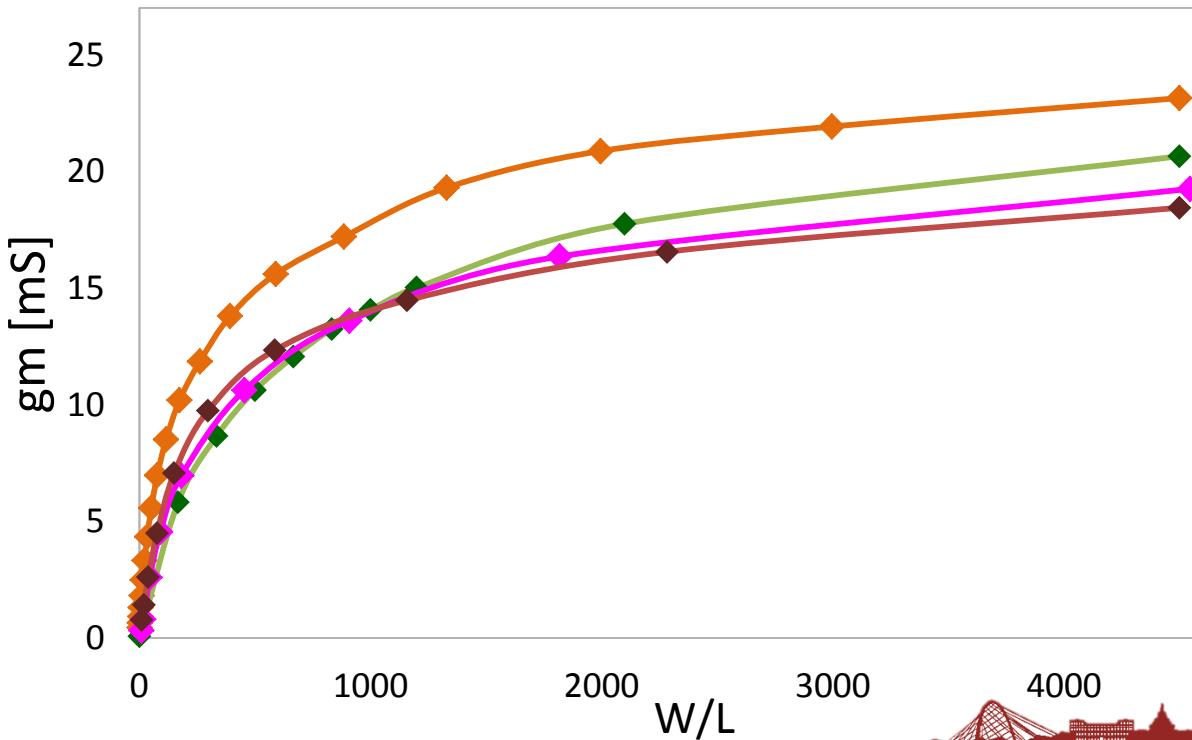
- Parasitics control → layout techniques
- Light architectures → minimum number of MOSFETs
- Low power → small MOSFETs → less parasitics → faster transients
- S/N optimization → larger g_m
- Different technology nodes comparison → g_m scaling effect



- 350 nm
- 110 nm
- 65 nm
- 28 nm

Front-end electronics optimization

NMOS scaling effect: g_m vs $\frac{W}{L}$



110nm

350nm

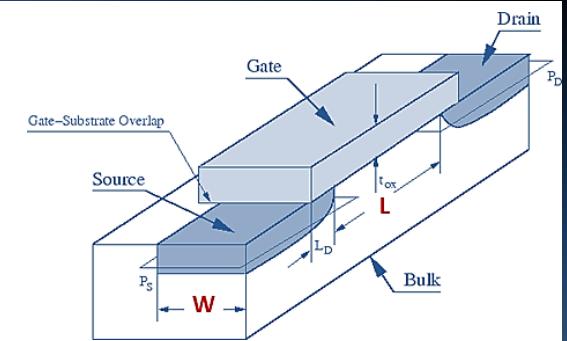
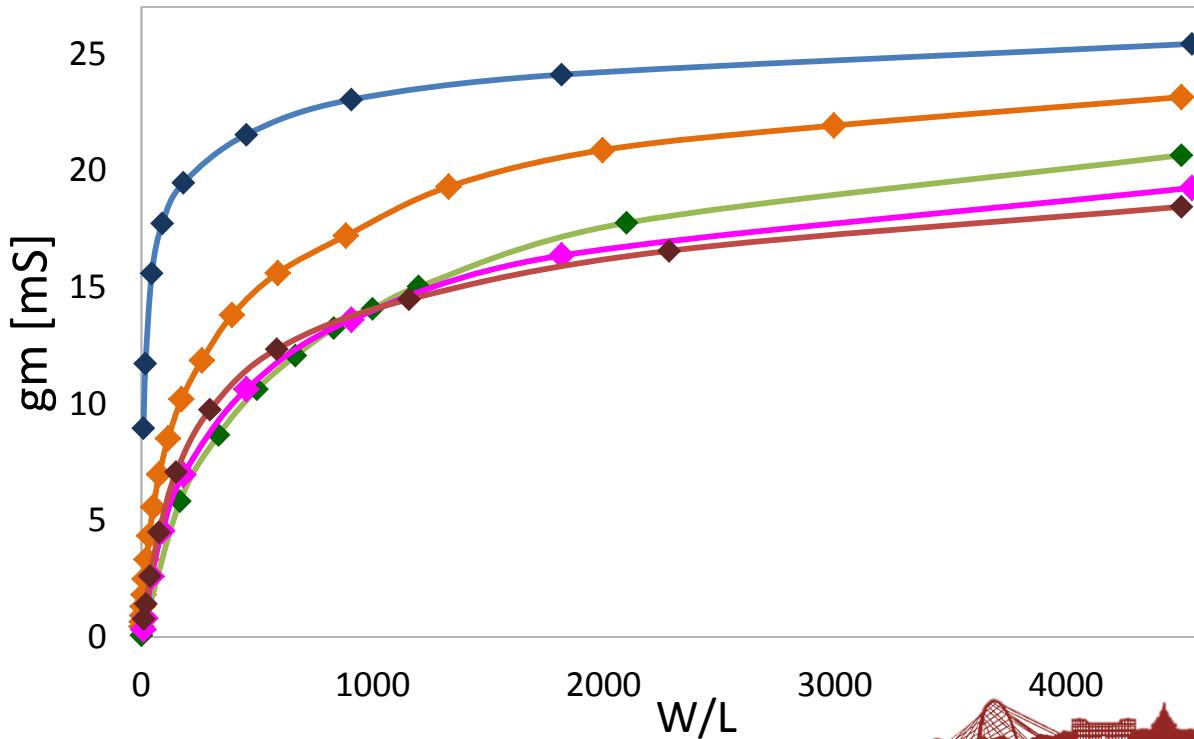
28nm

65nm

$$gm = \frac{\partial V_{GS}}{\partial I_{DS}} |V_{DS} = const$$

Front-end electronics optimization

NMOS scaling effect: g_m vs $\frac{W}{L}$



— 110nm_RF

— 110nm $g_m = \frac{\partial V_{GS}}{\partial I_{DS}} |V_{DS} = \text{const}$

— 350nm

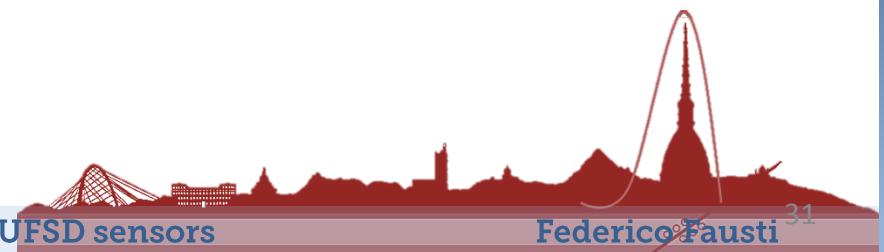
— 28nm

— 65nm

Front-end electronics optimization

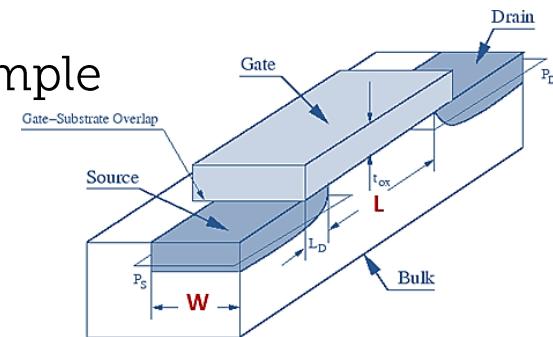
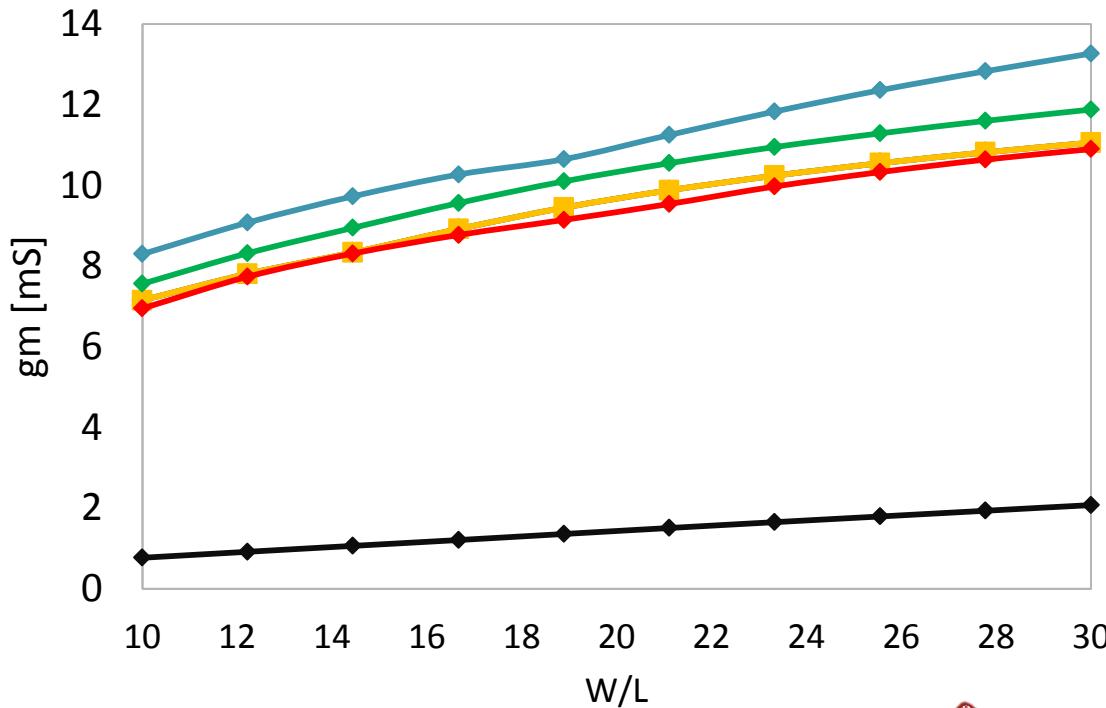
Looking for a low-power, 20 ps Jitter VFE:

- Parasitics control → layout techniques
- Light architectures → minimum number of MOSFETs
- Low power → small MOSFETs → less parasitics → faster transients
- S/N optimization → larger g_m
- Different technology nodes comparison → g_m scaling effect
- MOSFETs characterization for timing (RVT, LVT, HVT, RF...)



Front-end electronics optimization

MOSFETs characterization for timing: the 65 nm example



standard

RF

RF_a

RF_b

RF_25

RF_HVth

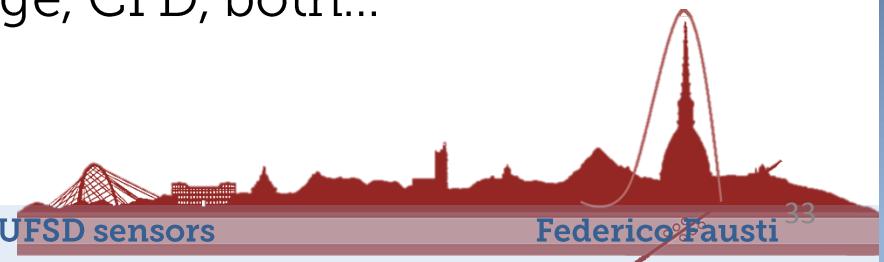
RF_LVth

$$gm = \frac{\partial V_{GS}}{\partial I_{DS}} |V_{DS} = const$$

Front-end electronics optimization

Looking for a low-power, 20 ps Jitter VFE:

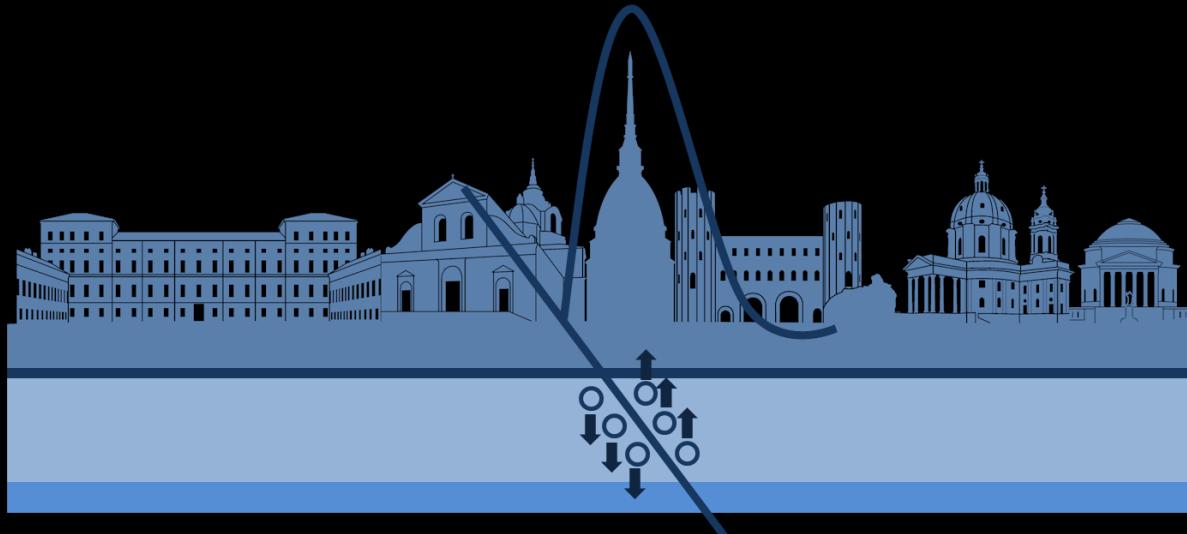
- Parasitics control → layout techniques
- Light architectures → minimum number of MOSFETs
- Low power → small MOSFETs → less parasitics → faster transients
- S/N optimization → larger g_m
- Different technology nodes comparison → g_m scaling effect
- MOSFETs characterization for timing (RVT, LVT, HVT, RF...)
- Discriminator type → leading edge, CFD, both...



Outlook

VFE design strategy

- Device level characterization for timing applications
- Technology node choice
- Amplifier choice
- Multiple discriminator possibility
- Prototype development → test on silicon



Thank you for your attention

We kindly acknowledge the following funding agencies:

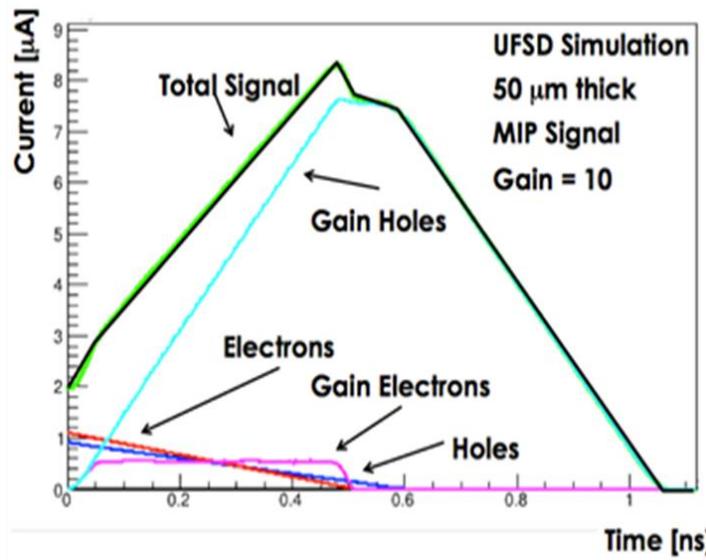
INFN – GruppoV

Horizon 2020 Grant URC 669529

Ministero degli Affari Esteri, Italy, MAE

Backup

UFSD: Weightfield2 signal profile



Prototype idea

16 channels VFE ASIC:

- 4 preampl. solutions
- x2 (redundancy)
- + RF MOSFETs

