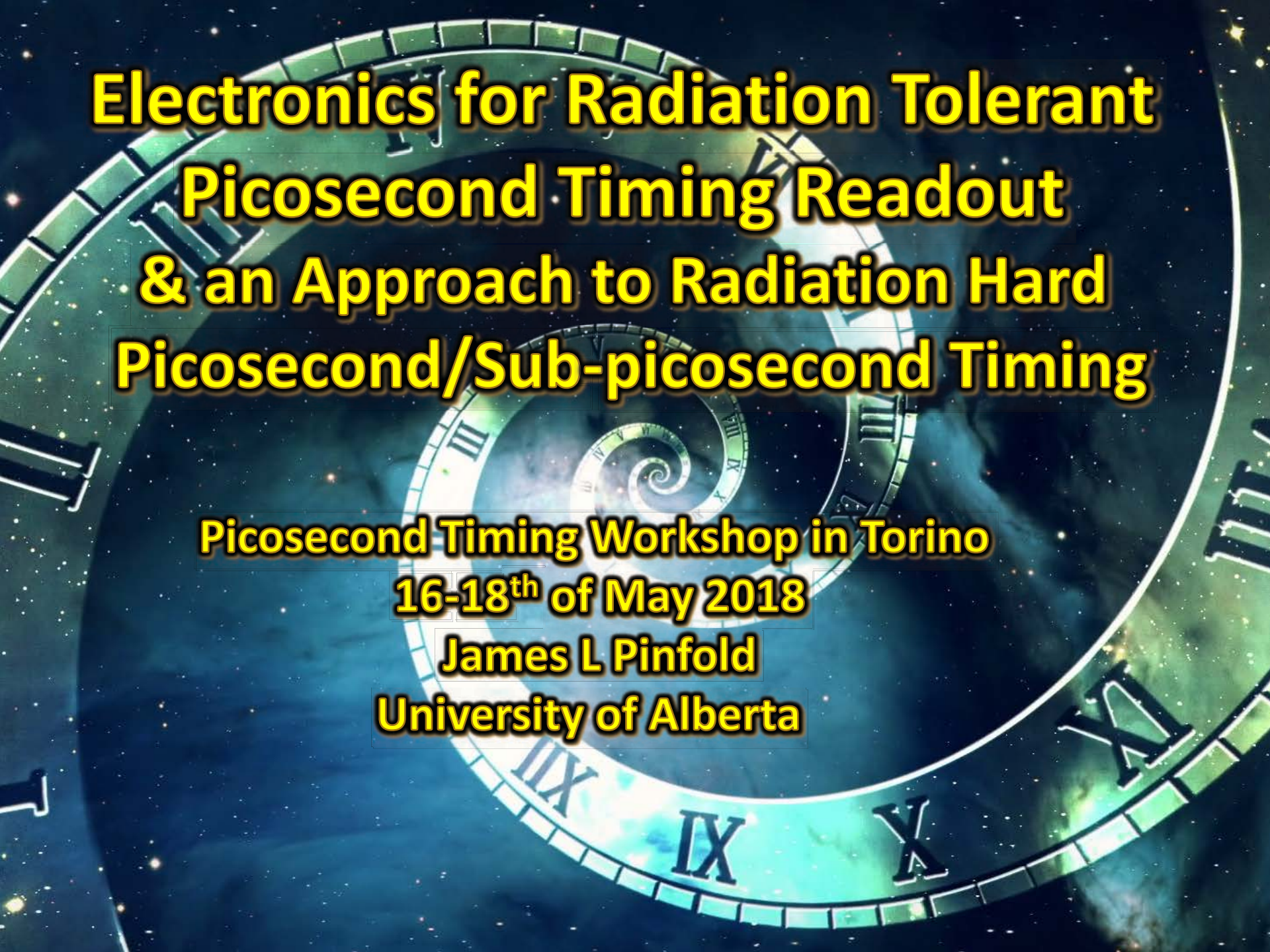


Electronics for Radiation Tolerant Picosecond Timing Readout & an Approach to Radiation Hard Picosecond/Sub-picosecond Timing

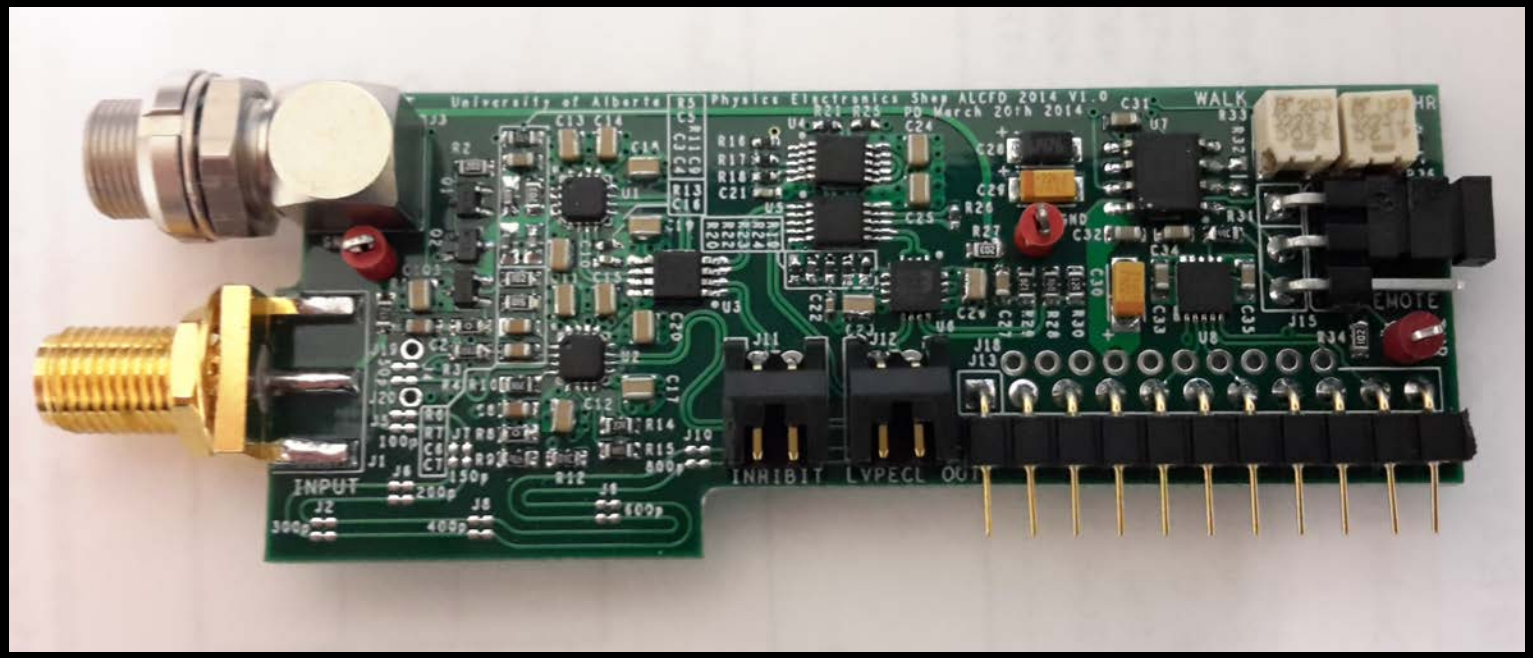
Picosecond Timing Workshop in Torino
16-18th of May 2018

James L Pinfold
University of Alberta


MENU
1) Introduction
2) Electronic Readout for AFP with 15 ps resolution
3) Radiation Tolerant readout for AFP
4) The future with the new HPTDC with 3ps resolution
5) Possible Solutions for radiation hard and/or sub-picosecond timing electronics
BEER
BREWERY
ABV
NO SMOKING

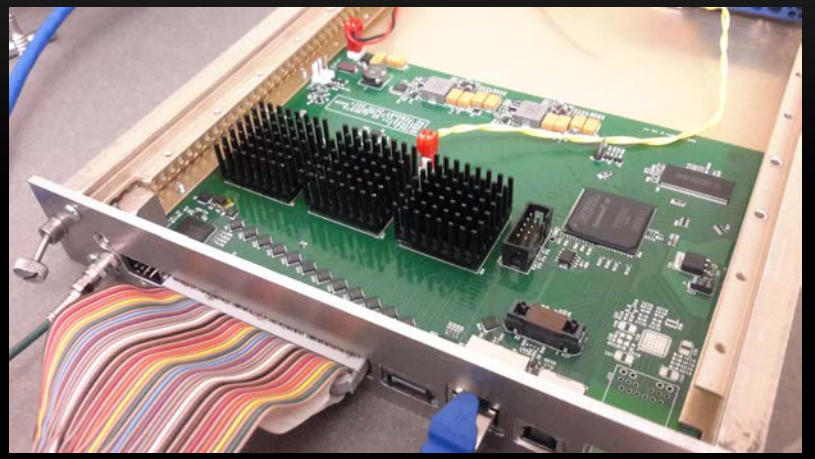
AFP Constant Fraction Discriminators

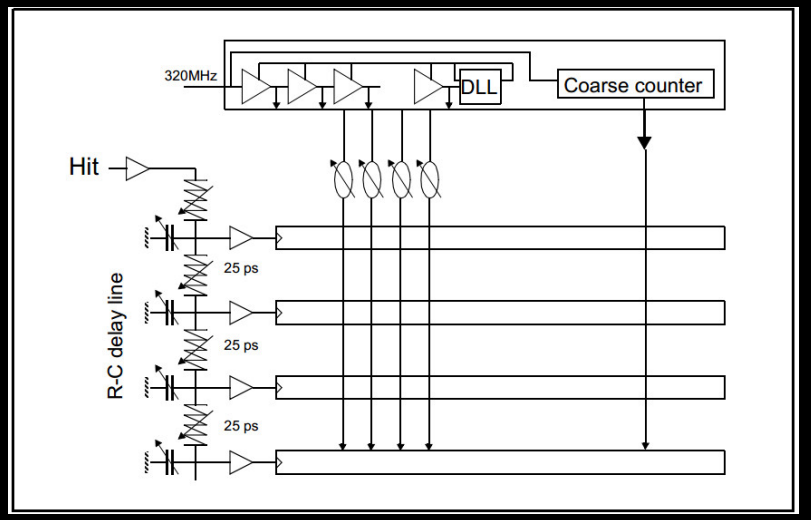
- *CFDs worked well during 2017 running except for a few infant failures the cause of which still need to be investigated. Threshold can be set remotely. Time walk ~3ps rms*



The AFP HPTDC Board

- *12 channels with 25ps binning and ~15ps resolution*
- *I^2C output controls CFD thresholds and trigger board settings and can read out monitoring information*
- *Calibration muxes allow alternate signals to be injected into the hit inputs for test and calibration purposes*
- *ToT implemented*
- *Trigger output formed from coincidence of hit signals (4ns window)*





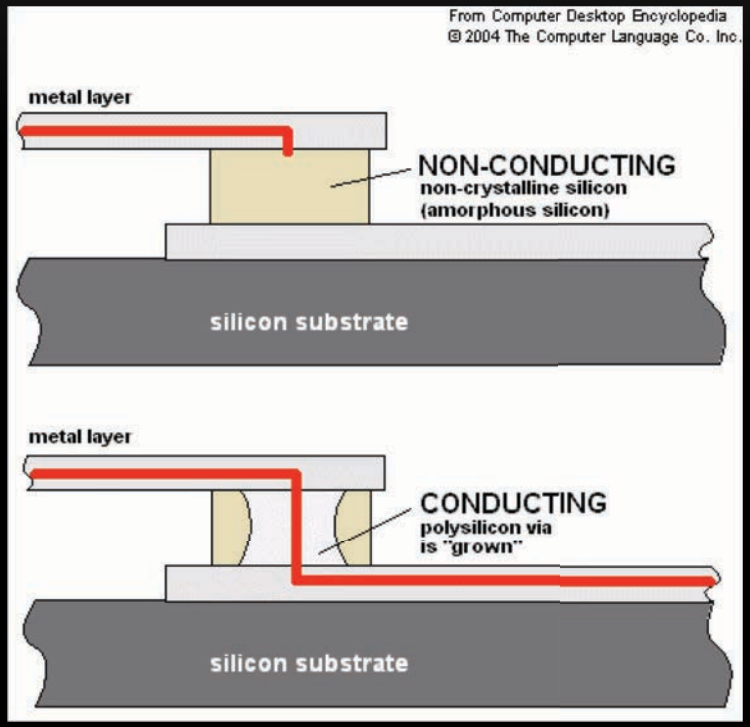
High Performance Time to Digital Converter Manual Version 2.2, March 2004, pg8. Jorgen Christiansen

Rationale for Radiation Tolerant Upgrade of HPTDC Board

- *The 32-channel HPTDC, been implemented in IBM 0.25 µm CMOS technology*
  - *The HPTDC has been implemented in a radiation tolerant technology, standing up to levels of 30 Krad total dose with slight increase in power consumption.*
- *Current TDC FPGA chip has SEUs in configuration RAM at a much higher frequency than expected (~10 upsets/day at peak luminosity ~10^{34} cm^{-2} s^{-1}).*
- *Originally planned mitigation, reset on SEU, would cause too much ATLAS busy. Current mitigation has potential for undetected errors.*
- *FPGA is being changed to a more radiation tolerant version.*

Antifuse FPGAs

- *A good radiation tolerant approach to FPGA technology is the MICROSEM(ACTEL) Antifuse FPGA*
- *In this case the FPGA logic is one time programmable eg "hard wired" – good to few Mrads*
- *Problem is that each time we need to reprogram the FPGA we need a new (and expensive) FPGA.*



Basic idea of an antifuse one-time Programmable FPGAs

A Radiation Tolerant FPGA (2)

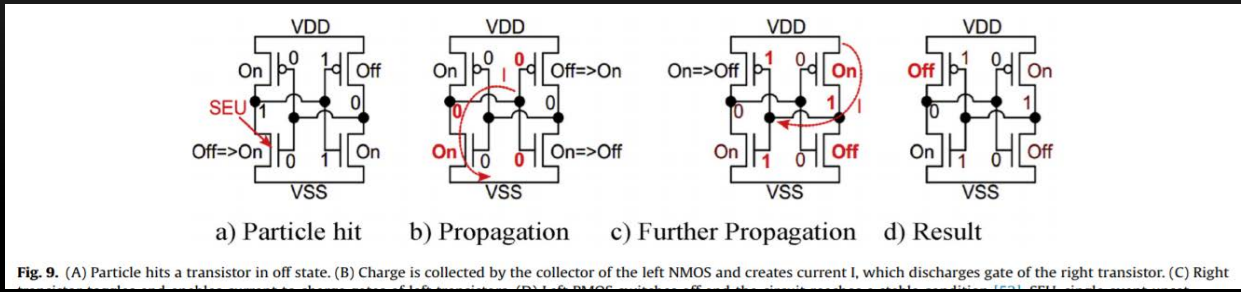
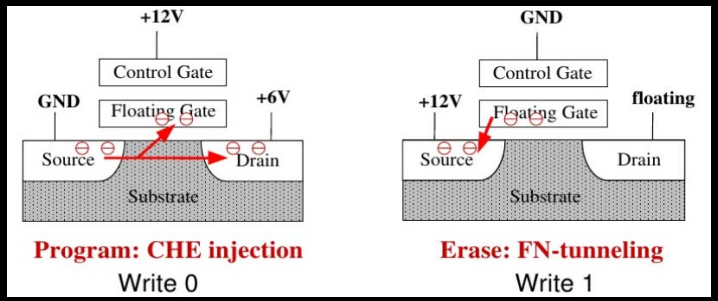


Fig. 9. (A) Particle hits a transistor in off state. (B) Charge is collected by the collector of the left NMOS and creates current I, which discharges gate of the right transistor. (C) Right

- *SRAM cell is formed by two inverters in a positive feedback loop. Charge injection into one of the off transistors causes a transient change of state that is then reinforced by the feedback loop causing a bit flip.*

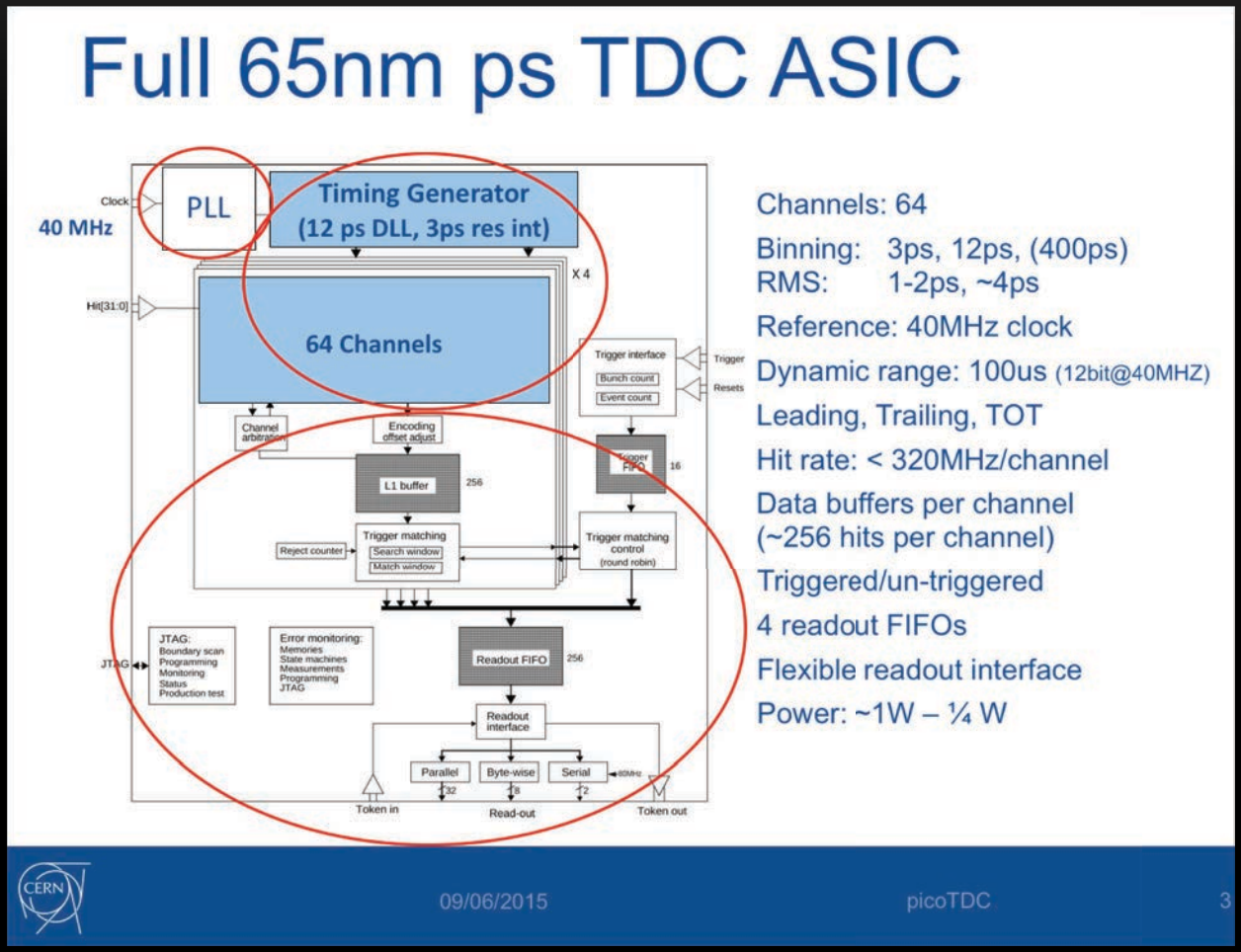


- *Flash memory has a floating gate. Charge is stored on the floating gate through hot carrier injection and erased via Fowler–Nordheim tunneling. No feedback Mechanism*

We Chose the Flash Technology For Installation in June 2018

- *Replace existing Xilinx (SRAM) FPGA Tech. with Microsemi Igloo2 M2GL025T (flash) FPGA.*
  - *Marginally smaller to the previous Xilinx FPGA – 27696 vs 28848 Logic Elements*
  - *More RAM - 1130496 bits vs 608256 &Fewer use I/O points 267 vs 238*
  - *Slightly slower Max Clock Rate of 400MHz vs 480MHz will result in slightly less resolution of ToT and lower granularity of trigger.*
  - *Igloo2 used in CMS HCAL and Muon detectors*
- *Some tests have been performed of the Igloo2 showing that it can take a TID of up to 100-400 Gray*
- *Configuration upsets practically eliminated (up to LET of 90 MeV with 3 x 10^9 per cm^2 fluence).*
- *First rad. tolerant AFP HPTDCs (with flass FPGAs will be installed this June*

The Next Step - the picoTDC (1)



*Jorgen Christiansen *CERN, Moritz Horstmann, Lukas Perktold (Now AMS), Jeffrey Prinzie (KU Leuven)*

The Next Step - the picoTDC (2)

- *A delivery of the current iteration of the chip is expected in June 2018. We hope to test the new chip during a late 2018 test beam*
- *PicoTDC uses a similar scheme for timing as current TDC but uses higher clock speed and resistive interpolation of the DLL instead of channel interpolation*
- *65nm technology TID tolerant*
  - *SEU detection and minimize effects from SEU when it can have major consequences (system sync). As done in HPTDC.*
  - *Protected deploymnet needed at the HL-LHC?*

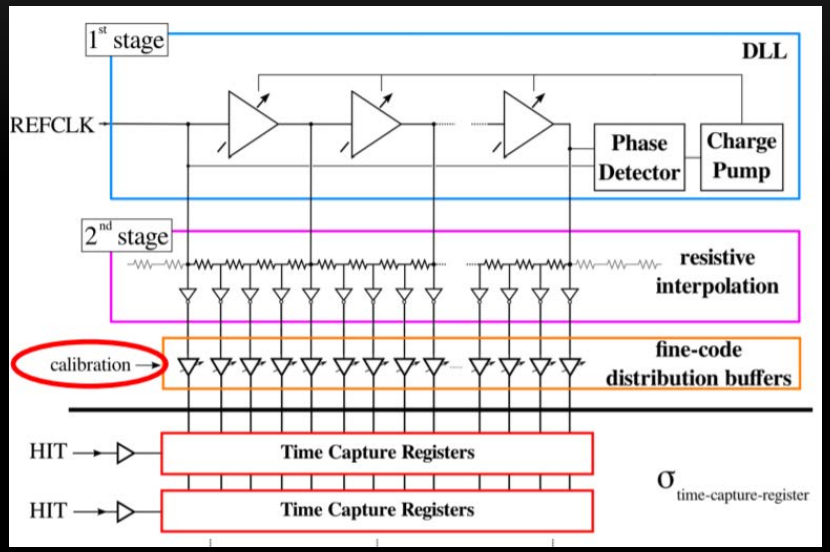


Image from picoTDC: Pico-second TDC for HEP, Jorgen Christiansen, Morit Horstmann, Lukas Perktold, Jeffery Prinzie, 2005

Max int. clock rate 2.56 GHz compared to 320 Hz for the HPTDC

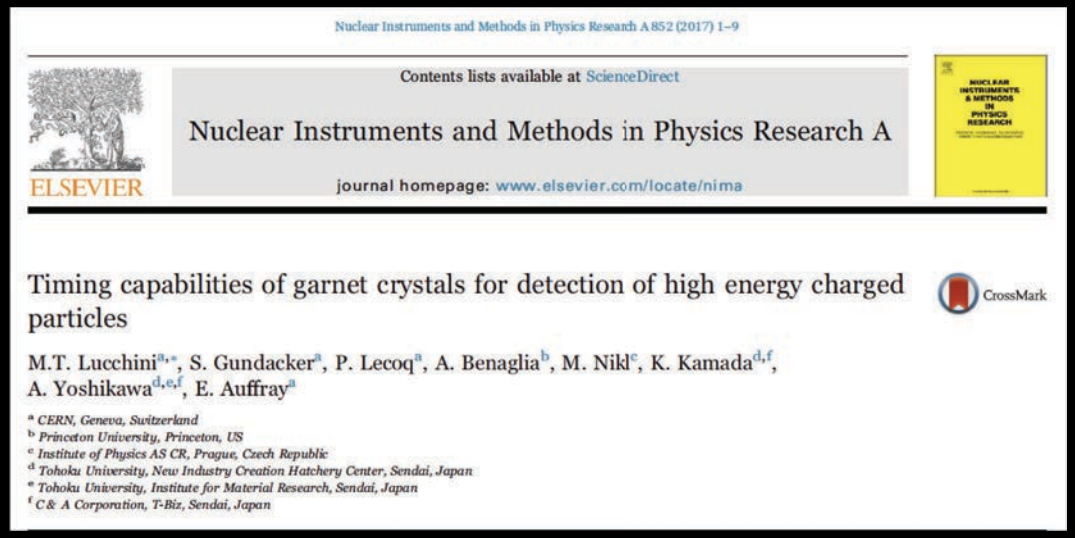
Approach to Radiation Hard Picosecond →Sub Picosecond Timing

- *Basic Philosophy to achieve picosecond and then sub-picosecond timing precision*

1. *Good per channel resolution PicoTDC – 3 ps bin (1.8 ps RMS); HPTDC - 100 ps bin.*
2. *Combine channels (eg AFP - HPTDC – 4 channels combined → 25ps bin width → ~15 ps RMS)*
3. *The resolution of N uncorrelated measurements of the same quantity each with resolution σ has a resolution of $\sigma/\sqrt{N}$ eg 30 ps measurement (detector+ readout) with 9 measurements → 10 ps resolution (30 /√ 9)*

Achieving Picosecond/Sub-picosecond Timing Resolution (1)

- *Picosecond/sub-picosecond timing resolution for the electronics should be possible with the picoTDC*
  - *When 2-4 channels are combined & RMS resolution for one channel is 1.8 ps*
- *The Main problem is the detector resolution. What can we assume for the best detector resolution we can get with existing/forseeable technology? It looks like 16 ps is a reasonable number.*



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Timing capabilities of garnet crystals for detection of high energy charged particles

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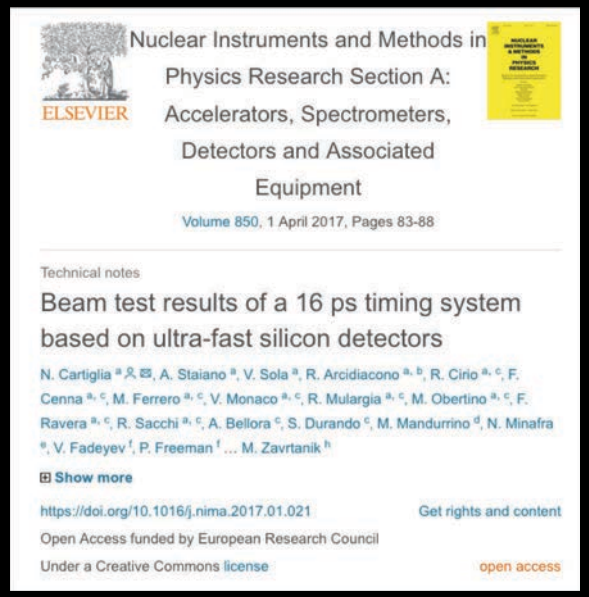

Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment

Volume 850, 1 April 2017, Pages 83-88

Technical notes

Beam test results of a 16 ps timing system based on ultra-fast silicon detectors

N. Cartiglia [a], A. Staiano [a], V. Sola [a], R. Arcidiacono [a, b], R. Cirio [a, c], F. Cenna [a, c], M. Ferrero [a, c], V. Monaco [a, c], R. Mulargia [a, c], M. Obertino [a, c], F. Ravera [a, c], R. Sacchi [a, c], A. Bellora [c], S. Durando [c], M. Mandurrino [d], N. Minafra [e], V. Fadeyev [f], P. Freeman [f] ... M. Zavrtanik [h]

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https://doi.org/10.1016/j.nima.2017.01.021

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Achieving Picosecond/Sub-picosecond Timing Resolution (2)

- *To obtain 1 ps overall resolution or better with a detector with a basic resolution of 16 ps we need at least 256 measurements !*
- *The detectors we mentioned can feasibly (?) make (on average) 10 measurements per cm:*
  - *In the case of the crystal scintillator (eg LSO, LYSO) the thickness of the detector could be as little as ~2mm (22K photons/MeV) we have enough light to make 4 measurements/detector with 5 detectors/cm → we can make 20 measurements per cm → we would need a ~13 cm long detector.*
  - *We should be able to make as many measurements/cm with the Low-Gain Avalanche Detector (LGAD) design,*

UFSD Timing resolution		
	Vbias = 200 V	Vbias = 230 V
N = 1	34 ps	27 ps
N = 2	24 ps	20 ps
N = 3	20 ps	16 ps

Dimensions [mm^3]	Crystal type	E_{dep}^{peak} (E_{dep}^{mean}) [MeV]	$\sigma_{t,corr.}^{single}$ [ps]
6×6×3	LYSO:Ce	2.7 (3.2)	17.5 ± 1.1
2×2×5	LSO: Ce, Ca	4.7 (5.5)	17.2 ± 1.0

Radiation Hard Solutions to Picosecond Timing?

- *ATLAS is proposing UFSD as one of the technical options for the High Granularity Timing Detector[1] located in front of the FCAL.*
- *CMS is considering UFSD to be the timing detectors for the forward Precision Proton Spectrometer (CT-PPS)[2].*
- *In both cases, the UFSD would have moderate segmentation (a few mm^2) with challenging rad. requirements (several 10^{15} neq/cm^2)*
- *We also considered here crystal-scintillators lutetium oxyorthosilicate (LSO) & lutetium-yttrium oxyorthosilicate (LYSO). The rad. hard properties of LSO and LYSO are well established[3]*

1) D. Zerwas, ECFA 2016, High Lumi. LHC Experiments Workshop, https://indico.cern.ch/ event/524795/ contributions/2237331/attachments/1349507/2036492/161006_AixLesBains.pdf

2) C. Royon, N. Cartiglia, "The AFP and CT-PPS projects", Int. J. Mod. Phys. A 29, 1446017 (2014)

3) R.H. Mao, L.Y. Zhang and R.-Y. Zhu, Gamma Ray Induced Radiation Damage in PWO and LSO/LYSO Crystals , Paper N32-5 in NSS 2009 Conference Record (2009).

Conclusion

1) We have achieved 15ps time resolution for the current AFP TOF system. As far as the AFP ToF electronics is concerned we appear to have a solution for LHC Run-3. Hopefully, we will have the picoTDC for Run3 making the contribution to the AFP's timing resolution negligible compared to the detector.

2) Radiation hard picosecond & (just) sub-picosend detectors look feasible utilizing existing technology at a first quick look

A number of challenging technical gotchas have to be investigated in detail, such as noise and cross-talk issues

EXTRA SLIDES

Flash Failure Mechanisms

- *Hot carrier injection causes crystal defects resulting in charge being trapped in insulation between floating gate and channel eventually shielding the floating gate. ~10000+ programming cycles.*
- *Ionizing radiation also deposits charge in the insulating layer. Failure usually first shows as inability to erase device.*
- *Charge pump for generating voltages for programming/erasure can also be susceptible to radiation induced failure rendering reprogramming impossible.*
- *Gate propagation delay increases as floating gate becomes shielded Eventual operational errors due to timing violation. Can be mitigated with additional timing margin.*