ASICs for precision timing

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Ps workshop, May 16th

The case for fast timing

- Traditionally, high resolution timing detectors are used in HEP to identify particles
  - Measure the time to fly between two points to obtain the velocity
  - Combine with momentum information to derive the mass
  - Large systems: ALICE ToF: 160 m^2. Similar area for the CBM ToF wall at FAIR

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  - Mass analysis with ToF mass spectrometry
  - Positrom Emission Tomography: ToF reduces image noise

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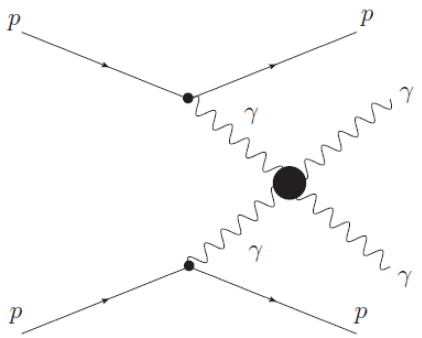
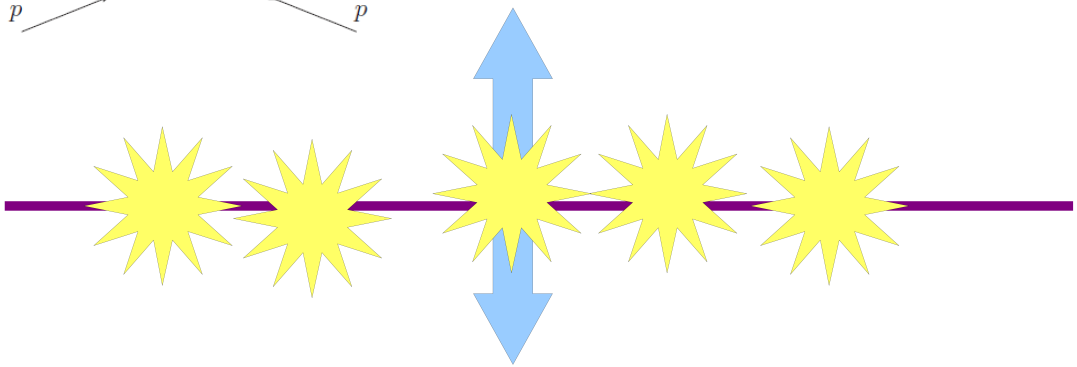
  - Positrom Emission Tomography: ToF reduces image noise
- With a peak luminosity of $\approx 10^{35}$, the HL-LHC will produce 140 to 200 collisions per bunch crossing
  - Disentangling interesting events from background only with tracking and vertexing becomes challenging
  - The average collision distance in time is $100 \div 170$ ps

Extra dimensions?

- Collision survivors can be used to probe new physics



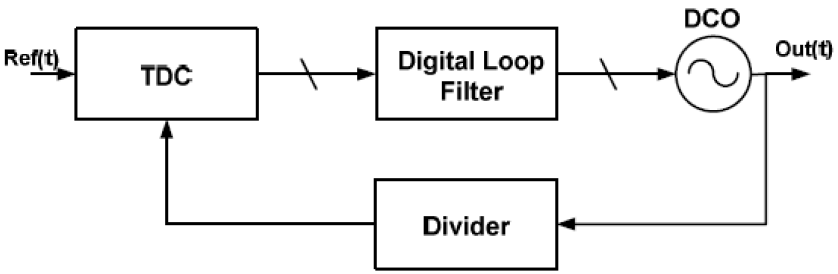
$$pp \rightarrow p\gamma\gamma p$$

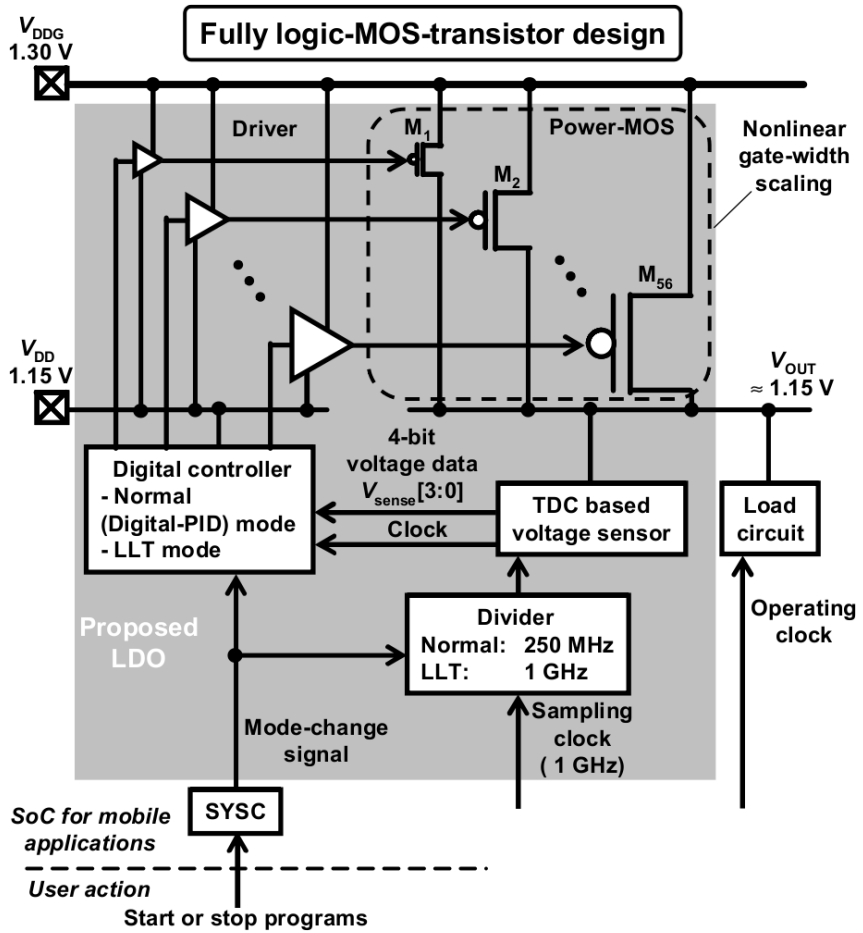


- $pp \rightarrow p\gamma\gamma p$ sensitive to extra-dimensions
- Intact protons detected 250 m far from the collision point
- Need of 10 ps timing to suppress pile-up

Practical use of timing

- TDC used to measure phase difference in ADPLL
- With scaling technologies speed of gates increases
- Work in the time domain also to measure voltages

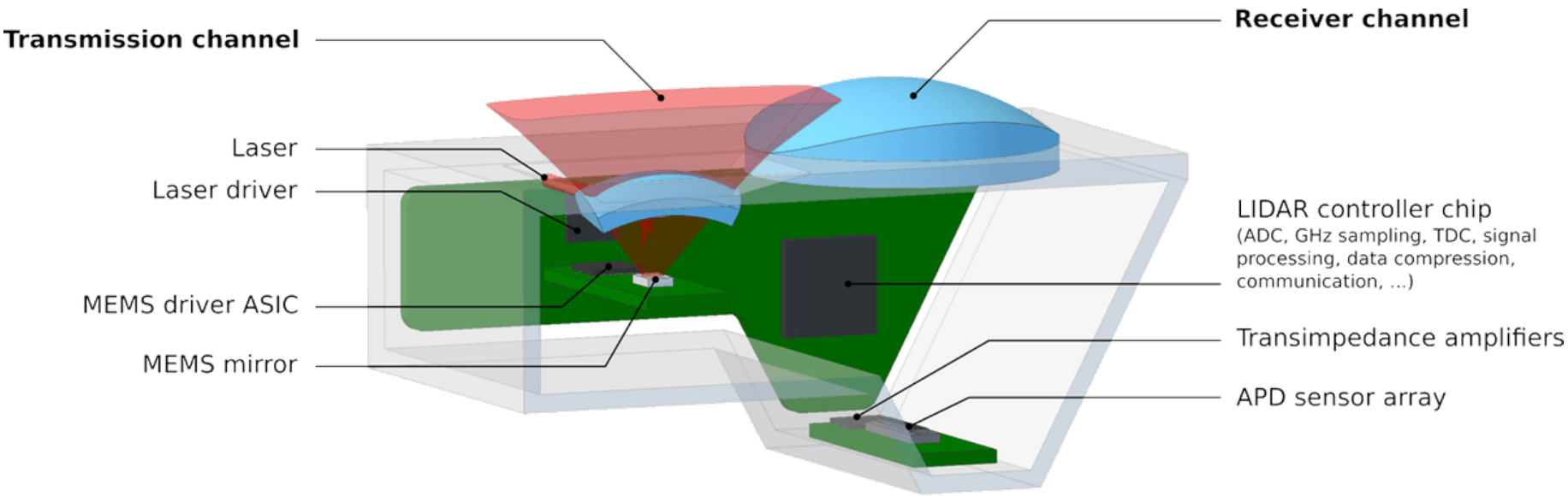




K. Otsuga et al,

IEEE International SoC Conference, 2012

LiDARs

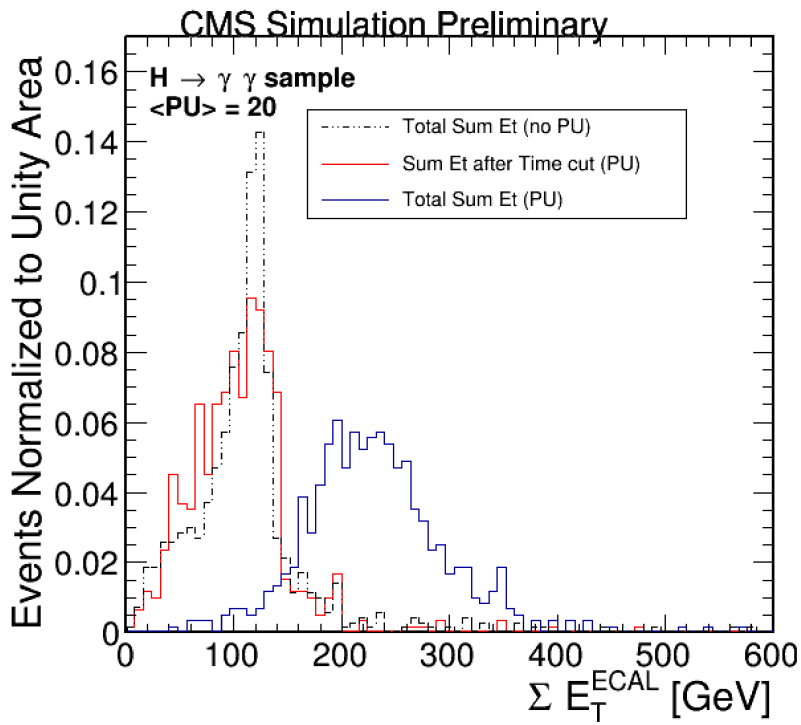


- Timing can be one key ingredient for self-driving cars

Timing with slow systems

- Calorimeters can profit from large signals to make timing is easier!

- Calorimeters already achieve quite good time resolution
- System resolution now saturates at around 100 ps
- Exact values depends on the situation considered
- Interaction region $\approx$ 6 cm
- With 30 ps resolution event origin confined to 1 cm.
- Need a 4-5x improvement with respect to today standard

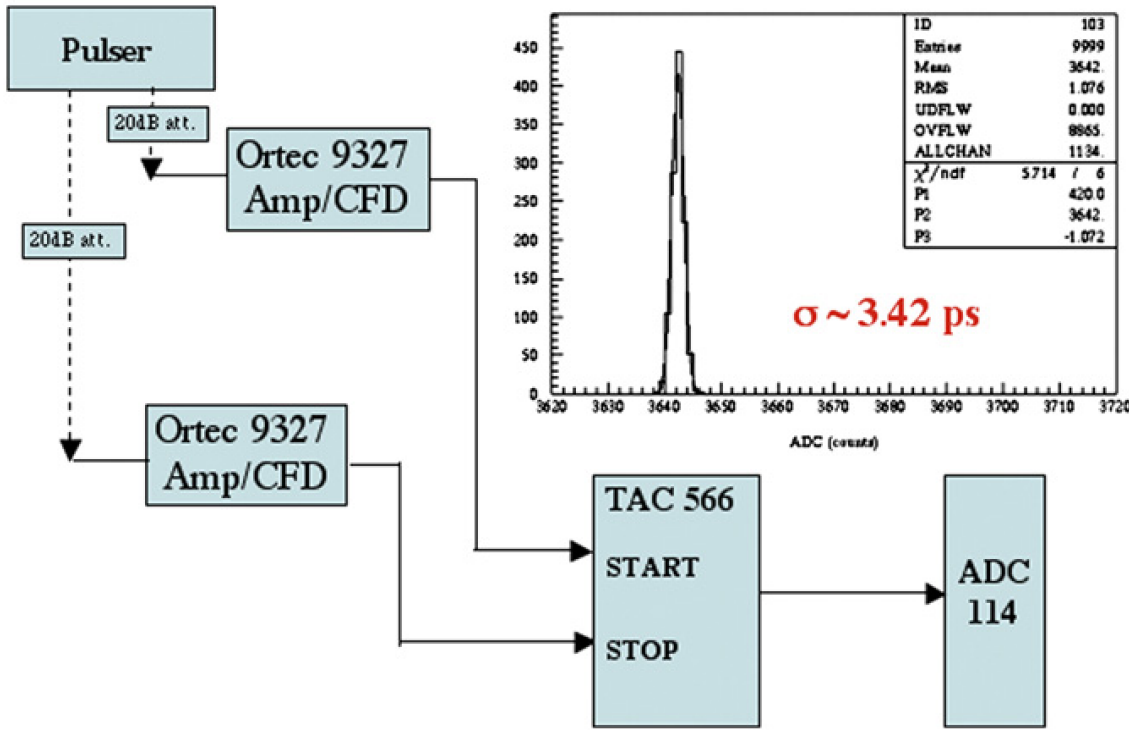


From D. Del Re, J. of Physics: Conference Series 587 (2015), doi:10.1088/1742-6596/587/1/012003

Trends in timing systems

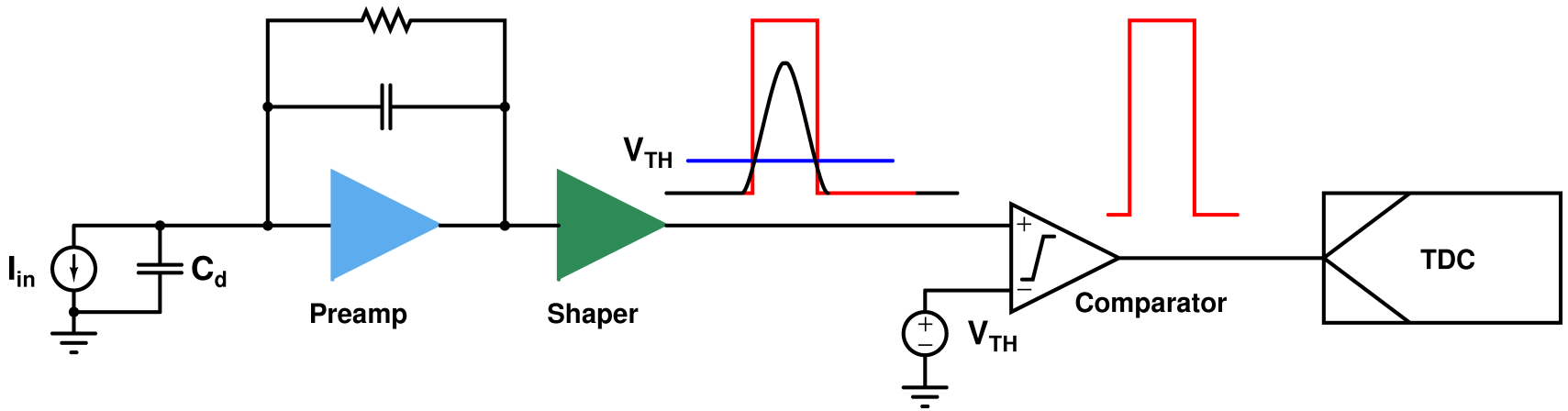
- Improve time resolution well below 100 ps (target 10 ps or less)
- Extend timing to densely packed detector systems
- Make large detector cheaper
- Need of highly integrated ASICs for timing
- Timing involves two critical processes:
  - Signal generation in the sensor
  - Signal processing in the front-end electronics

Timing from the sixties



- Electronics timing resolution is very good since a while
- The challenge is to replicate it over many channels

Architecture for timing ASICs: single sampler



- The sensor signal is usually amplified and shaped
- A comparator generates a digital pulse
- The threshold crossing time is captured and digitized by a TDC
- Time walk can be calibrate off-line or corrected online with CFD

- The key building block is a fast, compact, and low-power TDC

State-of-the-art TDC

A 9-bit, 1.08ps resolution Two-Step Time-to-Digital Converter in 65 nm CMOS for Time-Mode ADC

Junjie Kong[1,2*], Stephan Henzler[2], Doris Schmitt-Landsiedel[2], Liter Siek[1]
[1]School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore
[2]Lehrstuhl für Technische Elektronik (LTE), Technische Universität München, Germany
*Email: kong0086@e.ntu.edu.sg-mail

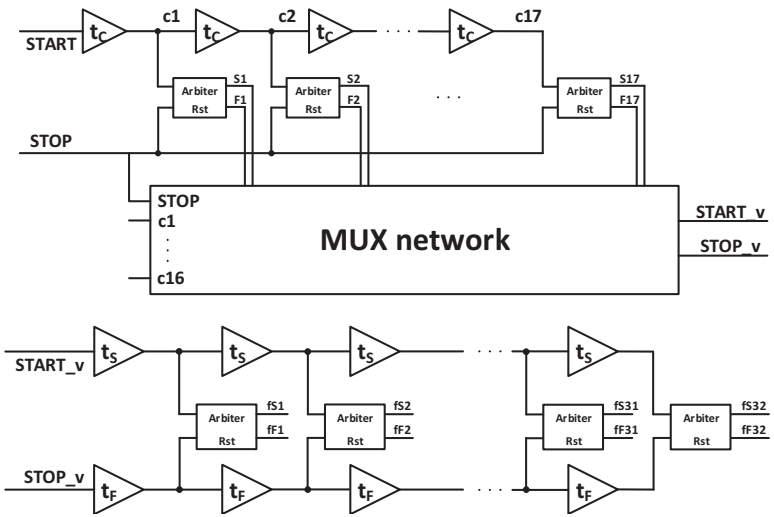


TABLE I. PERFORMANCE COMPARISON WITH OTHER ARCHITECTURES

Reference	[1]	[2]	[3]	[4]	[5]	This work
No. of bits	8	9	7	9	9	9
Resolution (ps)	2.6	1.12	3.75	1.2	1.25	1.08
f_S (MHz)	80	250	200	150	10	200
DNL (LSB)	1.84	0.6	0.9	0.67	±0.8	-0.097 / 0.2
INL (LSB)	2.36	1.7	2.3	0.62	±2	-0.12 / 0.41
Power (mW)	2	15.4	3.6	8.299	3	0.667
FoM [pJ/(con.step)]	0.0977	0.325	0.463	0.108	0.586	0.0065
Scheme	Time Amp.	Pipeline	Time Amp.	Two-step	Two-step	Two-step
Technology (nm)	65	65	65	65	90	65

978-1-5090-1570-2/16/$31.00 ©2016 IEEE

APCCAS 2016

- Ultra-high resolution TDCs designed for ADPLL or time-domain ADC
- Usually limited dynamic range, but....

State-of-the-art TDCs

- ...not so much!

A 14-Bit, 1-ps Resolution, Two-Step Ring and 2D Vernier TDC in 130nm CMOS Technology

Hechen Wang and Fa Foster Dai
Dept. of Electrical and Computer Eng., Auburn University, Auburn, AL 36849

TABLE I. TDCs PERFORMANCE COMPARISON

	VLSI 14 [7]	ISSCC 15 [8]	ISSCC 16 [9]	CICC 17 [2]	ISSCC 17 [1]	**This work**
Topology	Cyclic	Stochastic	SS-ADC	2D Vernier	SAR-ADC	**Ring+2D Vernier**
Process	28nm	14nm	65nm	45nm	14nm	**130nm**
NoB	12	10	6.1	8	7	**14**
ENoB (1)	9.74	8.28	5.76	7.58	3.68	**13.2**
Resolution	0.63ps	1.17ps	6ps	1.25ps	0.2ps	**1.0ps**
ER (2)	3.15ps	3.85ps	7.60ps	1.67ps	2ps (4)	**1.74ps**
Speed [MHz]	10	100	40	80	26	**10**
DNL [LSB]/[ps]	0.5/0.32	0.8/0.94	---/---	0.25/0.31	---/---	**0.41/0.41**
INL [LSB]/[ps]	3.8/2.39	2.3/2.7	0.27/1.6	0.34/0.4	9/1.8	**0.79/0.79**
Power [mW]	0.82	0.78	0.36	0.33	---	**2.4**
FoM (3)	0.02	0.01	0.13	0.02	---	**0.02**

1. ENoB = NoB – $\log_2$ (INL+1).
2. Effective Resolution (ER) = Resolution × $2^{(NOB - ENOB)}$.
3. FoM = Power / ($2^{NOB} \times F_S$) [pJ / conv-step].
4. calculated based on in-band phase noise. PN = $10\log(N^2(2\pi f_r)^2 t_{res}^2/12/f_r)$.

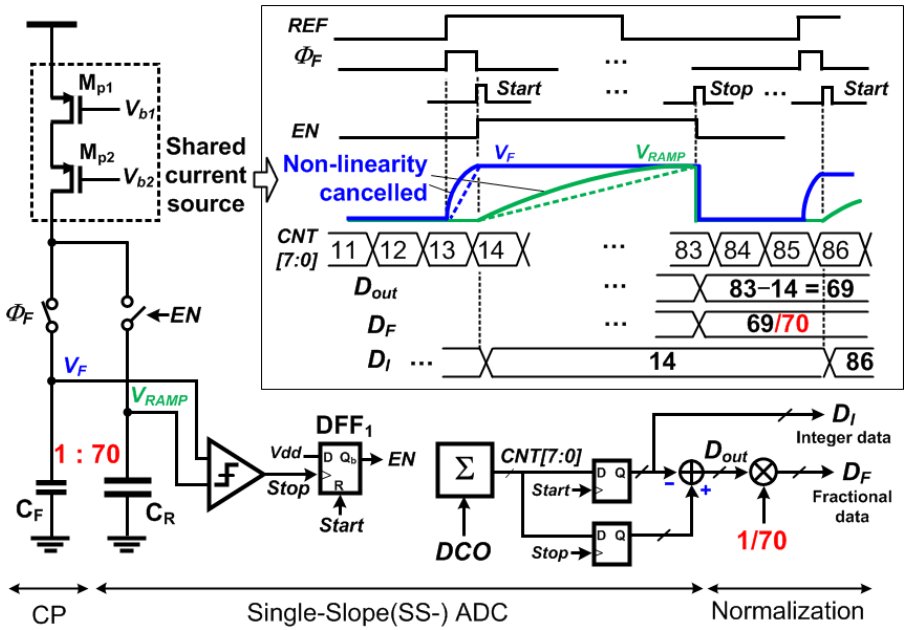
- With 1 ps and 14 bits, the reference clock can be just 60 MHz

You can still do a lot with a capacitor

19.7 A 65nm CMOS ADPLL with 360μW 1.6ps-INL SS-ADC-Based Period-Detection-Free TDC

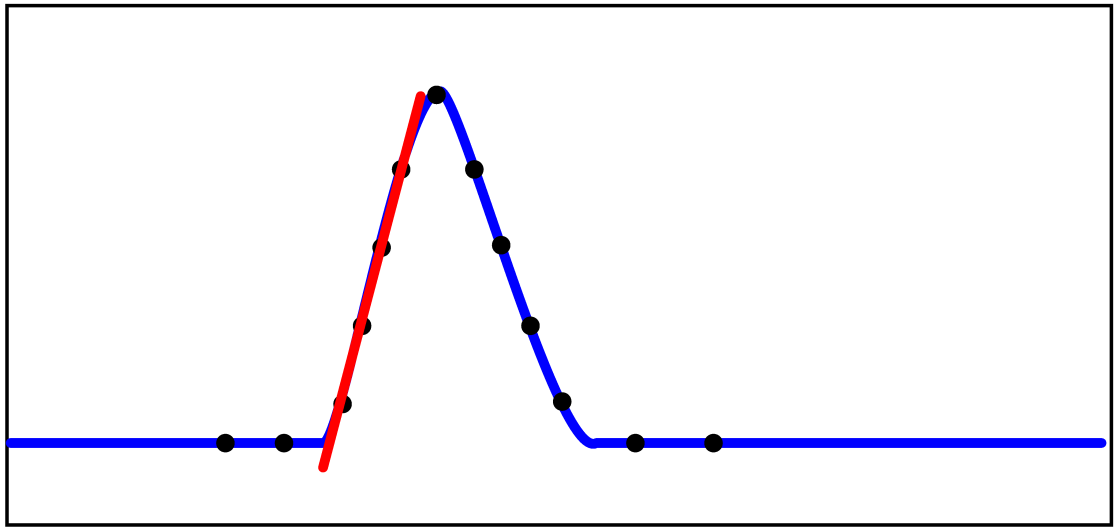
Akihide Sai, Satoshi Kondo, Tuan Thanh Ta, Hidenori Okuni, Masanori Furuta, Tetsuro Itakura

Toshiba, Kawasaki, Japan



		[3] ISSCC'10	[4] JSSC'15	[5] CICC'13	[6] ISSCC'15	This work
Architecture		VDL+DTC	TA+TDC	CP+SAR-ADC	Stochastic	CP+SS-ADC
Supply Voltage		1.2V	1.0V	1.0V	1.2V	1.2V
Technology		65 nm CMOS	65 nm CMOS	65 nm CMOS	14 nm FinFET	65 nm CMOS
Cal. Needed? (Time)		Yes (120ms)	Yes (38us)	Yes (-)	Yes (-)	No
Measurement Type		-	-	Static	Static	Dynamic
w/ ADPLL?		Yes	Yes	No	No	Yes
TDC	Sample Rate	35MS/s	50MS/s	40MS/s	100MS/s	40MS/s
	State Resolution	6.8ps 5.4bit	0.9ps 4bit	0.84ps 8bit	1.17ps 10bit	6.0ps 6.1bit
	Effective Resolution	-	-	-	-	8.9ps 5.5bit
	INL	-	1.25ps(sim)	2.3ps 2.7LSB	2.7ps 2.3LSB	1.6ps 0.27LSB
	Power	-	0.2mW (Except DTC)	2.7mW	0.78mW	0.36mW (Except CNT)
ADPLL	In-band Worst Frac. Spur	-52dBc @3kHz	-51.5dBc @392kHz	-	-	-52.6~-43dBc 2.4k~40MHz
	Ref. Spur	-	-69dBc	-	-	-66dBc
	In-band PN@2.24G	-105dBc/Hz	-112dBc/Hz	-	-	-106dBc/Hz

Architectures for timing ASICs: multiple sampler



- The sensor signal is usually amplified and shaped
- The full waveform is sampled and digitized at high speed
- In many systems, sampling and digitization are decoupled
- Timing is extracted with DSP algorithms from the digitized waveform samples

- The critical blocks are ultra-fast analog memories and compact, low-power ADCs

Timing jitter in multiple-sampling

- Sample the input signal beyond Nyquist
- Assume first-order system relationship

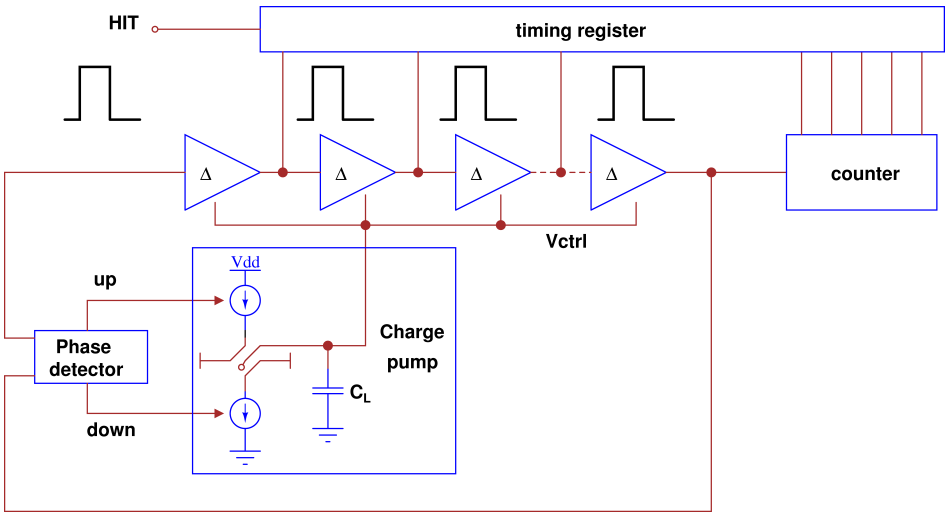
$$\sigma_t = \frac{t_r}{SNR}\frac{1}{\sqrt{N}} \qquad N = \frac{t_r}{t_s}$$

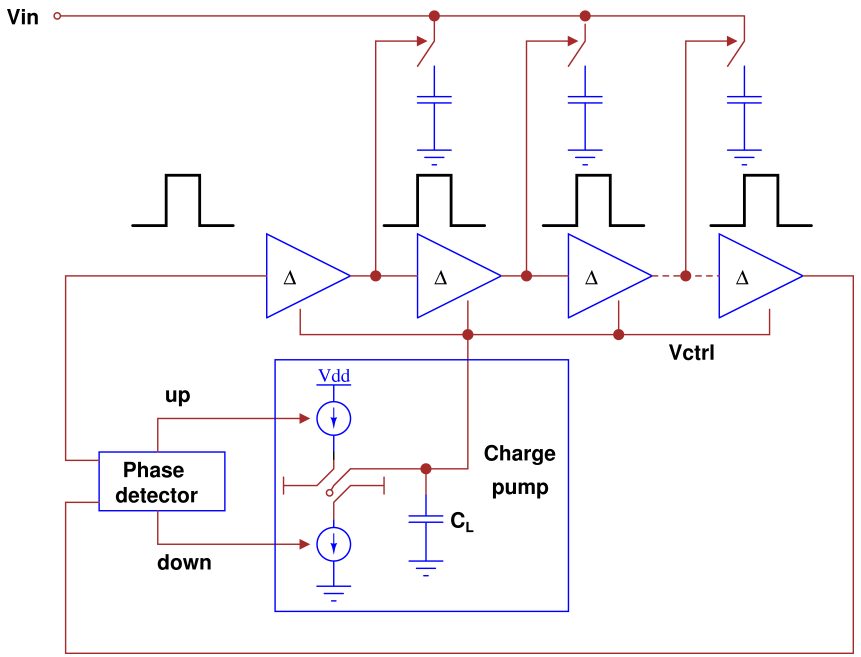
$$\sigma_t = \frac{1}{SNR}\sqrt{\frac{0.35}{BW \cdot f_s}} = \frac{1}{SNR}\frac{1}{\sqrt{3 f_{-3dB} f_s}}$$

SNR	f_s	f_{-3db}	σ_t
10	1 Gs/s	150 MHz	150 ps
10	10 Gs/s	1.5 GHz	15 ps
100	1 Gs/s	150 MHz	15 ps
1000	10 Gs/s	1.5 GHz	0.15 ps

- Redundancy is advantageous only if noise in uncorrelated
- This is a kind of ultimate limit
- The challenge is more in the SNR than in the sampling frequency

Multi-GHz sampling

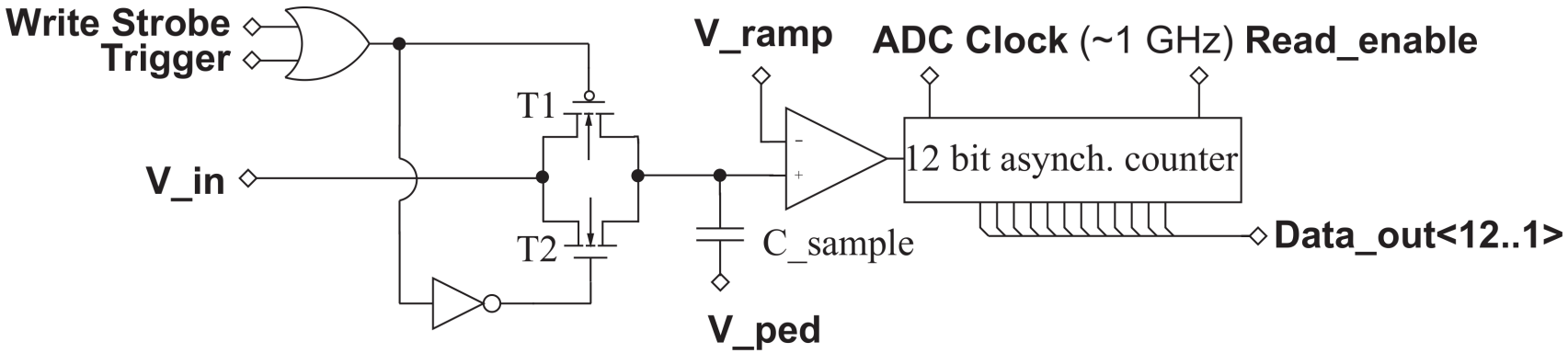




- In a TDC, the delayed pulses are captured into registers when the hit arrives
- In a WS, the delayed pulses are used to control the analog storage cells
- Sampling frequency is $1/\Delta$ and can be well above 10 GHz in modern technologies
- In earlier implementations open loop buffers were employed. Today the use of DLL and PLL prevalent (jitter and sampling time uniformity)

An example of sampling cell

E. Oberla et al., NIM A 735 (2014) 452-461

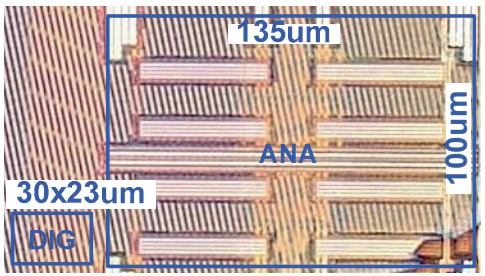


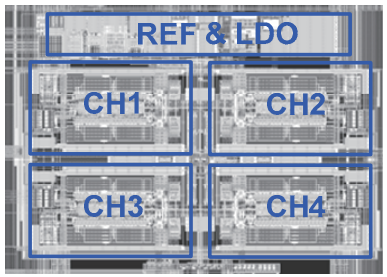
- Small sampling capacitance (20 fF) to guarantee 1.5 GHz analog bandwidth
- A Wilkinson ADC integrated in each cell
- Common ADC ramp generated externally to the cell

Full sampling with ADCs

A 0.014mm^2 10-bit 2GS/s Time-Interleaved SAR ADC with Low-Complexity Background Timing Skew Calibration

Lei Luo, Song Chen, Minchao Zhou, Tianfeng Ye
Marvell, Shanghai
lluo@marvell.com





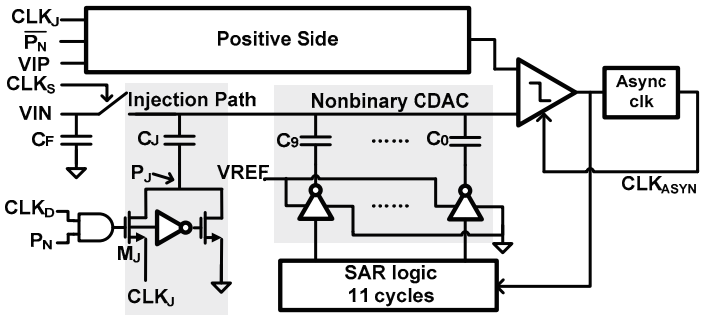


Table I Performance summary

	ISSCC 15 [5]	ISSCC 16 [7]	VLSI 16 [3]	This work
Process (nm)	45	40	16	16
Architecture	12x FATI	16x TI	4x TI	4x TI
Resolution (bit)	10	10	10	10
Speed (GS/s)	1.7	2.6	1.6	2
Skew Calibration	Ana+Dig	Dig	Dig	Ana+Dig
Input Swing (Vpp)	N/A	1.4	1	1.1
Supply (V)	1.2	1.1	0.95	0.85/1.5
Power (mW)	15.4	18.4	9.8	10.4
SNDR* (dB)	57.2/56.1	54.2/50.6	55/50.3	54.5/50.1
FOM* (fJ/c-s)	15.5/21	16.8/25.6	13.3/23	12/20
Area [mm^2]	0.36	0.825	0.023	0.014**

* low freq / Nyquist
** Include calibration digital unit

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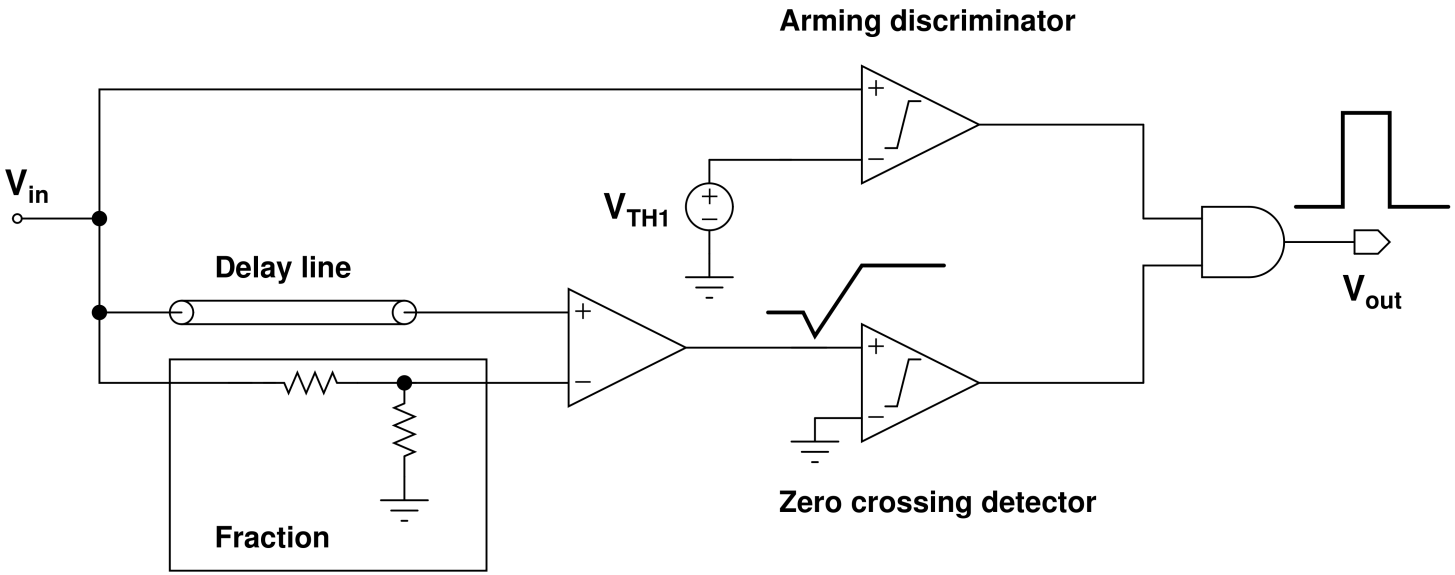
Digital timing extraction

- Different algorithms are used to compute the timing from the digitized samples
- There is nothing such an optimal method
- Some techiques can be more suited that others for real time execution on FPGA

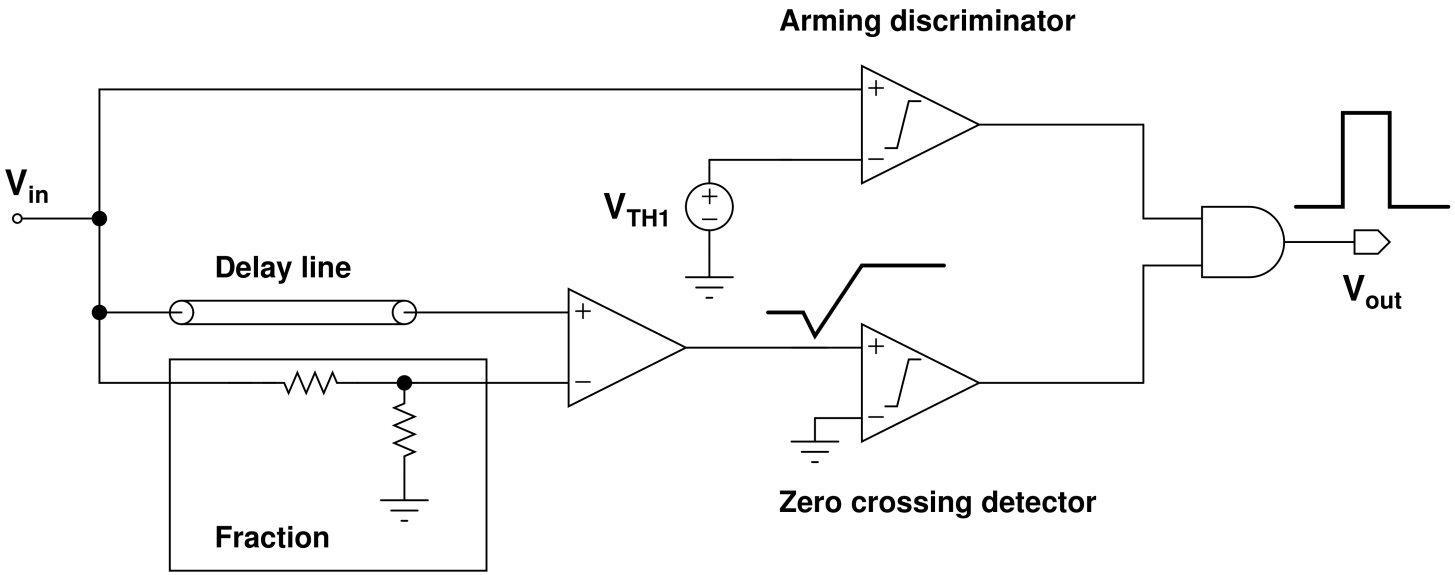
- Some examples of digital algorithm:
  - Digital leading edge
  - Digital constant fraction
  - Interpolation
  - Initial slope approximation
  - ...

To learn more: E. Delagnes, Precise Pulse Timing based on Ultra-Fast Waveform Digitizers, Lecture given at the IEEE NSS Symposium, Valencia, 2011

CFD: the principle

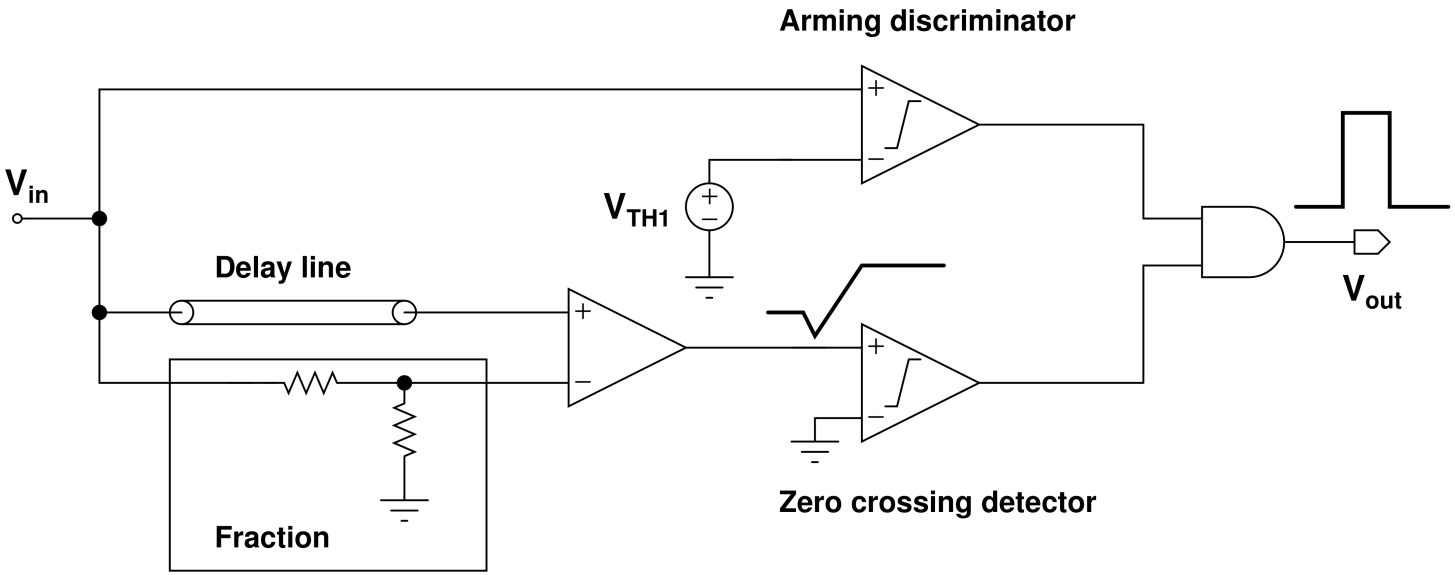


CFD: the principle



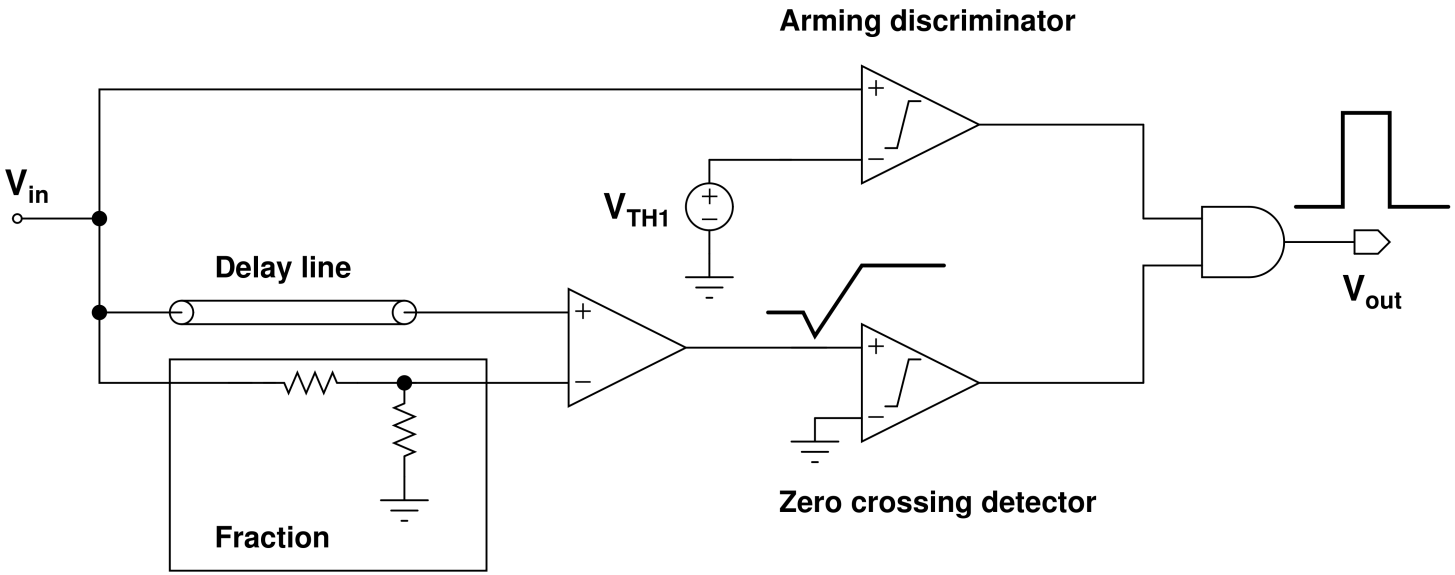
- The input signal is both delayed and attenuated

CFD: the principle



- The input signal is both delayed and attenuated
- The delayed and attenuated signals are combined to yield a bipolar waveform

CFD: the principle

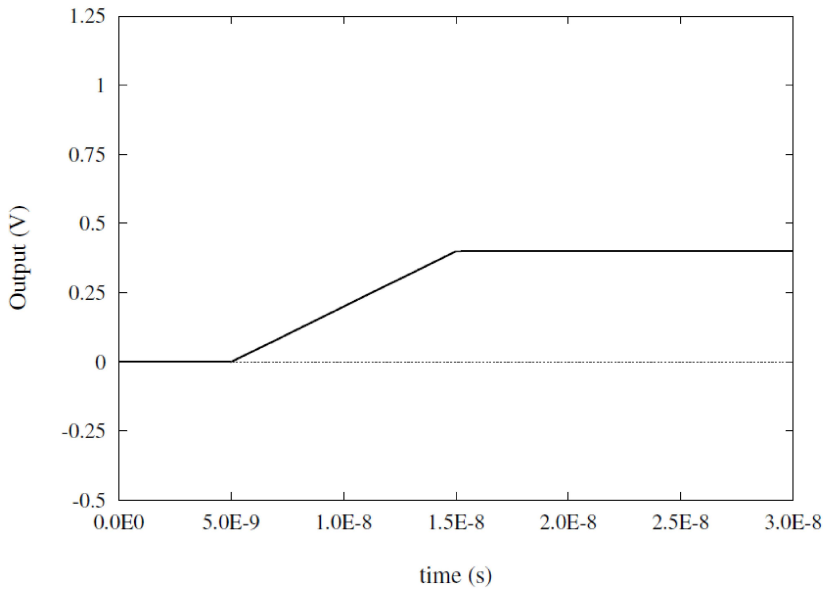


- The input signal is both delayed and attenuated
- The delayed and attenuated signals are combined to yield a bipolar waveform
- The zero crossing of the bipolar waveform is used for timing

CFD: the algorithm

Assume a step input signal:

$$V(t) = \begin{cases} 0 \text{ for } t < 0 \\ \frac{t}{t_r} V_0 \text{ for } 0 < t < t_r \\ V_0 \text{ for } t > t_r \end{cases}$$



$t_d > t_r$, amplitude compensation

$fV_0 = \frac{t-t_d}{t_r} V_0 \qquad t_{zc} = ft_r + t_d$

$t_d < t_r$, ARC compensation

$f \frac{t}{t_r} V_0 = \frac{t-t_d}{t_r} V_0 \qquad t_{zc} = \frac{t_d}{1-f}$

CFD: in practice

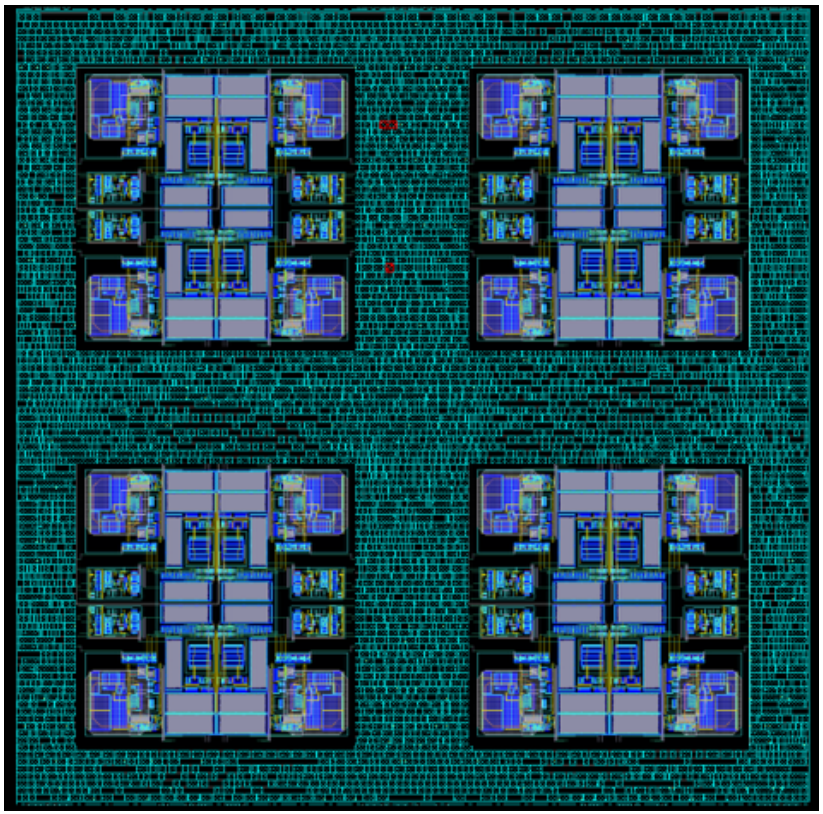
Take now simple $CR - RC$ shaping and an ideal delay line:

$$\frac{t - t_d}{\tau} e^{-\frac{t-t_d}{\tau}} - f \frac{t}{t_d} e^{-\frac{t}{\tau_d}} = 0 \rightarrow t_{zc} = \frac{t_d e^{\frac{t_d}{\tau}}}{e^{\frac{t_d}{\tau}} - f}$$

- Jitter optimization: $\tau = t_{coll} \rightarrow$ sensitivity to pulse shape fluctuations!
- Can be reduced by reducing t_d, f, or both...
- CFDs rely of fully linear signal processing
- The analog version is not trivial to implement in modern CMOS technologies due to the reduced voltage headroom, but it can be done.

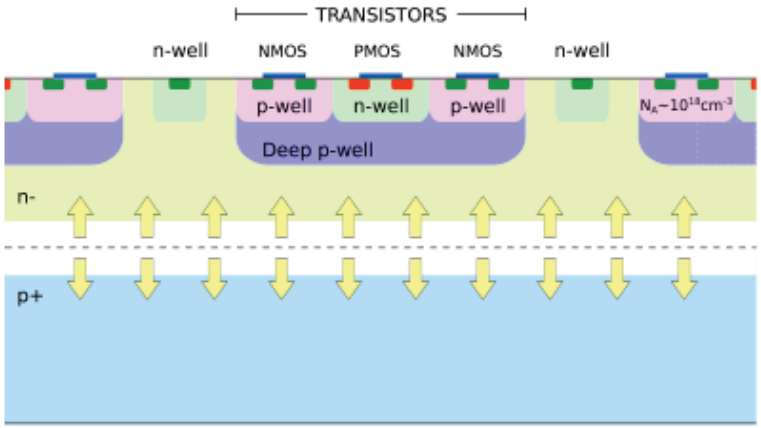
Toward 4D tracking pixels

- Need to combine traditional performance of hybrid pixels with timing

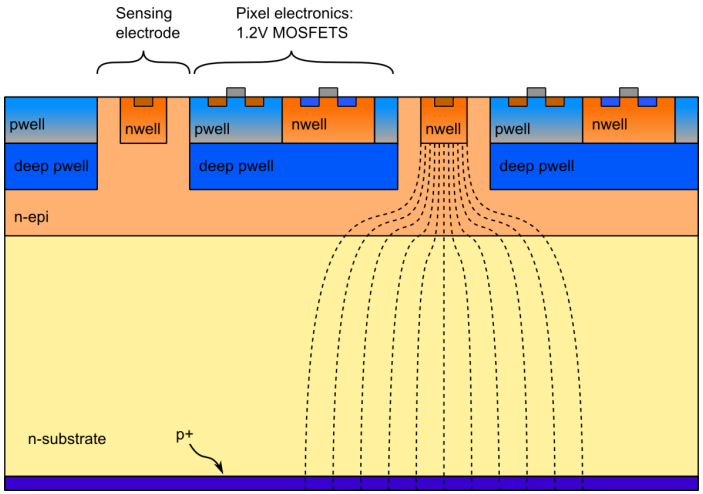


- 50 micrometer pitch
- Charge measurement for interpolation (and time-walk correction!)
- Latency buffer for trigger matching (or data queuing)
- It is matter of integration density
- Technologies beyond 65 nm probably needed
- Starting R&D in 28 nm

Timing with CMOS sensors



Investigator chip (CERN)
TJ 180 nm CMOS
Full depletion of the epitaxial layer



SEED project (INFN-LFoundry)
LF 110 nm CMOS
Back-side processing
Full bulk depletion (300 um or more)

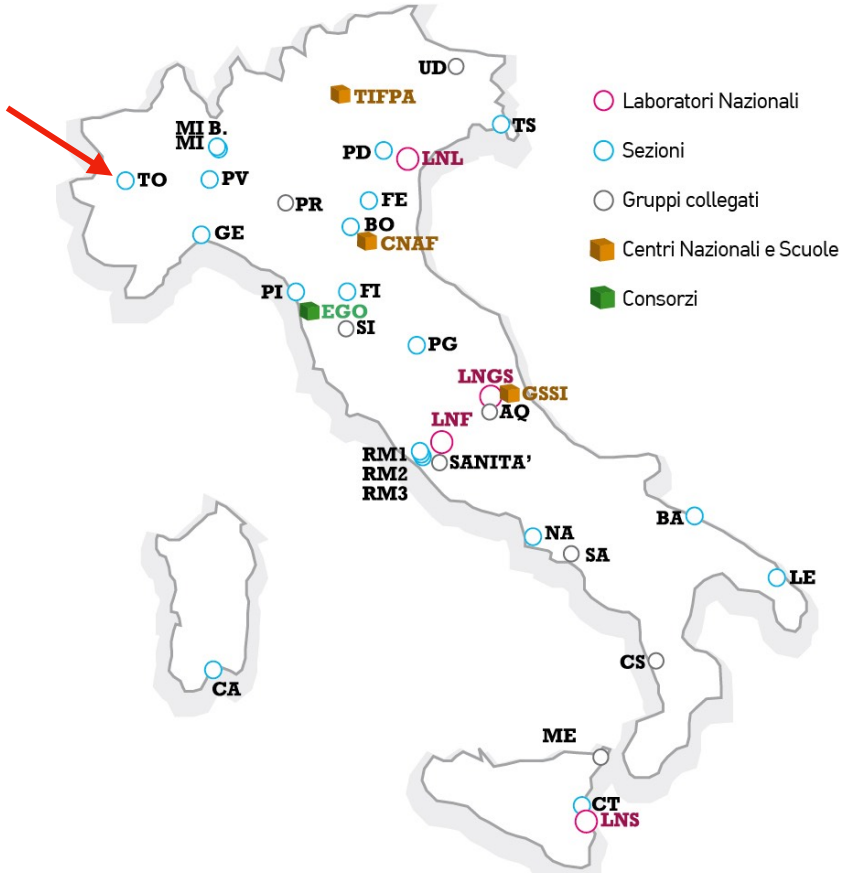
- Many effort worldwide towards fully depleted CMOS sensors
- Charge collection only by drift improves radiation hardness and charge collection time
- Low collection capacitance
- Can be very promising also for fast (and cheap) timing

To partially conclude...

- Several factors challenge the timing accuracy of a system:
  - Random noise internal to the front-end electronics (can be traded with power)
  - Random noise from external sources (e.g. clock distribution system)
  - Signal integrity (substrate noise, PSSR, etc..)
  - Pulse amplitude variations
  - Pulse shape variations

- Timing below 100 ps rms is not trivial!!
- Electronics for ps timing is (in principle) already there!
- But what about sensors?
- Sensor and front-end codesign essential to achieve best possible timing

A little bit of geography



- Founded before the Romans
- First capital of Italy

INFN in Torino

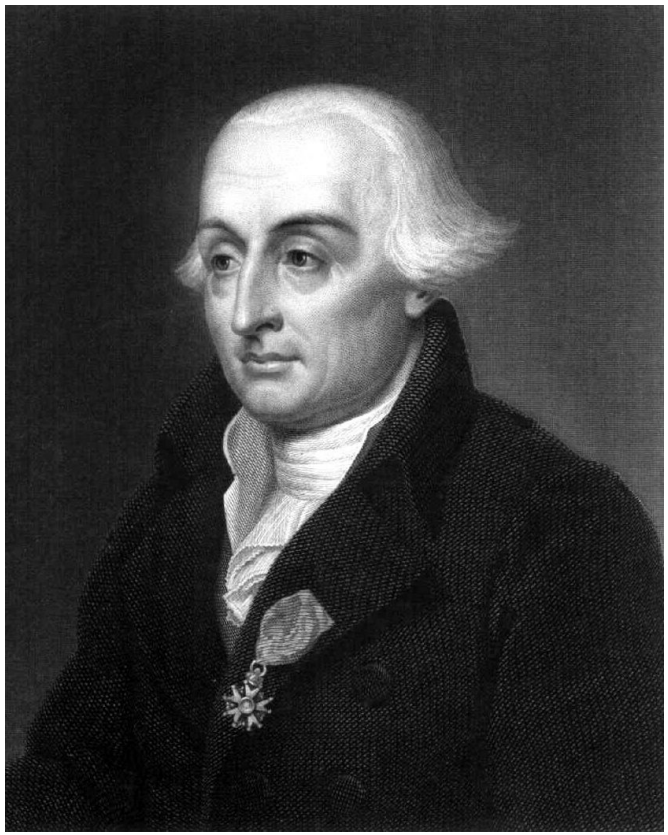
- Turin was one of the founding Section of INFN
- Today very active in all INFN scientific lines
  - particle physics
  - astroparticle physics
  - nuclear physics
  - theoretical physics
  - instrumentation development, medical physics
- Strong tradition in
  - Electronics and microelectronics
  - Computing
  - Mechanics

The ASIC design group

- The group is part of our electronics lab (14 permanent staff member)
- ASIC, FPGA, PCB design, integration...
- ASIC folks
  - 4 design engineers + 1 test engineer
  - 3 technicians
  - 15 students
  - dedicated PhD program with the local engineering school (Politecnico di Torino)
- Activities
  - Design of mixed-signal front-end ASICs
  - From the idea to the system integration and follow-up
  - In stand-alone or in cooperation with other partners
  - Both R&D and system design

Some guys from Torino (not from the ASIC group...)

- Giuseppe Lodovico Lagrangia (1736 - 1813)



- Lorenzo Carlo Amedeo Romano Avogadro (1776-1856)

Other highlights of the city...

...and its surroundings

To really conclude

- Welcome to Torino...

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- Welcome to Torino...
- Have a very productive workshop...

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- Welcome to Torino...
- Have a very productive workshop...
- ...but properly adjust your timing to enjoy also the city!