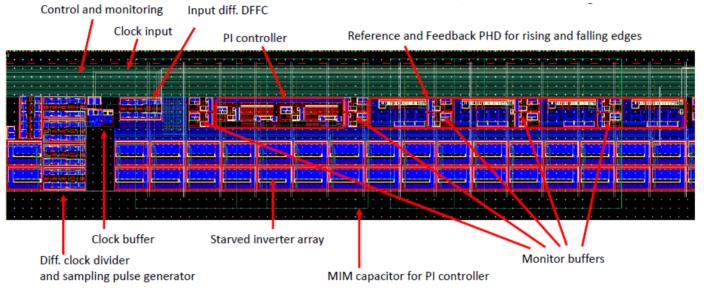
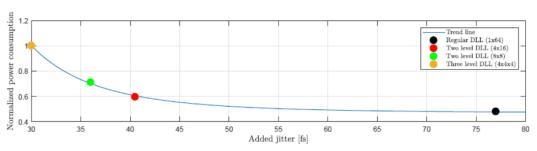
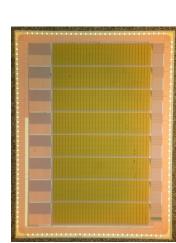
Waveform Sampling Readout – Lessons from the 10's of ps Belle II TOP and toward the fs regime







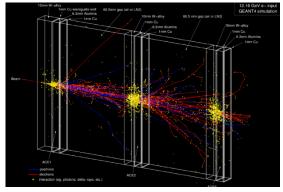
Peter Orel and Gary S. Varner
University of Hawai'i
psTiming WS, Torino June 2018

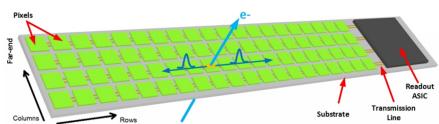


Outline

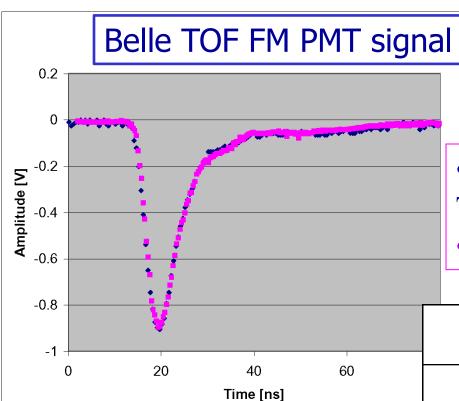
- Belle II Time Of Propagation
 [10's of ps]
 - Highly integrated
 - First collisions
- ACE Calorimeter [few ps]
 - RF prompt component
 - Extension of techniques
- Strawman Timing Vertexer [100's fs]
 - 1. Explore space-time limit
 - 2. High precision timing (latest)
 - 3. Higher density







An Easily understood Starting Point





- 2 GSa/s, 1GHz ABW Tektronics Scope
- 2.56 GSa/s LAB

"oscilloscope on a chip"

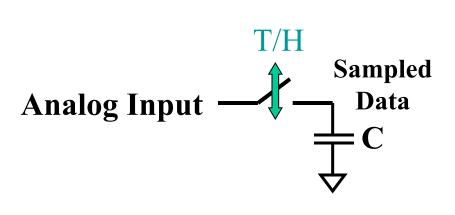


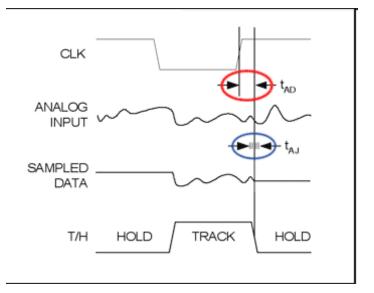


	WFS ASIC	Commercial
Sampling speed	0.1-6 GSa/s	2 GSa/s
Bits/ENOBs	16/9-13+	8/7.4
Power/Chan.	<= 0.05W	Few W
Cost/Ch.	< \$10 (vol)	> 100\$

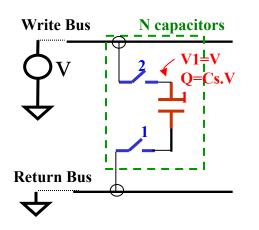
Underlying Technology

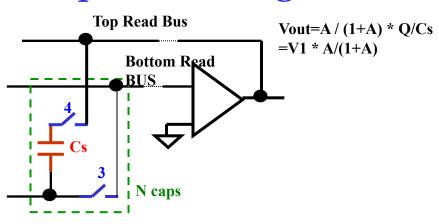
• Track and Hold (T/H)



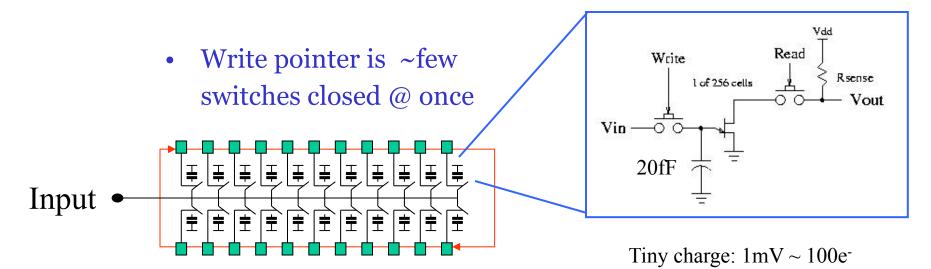


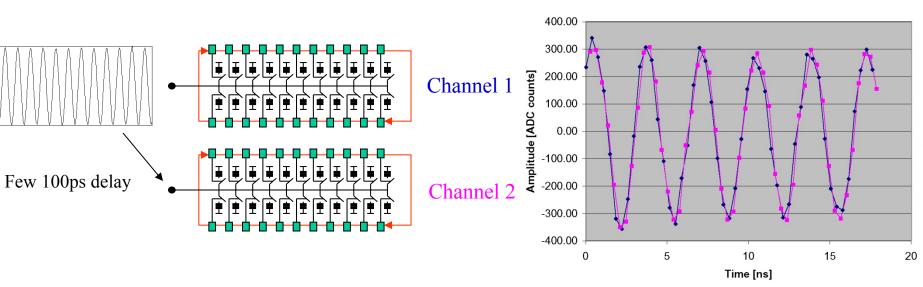
 Pipelined storage = array of T/H elements, with output buffering





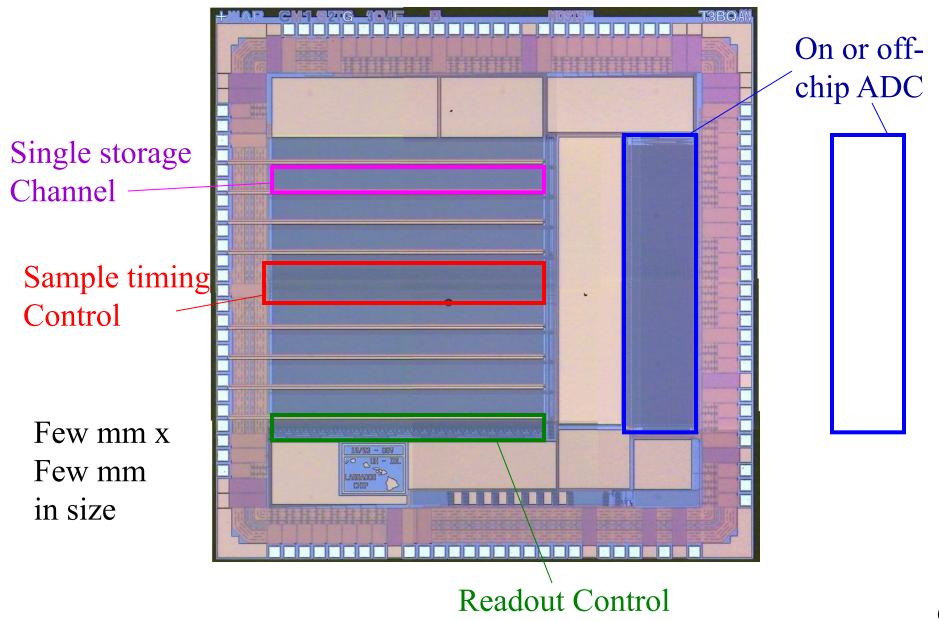
Switched Capacitor Array Sampling





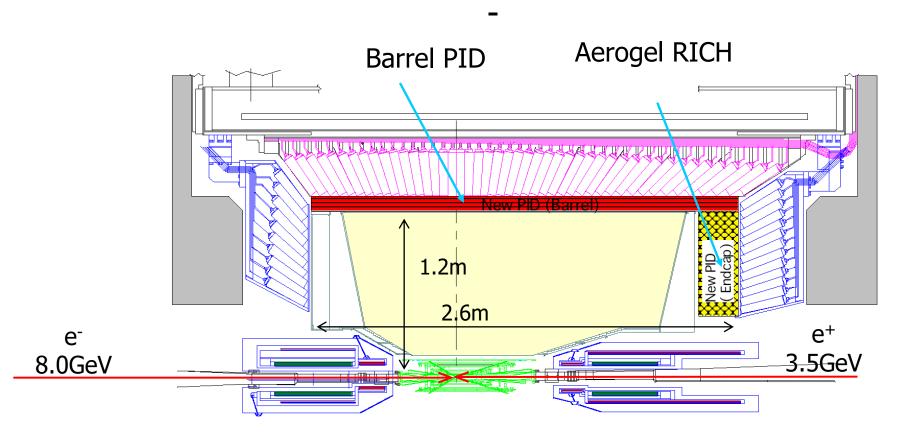
300MHz RF Sine [50mV amplitude]

Basic Functional components



A specific example: Upgraded Belle detector

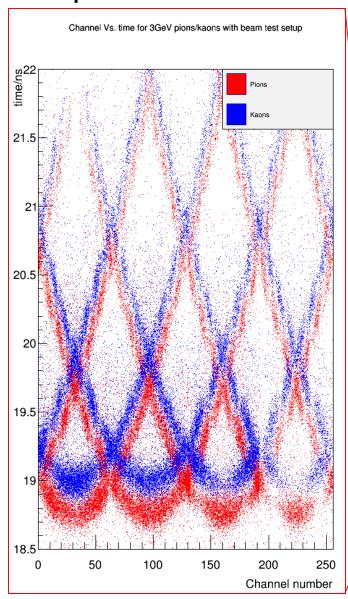
- PID (π/K) detectors
- Inside current calorimeter
- Use less material and allow more tracking volume
 - → Available geometry defines form factor

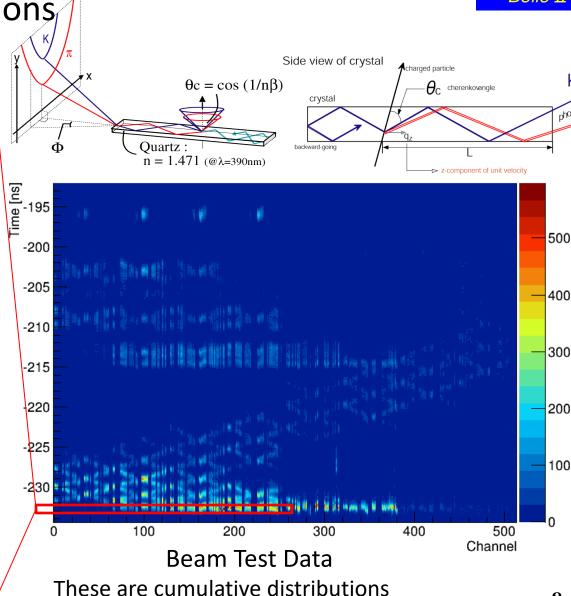


iTOP relativistic velocity



Space-time correlations/



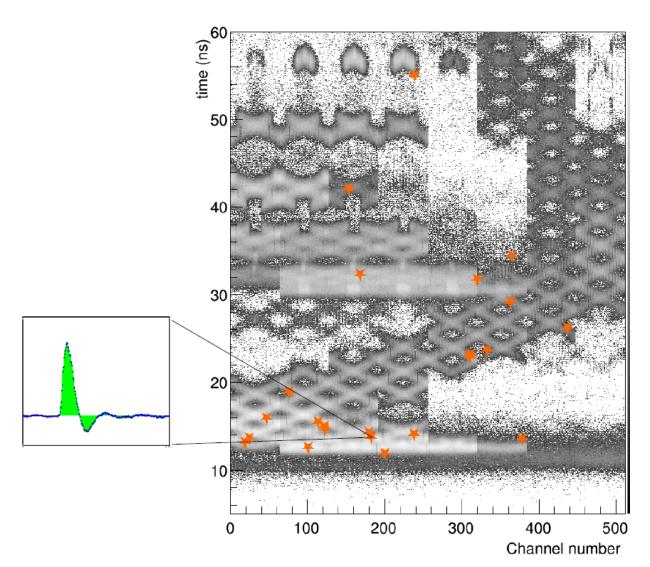


Actual PID is event-by-event



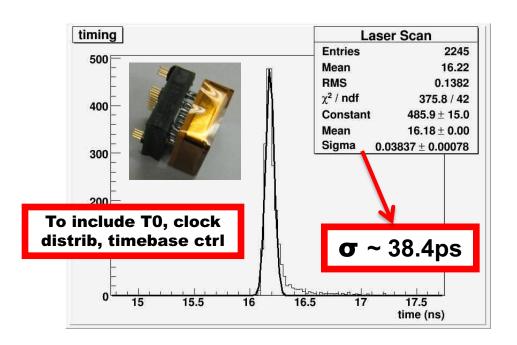
Test most probable distribution

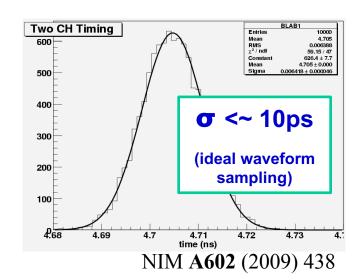
Beamtest Experiment 2 Run 568 Event 1

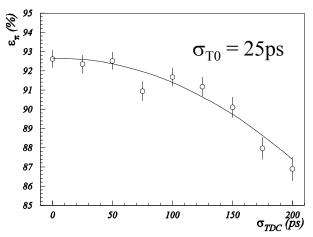


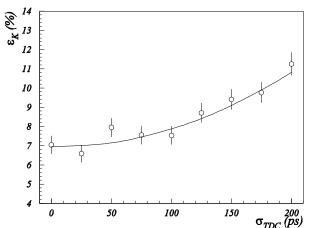
Single photon detection for TOP

Single photon timing for MCP-PMTs







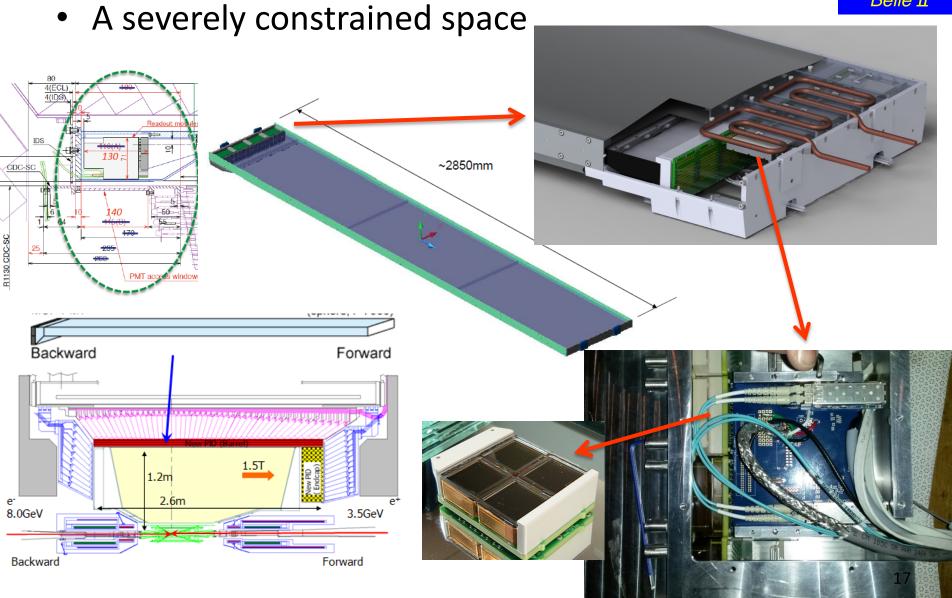


σ <~ 50ps target

NOTE: this is singlephoton timing, <u>not</u> event start-time " T_0 "

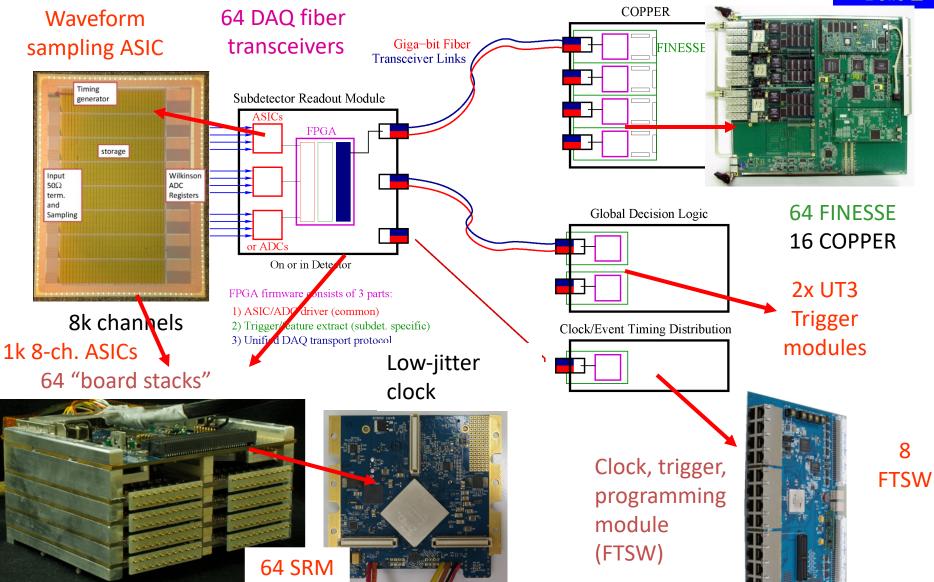
Highly integrated services





imaging TOP Readout (FDIRC proto)

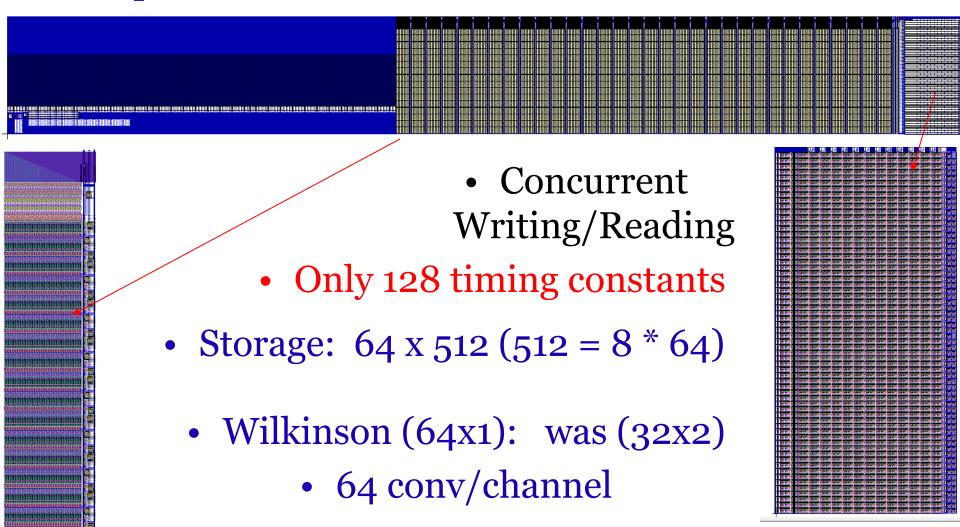




IRSX Single Channel

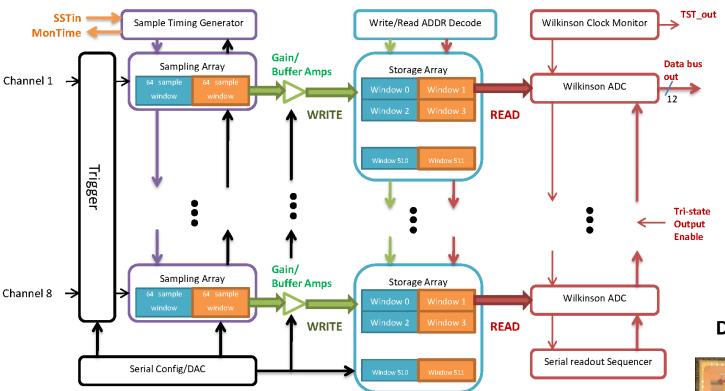
• Sampling: 128 (2x 64) separate transfer lanes

Recording in one set 64, transferring other ("ping-pong")



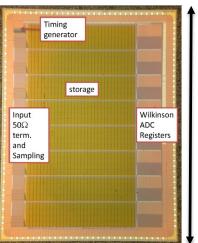
IRSX ASIC Overview





Die Photograph

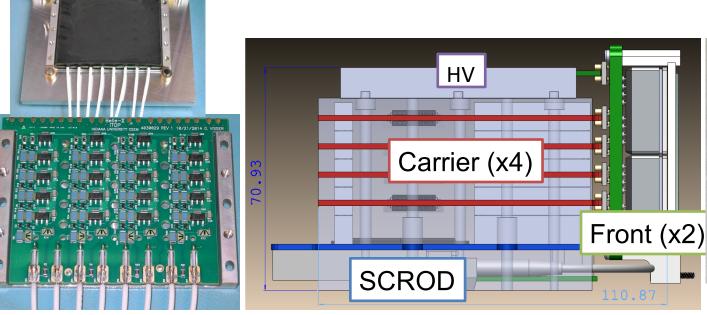
- 8 channels per chip @ 2.8 GSa/s
- Samples stored, 12-bit digitized in groups of 64
- 32k samples per channel (11.6us at 2.8GSa/s)
- Compact ASICs implementation:
 - Trigger comparator and thresholding on chip
 - On chip ADC
 - Multi-hit buffering

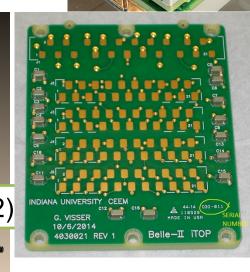


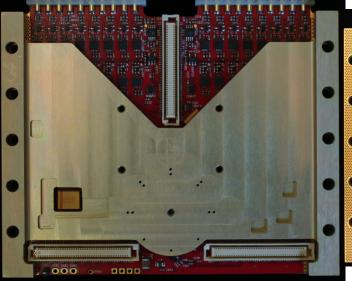
8mm

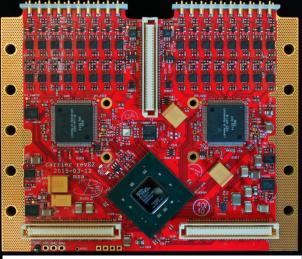
iTOP Readout "boardstack"

(1 of 4 per TOP Module)







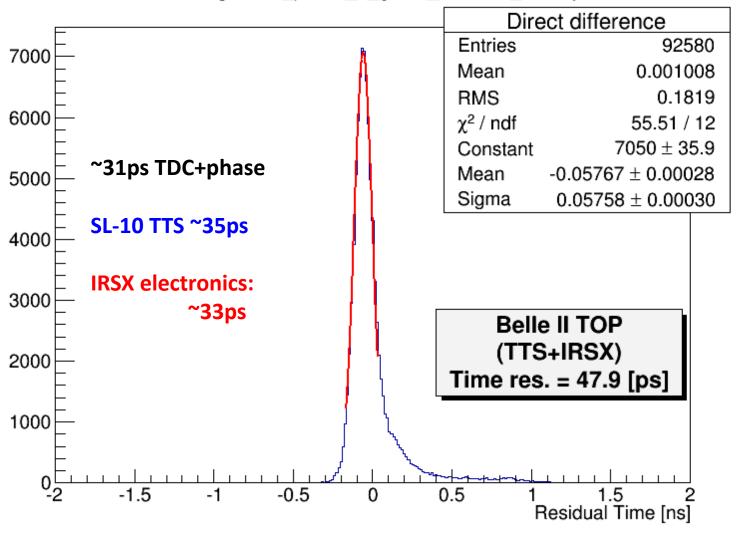




Production single photon testing

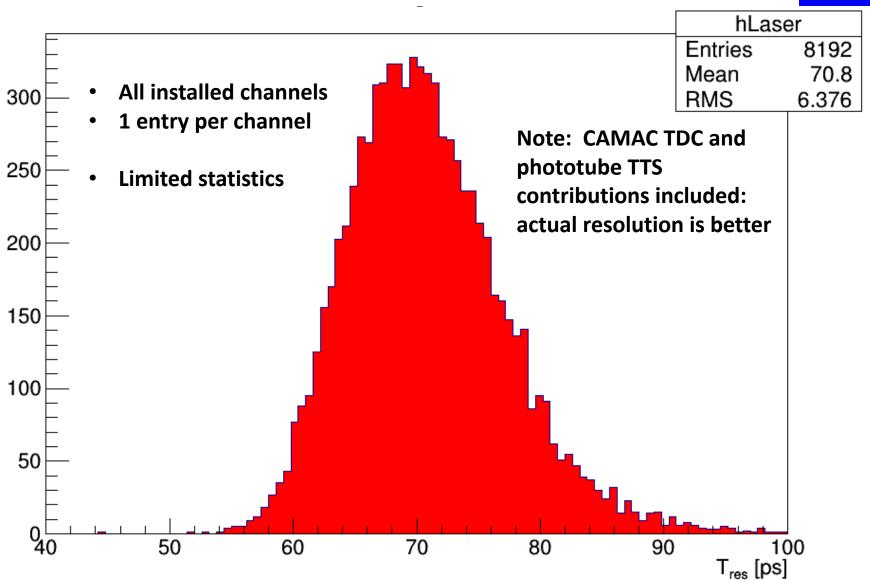


Laser timing: laser_pixel3_0_gain4_HV3201_18may2015



Production – initial single photon timing

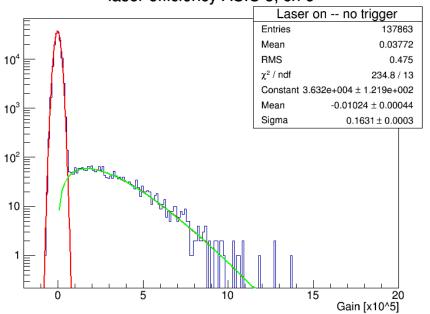


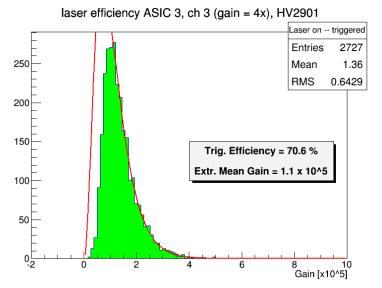


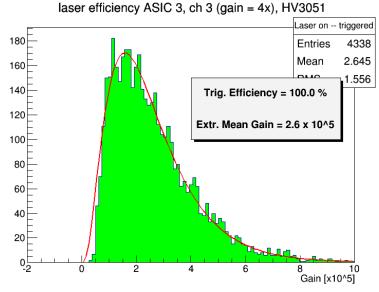
If single photon, why bother?

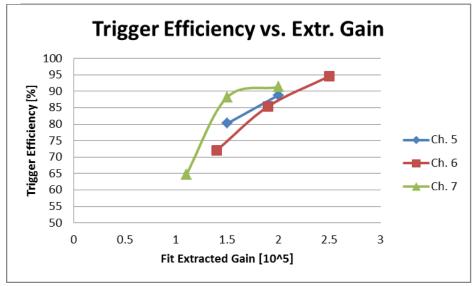


laser efficiency ASIC 3, ch 6





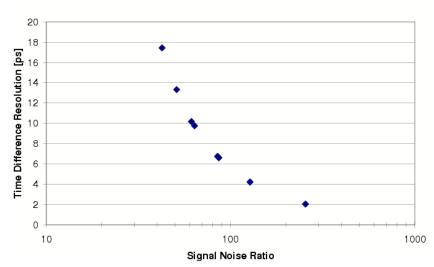




Technology has room to improve

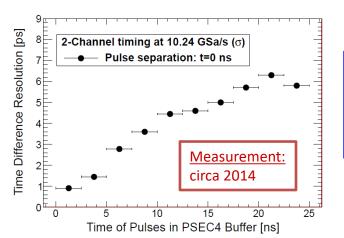
1GHz analog bandwidth, 5GSa/s

Time Difference Dependence on Signal-Noise Ratio (SNR)

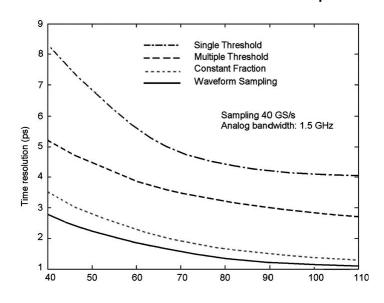


G. Varner and L. Ruckman NIM A**602 (2009) 438-445**.

E. Oberla, J-F Genat, H. Grabas, H. Frisch, K. Nishimura, G. Varner NIM A**735 (2014) 452-461**.



Simulation includes detector response



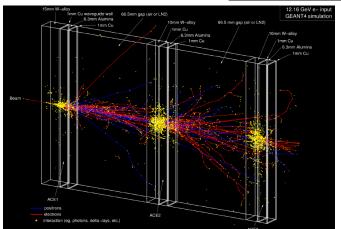
J-F Genat, G. Varner, F. Tang, H. Frisch NIM A**607 (2009) 387-393**.

Extending to 1ps and lower, with advanced calibration techniques

A very different kind of Calorimeter

Askaryan Calorimeter Exp (ACE)

matching transition, low-noise amplifiers Induced microwave Tungsten Cherenkov Prepulse shower block Beam/shower Additional tungsten Alumina-loaded WR51 Waveguides Shorted end (causes reflection)

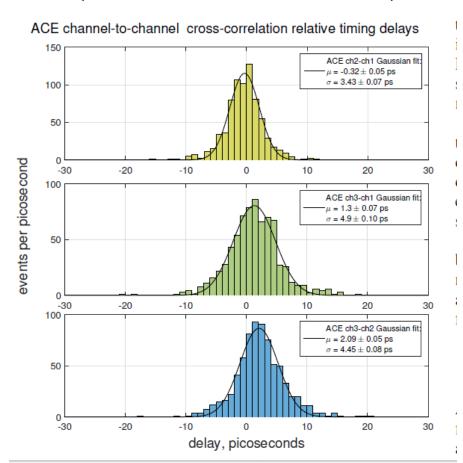


Radio (mm wave)

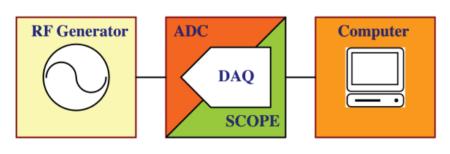
arXiv:1708:01798

2.3ps intrinsic timing resolution

(SLAC ESTB measurement)

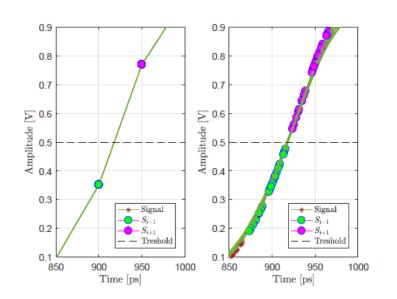


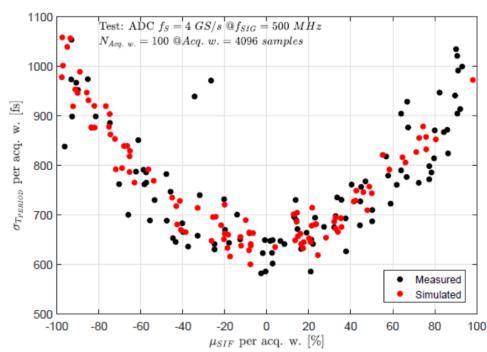
Understanding waveform sampling limits



DAQ	f_{SIG}	Measured $\sigma_{T_{PER}}$	Simulated $\sigma_{T_{PER}}$
SCO1	3 GHz	1.78 ps	2.96 ps
SCO1	6 GHz	2.28 ps	3.03 ps
SCO2	3 GHz	1.38 ps	1.42 ps
SCO2	4 GHz	1.68 ps	1.58 ps
SCO3*	400 MHz	5.68 ps	5.86 ps
SCO3*	500 MHz	4.27 ps	5.75 ps

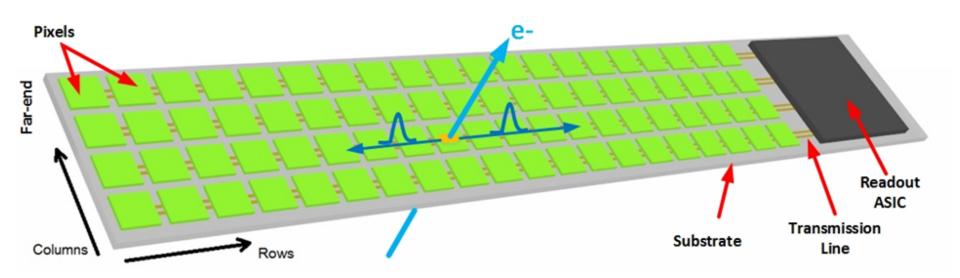
 $^{^*}$ Signal amplitude equal to 0.475 Vpp.





Detailed simulation model developed to allow exploration of phase space – first need to verify results

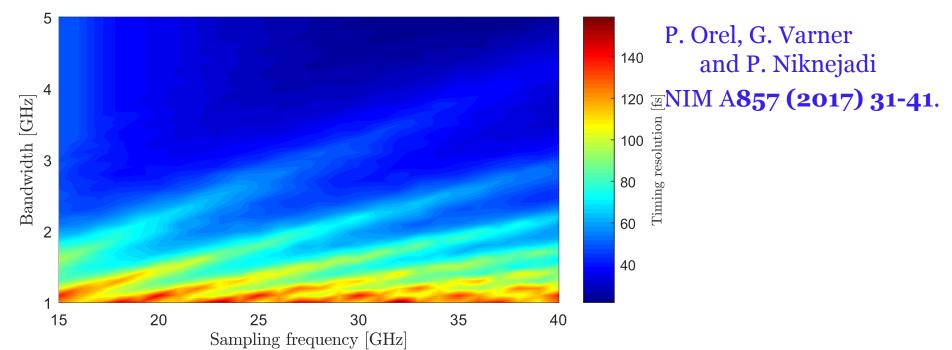
What would it take?



- Micron spatial pixel resolution (using timing)
- → Fast timing brings many benefits:
 - Minimal pile-up (fast clearing)
 - ➤ Improved event timing (direct T0 for TOF/TOP measurements)

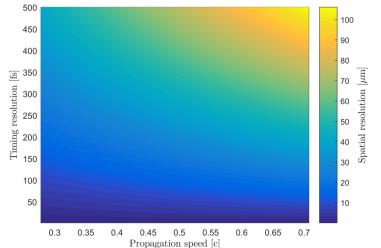
Pushing to the femtosecond regime

Pushing sampling speed and analog bandwidth



And pushing the **space-time limit**(new type of PID or DIRC devices?)

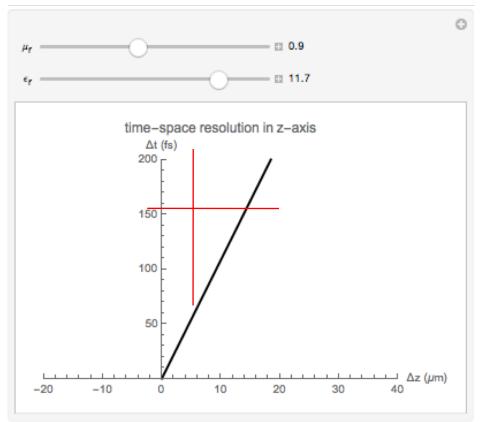
P. Orel and G. Varner
IEEE Trans. Nucl. Sci. **64 (2017) 1950-1962**.

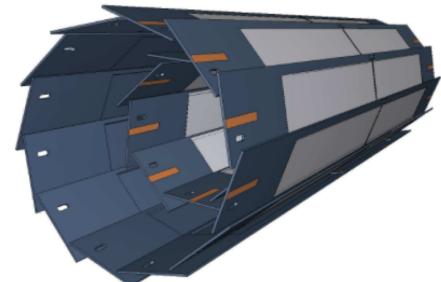


Exploration of the space-time limit

- -Sampling at high sampling rate and high bandwidth
- -Resolve small distances

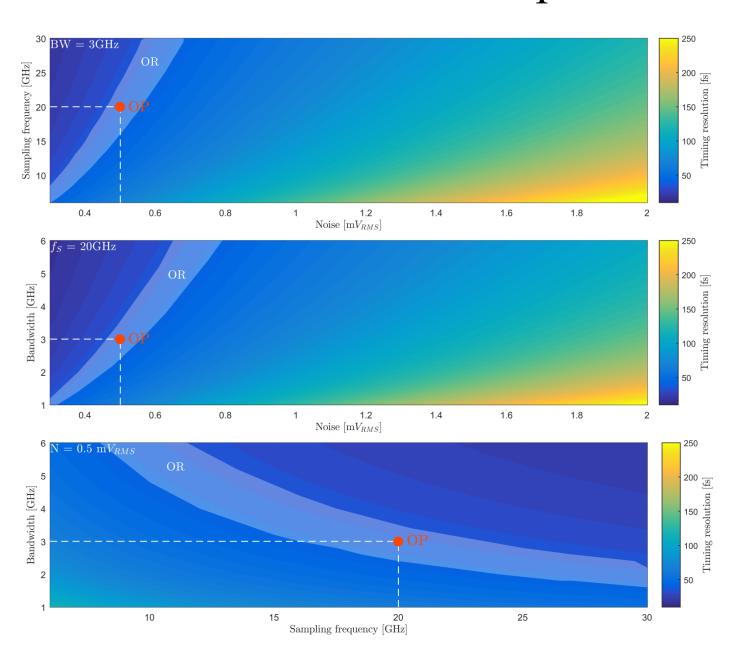
Current Goals: Spatial resolution of 10μm in z and 20μm in rφ
In Silicon 10μm in z corresponds to timing resolution of about 100fs
20μm in rφ will depend on the SNR





Pixel detector (PDX) at SuperKEKB

Performance Parameter Space



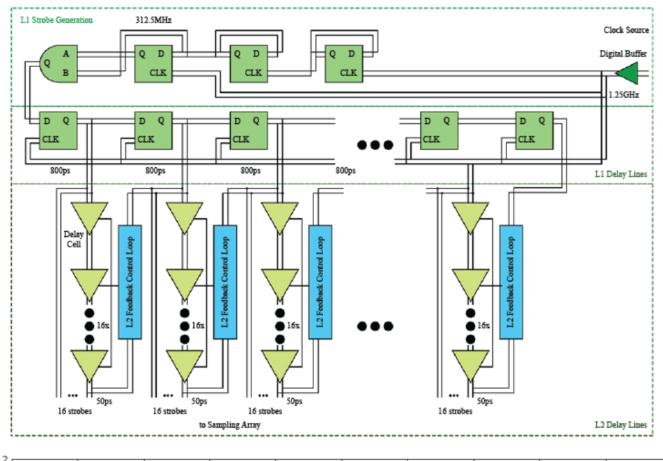
Target Specifications

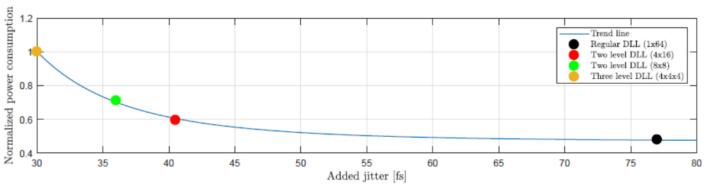
Parameter	Minimum desired value	
Sampling frequency (ASIC)	20 GHz	
Bandwidth (Detector and ASIC)	3 GHz	
Signal to Noise Ratio (Detector and ASIC)	58dB (V _{signal} =1 Volt)	
Velocity of Propagation (Transmission Line/ strip line)	0.35c	
Number of Bits of Resolution	9.4 bit	

This is an ongoing study – update Completed as P. Orel PhD Thesis

Getting to < 200fs very challenging, but device with <=1ps (independent of aperture) interesting

Example of a critical component





sampling pulse generation, clock divider (differential) sampling array CH2 DLL input transmission line (layer 8) sampling array CH1 wires from sampling cell to storage cell storage array CH1 space for storage array timing and control storage array CH2

RFpix1 ASIC Design Status

Key Design components verified

Work still needed on the digital control/address decoding

Parameter	$Desired\ value$	$Simulated\ value$
Sampling period	50~ps @20~GS/s	50~ps~@20~GS/s
Analog bandwidth ^a	$\approx 3~GHz$	$\approx 3.56~GHz$
Input referred noise ^b	$\leq 0.5~mV_{RMS}$	$\approx 1.05 \ mV_{RMS}$
Added jitter per channel	$\approx 40 \ fs$	$\approx 29 \ fs$
ENOB ^c	≥ 10	≈ 9.6
Power consumption per channel ^b	40 mA	41.71~mA

^a The simulated value is the tracking bandwidth of the SCA.

^b The simulated value does not take into account the input buffer.

^c The simulated value does not take into account distortion.

Summary

Numerous ASICs have been developed and evolving toward exquisite timing performance

Optical Cherenkov:

- > 10's of ps resolution
- > Low power, high density

• RF impulse:

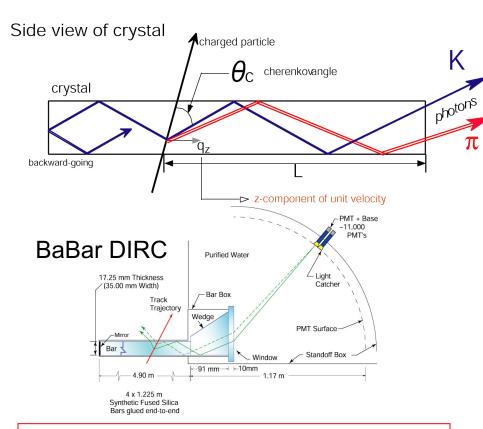
- > Single ps
- > At reach of existing devices

Toward the space-time limit:

- > Spatial extent of electronics at 100's fs level
- > Detailed engineering, but nothing fundamental

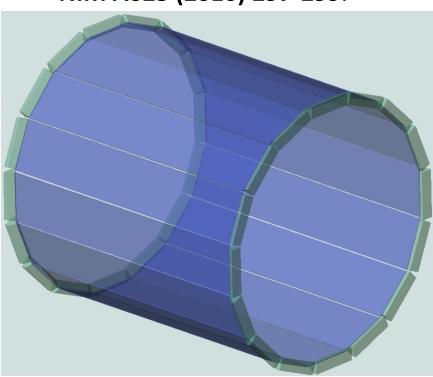
imaging TOP (iTOP)

Concept: Use best of both TOP (timing) and DIRC while fit in Belle PID envelope



Use wide bars like proposed TOP counter

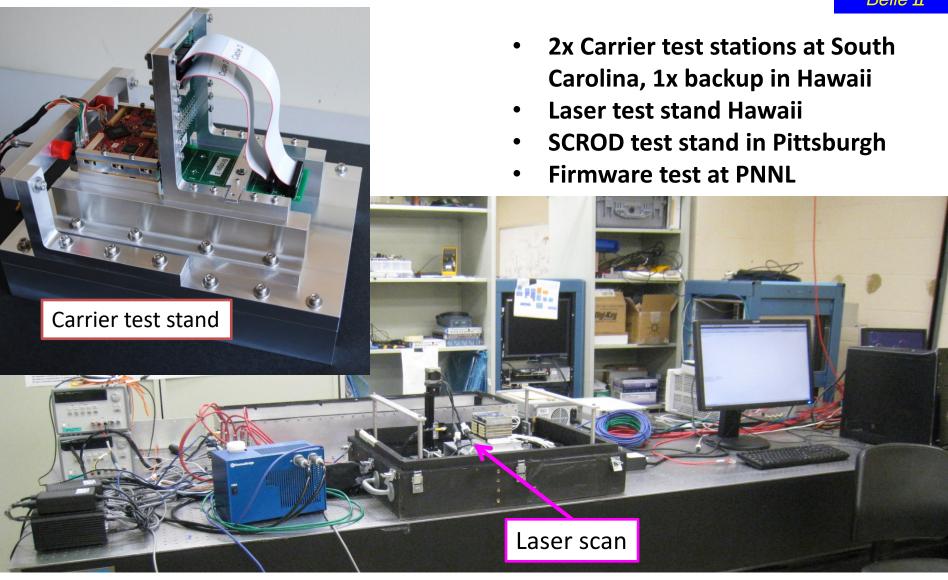
NIM A623 (2010) 297-299.



- Use new, high-performance MCP-PMTs for sub-50ps single p.e. TTS
- Use simultaneous T, θ c [measured-predicted] for maximum K/ π separation
- Optimize pixel size

iTOP Readout Production Testing





Laser timing calibration/alignment

- To synchronize the channels within a single module, we flash them with a pico-second laser pulse through optical fibers.
- The system has been developed by Italian group (Padova/Torino)

