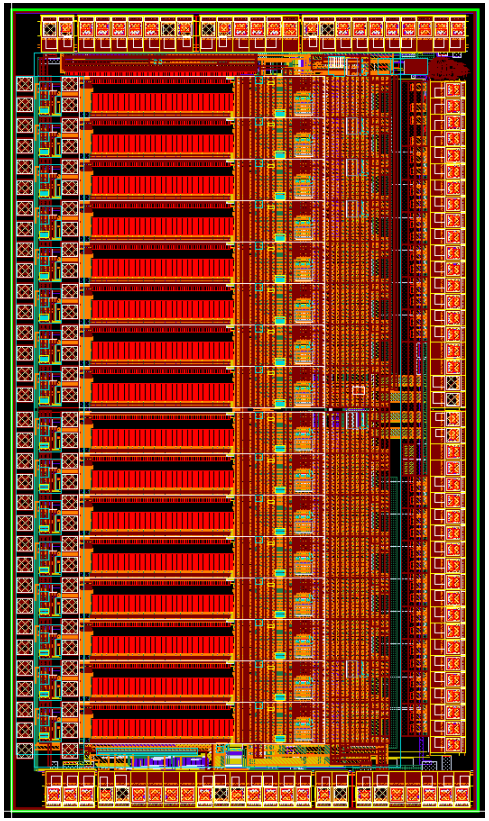

LATEST RESULTS FROM SAMPIC

D. Breton[2], E. Delagnes[1], H. Grabas[1,3], O. Lemaire[2], J. Maalmi[2], P. Rusquart[2], P. Vallerand[2]

[1] CEA/IRFU Saclay (France)
[2] CNRS/IN2P3/LAL Orsay (France)
[3] Now with SCICPP Santa Cruz (USA)

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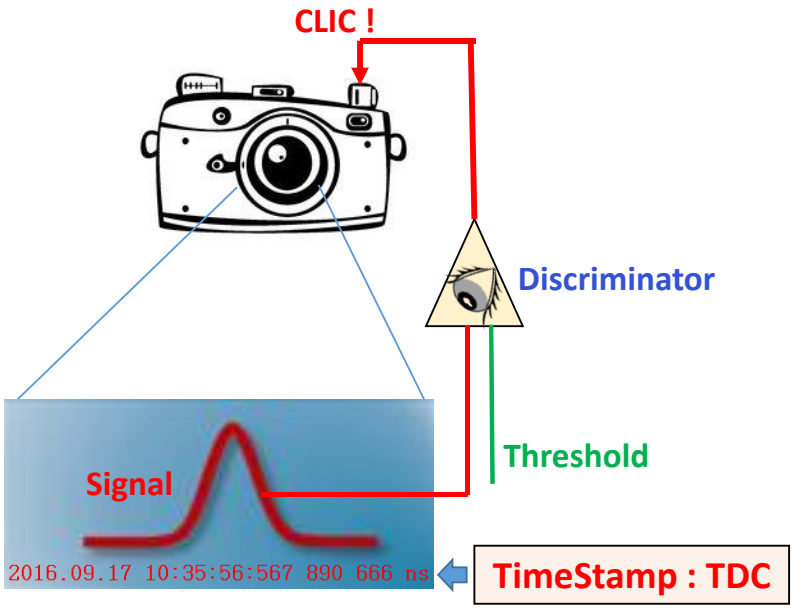
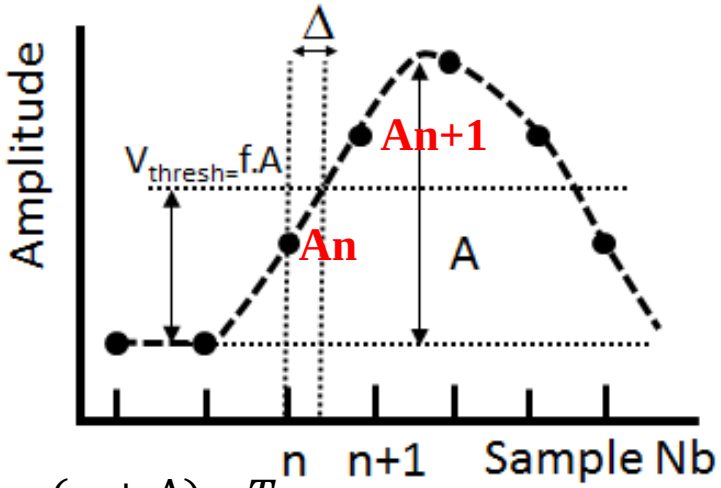
The ***TICAL*** ERC project (grant number 338953 from EU; PI: Paul Lecoq) has also contributed to the developments of the TOT features integrated in the chip

The « Waveform TDC » Concept (WTDC)

WTDC: a TDC which also permits taking a picture of the real signal. This is done via sampling and digitizing only the interesting part of the signal.

Based on the digitized samples, making use of interpolation by a digital algorithm, fine time information will be extracted.





$$t_0 = (n + \Delta) * T_s$$

with $\Delta = \frac{f*A - A_n}{A_{n+1} - A_n}$

- **Advantages:**
  - Time resolution ~ few ps
  - No “time walk” effect
  - Possibility to extract other signal features: charge, amplitude…
  - Reduced dead-time…
- **But:**
  - waveform conversion (200 ns to 1.6 µs) and readout times don’t permit counting rates as high as with a classical TDC

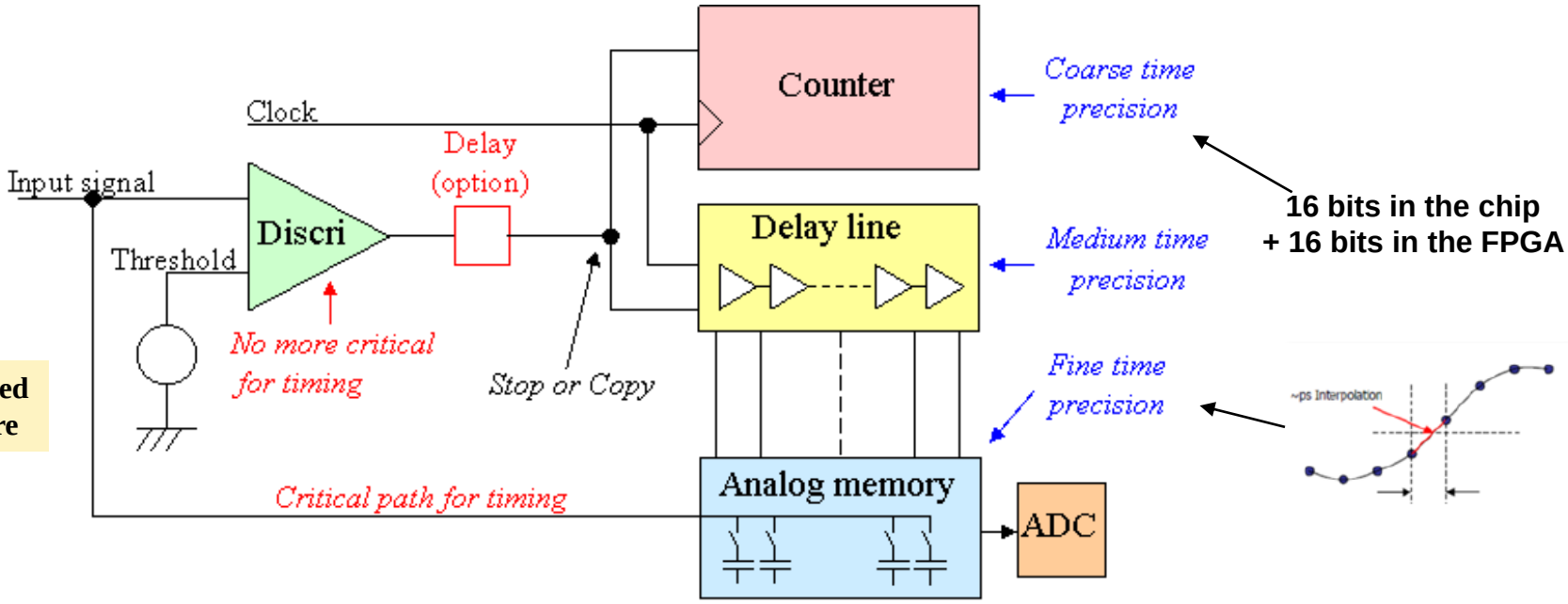
THE « WAVEFORM TDC » STRUCTURE

- **Mix of DLL-based TDC and of analog-memory based Waveform Digitizer**

- The TDC gives the time of the samples and the samples give the final time precision after **interpolation** => **resolution of a few ps rms**

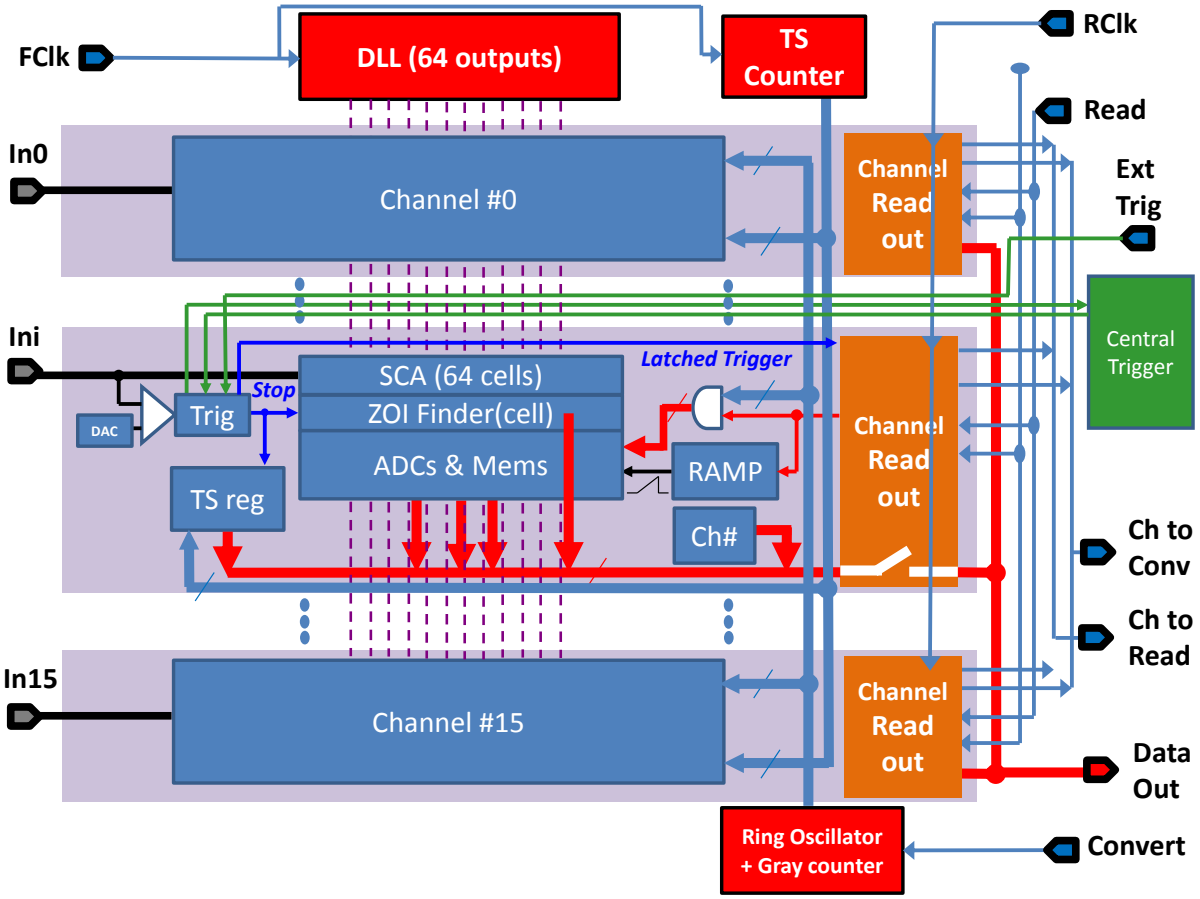
- **Digitized waveform gives access to signal shape…**

- **Conversely to TDC, discriminator is used only for triggering, not for timing**



© Patented Structure

Global architecture of SAMPIC



- **One Common 16-bit Gray Counter** (FClk up to 160MHz) for **Coarse Time Stamping (TS)**.

- **One Common servo-controlled DLL**: (from 0.8 to 10.2 GS/s) used **for medium precision timing & analog sampling**

- **16 independent WTDC channels each with :**
  - ✓**1 discriminator for self triggering**
  - ✓**Registers to store the timestamps**
  - ✓**64-cell deep SCA analog memory**
  - ✓**One 11-bit ADC/ cell**

  (Total : 64 x 16 = 1024 on-chip ADCs)

- **One** common 1.3 GHz oscillator + counter used as timebase for all the **Wilkinson A to D converters**.

- **Read-Out interface: 12-bit LVDS bus running at > 160 MHz (> 2 Gbits/s)**
- **SPI Link** for Slow Control

A LITTLE BIT OF HISTORY

- **SAMPIC_V0 submitted in February 2013. First test in July 2013.**

  ➔validated the concept but a few bugs were found. PhD of H. Grabas

- **SAMPIC_V1: V0 + bugs fixed, improved memory cell. Submitted in November 2014.**

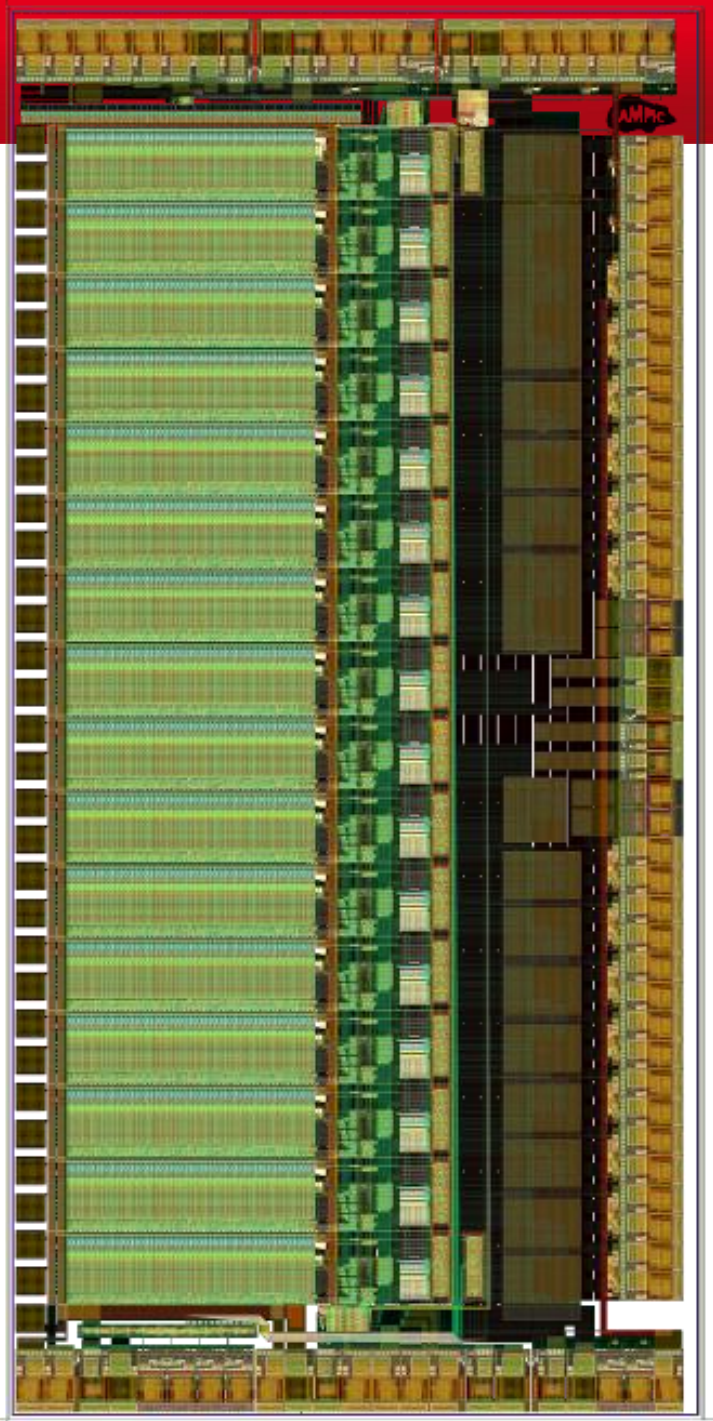
  ➔ It was considered as releasable to users end of 2015.

  ➔This was the baseline version used by different teams (CEA, CERN, Univ of Kansas, CMS/TOTEM, ATLAS, SHiP, PANDA, …) for their test benches or detectors (PMTs, MCPPMTs, APDs, SiPMs, fast Silicon Detectors, Diamonds, …)

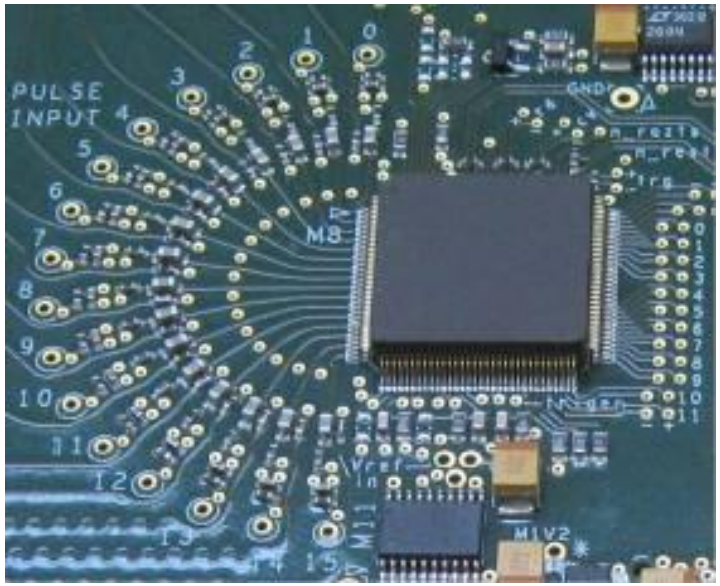
- **A lot of feedback concerning the chip, the module and the software => most important was to improve the system integration aspects (rather than concentrate on the already good time resolution).**

- **We thus mostly worked since on performing many improvements on digital blocks (ASIC & FPGA) and software.**

SAMPIC_V1

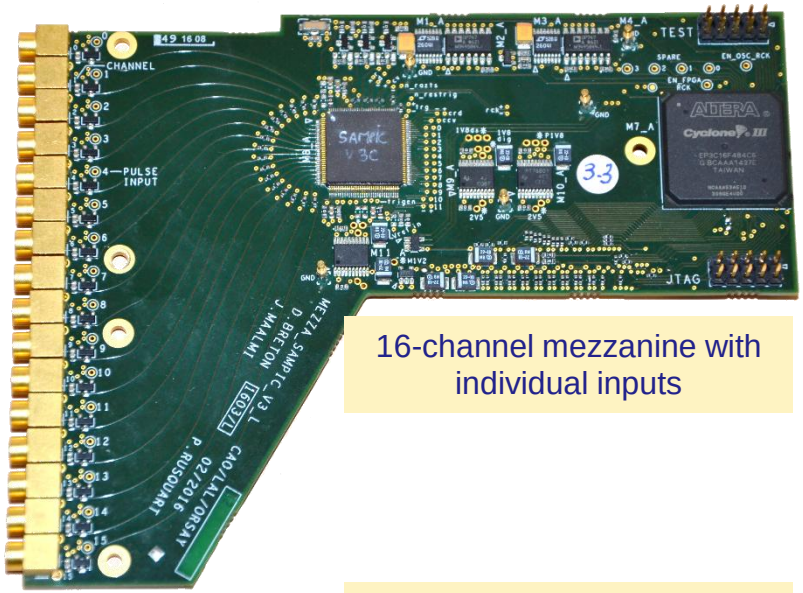


- Technology: **AMS CMOS 180nm**
- Surface: 8 mm^2
- Package: QFP 128 pins, pitch of 0.4mm



SAMPIC MODULE & DAQ SETUP

- First module developed is a 32-channel module integrating 2 mezzanines
- This mezzanine has a “L” shape permitting the injection of 16 channels via individual MCX connectors
- 1 SAMPIC/mezzanine



16-channel mezzanine with individual inputs

- The motherboard is a multi-purpose standard board developed at LAL with USB2 & Gbit Ethernet UDP (RJ45 & Optical)
- 32 channels => 3 layers of boards

32-channel module

- Triggers are tagged by a counter and the information is added to the hit events

=> permits synchronization with other systems

- A two-level trigger has been implemented

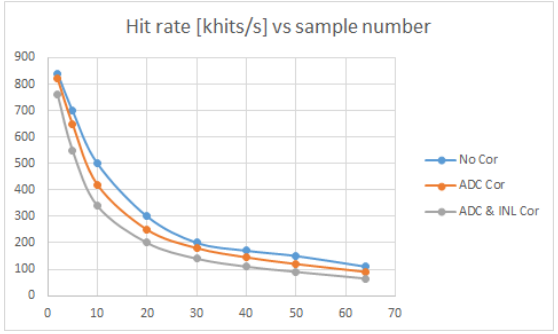
=> permits wide coincidences

ACQUISITION SOFTWARE

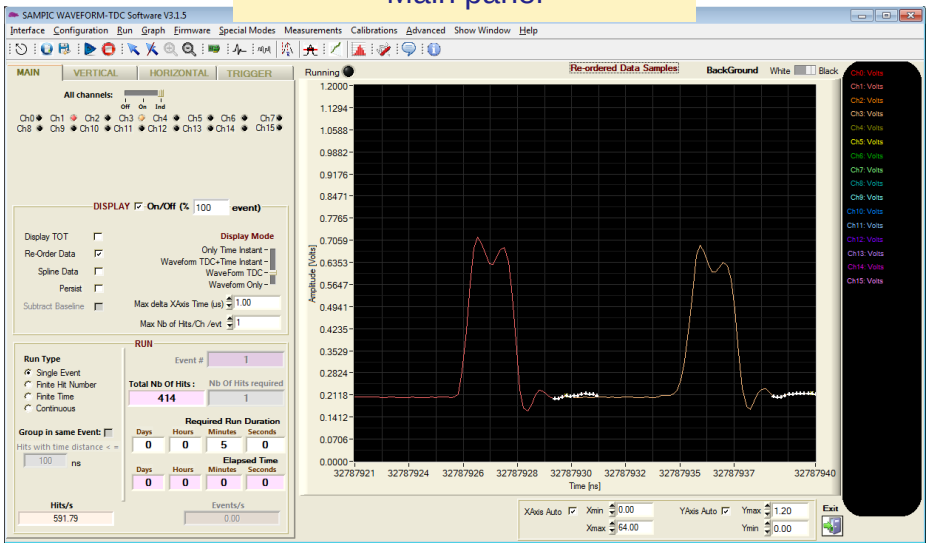
- **Acquisition software** has been developed (& soon C libraries)

=> full characterization of the chip & module

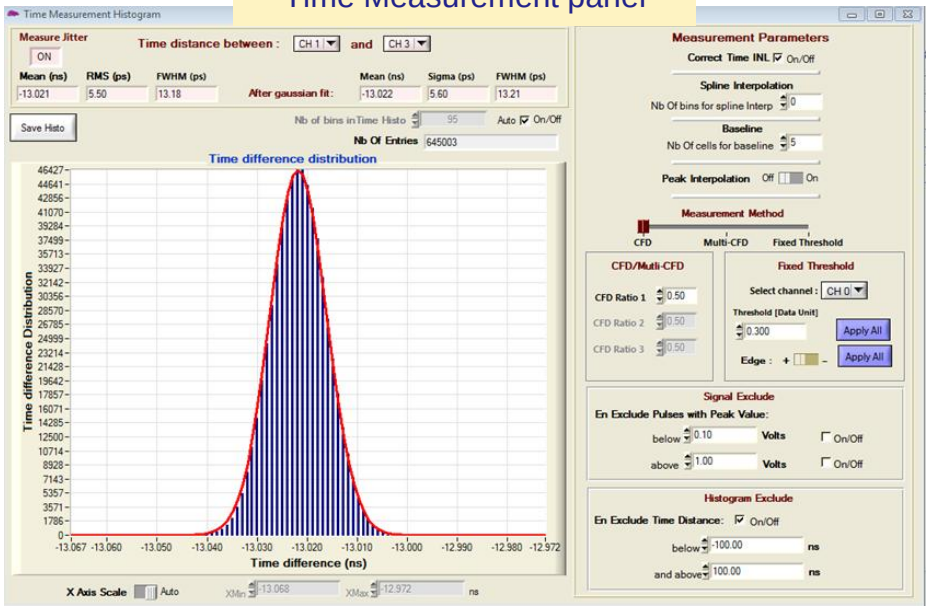
- **Special display** for **WTDC mode**
- Data saving on disk.
- Used by all SAMPIC users.
- A smart panel dedicated to **time measurement** is available
- It permits selecting the parameters used for extraction of time
  - Optional spline interpolation on the peak area and on the threshold area
  - Fixed threshold option
  - CFD: ratio, nb of applied thresholds (1 to 3)
- Recorded hit rate depends on: the number of waveform samples, the corrections applied (ADC, Time INL), the saving on disk (none, ASCII, binary)...



Main panel



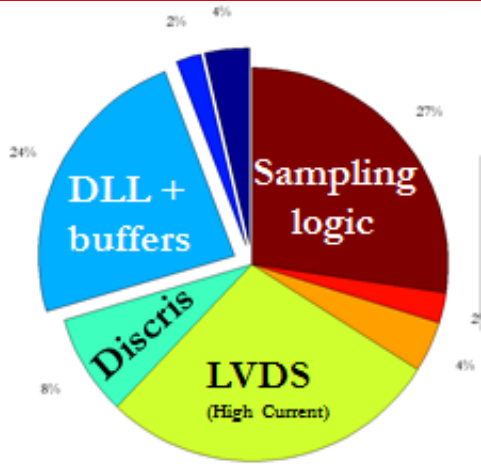
Time Measurement panel



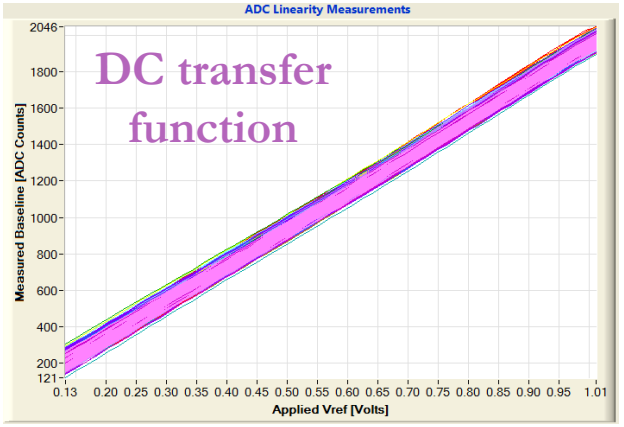
SAMPIC_V1 PERFORMANCES

- Power consumption: **10mW/channel**
- 3dB bandwidth > **1 GHz**
- Discriminator noise **~ 2 mV rms**
- Counting rate **> 2 Mevts/s** (full chip, full waveform), up to 10 Mevts/s with Region Of Interest (ROI)

Power distribution

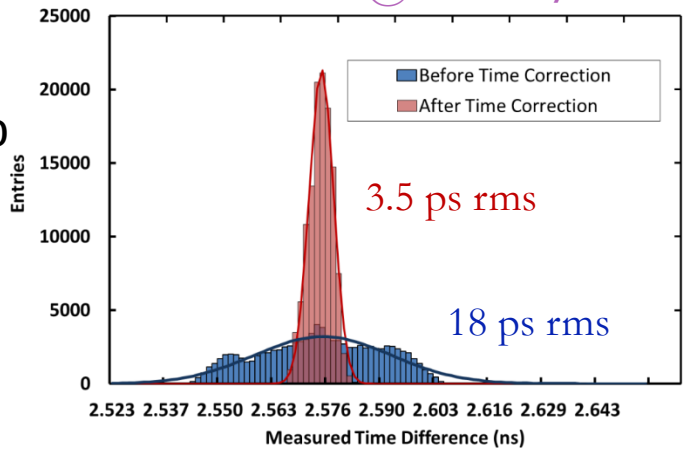


- Wilkinson ADC works with internal **1.3 GHz** clock
- Dynamic range of **1V**
- Gain dispersion between cells ~ **1%** rms
- Non linearity **< 1.4 %** peak to peak
- After correction of each cell (linear fit): noise = **0.95 mV rms**



- Time Difference Resolution (TDR):
- Raw non-gaussian sampling time distribution due to DLL non-uniformities (TINL)
- Easily calibrated & corrected (with our sinewave crossing segments method [D. Breton&al, TWEPP 2009, p149])

Ex: TDR @ 6.4 GS/s



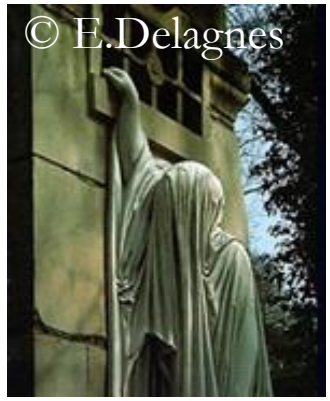
NEW VERSIONS SINCE SAMPIC_V1

- **SAMPIC_V2:** submitted in November 2015
  - Introduction of many new blocks and functionalities
  - Preliminary results shown in Kansas City workshop
  - Ok, **but** BW limitation due to input switch (500MHz)

- **SAMPIC_V3** submitted in November 2016.
  - Correction of BW problem + new blocks and functionalities
  - Back in April 2017, **but** huge over-consumption
  - Default finally identified after a few weeks
  - Could not be seen in simulation or DRC!
  - Was functional **but** … slow (digital blocks undersupplied)

- Fixed in June 2017
  - **But** … change of technology (fab moved to Austria)
  - Changes equivalent to Spanish to Catalan translation

But…



IR analysis: something is heating !!!

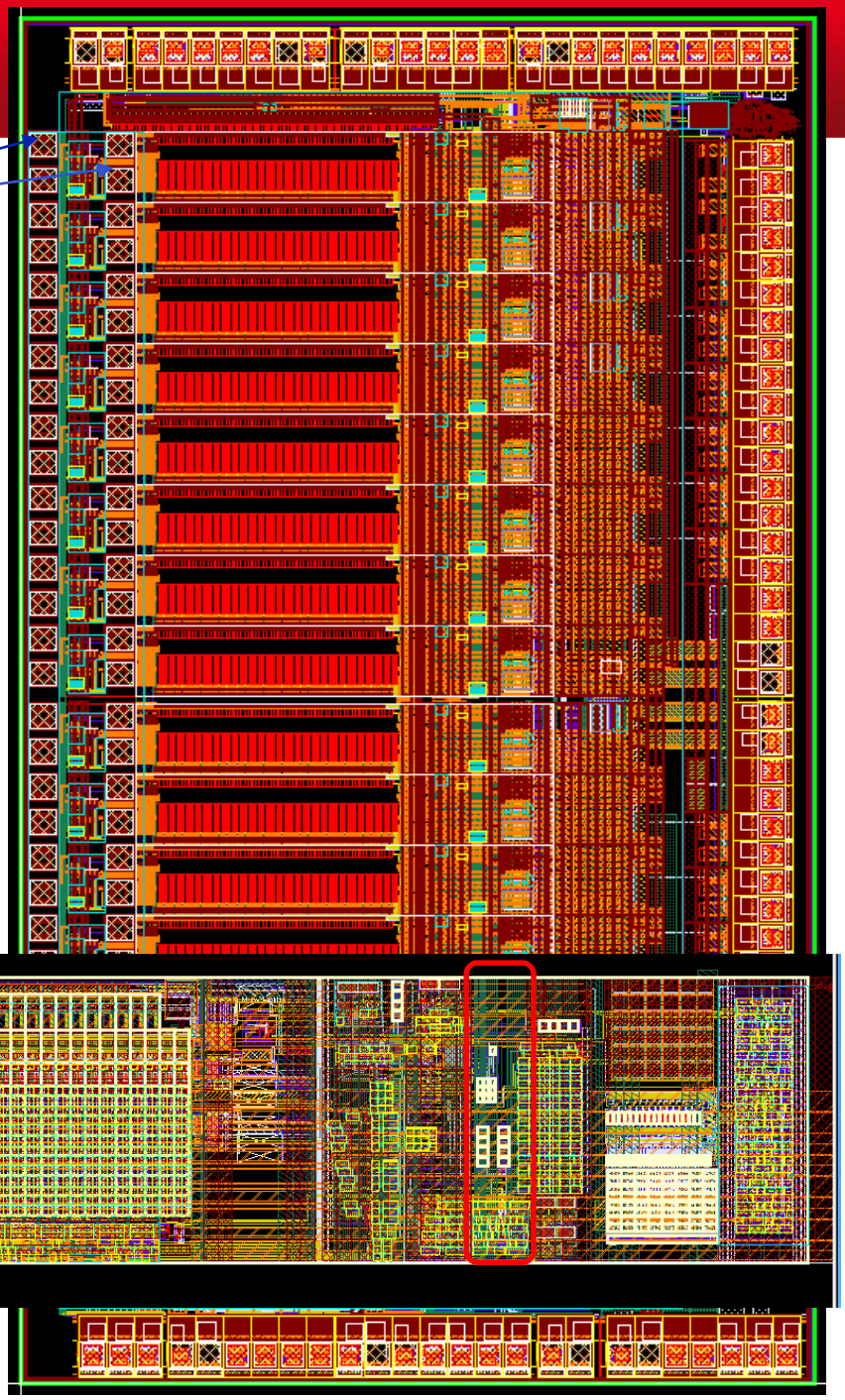
- The new chip came back end of November 2017 and works well!

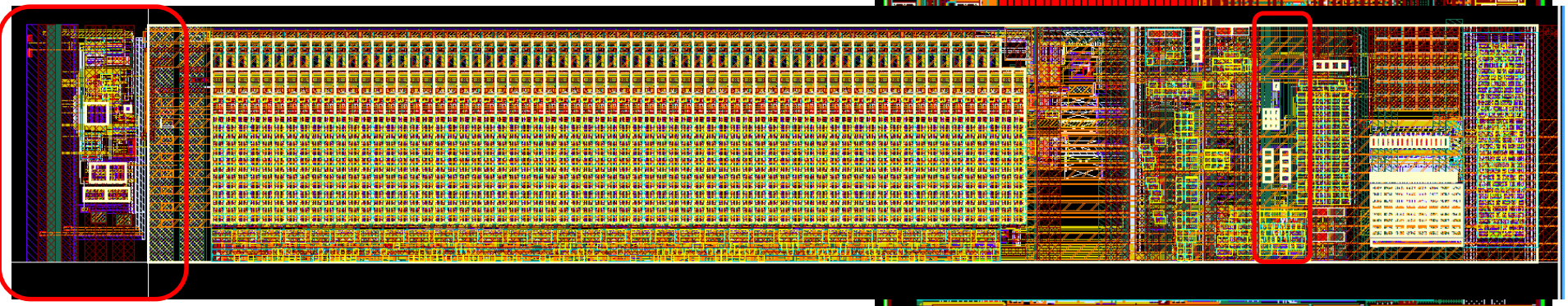
NEW FEATURES OF SAMPIC_V2 & V3

- Integration of all DACs to control the chip
- ADC resolution internally selectable in the range 7 to 11 bits
- **New input block**
- **Auto-conversion mode for ADC:** the conversion is now automatically started when an event is detected, independently for each channel.
  - ➔ Reduces the required external digital electronics
  - ➔ External mode (handshake with FPGA) still available. Permits building a two-level trigger based on many chips for a common event selection.
- Wider sampling frequency range (0.8 GS/s to 8.5 GS/s but 10 GS/s no more possible with the new techno)
- **Coarse timestamp extended to 16 bits**
- Improved “central trigger” (multiplicity of 1, 2, or 3) with possibility of common deadtime & smart channel selection
- Improved **PostTrig**
- Individual integrated **TOT measurement** + **Trigger Filter based on TOT**
- **“Ping-Pong” (toggling) mode + channel chaining**

SAMPIC_V3 LAYOUT

- **Double raw of input pads**:
  - External row: standard cabling for usual applications where translator stage can be used and self calibration performed
  - Internal row: for optimal bandwidth, time precision and testability
- No more NC pins.



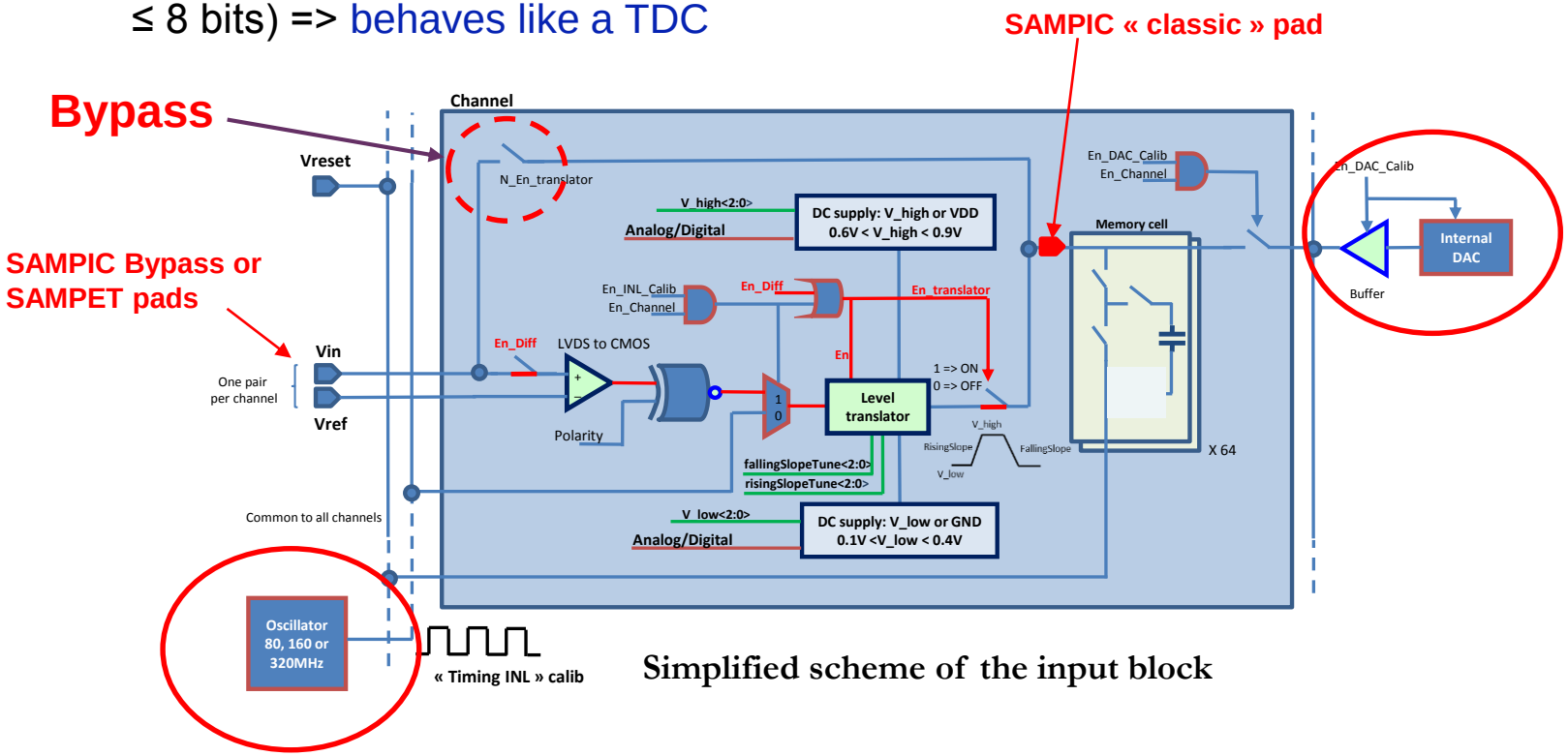


• Dimensions of a channel: 200µm x 1.3mm

NEW INPUT BLOCK OF SAMPIC

- Translator input block : **input signal can feed the memory directly** (**Bypass Mode**) or pass through a translator (SAMPET mode: from differential digital to internal levels optimized for SAMPIC)
- It permits among others:
  - **Self calibration of the chip (amplitude & time)**
  - Compatibility with (small amplitude**) digital differential signaling**

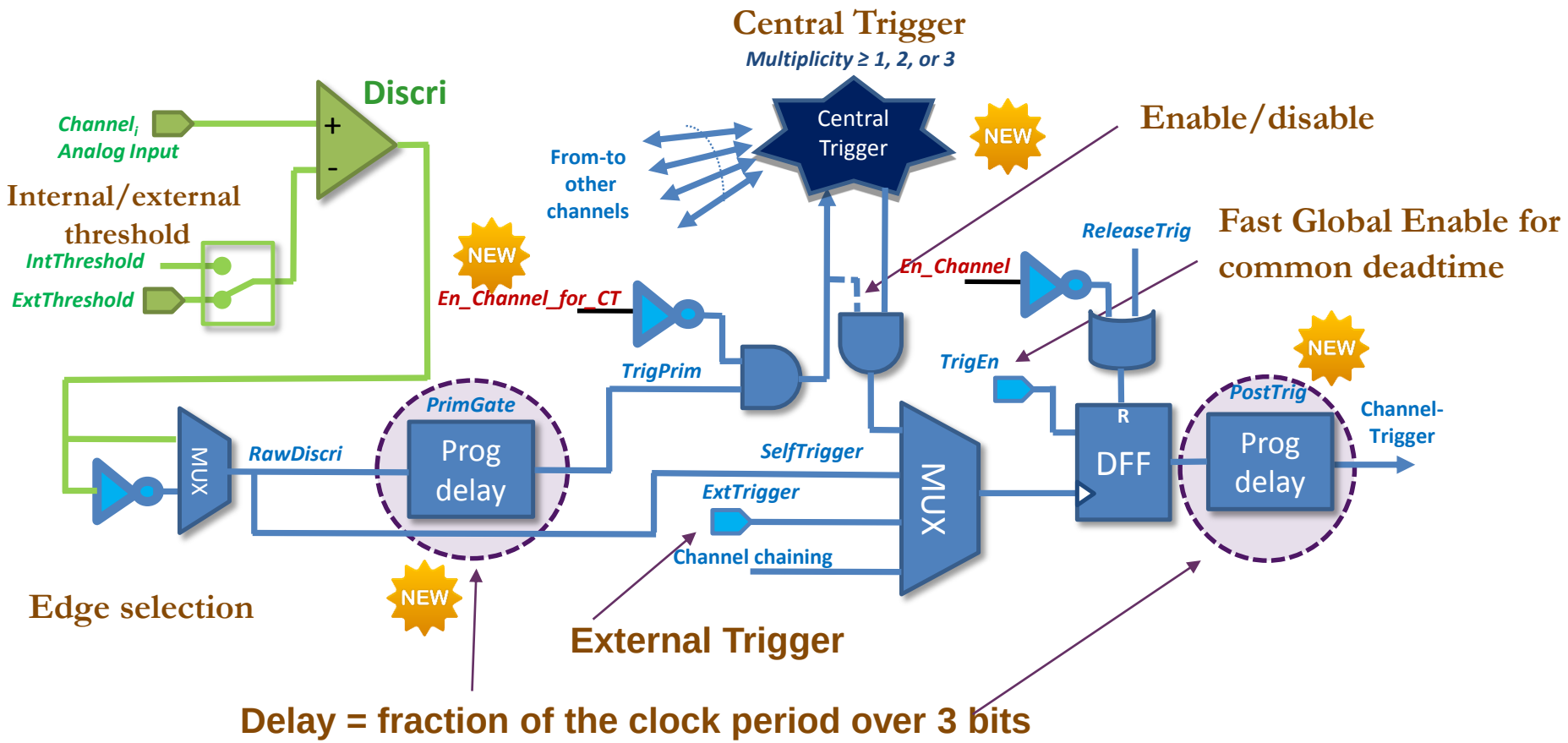
- Fixed amplitude at translator output => only a few samples (ROI) and fast conversion (≤ 8 bits) => behaves like a TDC



Simplified scheme of the input block

NEW TRIGGER SCHEME

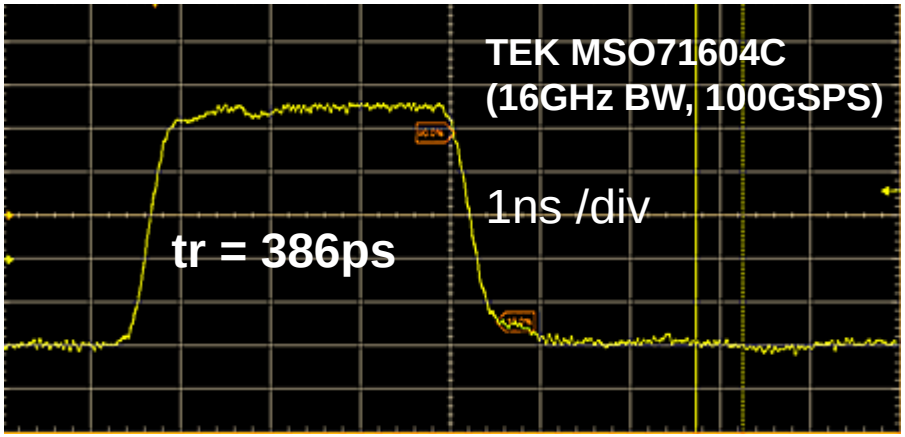
- One very low power signal discriminator/channel
- One 10-bit DAC/channel to set the threshold (which can also be external)
- Several trigger modes programmable for each channel:

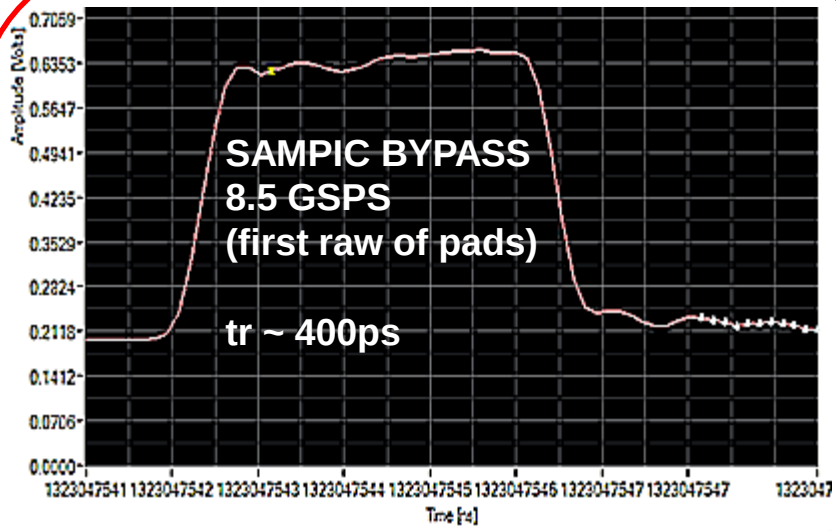


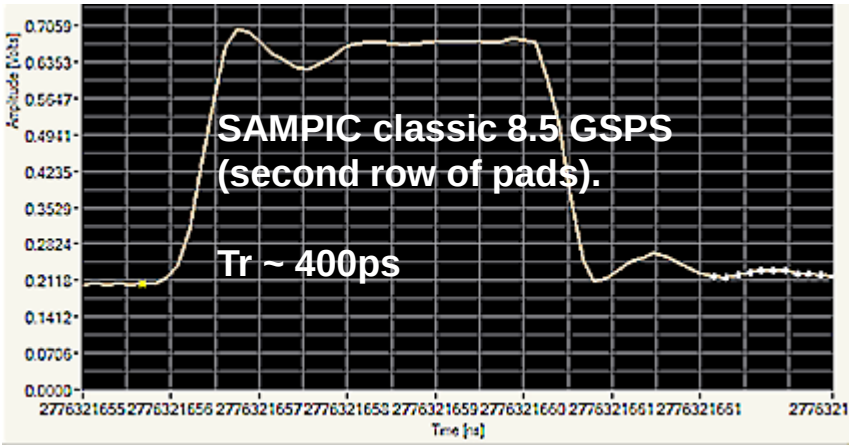
⚠ Only the triggered channels are in dead time

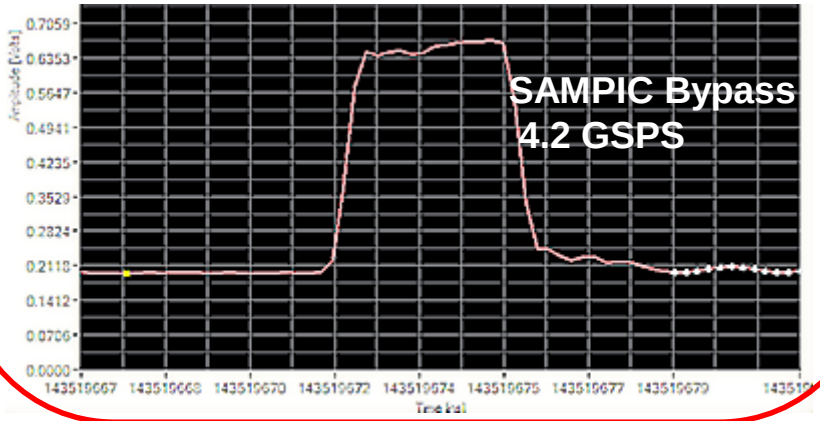
WAVEFORM RESPONSE WITH NEW INPUT CONFIGURATION

- **Pulse (~460 mV pp) with sharp edges => compare the response from SAMPIC and from a 16 GSPS oscilloscope**:
  - Signal produced by a LeCroy 9214 generator.
  - Permits estimating **SAMPIC bypass bandwidth: > 1 GHz**



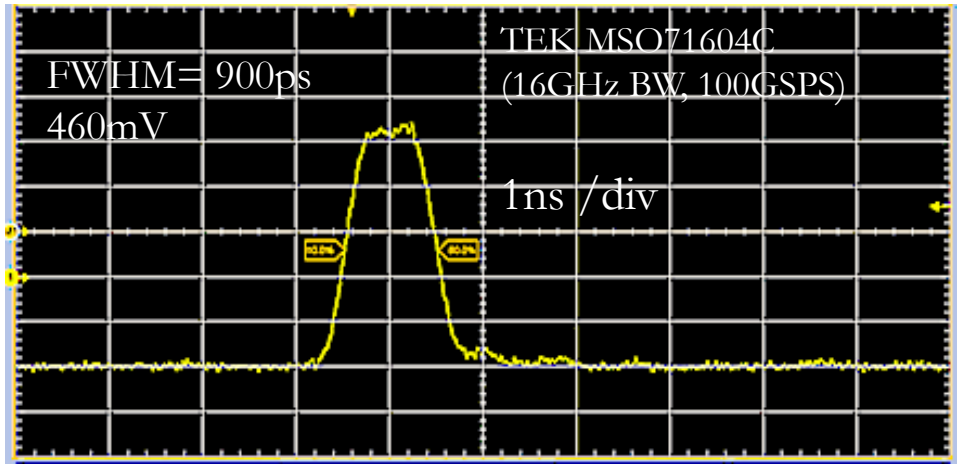


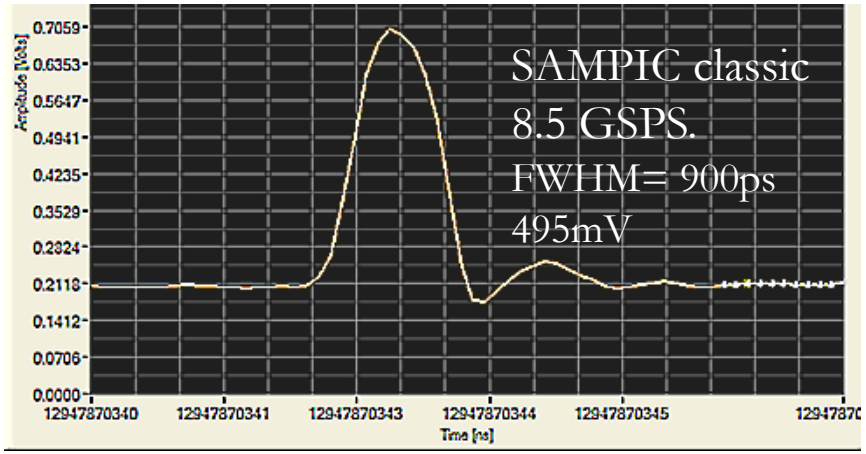


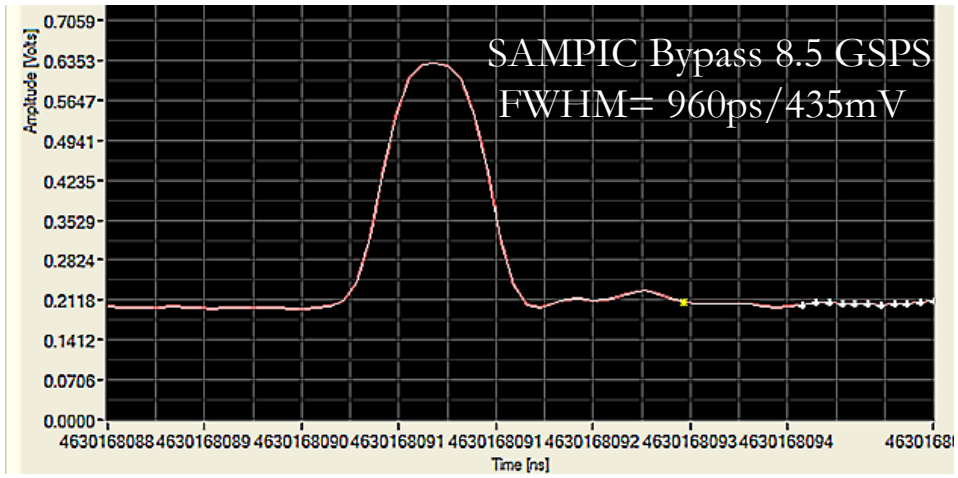


SHORT SIGNAL RESPONSE

Lecroy 9214 signal with 900 ps width







TIME RESOLUTION

- The new DLL has been re-worked for improving the resolution for the lower sampling frequencies
- Delays made by a cable box => rise time degrades with delay …

- With external time-calibration :
  - A TDR of ~5 ps rms if 4.2< Fs<8.5 GS/s
  - The TDR < 10 ps rms for 3.2 GS/s
  - TDR < 18 ps rms for 1.6 GS/s

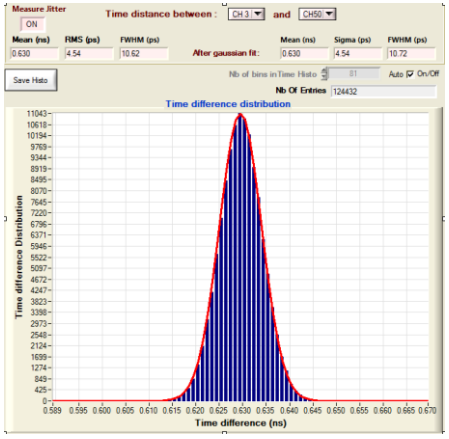
- With **self-calibration**
  - Limited jitter degradation (~20%)
  - Permits full integration in compact detection systems …

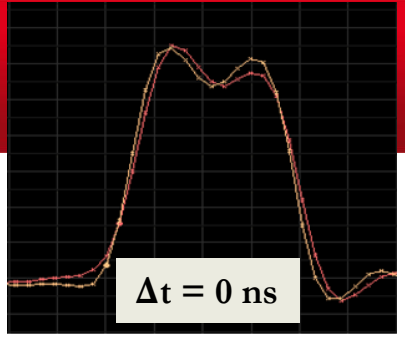
- Between 2 chips:

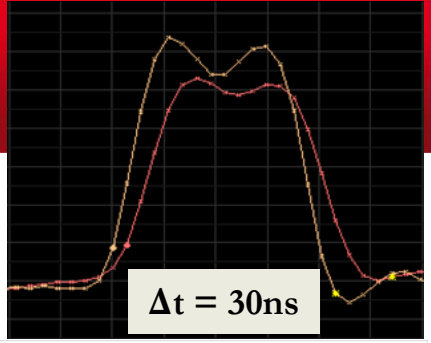
@ Fs = 6.4 GS/s

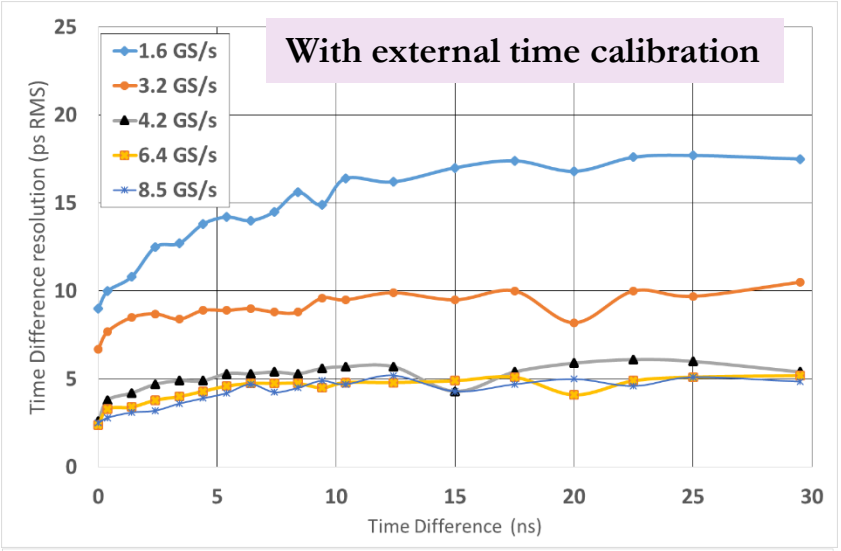
Δt = 0.63 ns

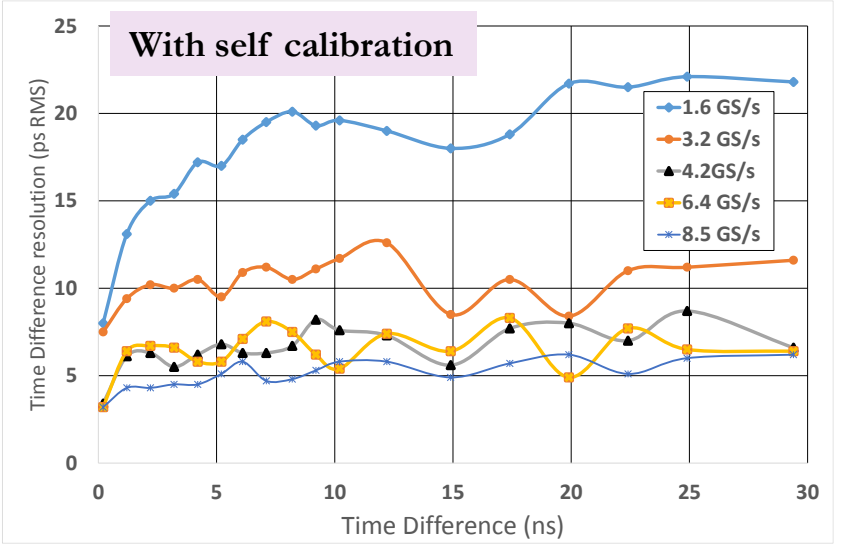
=> TDR = 4.5 ps rms



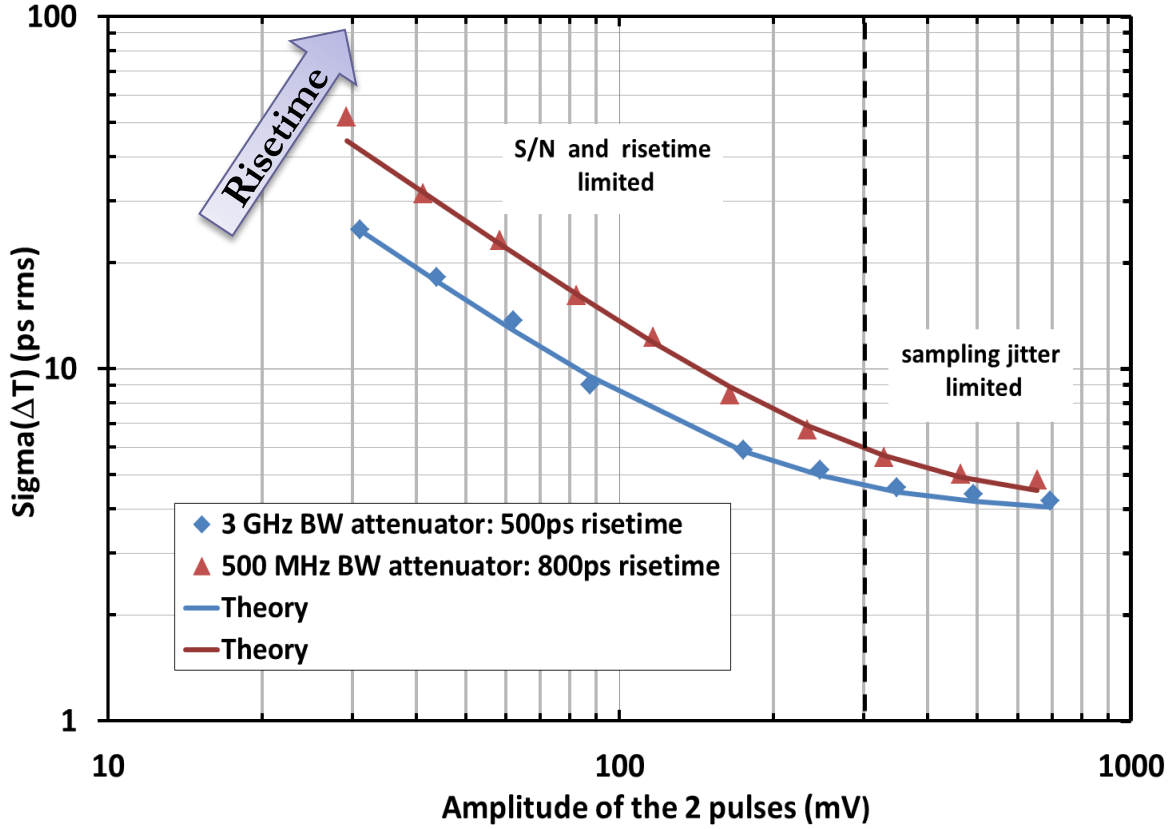








TIMING RESOLUTION VS AMPLITUDE & RISETIME
1-NS FWHM - 15 NS DELAY, DIGITAL CFD ALGORITHM



Measurements consistent with the theoretical formula:

$$\sigma(\Delta t) = \sqrt{2} \times \sqrt{\sigma_j^2 + \alpha \times \left(\frac{\sigma_n}{Slope}\right)^2}$$

Assuming: :

* Voltage noise σ_n = 1.1 mV RMS
* Sampling jitter σ_j = 2.8 ps RMS
* α = 2/3 (theory for perfect CFD)

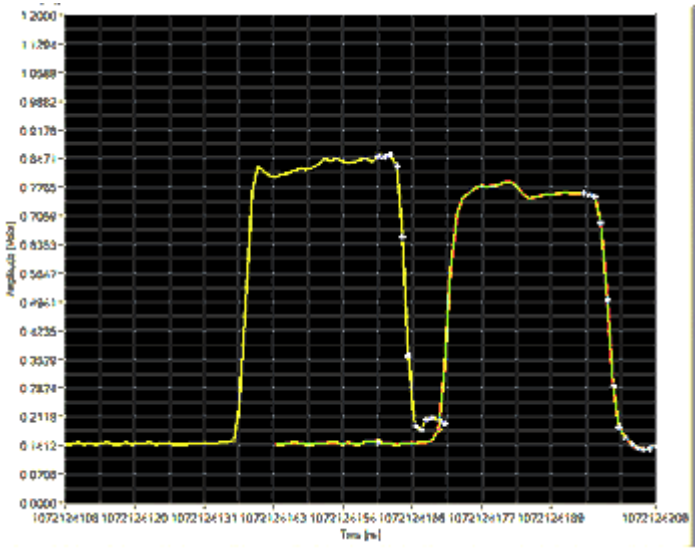
arXiv:1606.05541v1

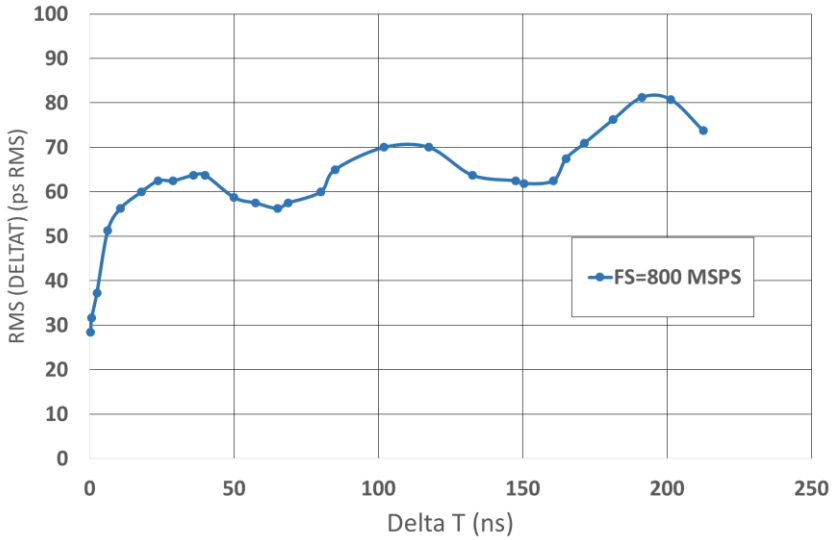
- 2 zones: sampling jitter or S/N limited zones.
- TDR < 8 ps rms for pulse amplitudes > 100mV
- TDR < 20 ps rms for pulse amplitudes > 40 mV

- Can be improved by using mores samples (if feasible and uncorrelated) since dCFD uses only 2 samples

NEW in SAMPIC V3: 800 MS/s mode

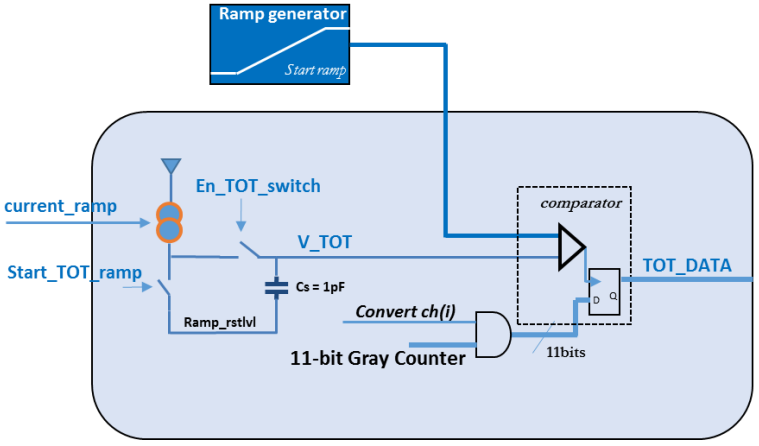
- Was not possible in the previous SAMPIC versions
- The 64 cells cover a 80 ns window with 1.25 ns steps
- Tested here with an external clock with unknown jitter + cables that degrades the slopes for larger delays
- < 40ps RMS resolution for a single signal
- Could be usefull for applications with slower detectors (semiconductors, moderate-speed light detector)

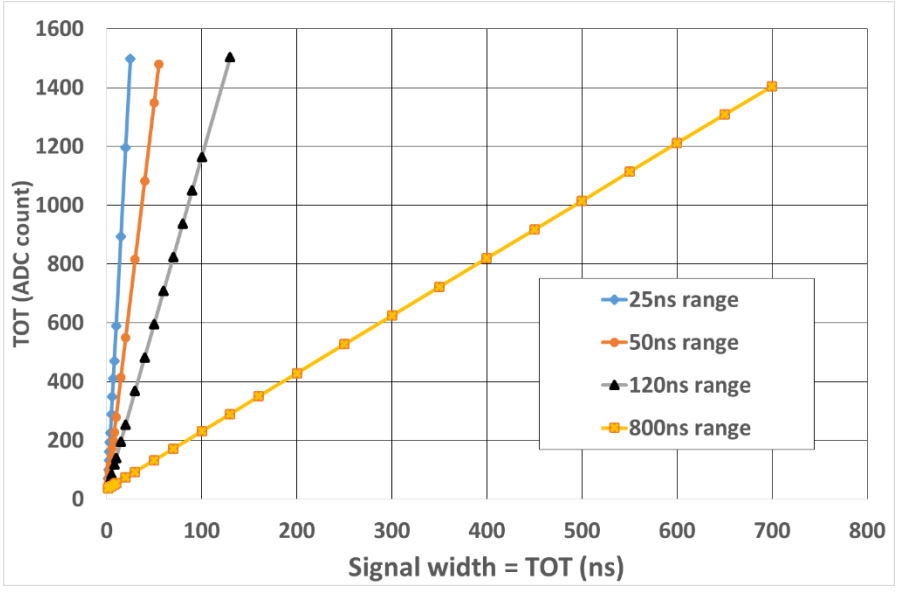


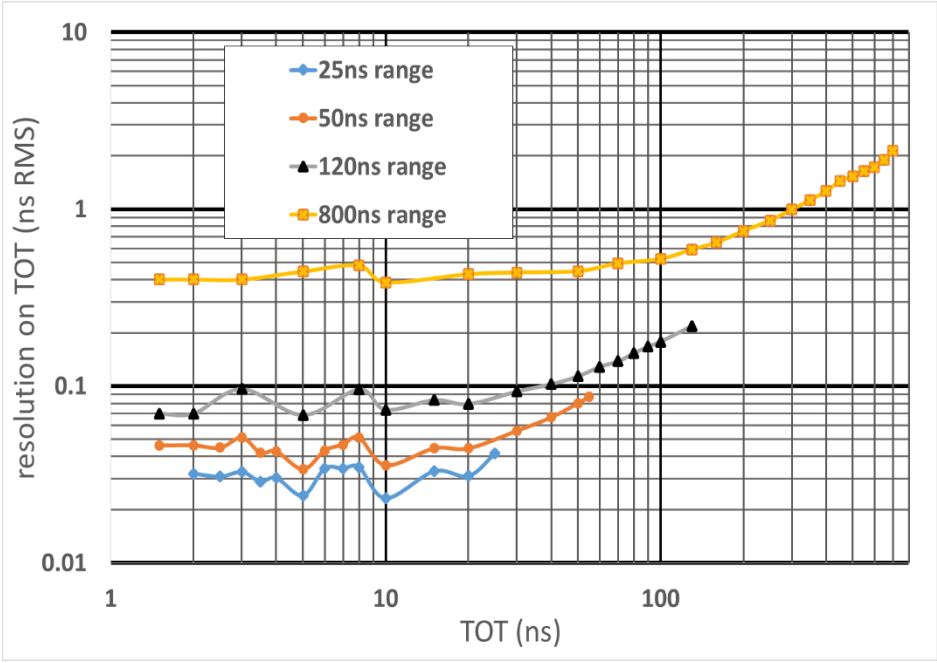


NEW in SAMPIC V3: TOT MEASUREMENT

- SAMPIC is designed to digitize a short signal or only a small part of a longer one (eg rising edge) to extract the timing ➔ then the other edge is missed
- Addition of a **ramp-based Time to Amplitude Converter** for each channel seen as a 65th memory cell during digitization => >10bit TOT TDC



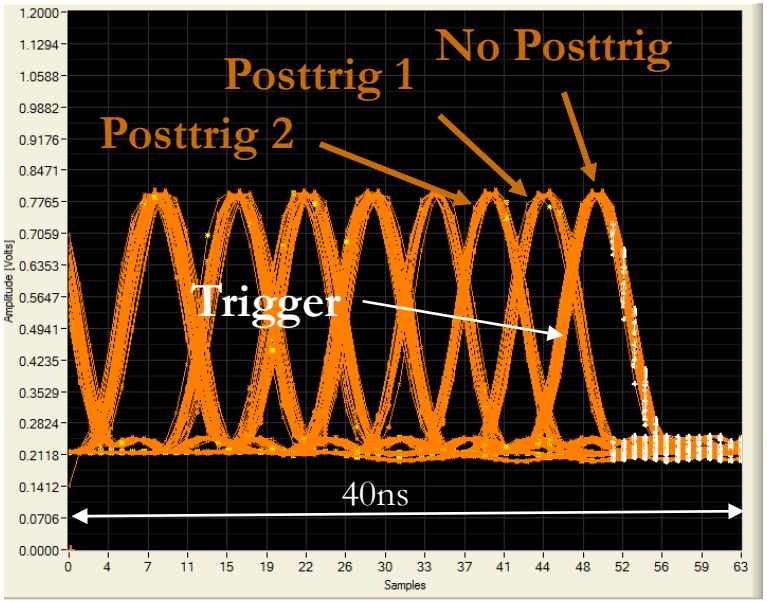




Measurement ranges between 2 and 700 ns.

NEW in SAMPIC V3 : PROGRAMMABLE POSTTRIG

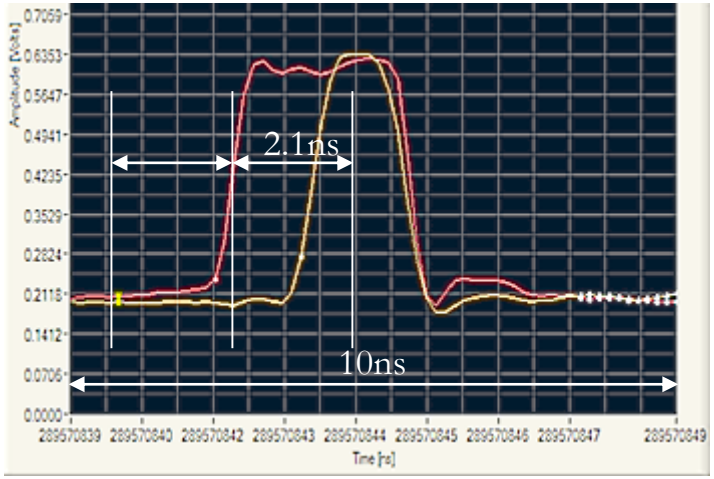
- Allows to “move the signal” by fractions of the acquisition window
  => oscilloscope-like PostTrig
- 8-step (~linear) programmable asynchronous delay that must be proportionnal to the sampling frequency
- Mostly useful for low sampling frequencies
- Based on a very compact delay-locked loop system, also reused for 3 other purposes in each channel



Effect of the 8 posttrig values (1.6 GSPS)

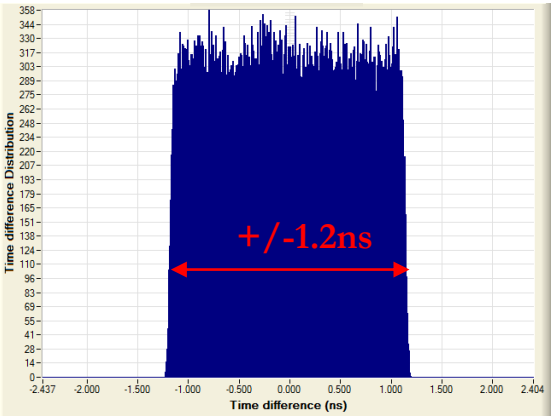
NEW IN SAMPIC: CENTRAL TRIGGER/ COINCIDENCE

- Each channel can be triggered by the CENTRAL TRIGGER: can be the **OR, or a Coincidence of ≥ 2 or ≥ 3 channels**
- Coincidence Gate generated by an asynchronous delay as previously described.
- **Only 1ns of extra latency on trigger decision**
- Test below using 2 signals (>> 1MHz) with random phases sent to 2 channels with 1.2 or 2.1ns coincidence gate.

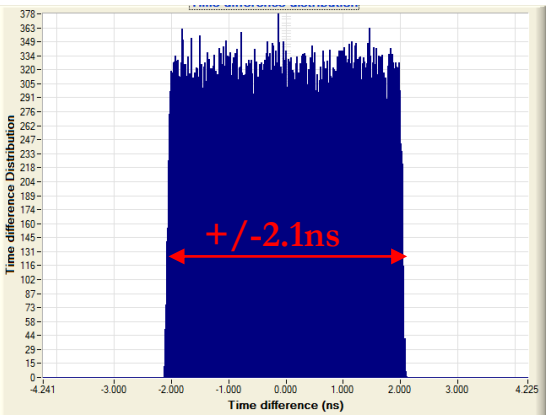


1 of the couples of signals digitized.
2.1 ns gate @ 6.4 GSPS

TimeDifference histogram (from the digitized waveform)



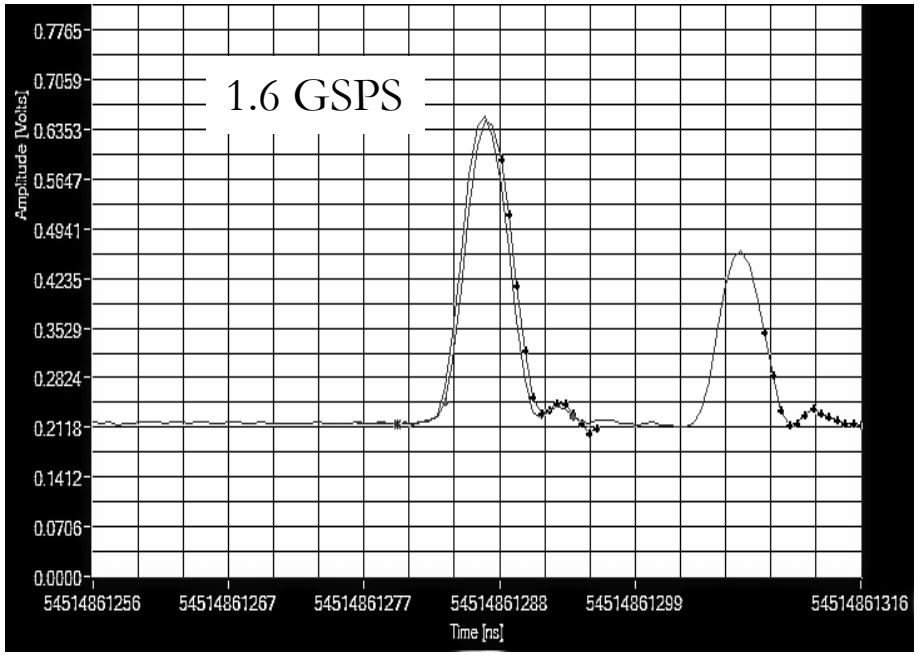
« 1.2ns » coincidence gate



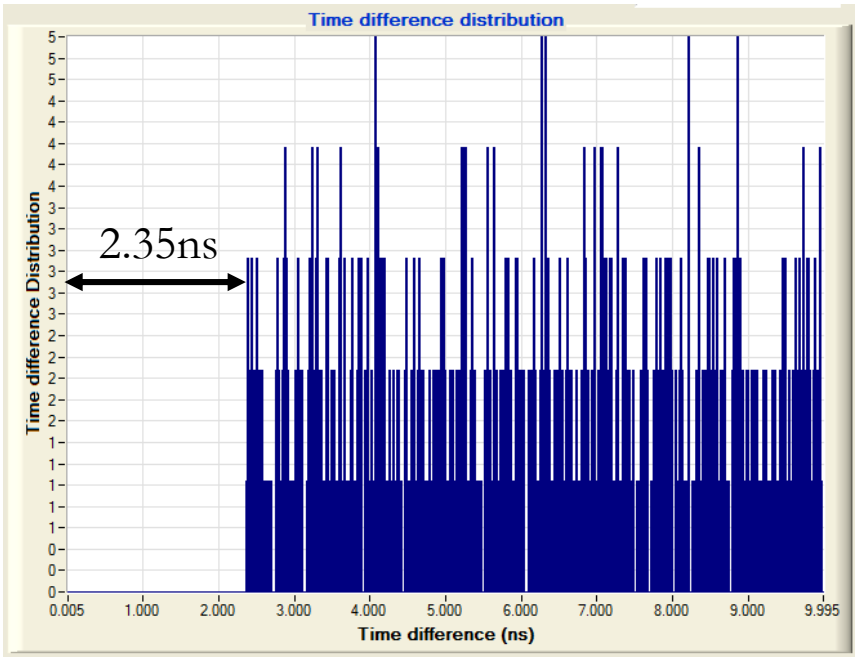
« 2.1ns » coincidence gate

NEW IN SAMPIC_V3: PING-PONG MODE

- **PING-PONG**: use alternatively 2 SAMPIC channels, connected or not to the same source, to reduce the dead time and allow double or conditionnal pulse detection.
- Min re-triggering distance : 2.35 ns (see below)
- Drawback: number of channels divided by a factor 2 if source is common



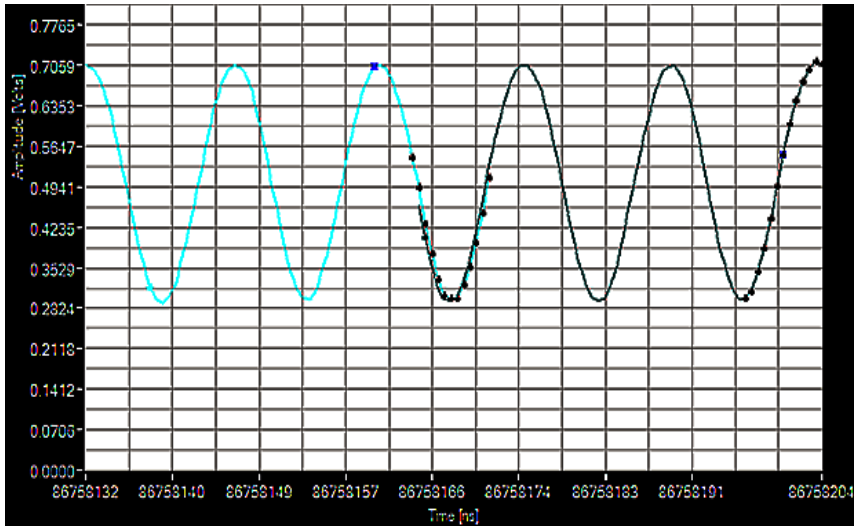
1st pulse recorded on channel 2
2nd pulse recorded on channel 3



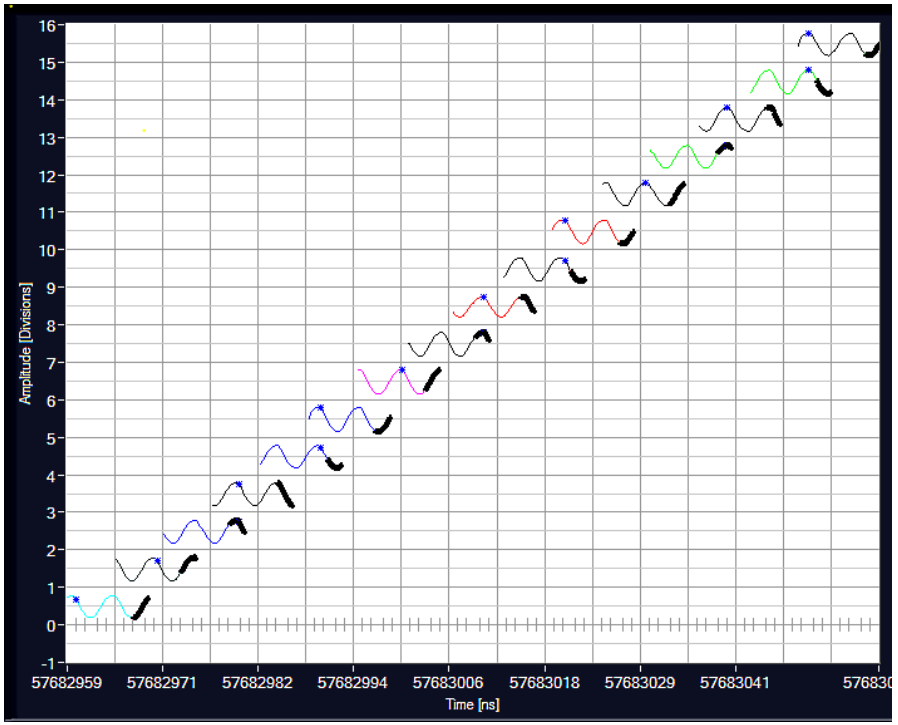
DeadTime (measured with 2 random pulses)
=> Time difference distribution

NEW IN SAMPIC_V3: CHAINED MODE

- Goal: extend the depth of SAMPIC by **chaining channels** connected to the same source or force triggering of successive channels
- Each channel can be defined as a Master that can successively trigger N (1 to 15) other « Slave » channels.
- Tens of possible configurations
- The delay between the channels is defined by the POSTTRIG



2 channels chained @1.6GSPS



16 channels chained @6.4GSPS

RECENT MODULE DEVELOPMENTS

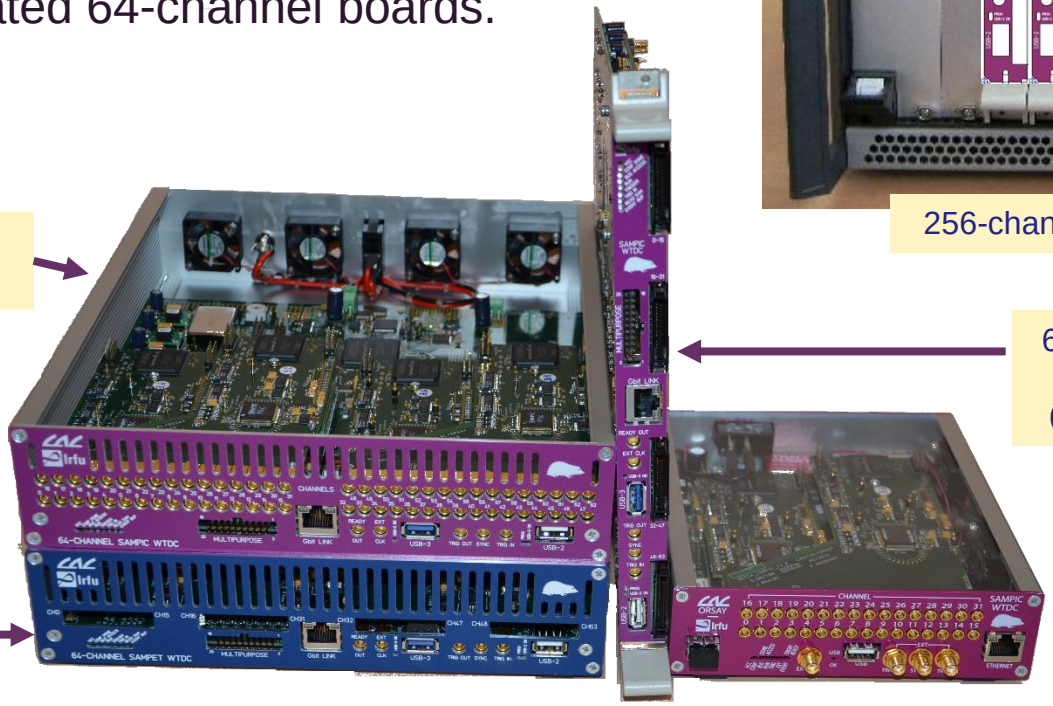
- In response to users' requests, we developed new modules and systems in order to increase the number of channels
- They make use of the new motherboard also developed for the WaveCatchers.
- 64-channel modules and board are almost ready for release.
- 256-channel mini-crate is under development with new more integrated 64-channel boards.

256-channel mini-crate

64-channel module with individual inputs

64-channel board with flat cable inputs (can be digital or analog)

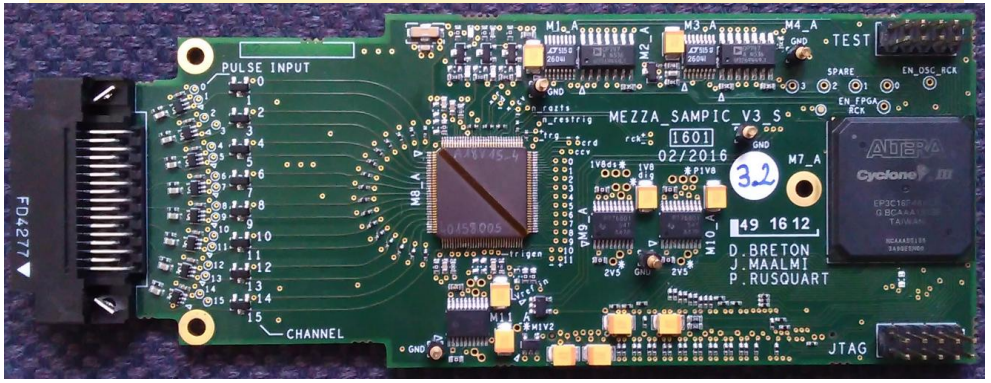
64-channel module with flat cable inputs (can be digital or analog)



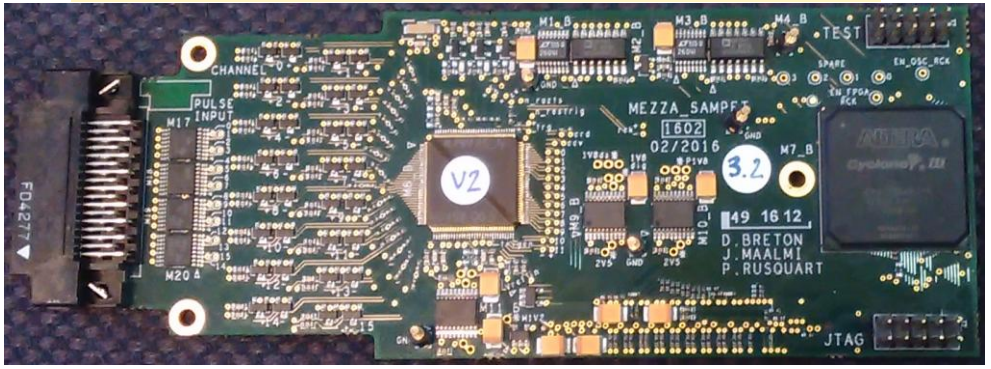
DAUGHTERBOARD DEVELOPMENTS

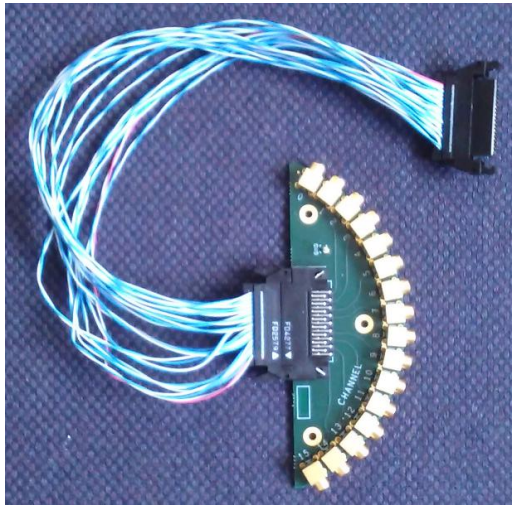
- Various mezzanine cards have been developed for housing the new versions of the chip (including the digital differential option)
  1. Analog/digital input with MCX
  2. Analog/digital input with flat cable
  3. Differential digital input with flat differential cable
- Adaptors have also been developed

Mezzanine with flat cable analog/digital input



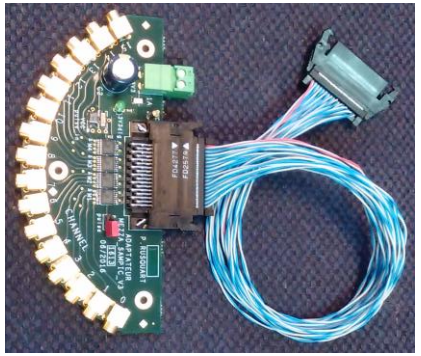
Mezzanine with flat cable differential digital input





16-channel individual to flat cable adaptor

16-channel individual to digital differential flat cable adaptor



RATE CAPABILITIES & BOTTLENECKS

- Each SAMPIC chip can produce ~2 Gbits/s of data
  - For usual test benches with a single computer, there are successive bottlenecks, the first being SAMPIC itself, the last being the software
  - A smart trigger permits selecting good events…

	On-Chip Digiti-zation		SAMPIC to FPGA Transmission 160 MHz link 1.92 Gbits/s		Theoretical Gbit UDP		Theoretical USB2 (240 Mbits/s)	
	11 bits	9 bits	All samples	16 samples	All samples	16 samples	All samples	16 samples
MEvent/ch	0.6	2.4						
MEvent/chip	9.6	38.4	2.8	9	0.9	3	0.24	0.72

/4 /3 /4

TAKING DATA WITH DETECTORS

- SAMPIC modules are already used with different detectors on **test benches or test beams. A lot of examples were presented at the WaveCatcher and SAMPIC workshop the 7th and 8th of February in Orsay.**
- Tested with **PMTs, MCPPMTs, APDs, SiPMs, fast Silicon Detectors, Diamonds**: performances are equivalent to those with high-end oscilloscopes
- Different R&Ds ongoing with the **TOF-PET** community (CERN, IRFU,…)
- SAMPIC has been used for test beams of **TOTEM and ATLAS HGTD at CERN**
- It was also used for **fast mesh-APD** characterization and test beams
- **TOTEM** has developed a CMS-compatible motherboard housing SAMPIC mezzanines which has been installed on the LHC
- SAMPIC is used for test beams of **SHIP** collaboration. It is now considered as baseline readout option for the Fast Timing Detector, the Surround Background Tagger and the Muon Detector.
- SAMPIC is in use at Giessen for **PANDA EndCap DIRC** caracterization.
- Envisaged for T2K ?

Initial request for SAMPET & funding by C. Williams (CERN+INFN) & K. Doroud (CERN)

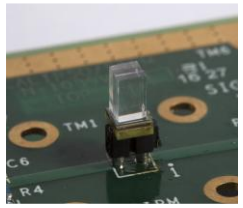
NEW in SAMPIC V3 : ON-CHIP TOT FILTER

- **Goal: demonstrate the noise rejection capability using the TOT filter which rejects events with TOT < programmable limit**
- SiPM coupled to crystals (here KETEK SiPM + PbWO4 + ^{22}Na Source, @ **20°C** => **1PE ~ 40mV**
- Th = 20 mV (0.5 PE), TOT_Filter OFF

=> 700 kHz rate of events / **4.5 MHz raw rate** (dark count)

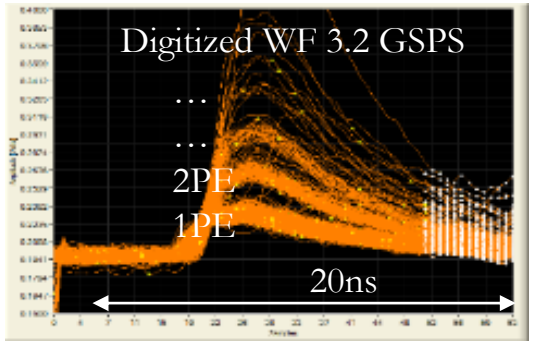
© S. Sharyy

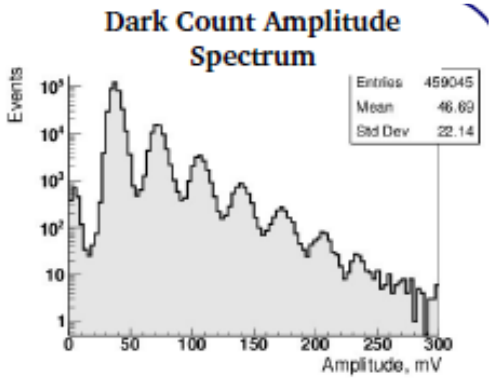
^{22}Na (511kev)



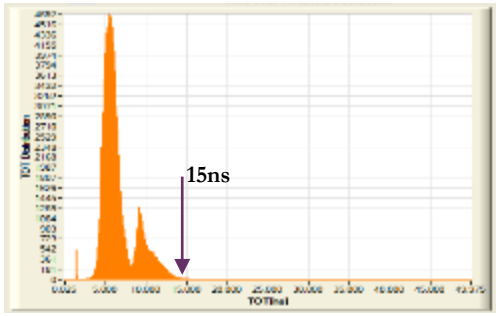
3x3x5 mm3
200 Ph/MeV
PBWO4
SiPM
3x3mm^2
20°C
Only few photons
Noisy
Ampli 40dB
SAMPIC

SiPM: KETEK PM3350TP-SB0
3x3 mm², 50µm pitch, trench design,
Operation @ 29V (2.5V overvoltage)

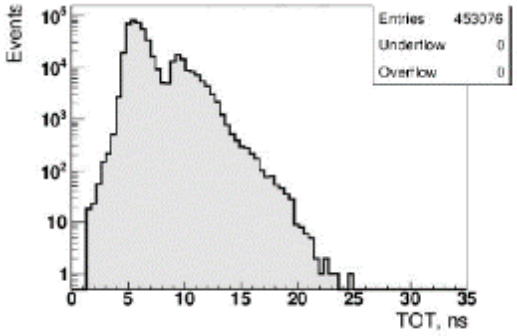




TOT spectrum (digitized by the chip)

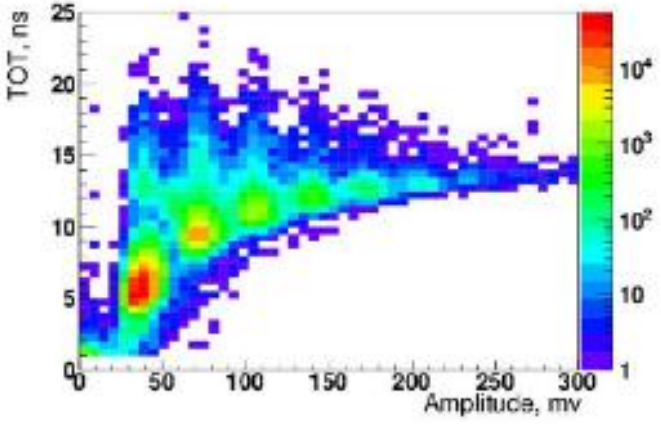


Lin scale



Log Scale

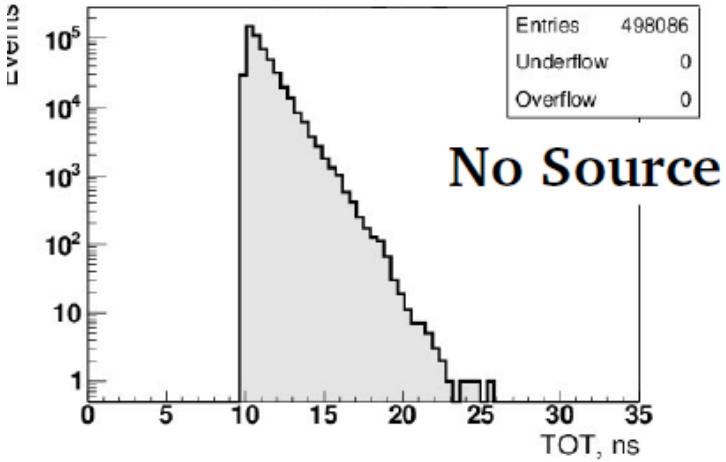
TOT vs Amplitude distribution

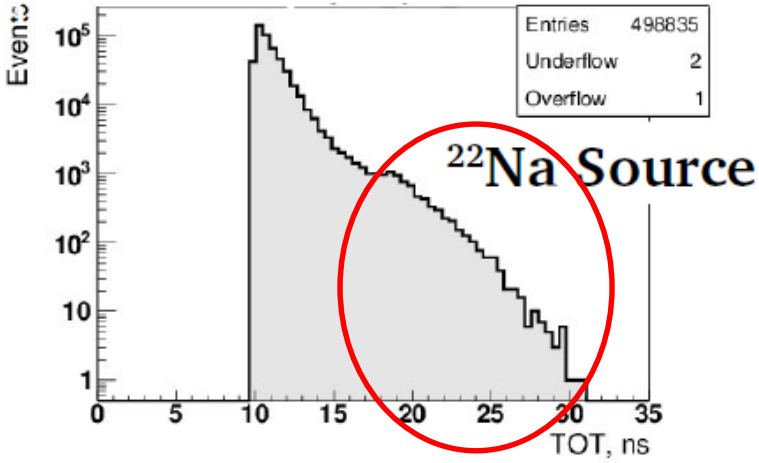


NEW in SAMPIC V3 : ON-CHIP TOT FILTER
=> noise filtering

© S. Sharyy

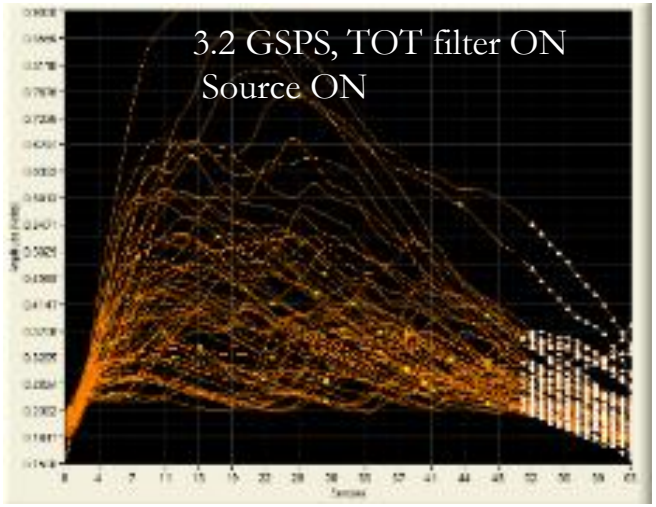
Threshold : 50 mV (1.25 PE), TOT filter = 10ns





TOT spectrum without source
(60kHz if TOT filter OFF)
60 Hz if TOT filter ON

TOT spectrum with source
(60kHz if TOT filter OFF)
200Hz TOT filter ON



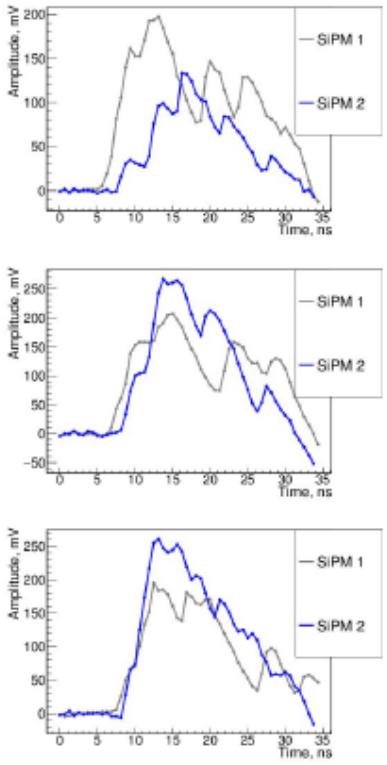
=> 140 Hz from source!

NEW in SAMPIC V3 : ON-CHIP TOT FILTER => noise filtering

- Now: 2 similar detectors, back to back with 22Na radioactive source inbetween
- Low threshold (<1 PE) + TOT filter + coincidence filter
- Data taking rate ~38 Hz (with noise >> MHz)

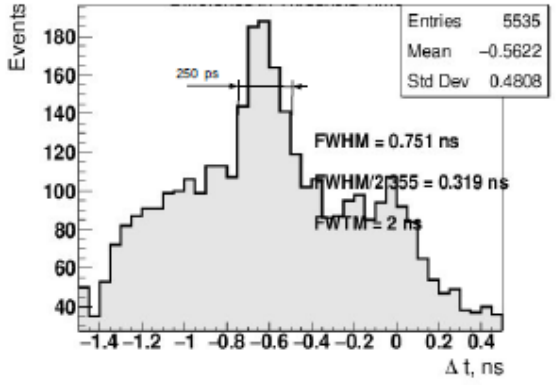
RESULTS FOR TWO DETECTORS IN COINCIDENCE

Typical Signals



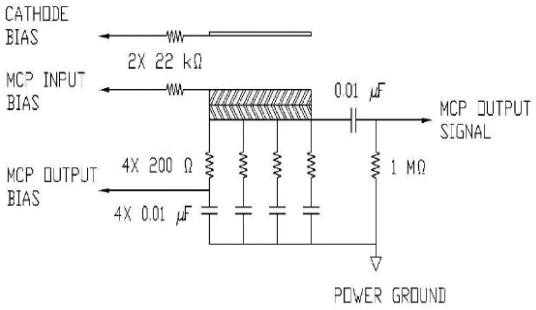
- Two similar detectors, back-to-back with ^{22}Na radioactive source between.
- Data taking rate ~38 Hits/s

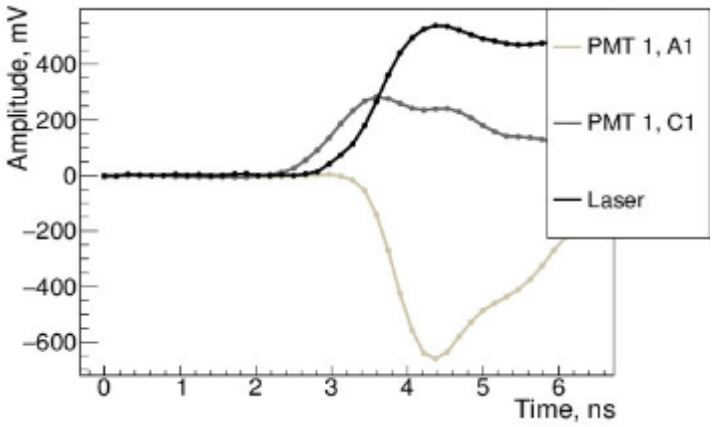
Difference in threshold time (8 mv)



Low threshold to catch the first photon

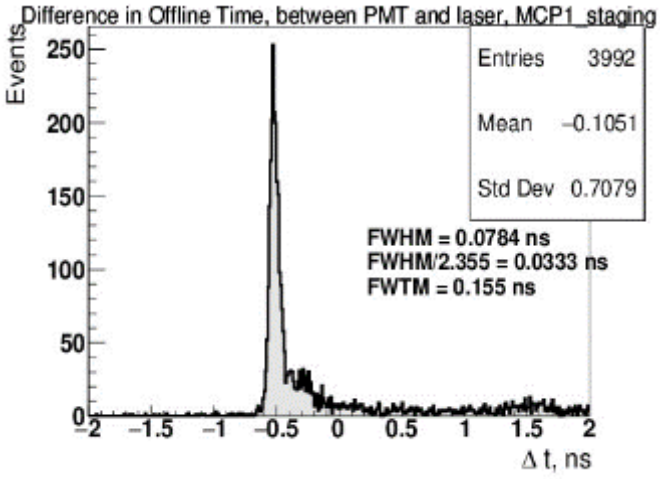
SCAN TEST OF MCP-PMT





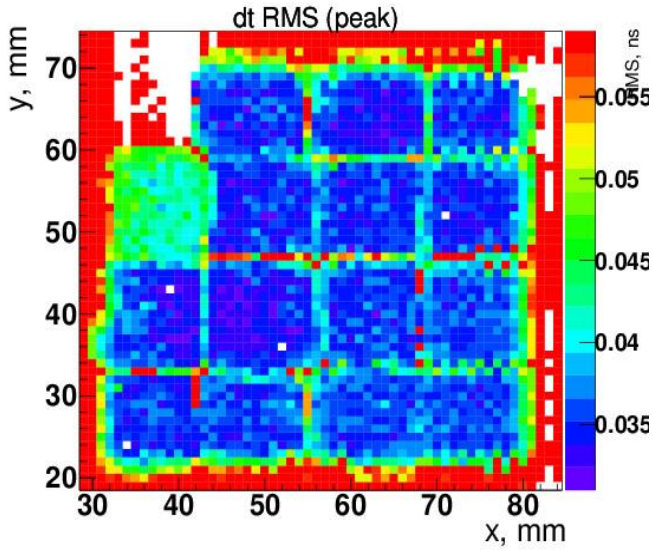
- PLANACON XP85012 used for CALIPSO/PECHE
- 53 mm x 53 mm, 64 anodes → 16 channels (groups of 4 anodes)
- Rise time 0.6 ns, pulse width 1.8 ns
- Use pulsed laser PILAS in the **single-photon mode**
- Beam duration 20ps collimated by a pin-hole with a diameter 0.4 mm
- Use automatic XZ staging station Zaber.
- Step size 1 mm , Precision ~10 μm
- SAMPIC in two-level trigger coincidence mode (anode & laser)
- Data taking: rate of ~50 kHz
- 2 sec / per stage, 0.5 sec / move
- **Total scan time ~2 hours**

Difference in time between laser trigger and anode signal

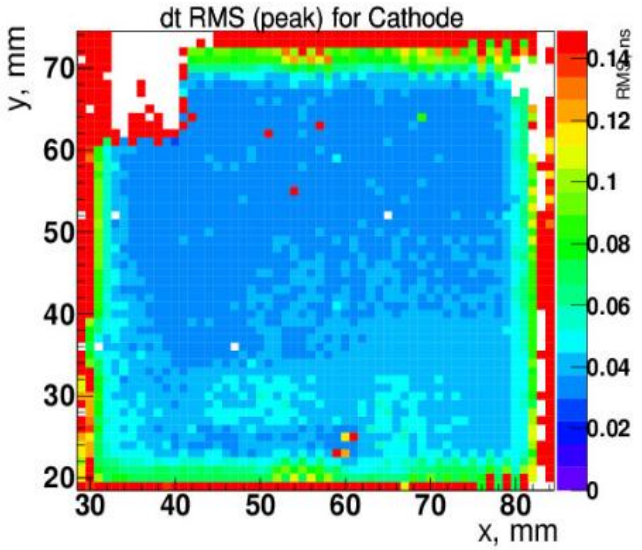


SCAN TIMING RESULTS

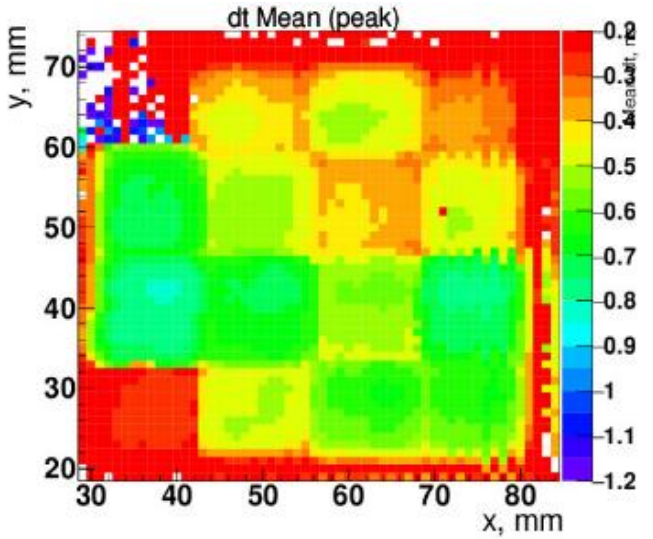
PMT resolution for anodes (ns rms)



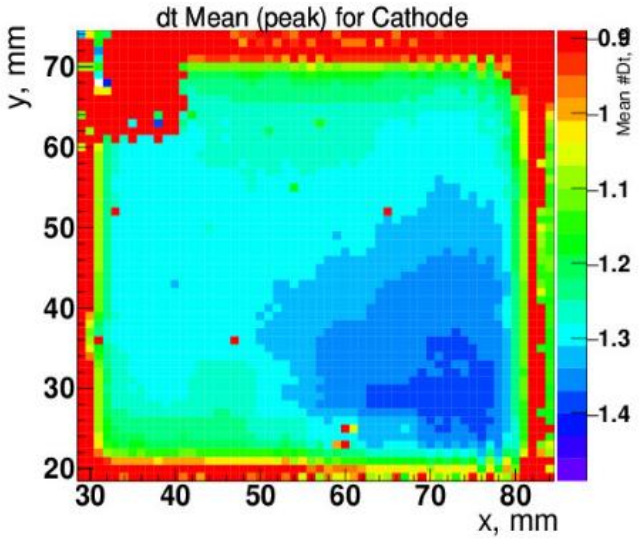
PMT resolution for cathode (ns rms)



PMT delay for anodes (ns)

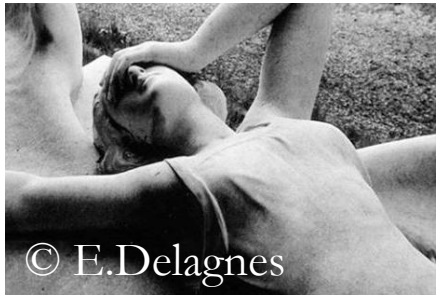


PMT delay for cathode (ns)



NEXT STEPS

- During the tests of the last version, we noticed that dealing with signal saturation was not fully effective
  - This was corrected and a new chip was submitted in December 2017. This also permitted increasing the stocks since we started getting bad news from AMS...
- The 15th of April, we learnt that the AMS 0.18 µm technology will definitely be discontinued at the end of 2018!
  - There are uncertainties for other AMS technologies…
  - We have a few 100's dies on the shelf and we will produce more for the ongoing projects in the last run…
  - We are studying the migration to another technology (Xfab 0.18 µm,…)



- Work remains on the detailed chip characterization: self-calibrations, bandwidth, readout speed, time resolution at large scale, …
- Firmware and software developments are also ongoing for the new boards and modules…

CONCLUSIONS

- SAMPIC is a full System On Chip
  - Analog or digital input, fully digital output
  - All the DACs and calibration generators are integrated
  - It just requires power, clock, and a simple interface with an FPGA
  - Small power consumption ~10 mW/channel
- All the channels can be fully independent
- Raw counting rate can thus go >> 100 kHz/ch.
- Large choice of smart triggers
- It can be used for a highly integrated tiny module (cm^3) as well as for large scale detectors (nuclear or high energy physics, TOF-PETs, …).
- Work remains on the complete chip characterization
- Firmware and software developments still ongoing
- End of AMS 0,18 µm => chip production and migration to another technology
  - Could be an opportunity to re-optimize the layout and think of radiation hardness…

- For more information: wpsist.lal.in2p3.fr/wasiw2018/

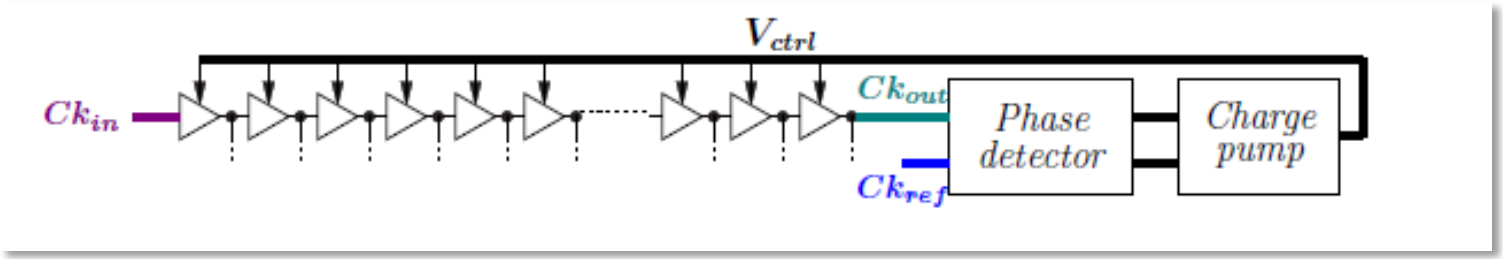
SAMPIC: PERFORMANCE SUMMARY

		Unit
Technology	AMS CMOS 0.18µm	
Number of channels	16	
Power consumption (max)	180 (1.8V supply)	mW
Discriminator noise	2	mV rms
SCA depth	64	Cells
Sampling speed	0.8 to 8.5 (10.2 for 8 channels only)	GSPS
Bandwidth	> 1	GHz
Range (unipolar)	~ 1	V
ADC resolution	7 to 11 (trade-off time/resolution)	bits
SCA noise	< 1	mV rms
Dynamic range	> 10	bits rms
Conversion time	0.1 (7 bits) to 1.6 (11 bits)	µs
Readout time / ch @ 2 Gbit/s (full waveform)	< 450	ns
Single Pulse Time precision before correction (4.2 to 8.5 GS/s)	< 15	ps rms
Single Pulse Time precision after time INL correction (4.2 to 8.5 GS/s)	< 3.5	ps rms

BACKUP SLIDES

TIMEBASE : VIRTUAL CLOCK MULITPLICATION BY 64

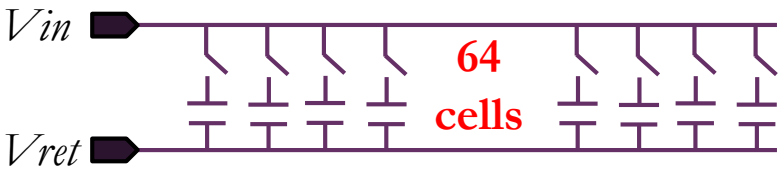
- **One single 64-step Delay Line Loop. 64 = tradeoff depth/(noise + speed**
- On chip servo-control to the timestamp counter clock
- Provides 64 incrementally **delayed** pulses **with constant width** used to drive the T/H switches of the **64 cells** for **each SCA channel**
- **'virtual multiplication'** by 64 of the TS Clock (100MHz =>6.4GHz)

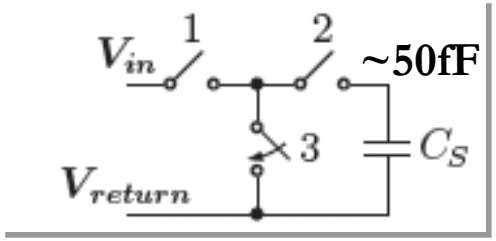


- Each controlable delay is the cascade of 2 starved inverters (inverters with slowed-down edges)
- Drawbacks:
  - Non uniform delays along the DLL ➔ skew that can be calibrated
  - For low sampling frequency:
    - Very slow edges (=> skew + jitter)
    - Limited locking range

ANALOG MEMORY (SCA) IN EACH CHANNEL

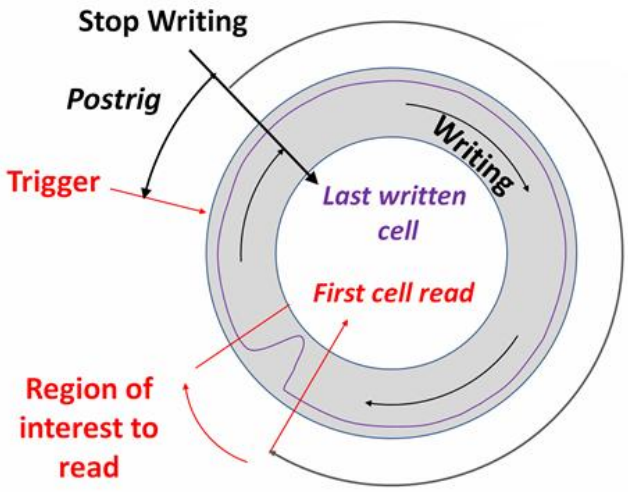
- **64-cell deep**, **No input buffer, single ended**
- Small capacitor + simple switches
- **~ 1 V usable range, > 1.5 GHz BW**





- **Waveform continuously recorded** (circular buffer), then **stopped** on trigger (which also catches the state of the coarse counter)

- **Trigger position marked on DLL cells => medium precision timing** and used for Optional **Region of Interest Readout (only few samples read)**

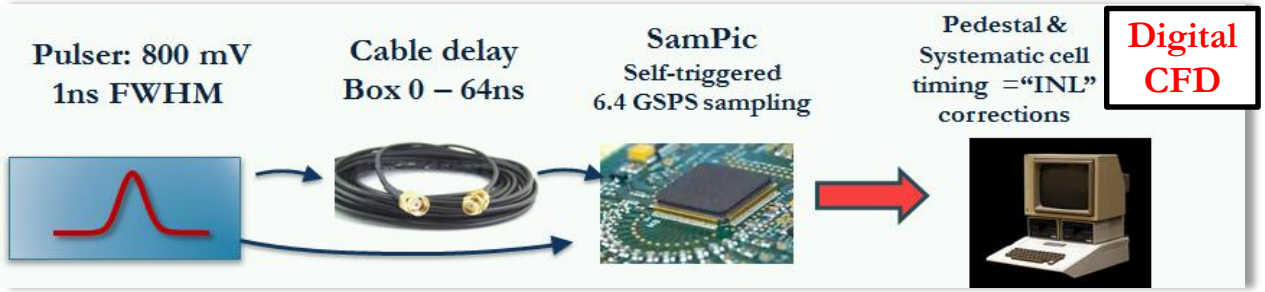


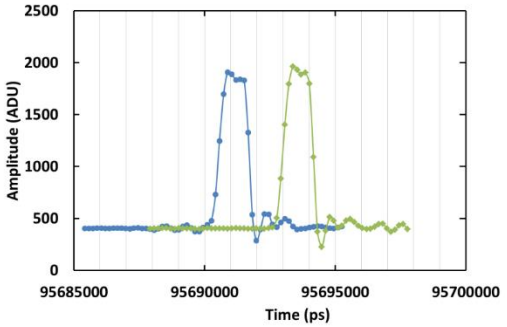
- Conversion by a Wilkinson (ramp) 11 bit ADC for each cell (clocked @1.25GHz)

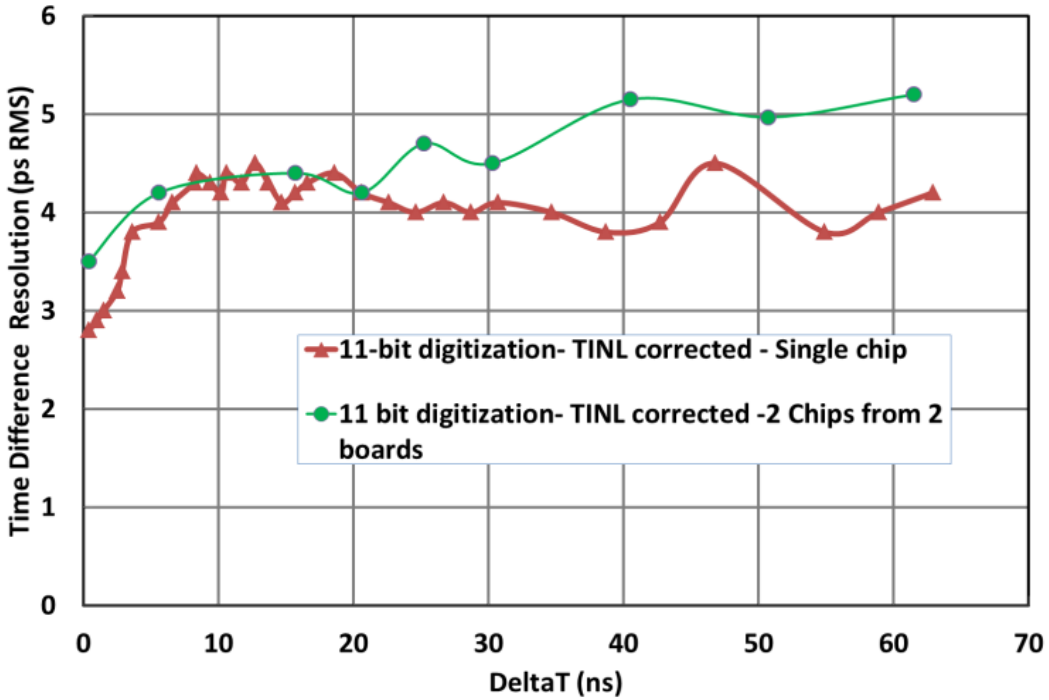
➔ compact and high speed for high precision: a cell/cell transfer function) calibration is required

- 1.6µs conversion time that can be decreased if lower precision is required.

ΔT RESOLUTION VS DELAY







- TDR < 5 ps rms after time correction.
- TDR is constant for Δt > 10ns

- ~ unchanged when using 2 chips from 2 mezzanines (slope here comes from slower risetime of 800ps)

=> measurement are uncorrelated

=> channel single pulse timing resolution is < 3.5 ps rms (5 ps/√2)

From these 2 types of measurements, we could extract the jitter from the motherboard clock source: ~ 2.2 ps rms

=> SAMPIC's own jitter < 2.5 ps rms

TIMING RESOLUTION (DIGITAL CFD) VS ADC NUMBER OF BITS

- ADC conversion can be sped up (by decreassing the resolution): factor 2 for 10 bits (800 ns), 4 for 9 bits (400 ns), 8 for 8 bits (200 ns), 16 for 7 bits (100 ns).

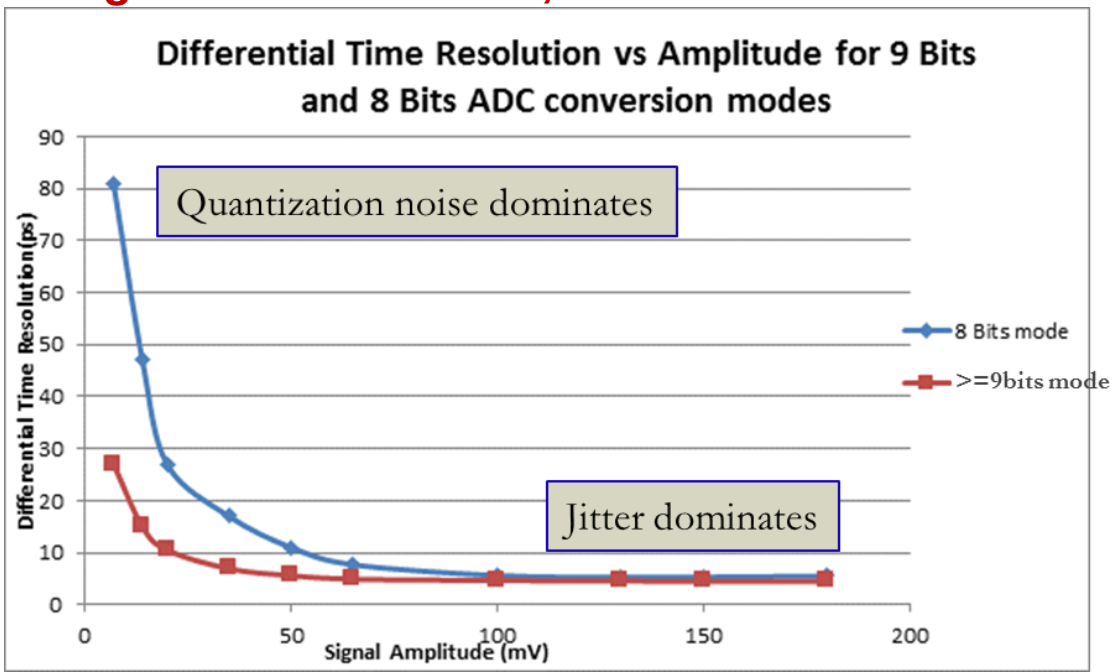
  ➔ decrease of channel dead time

- The quantization noise could affect the timing precision especially for small signals

But QN= 400µVrms for 9bit mode negligible compared to SAMPIC noise = 950µVrms

- **As expected no significative change measured for 11, 10 and 9-bit modes**

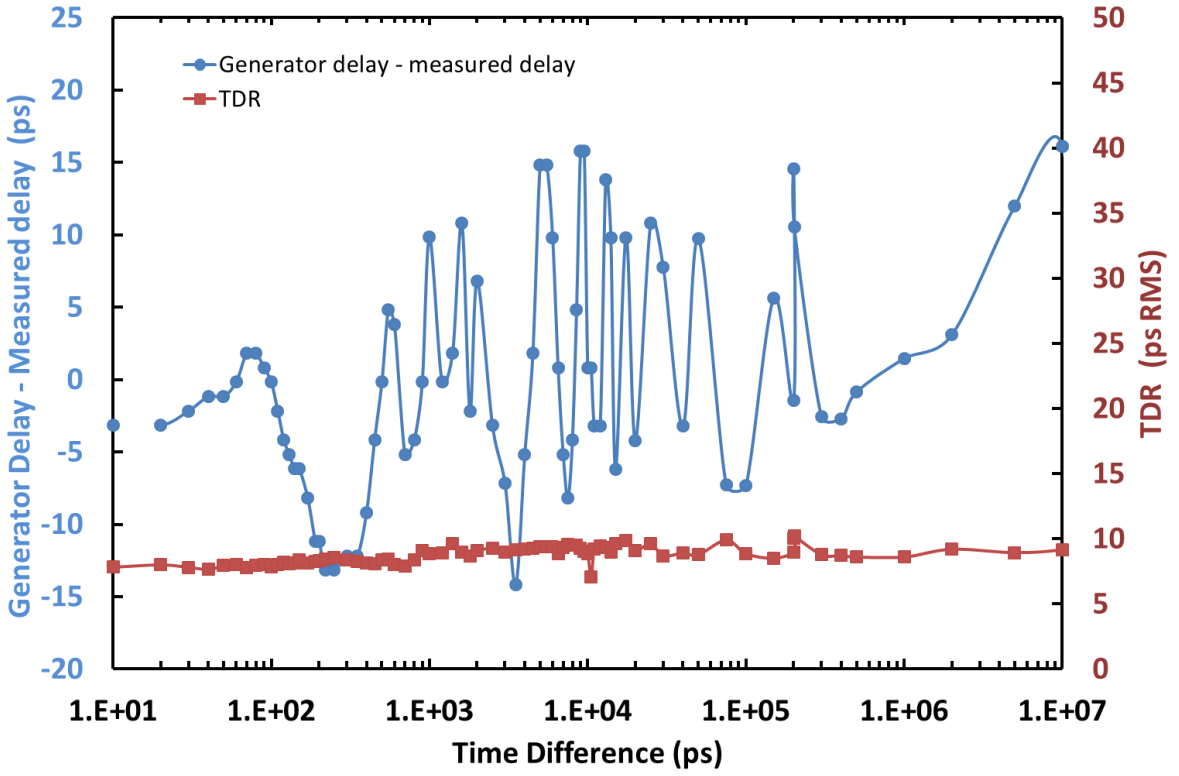
No degradation on timing for pulses above 100mV for 8 bits



EXPLORING LARGER DELAYS: TOWARD AN « ABSOLUTE » TIME MEASUREMENT

- Now we use 2 channels of a TEK AFG 3252 arbitrary waveform generator and program their relative delay (10-ps steps)
- Slower than the previous generator (2.5ns risetime min)
- TEK AFG 3252 is specified for an absolute precision of few 10 ps delay and a 100ps jitter

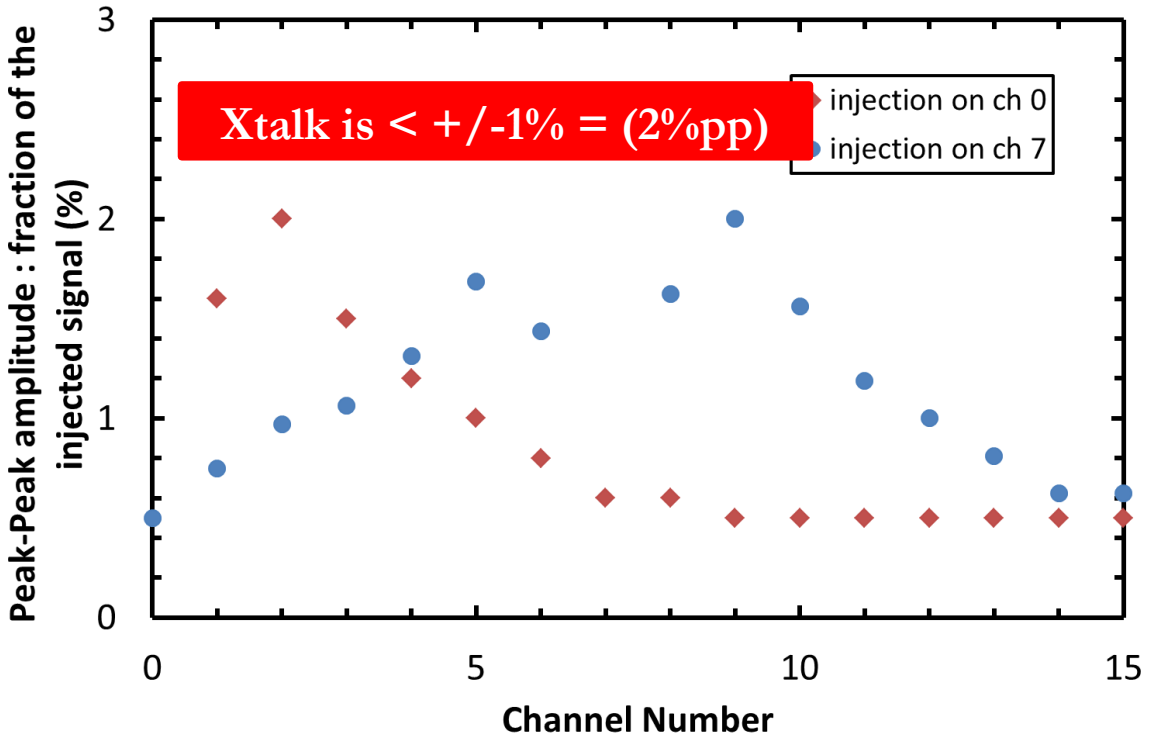
=> Measurements are clearly MUCH MORE better



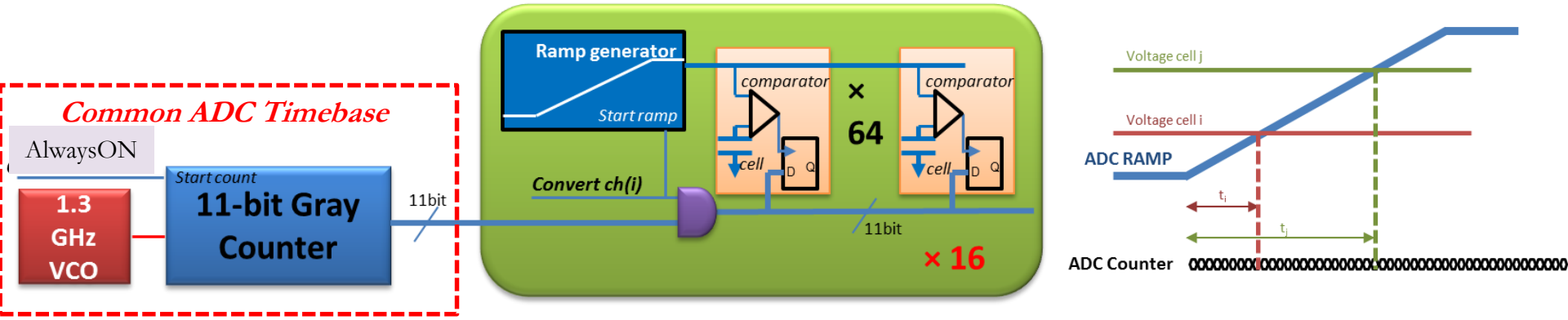
- TDR is < 10ps rms, even for delays up to 10 µs => 1-ppm RESOLUTION
- Difference between AFG programmed delay and measured value is < +/-15ps

SAMPIC_V0: XTALK MEASUREMENT

- 800mV, 1ns FWHM, 300ps risetime and falltime injected on **channel 7 (blue)**
- Signal measured on the other channels
- Xtalk = derivative and decrease as the distance to the injection channel
- Xtalk signal is bipolar with ~ equal positive and negative lobe
- Similar plot, but shifted if injection in another channel **(red)**



WILKINSON ADC WITH AUTO-CONVERSION MODE



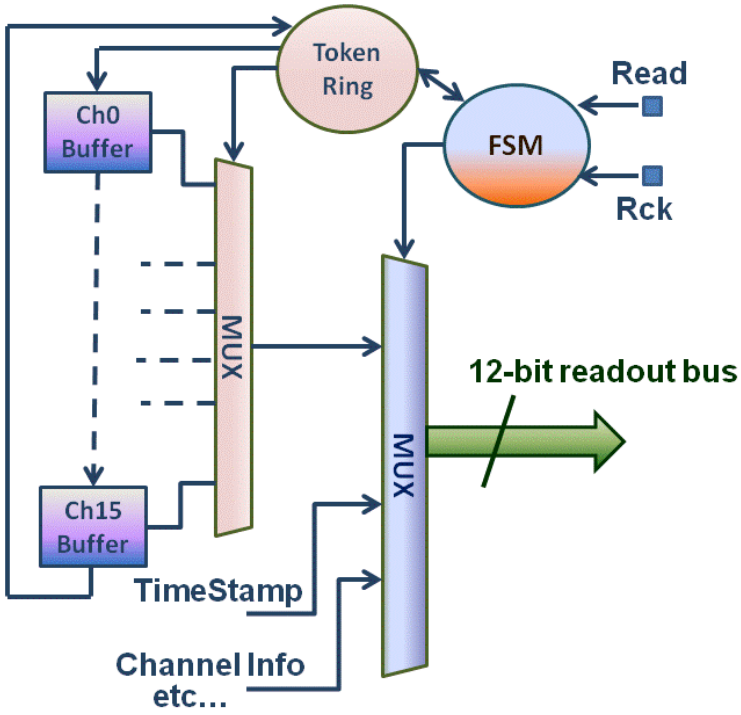
- **When triggered, each channel launches its auto-conversion.**
  - When ramp starts, the value of the continuously running counter is sampled in a dedicated channel register
  - When the ramp crosses the cell voltage => the current value of the counter is stored in the cell register (ramp offset).
  - **As soon as all discriminators of the channel have fired, Analog to Digital conversion of the channel is over => optimization of dead time**
  - During readout, the ramp offset is read before the channel waveform samples.

In "auto-conversion" mode , the ramp offset will be subtracted from the value of the waveform samples.

READOUT PHILOSOPHY

- Readout driven by **Read** and **Rck** signals => **controlled by FPGA**
- Data is read **channel by channel** as soon it is available
- Rotating **priority mechanism** to avoid reading always the same channel at high rate
- **Optional Region Of Interest readout** to reduce the dead time (**nb of cells read can be chosen dynamically**)
- Readout of converted data through a 12-bit parallel LVDS bus including:
  - Channel Identifier, Timestamps, Trigger Cell Index
  - The cells (all or a selected set) of a given channel sent sequentially
  - Standard readout at 2 Gbits/s

  => **Rate > 2 Mevts/s (full waveform)**



- **Channel is not in deadtime during readout, only during conversion (data register is really a buffer stage)**

CALIBRATION PHILOSOPHY

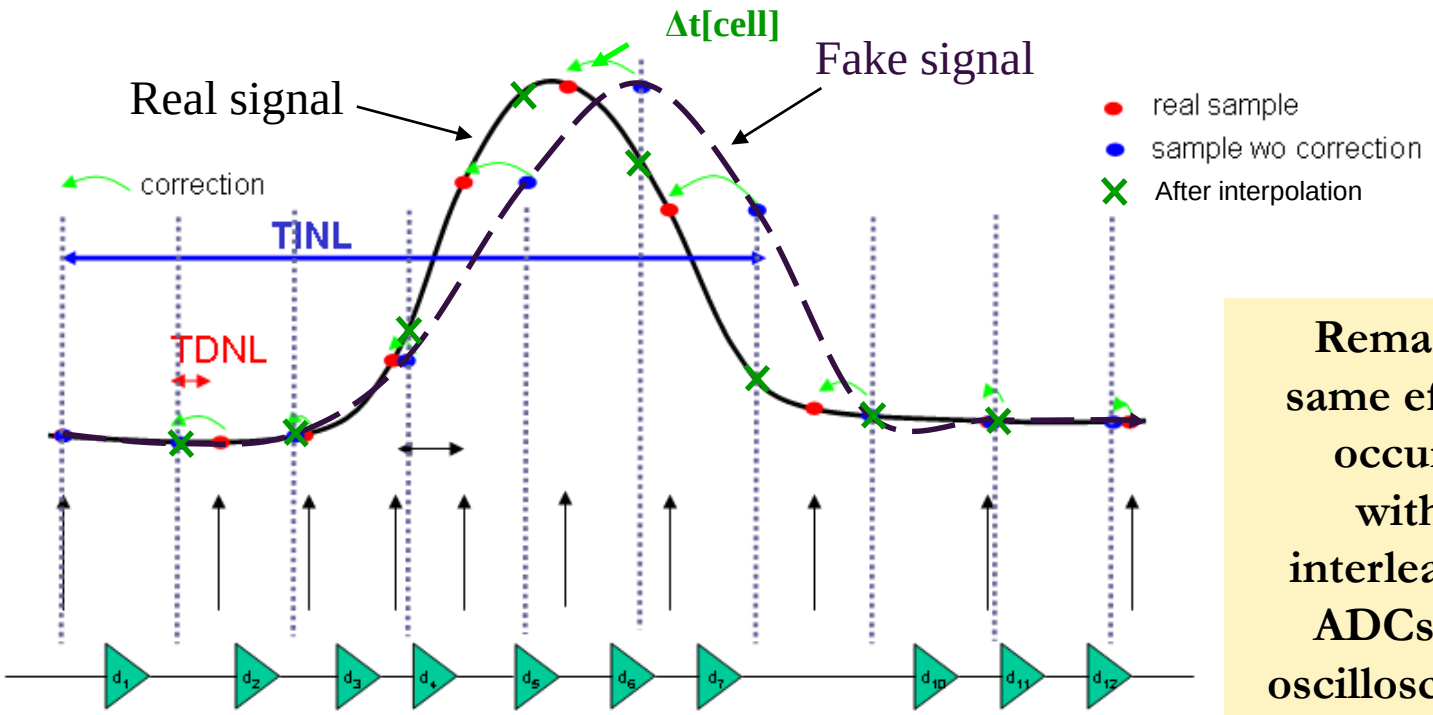
- SCAs-based chips exhibit reproducible non-idealities which can be easily corrected after calibration:
  - The goal is to find the set with the **best performance/complexity ratio**.
  - But also to find the right set for the **highest level of performance**.
- SAMPIC actually offers very good performance with only two types of simple calibrations :
  - **Amplitude: cell pedestal and gain** (**linear** or **parabolic** fit) => DC ramp
  - **Time: INL** (one offset per cell) => use of a **simple sinewave** (see backup)
  - This leads to a limited volume of standard calibration data (**4** to **6** Bytes/cell/sampling frequency => **5** to **8** kBytes/chip/sampling frequency) => can be stored in the on-board EEPROM (1Mbit).
- These simple corrections could even be applied **in the FPGA**.
- Highest level calibrations permit debugging the chip and pushing the performance to its limit (still unknown).

TIMING NON-LINEARITIES

- Dispersion of single delays => **time DNL**
- **Cumulative effect** => **time INL**. Gets worse with delay line length.
- **Systematic & fixed effect** => non equidistant samples => Time Base Distortion

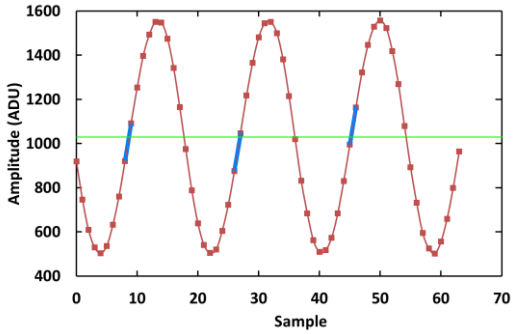
If we can measure it => we can correct it !

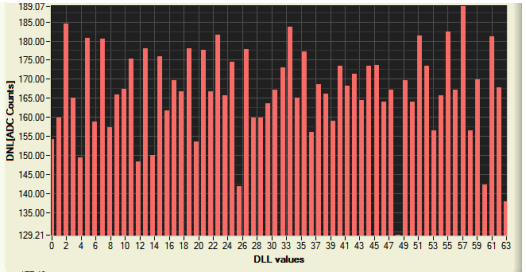
But calibration and even more correction have to remain "simple".

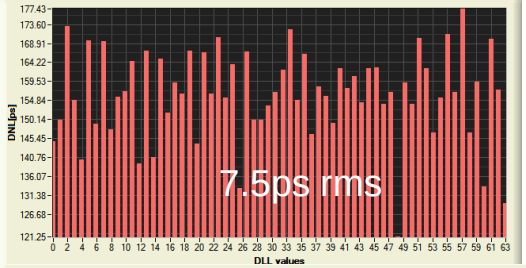


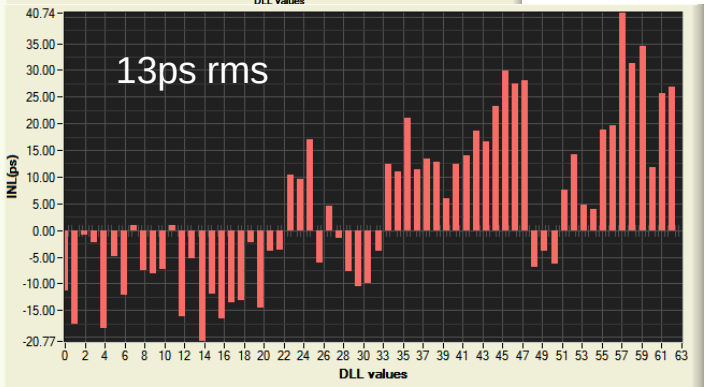
Remark: same effect occurs with interleaved ADCs in oscilloscopes

TIME INL CALIBRATION AND CORRECTION









Method we introduced in 2009 and used since for our analog memories, assuming that a sinewave is nearly linear in its zero crossing region: much more precise than statistical distribution

- Search of zero-crossing segments of a free running asynchronous sine wave

  => length[position]
- Calculate the average amplitude for zero-crossing segment for each cell.
- Renormalize (divide by average amplitude for all the cells and multiply by the clock period/number of DLL steps)

  => time duration for each step = "time DNL"
- Integrate this plot:

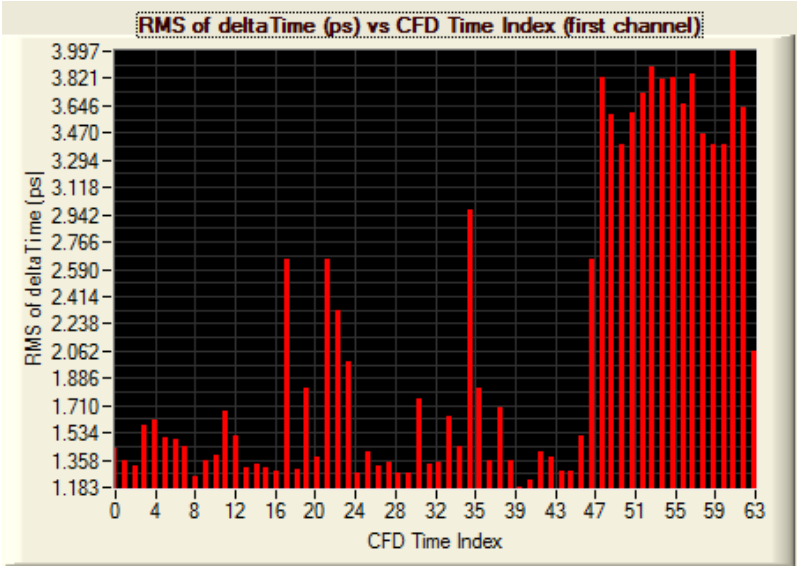
  ⇒ Fixed Pattern Jitter = correction to apply to the time of each sample = "time INL"

Time INL correction:

- **Simple addition** on T_{sample}
- Also permits the calculation of real equidistant samples by interpolation or digital filtering.

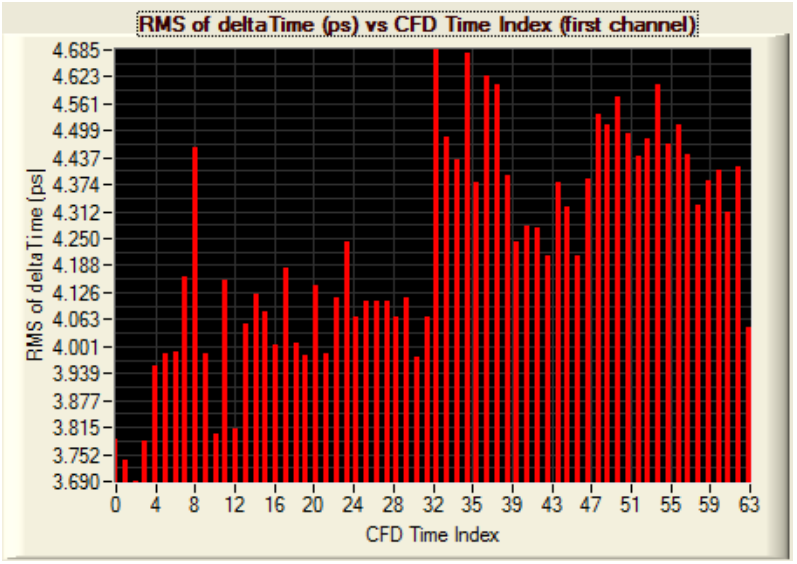
TRICKS FOR UNDERSTANDING RESOLUTION

- This is how we measure the contributions to the resolution: we run at 6.4 GS/s, send two 500 mV pulses separated by 2.5 ns to two channels:
  1. of the same mezzanine
  2. of two different mezzanines



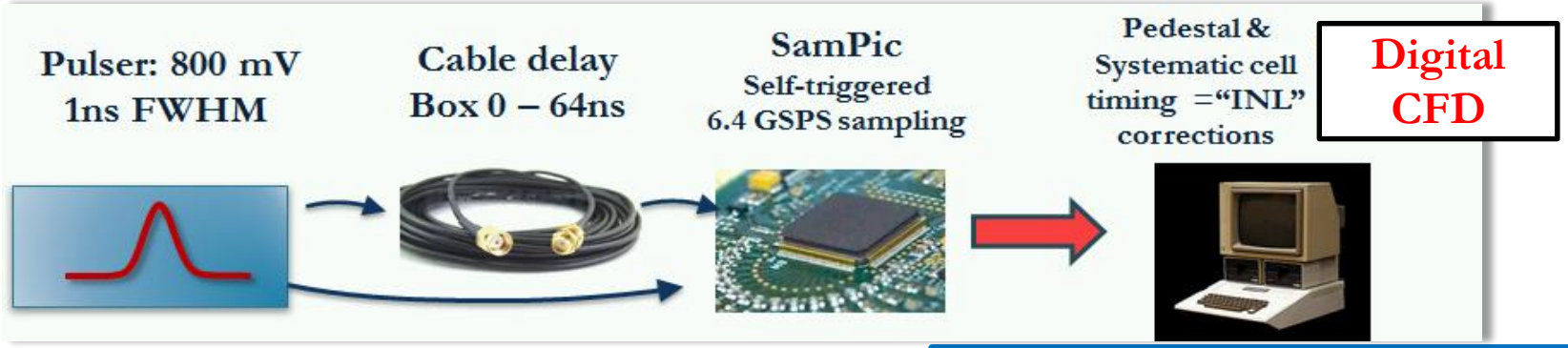
Same chip

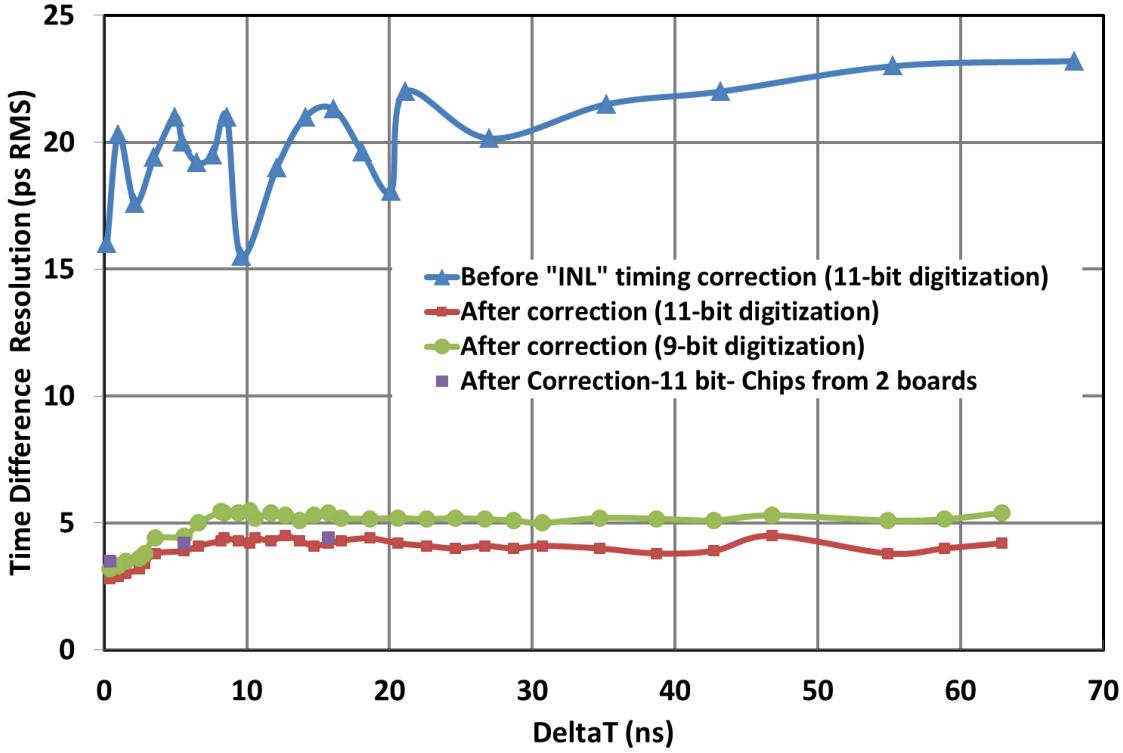
- From this we can extract that **the jitter contribution is:**
- **~ 1.5 ps rms from the DLL**
- **~ 1.8 ps rms from the clock distribution on the motherboard**
- **~ 2.4 ps rms from the clock distribution on the mezzanine**



Different chips

ΔT RESOLUTION VS DELAY





- TDR < 25 ps RMS before time cor.
- TDR < 5 ps RMS after time cor.
- TDR is constant after ΔT=10ns
- Unchanged for 2 chips from 2 different mezzanines (same clk source but different DLLs and on-chip clock path)

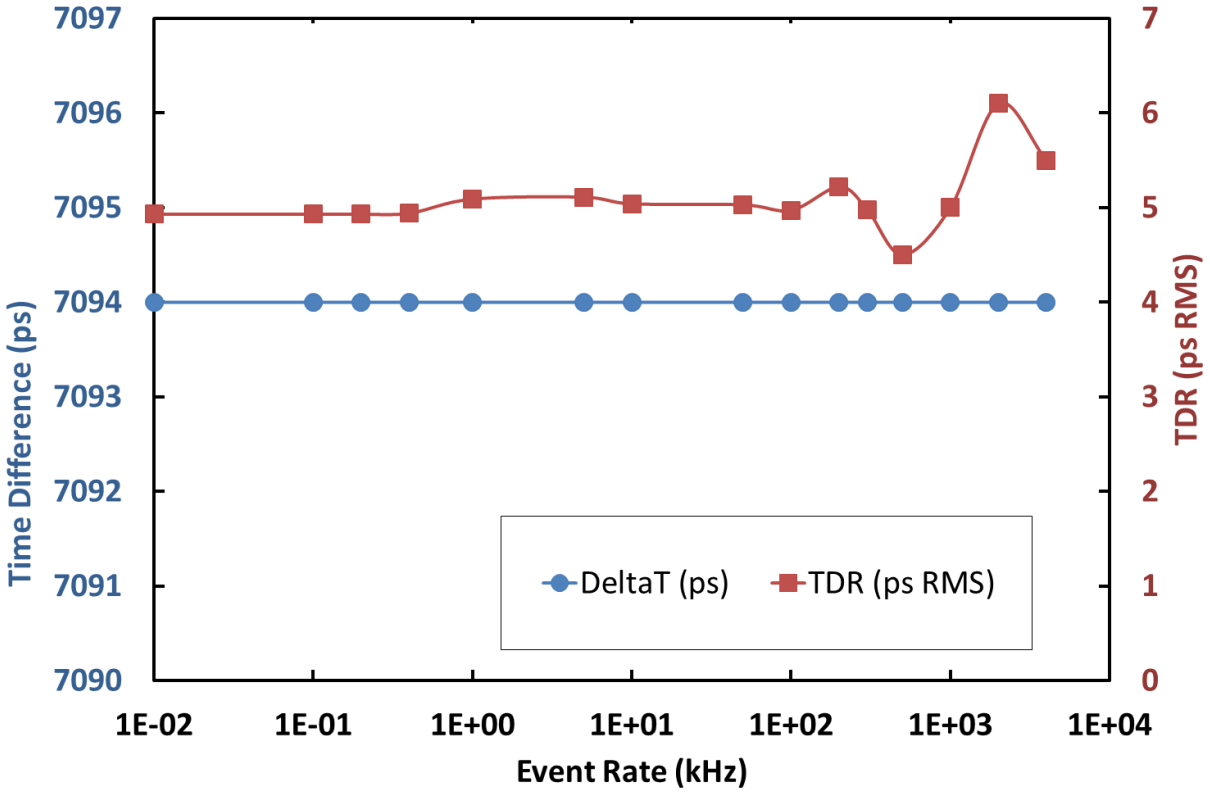
=> Channel single pulse timing resolution is < 3.5 ps RMS (5 ps/√2)

- For these large pulses TDR is worst by only 1ps RMS in 9-bit mode (digitization time divided by 4)

TIMING RESOLUTION VS RATE

1ns FWHM, 400ps risetime, 0.7V signals sent to 2 channels of SAMPIC

- 7.1ns delay by cable, 6.4 GS/s, 11-bit mode, 64 samples, both INLs corrected
- Rate is progressively increased.



The measured delay and its resolution are stable for channel rates up to 2 MHz

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Measurements of timing resolution of ultra-fast silicon detectors with the SAMPIC waveform digitizer

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ABSTRACT

The SAMpler for PICosecond time (SAMPIC) chip has been designed by a collaboration including CEA/IRFU/SEDI, Saclay and CNRS/LAL/SERDI, Orsay. It benefits from both the quick response of a time to digital converter and the versatility of a waveform digitizer to perform accurate timing measurements. Thanks to the sampled signals, smart algorithms making best use of the pulse shape can be used to improve time resolution. A software framework has been developed to analyse the SAMPIC output data and extract timing information by using either a constant fraction discriminator or a fast cross-correlation algorithm. SAMPIC timing capabilities together with the software framework have been tested using pulses generated by a signal generator or by a silicon detector illuminated by a pulsed infrared laser. Under these ideal experimental conditions, the SAMPIC chip has proven to be capable of timing resolutions down to 4 ps with synthesized signals and 40 ps with silicon detector signals.

http://arxiv.org/abs/1604.02385

Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment

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Study of timing characteristics of a 3 m long plastic scintillator counter using waveform digitizers

A. Blondel [a], D. Breton [b], A. Dubreuil [a], A. Khotyantsev [c], A. Korzenev [a] ✉, J. Maalmi [b], A. Mefodev [c], P. Mermod [a] ✉, E. Noah [a]

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Abstract

A plastic scintillator bar with dimensions 300 cm × 2.5 cm × 11 cm was exposed to a focused muon beam to study its light yield and timing characteristics as a function of position and angle of incidence. The scintillating light was read out at both ends by photomultiplier tubes whose pulse shapes were recorded by waveform digitizers. Results obtained with the WAVECATCHER and SAMPIC digitizers are analyzed and compared. A discussion of the various factors affecting the timing resolution is presented. Prospects for applications of plastic scintillator technology in large-scale particle physics detectors with timing resolution around 100 ps are provided in light of the results.

http://arxiv.org/abs/1610.05667