

TimeSpOT

TIME and SPace real-time Operating Tracker



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INFN Torino

17.05.2018, Workshop on pico-second timing detectors for physics and medical applications

1 TimeSpOT Overview

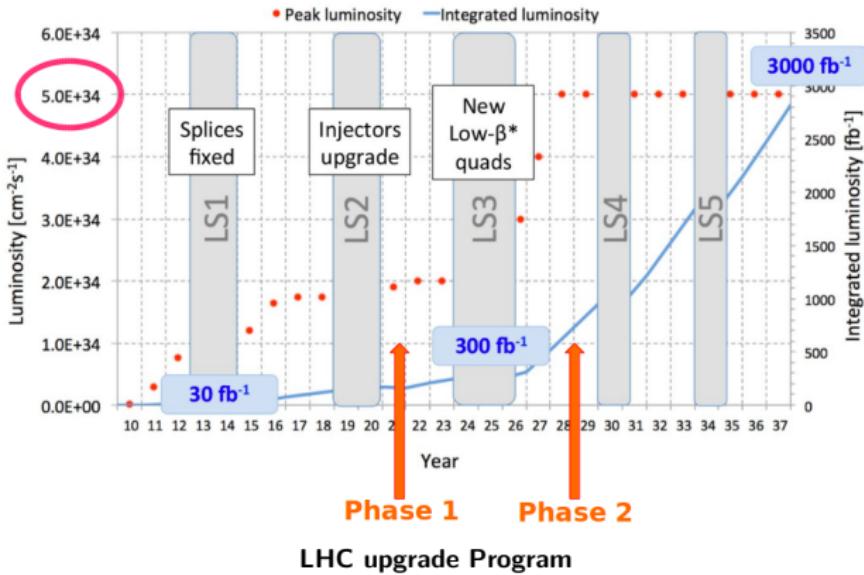
2 TimeSpOT Sensors

3 28nm Front-End Design

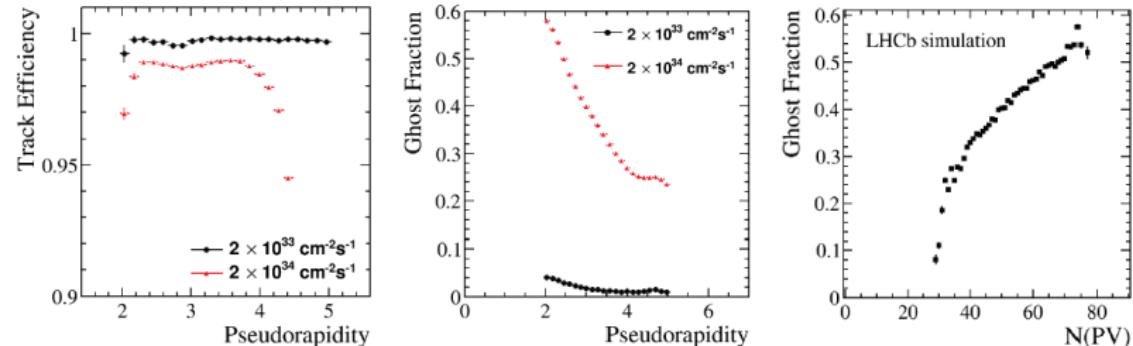
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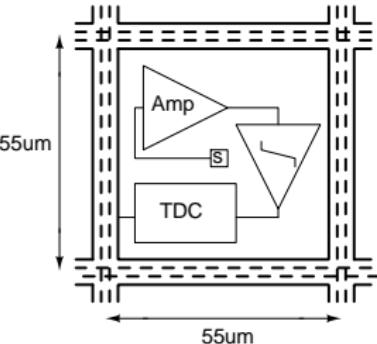
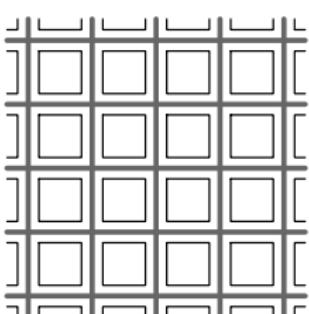
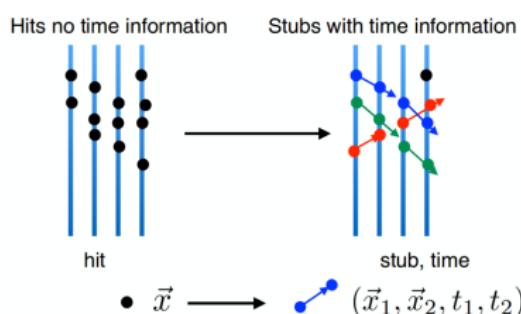
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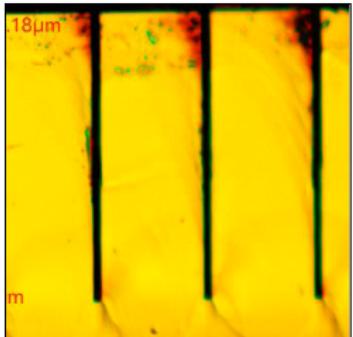
- Measure rare events → peak luminosity increase ($\sim 5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$)
- Pile-up events per bunch crossing increases from 27 to 200 → **loss in tracking efficiency**
- Detectors **radiation hardness** up to $10^{17} \text{ MeV}/\text{cm}^2 n_{eq}$



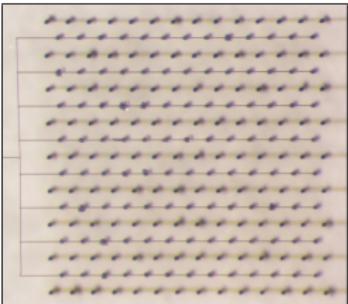
- Tracking efficiency reduced to 96 %
- **Ghost rates** $\sim 2\%$ $\rightarrow 40\%$
- Assigning correct PV essential for precise lifetime measurement
- VELO: **per-hit resolution** $< 200 \text{ ps}$ $\rightarrow 6.5\text{ps}$ PV resolution



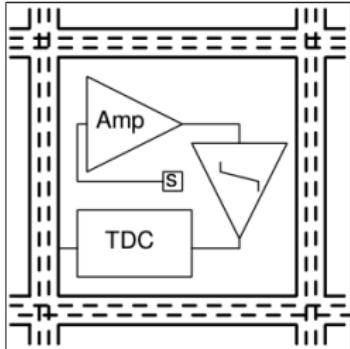
- TIMPESPO_T: R&D a **4D Tracking** Detector Prototype
- Requirements:
 - Pixel pitch $(55 \times 55)\mu m$
 - **Time resolution** on single hit < 100 ps
 - Radiation resistance: 10^{16} to $10^{17} n_{eq}/cm^2$
- System level solution → sensor, **front-end electronics** and tracking logic
- 10 INFN research unit with 25 FTE involved



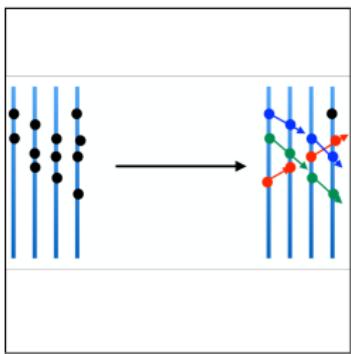
WP 1: Si 3D Sensor



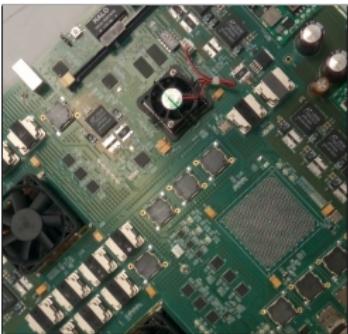
WP 2: Diamond 3D Sensor



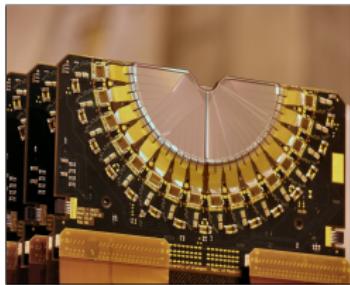
WP 3: 28nm Front-End ASIC



WP 4: Tracking Logic



WP 5: High Speed Readout Board

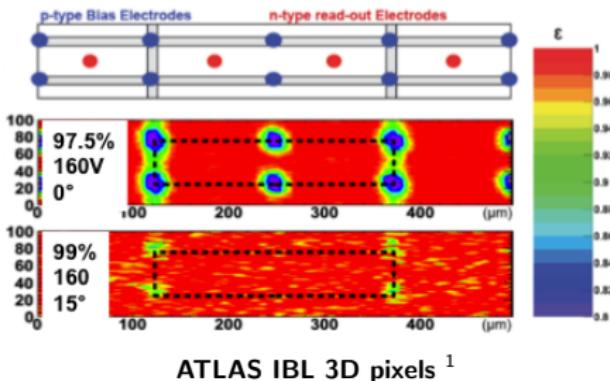
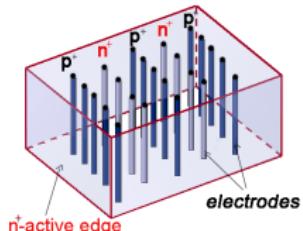


WP 6: System Integration & Testing

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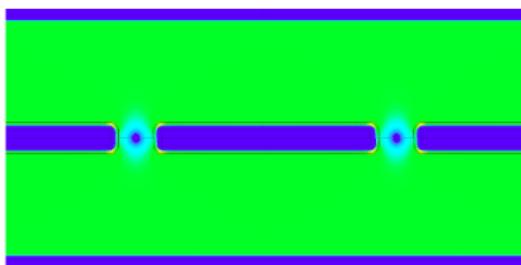
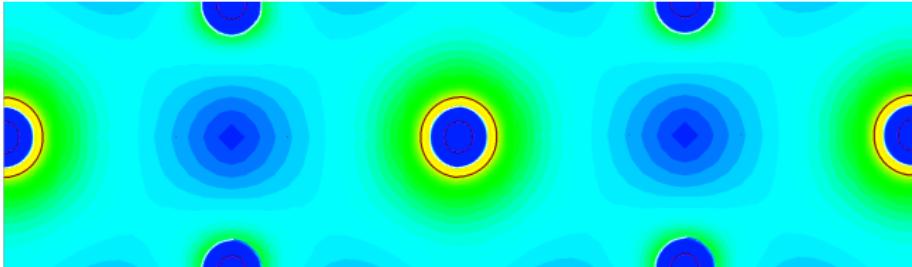
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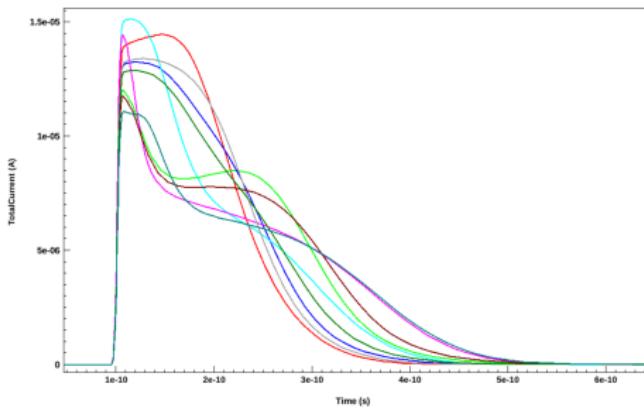
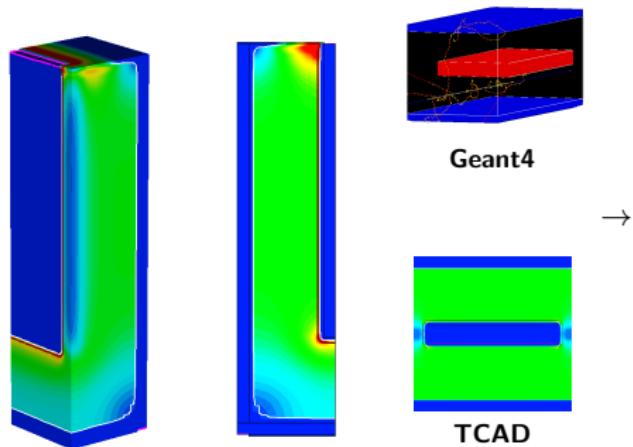


- **3D Sensors: electrodes extends in the whole sensor volume**
 - electrode distance (l) decoupled from active substrate thickness (d):
 - short l : high radiation hardness, fast signals, low bias voltage
 - signal amplitude decoupled from collection time: possible excellent timing performance
- **3D pixel with columnar electrodes:**
 - successfully used at LHC: ATLAS IBL, CT-PPS and ATLAS-AFP tracking systems
 - rad-hard up to $\sim 10^{16} \text{ } n_{eq} \text{ cm}^{-2}$

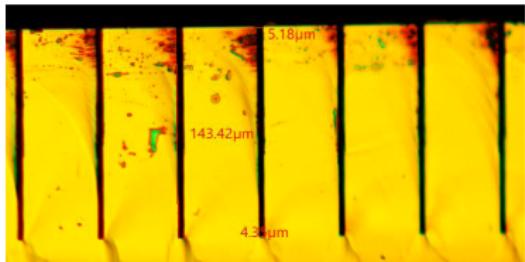
¹J. Lange et al., Radiation hardness of small-pitch 3D pixel sensors up to HL-LHC fluences, talk given at TIPP 2017, Beijing



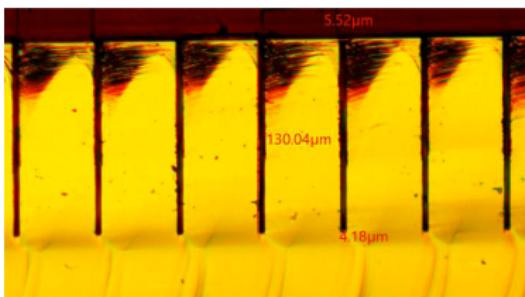
- Presence of **low-field zones** → **signal variability** → bad for timing
- Shape optimization → **trench** shaped electrodes:
 - segmented signal electrodes
 - long common bias electrodes



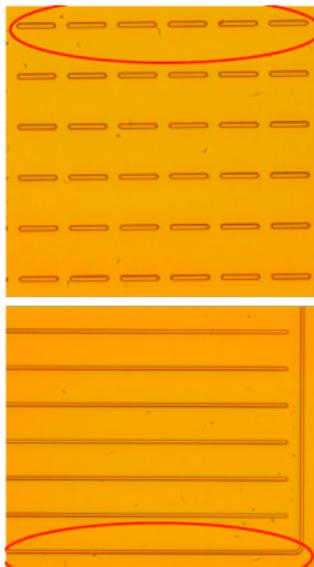
- Pixel cell size: $(55 \times 55 \times 150)\mu m^3$
- Radiation-mater interaction simulation → *Geant4*
- Sensor simulation (field & charge migration) → *TCAD*
- Simulated current pulses → used in front-end simulation



143 μm depth, width: 5.2 μm top 4.4 μm bottom



130 μm depth, width: 5.5 μm top 4.2 μm bottom



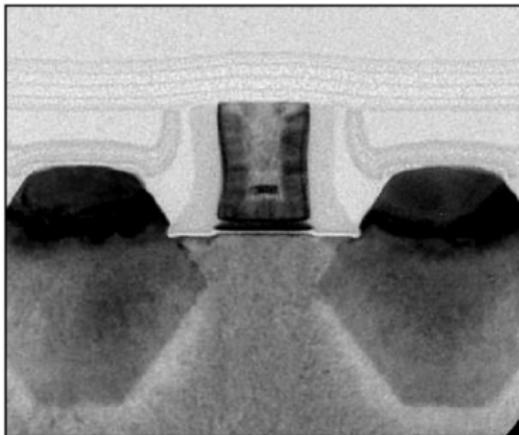
Top view

- Produced by *FBK* Trento in march 2018
- 6 μm nominal trenches width → **width modulation** due to *DRIE*
- *Vacuum bake* → improved **uniformity**
- Mechanically stable

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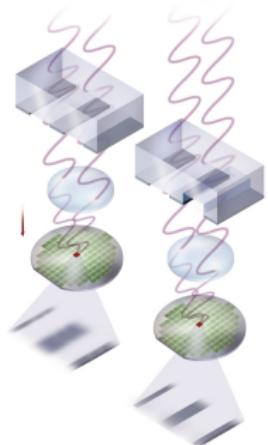
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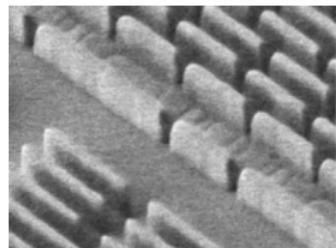
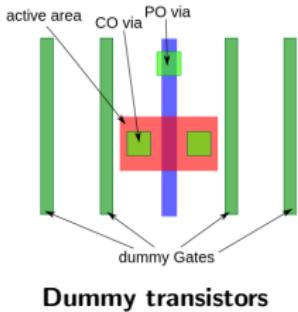


PMOS with Si-Ge diffusions (eSiGe), HK dielectric and Metal Gate (HKMG)

- **New technology** in the radiation detectors field
- More compact and power efficient → new integration possibilities
- **New materials** adopted in order to maintain good scaling
- Reduced power supply voltage → **less headroom for analog circuits**
- **New manufacturing process...**

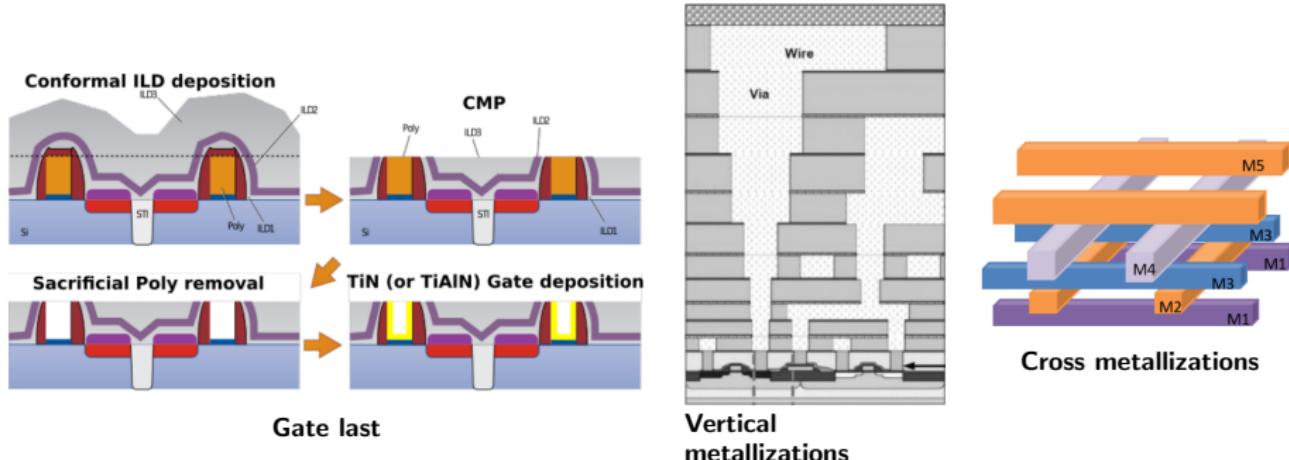


concept of PSM

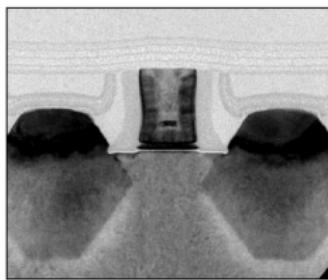


regular fabrics

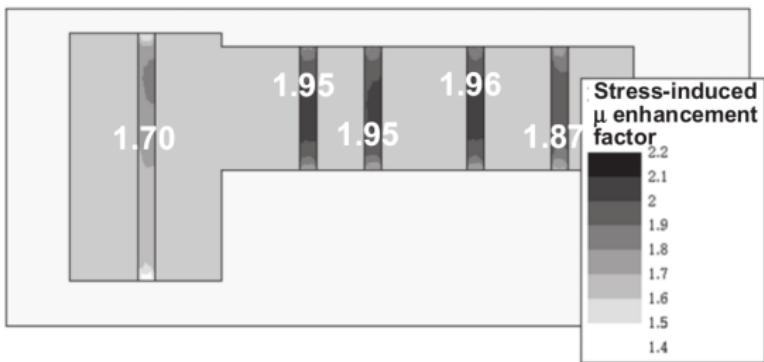
- Sub-diffraction-limit features → **interference lithography**
- **PSM:** interference of phase-shifted light → requires **regular layout**:
 - same direction gates
 - regular gate pitch (per block)
 - regular gate length (per block)
 - **dummy transistors** between blocks



- HK insulator compatibility & Work Function Engineering → **different gate materials** for NMOS and PMOS
- **Gate last** process → good planarization → **CMP (Chemical Mechanical Polishing)**
- CMP requires:
 - gate layer uniformity → **area uniformity** constraints
 - metallization uniformity → increasing metal thickness and cross-metallization

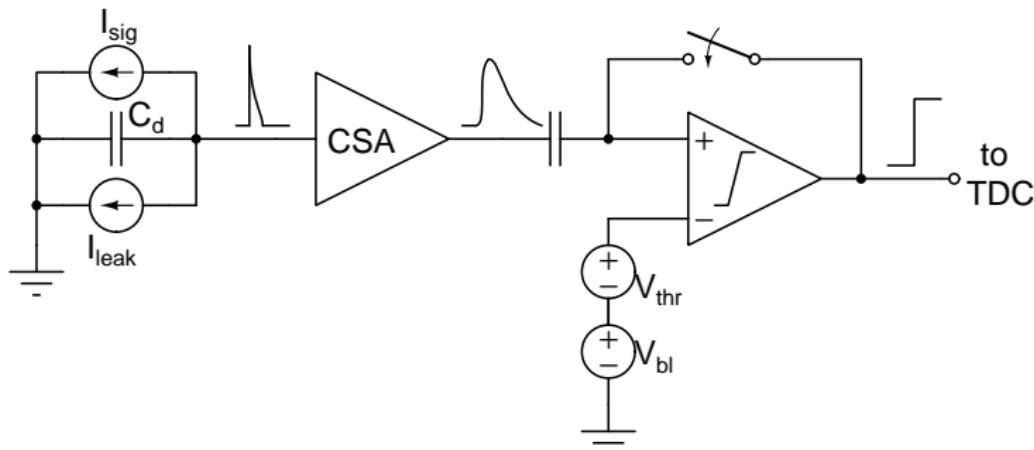


eSiGe

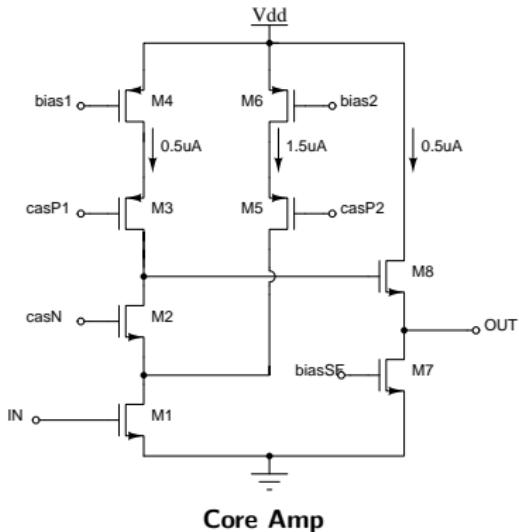
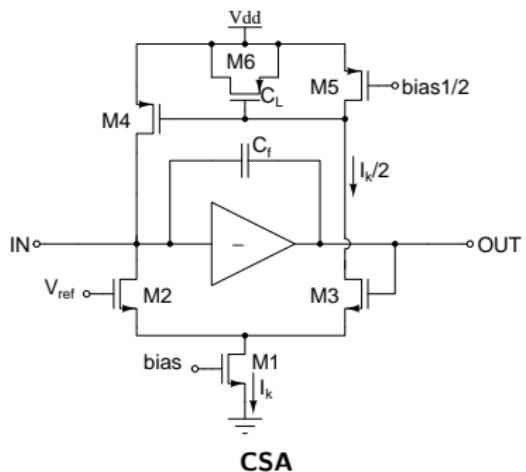


Effect of layout on stress

- PMOS holes **mobility enhancement** by **channel strain** → S and D **diffusions in SiGe**
- Strain effectiveness depends on nearby diffusions → mobility **variability**
- **Layout Dependent Effects** → prevented with regularities in layout

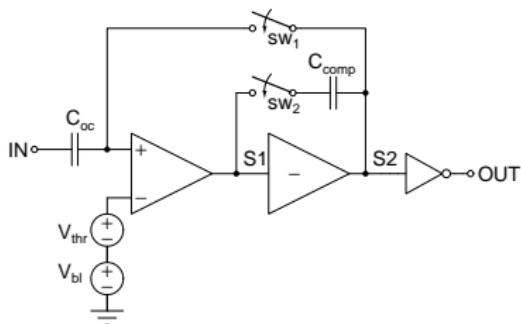
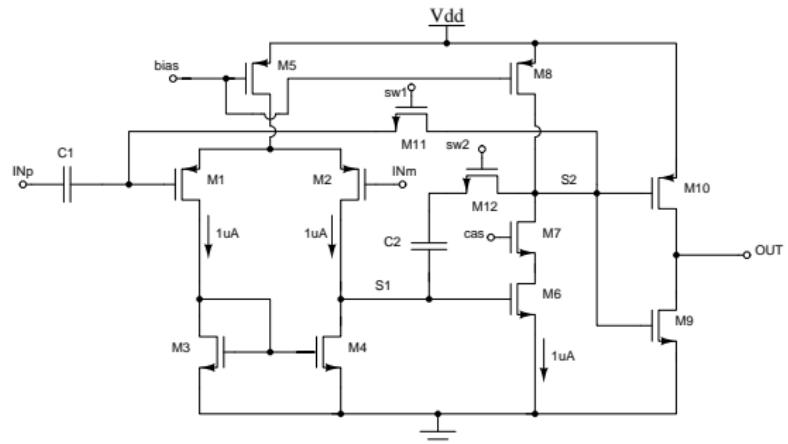


- **Binary front-end with time measure**
- Compact & low-power design
- Sensor modelled with parameters extracted from simulations
- Input amplifier: **Charge Sensitive Amplifier** with DC current compensation and DC voltage setting
- Discriminator: **Leading Edge Discriminator** with offset compensation



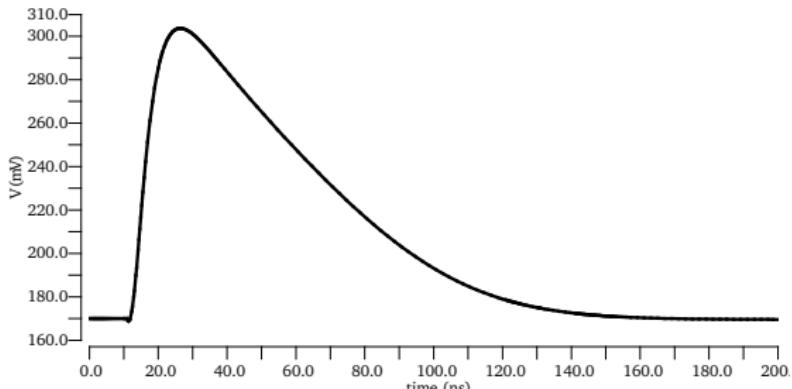
- **CSA:**

- Output **voltage amplitude** \propto **input charge**
- Constant peaking and falling times \rightarrow **good timing performance**
- **Low noise**
- **Krummenacher Filter:** active feedback & DC current compensation for **input leakage current**

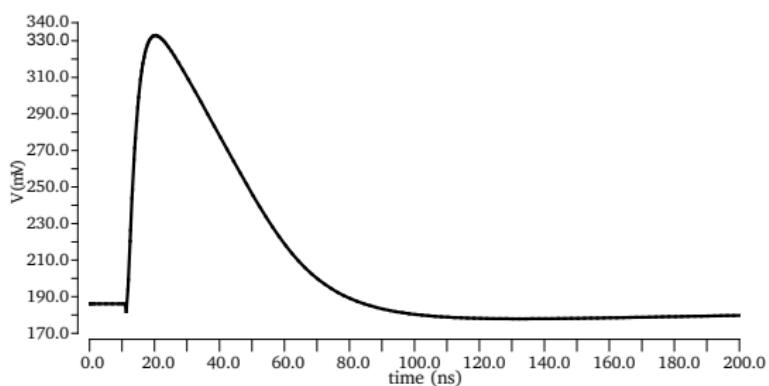
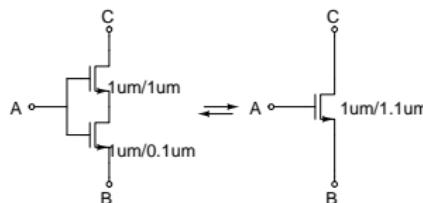


- 2 stages amplification:
 - 1st stage: **low gain, differential**
 - 2nd stage: **high gain**, single ended
- Inverter → **digital output buffer**
- **Offset Correction Circuit:** store offset variability inside C_{oc}
 - **correct intra-channels variability**
 - set input DC level

Passage to the 28nm Design



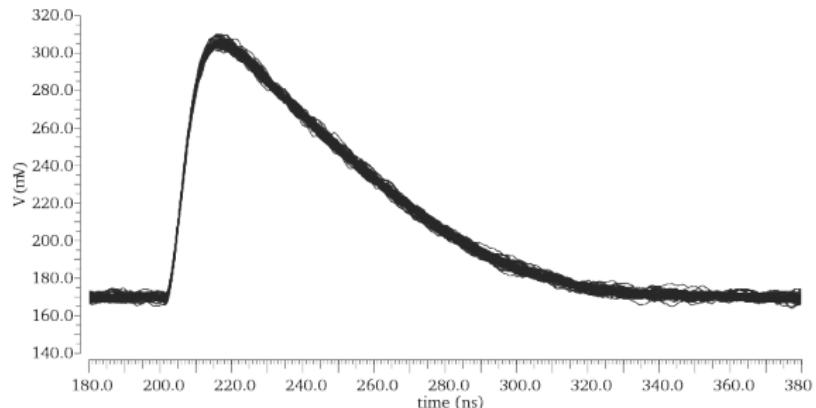
65 nm



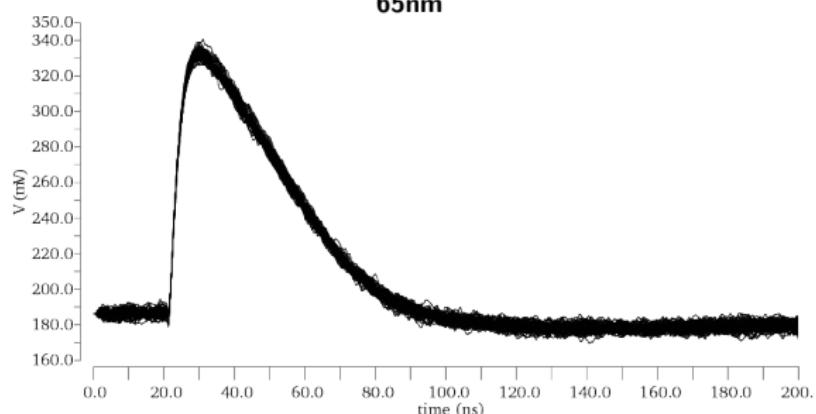
28 nm

- CSA successfully ported to the 28 nm node
- All transistors dimensions scaled by a 1/2 factor
- **Regular fabrics** → transistors split

Noise



65nm



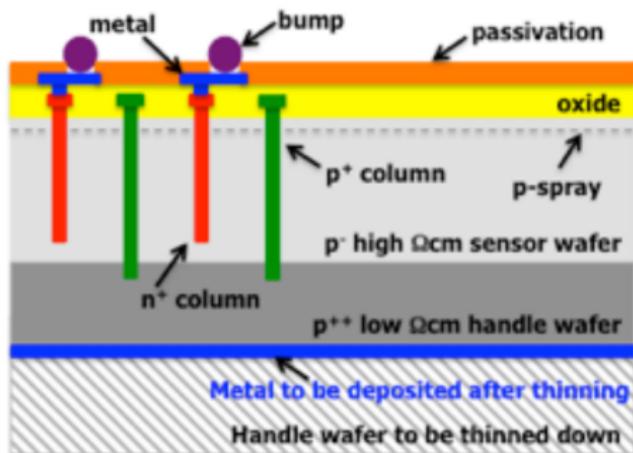
28nm

- Noise induced jitter: $\sigma_{tn} = \frac{T_{pk}}{SNR}$
- In 28 nm, for low range signals: SNR ~ 63 ,
- Simulated $\sigma_{tn} \sim 100$ ps RMS

- TIMESPOT is an INFN project dedicated to vertex trackers in Hi-Lumi environments
- It will operate in the years 2018-2020 with 6 WPs and a system-level approach
- 3D sensor design and technology tests are almost concluded
- first 3D sensors batches will be available in fall of this year for testing
- first 28-nm CMOS front-end prototype, with test structures and circuits are scheduled for October 2018

Thank you for your attention

Backup



- Single side process
- Signal electrodes connection with front-end on top with bump bonding
- Bias voltage supplied from the bottom through a low resistance wafer
- Aspect ratio up to 30:1 feasible with DRIE
- High breakdown voltage even after irradiation