

Wafer characterization

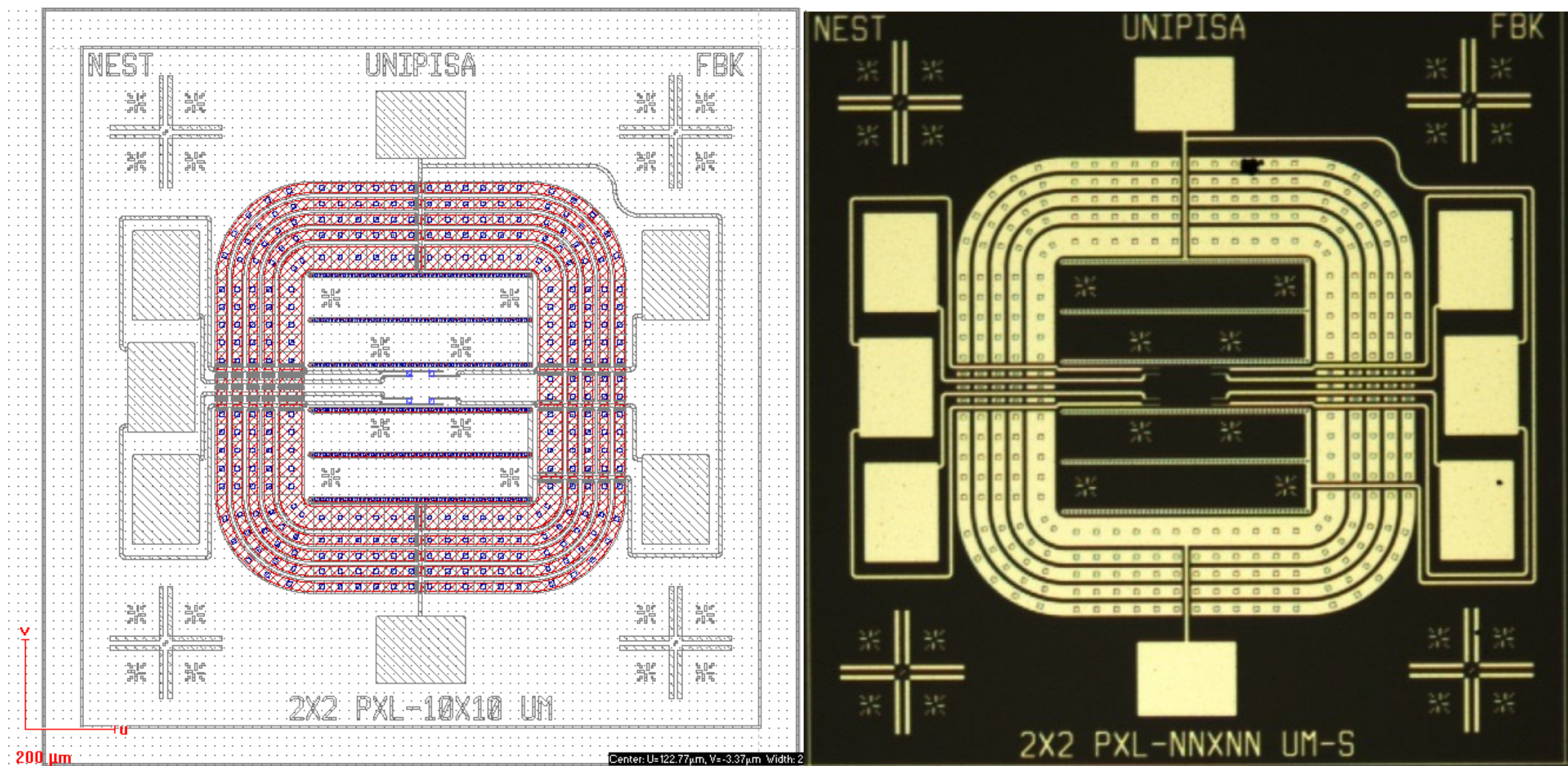
Julius Scherzinger
julius.scherzinger@df.unipi.it

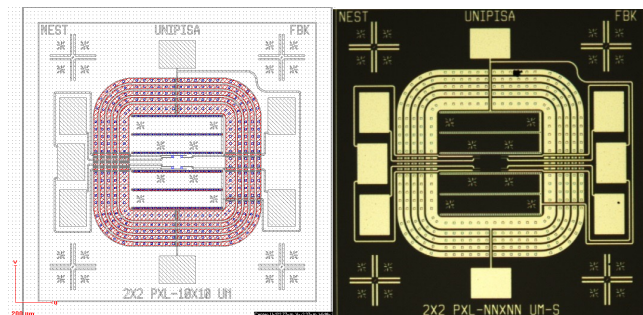
Daniele Goretti
daniele.goretti@pi.infn.it

Project

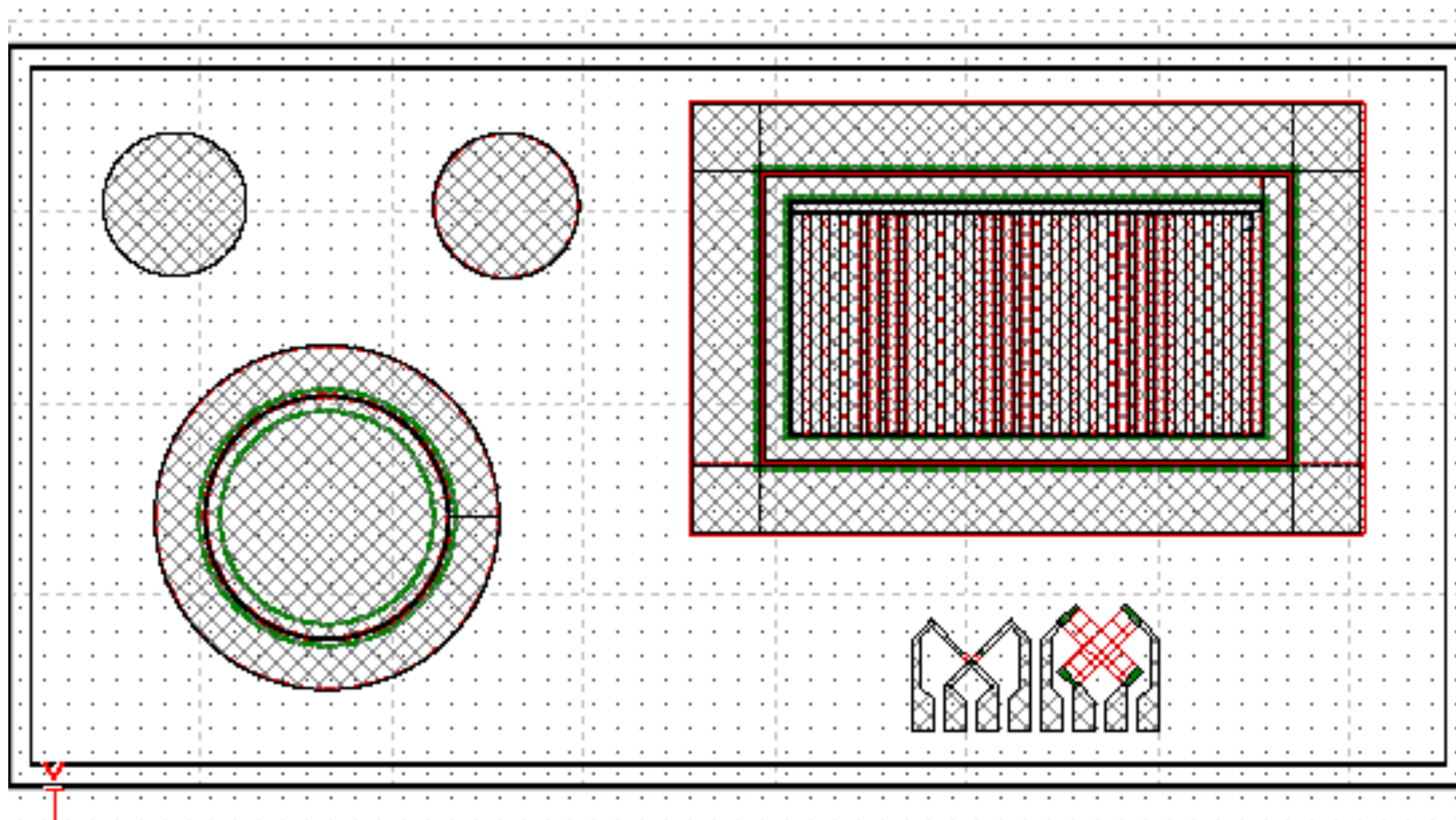
- Test FBK sensor structures
- 2 FBK test structures
 - Diode
 - Gate controlled diode
- Test Instruments in Clean Room
- Optimize LabVIEW VIs for tests in February

Project

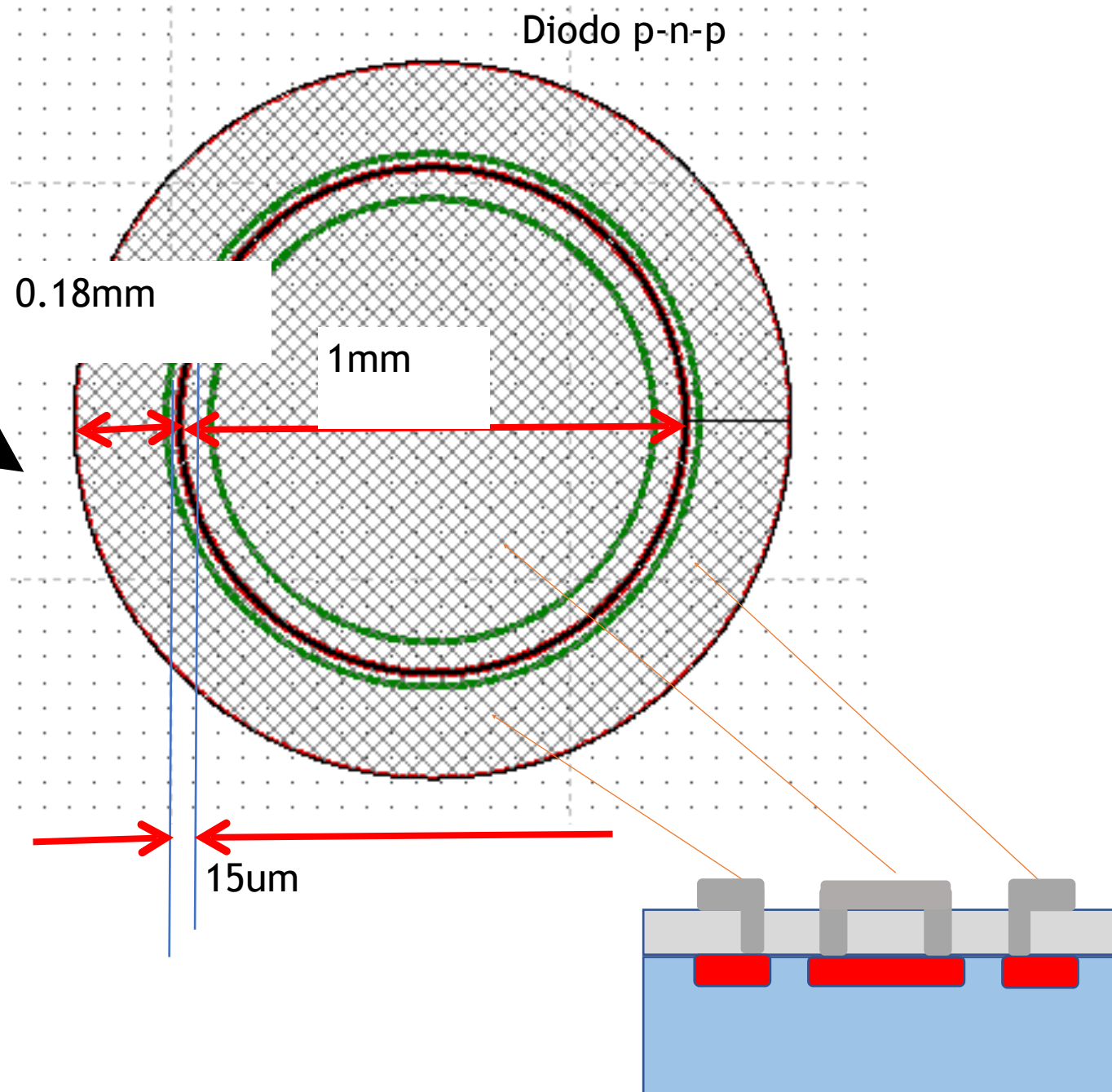
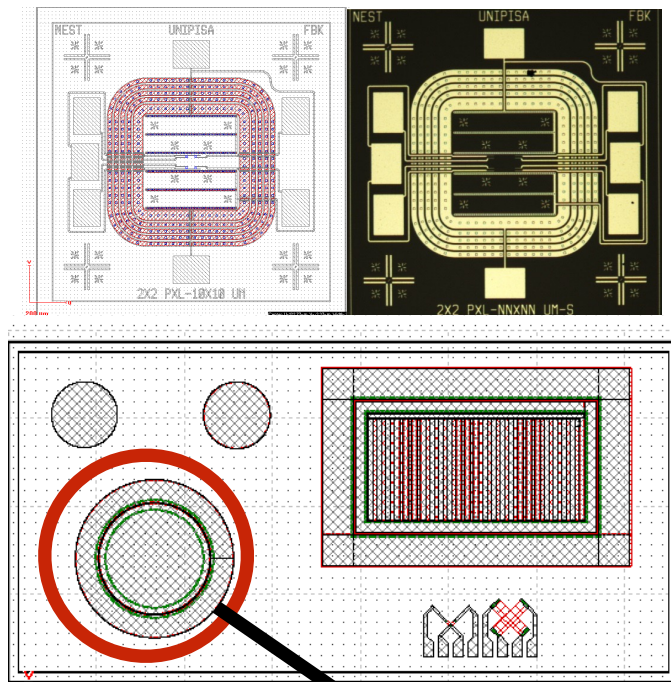




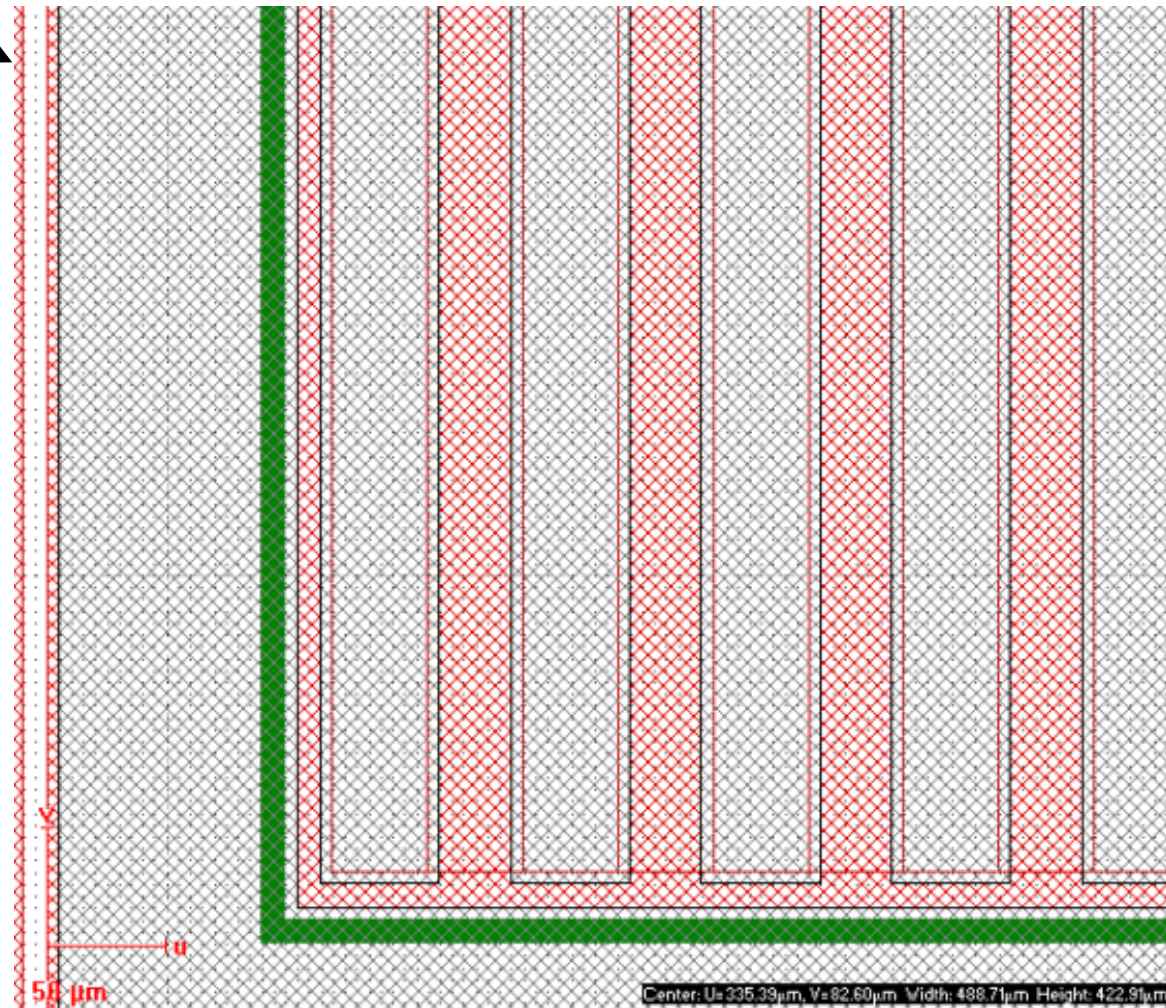
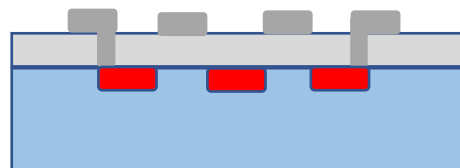
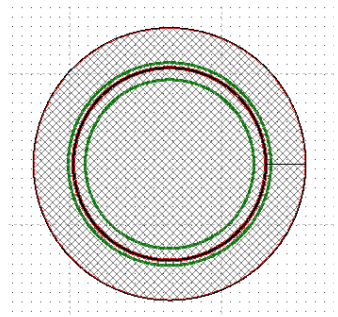
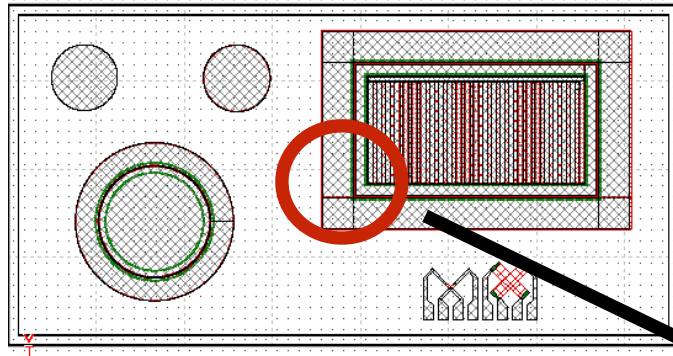
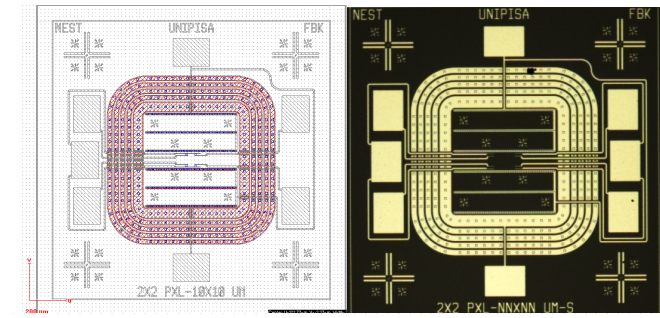
Project



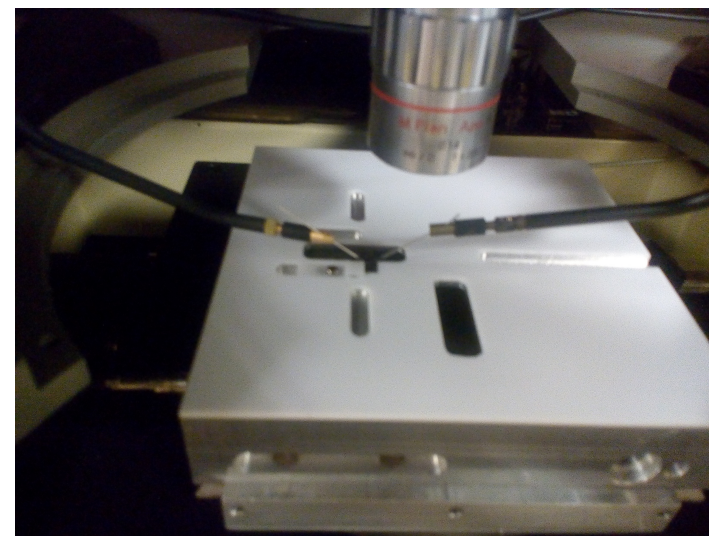
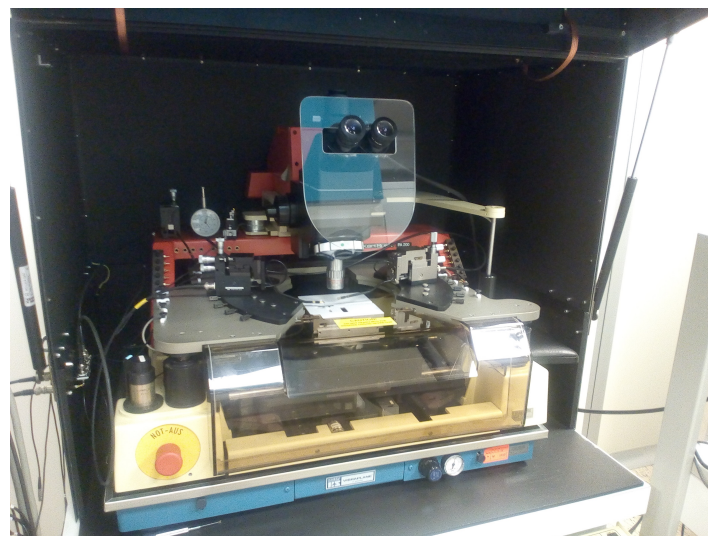
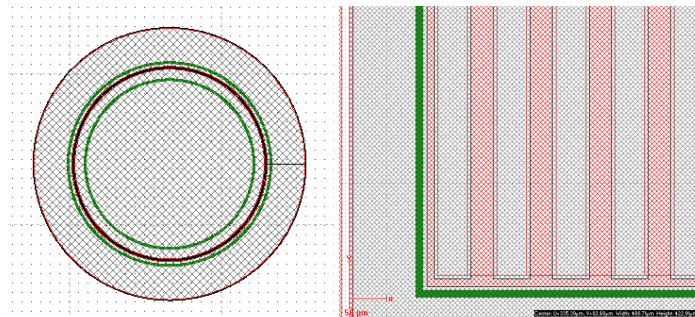
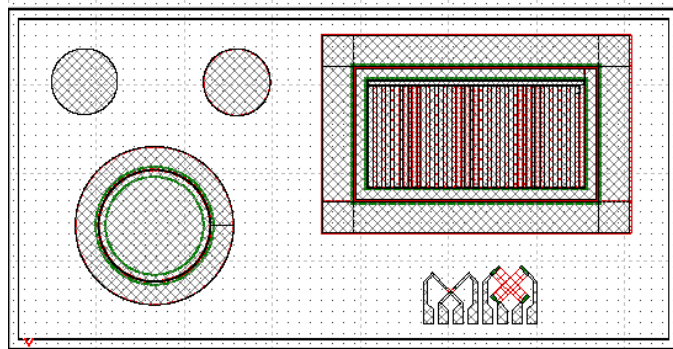
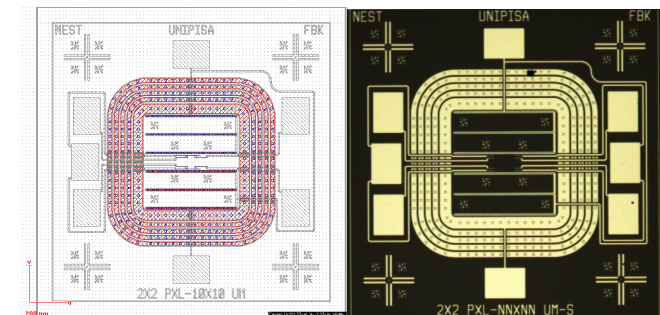
Project



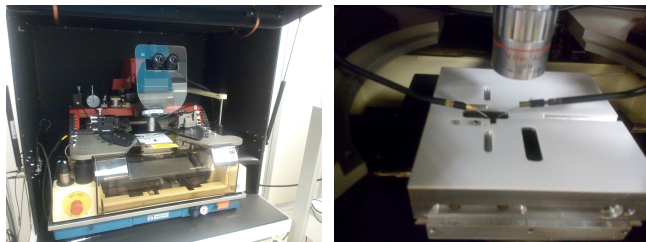
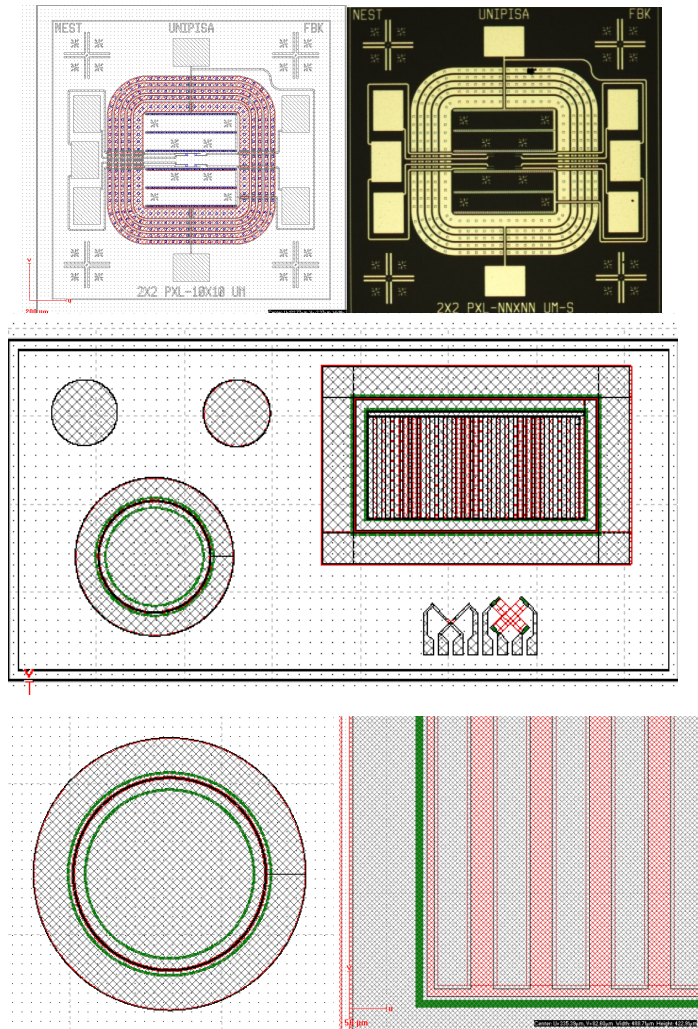
Project



Project



Project

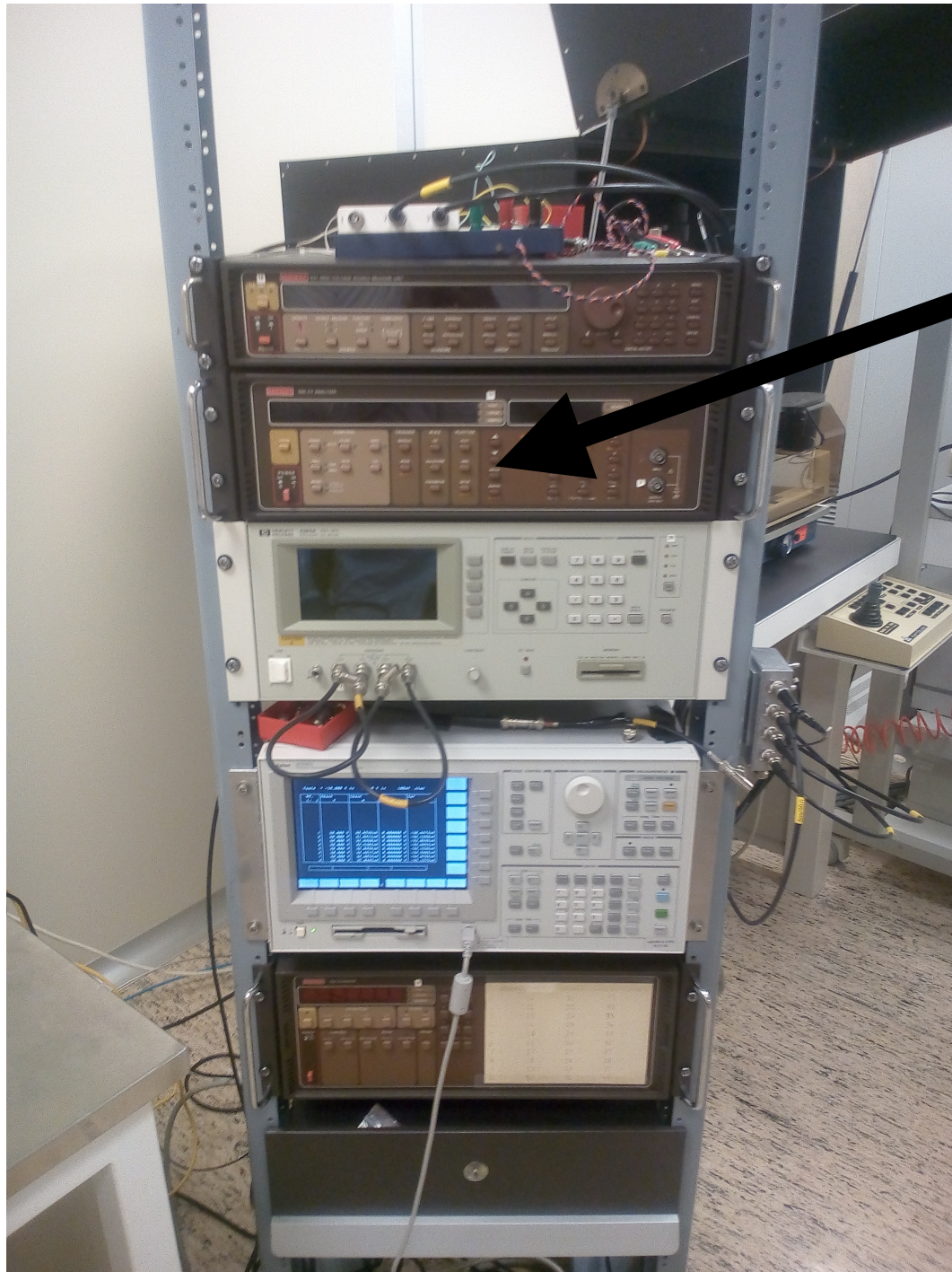


Instruments



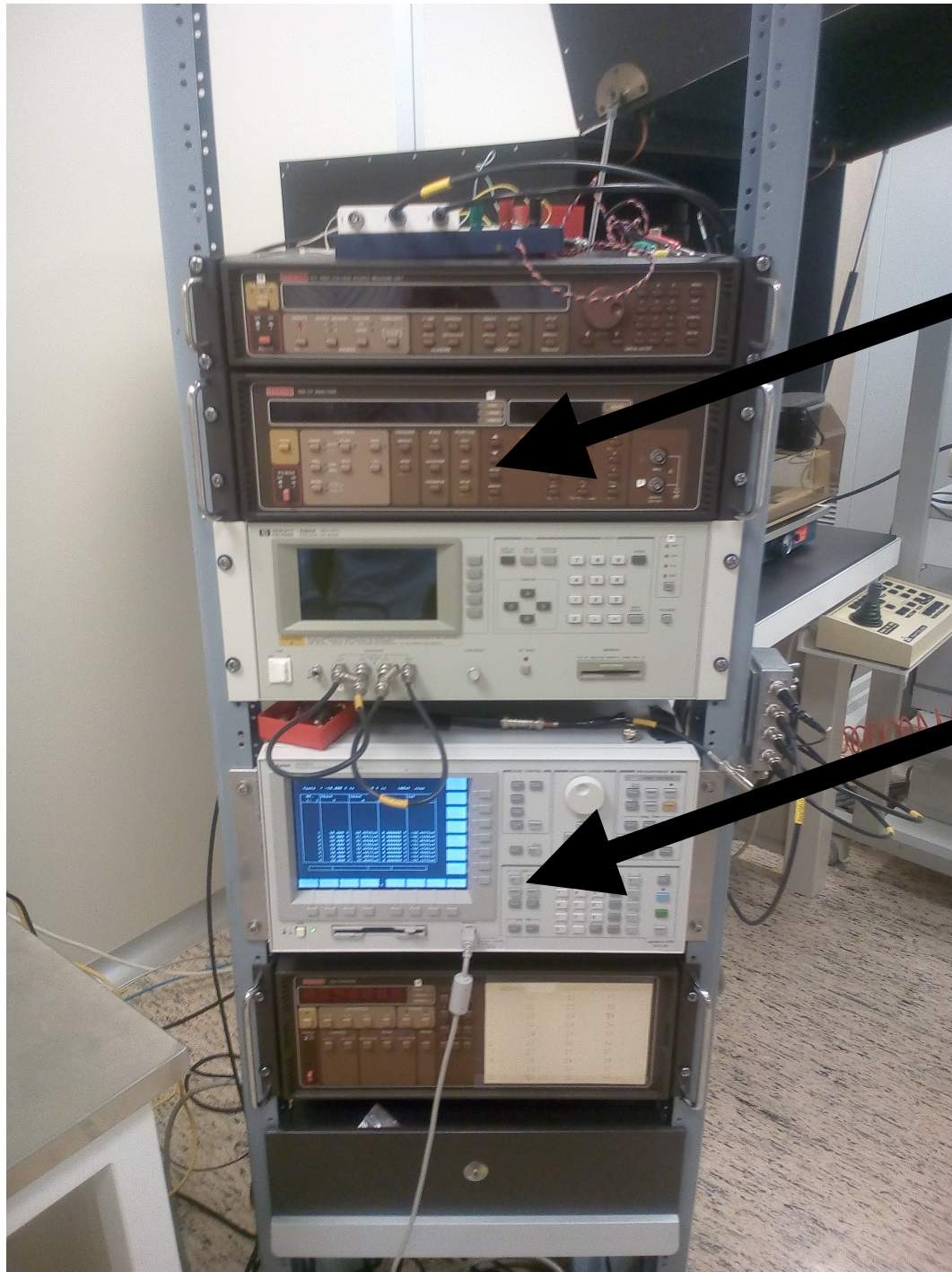
- KEITHLEY 590
 - CV Analyzer
- Agilent 4156C
 - Semiconductor Parameter Analyzer

Instruments



- KEITHLEY 590
 - CV Analyzer
- Agilent 4156C
 - Semiconductor Parameter Analyzer

Instruments



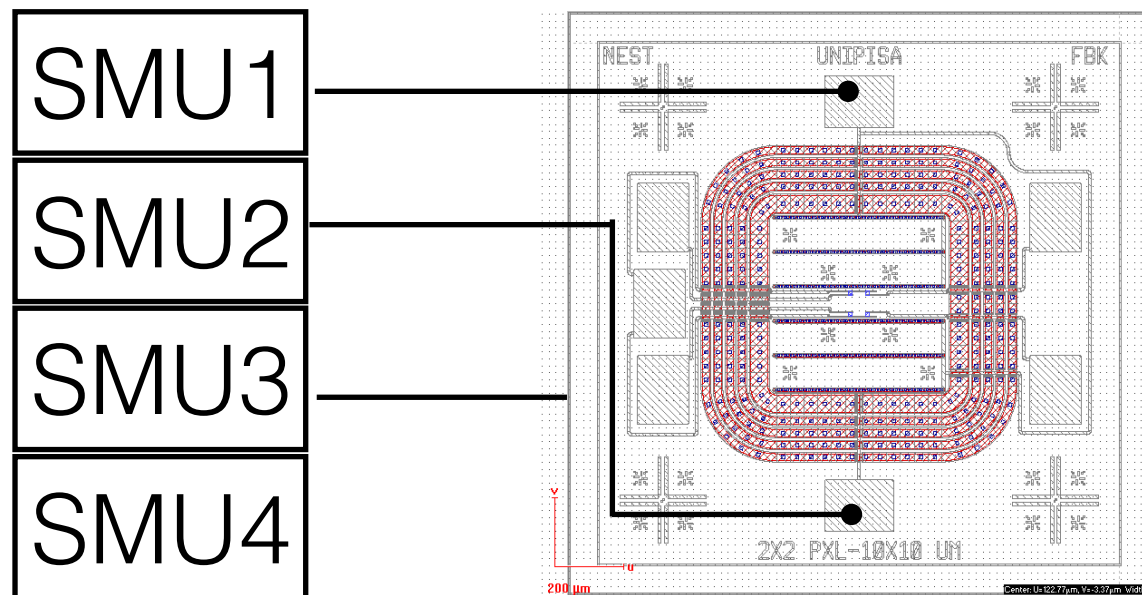
- KEITHLEY 590

- CV Analyzer

- Agilent 4156C

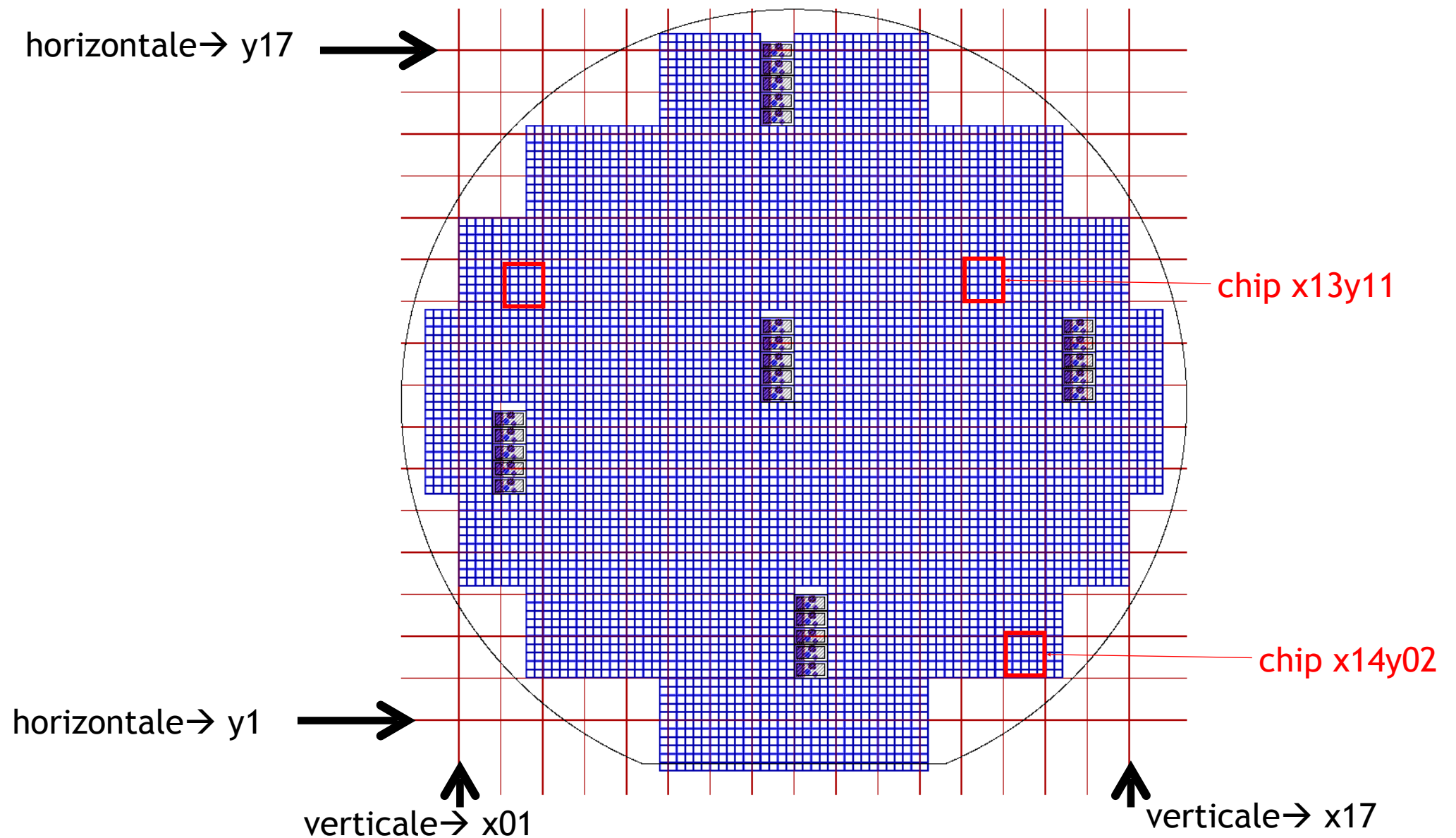
- Semiconductor Parameter Analyzer

Sensor Structures

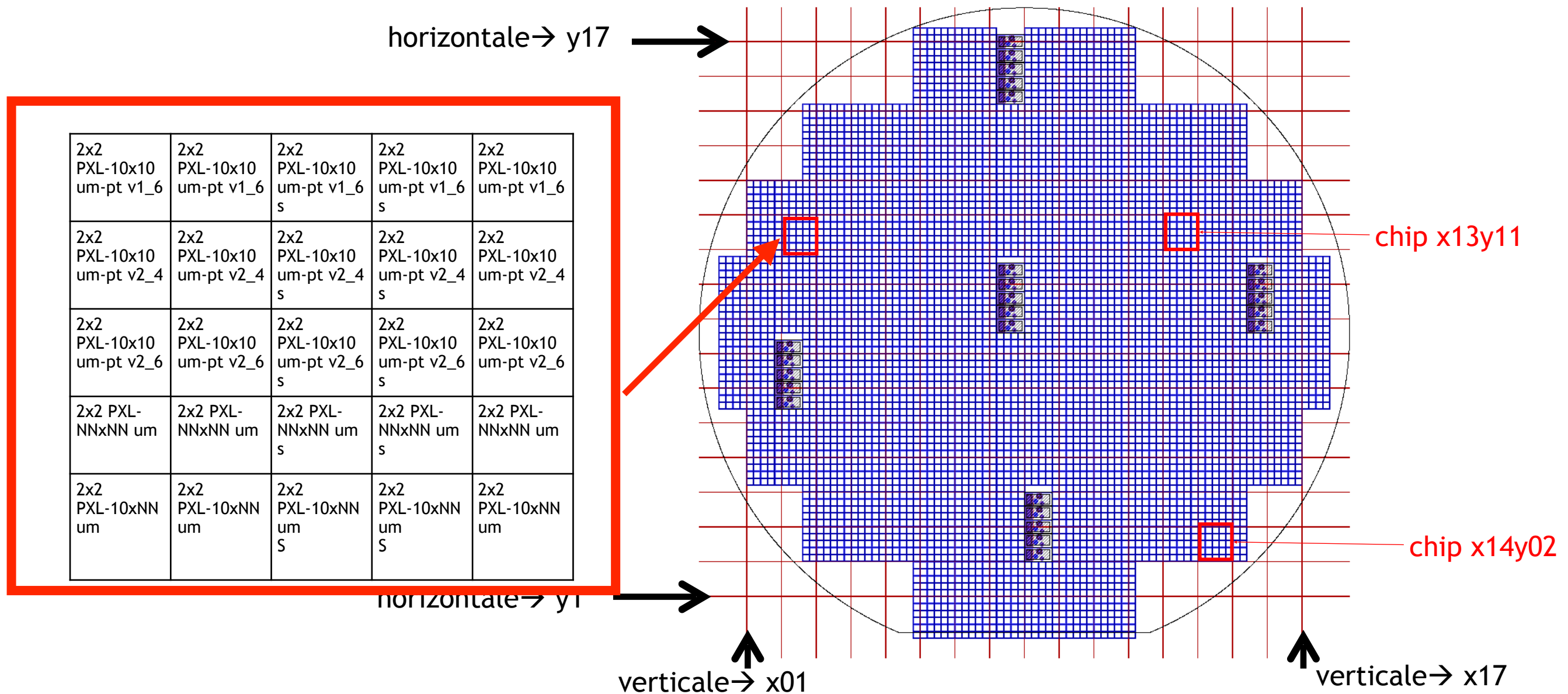


- I-V Curves
 - Reverse Bias 0 V - 50 V
 - 1 V steps
- $A = 0.25 \text{ mm}^2$

Sensor Structures

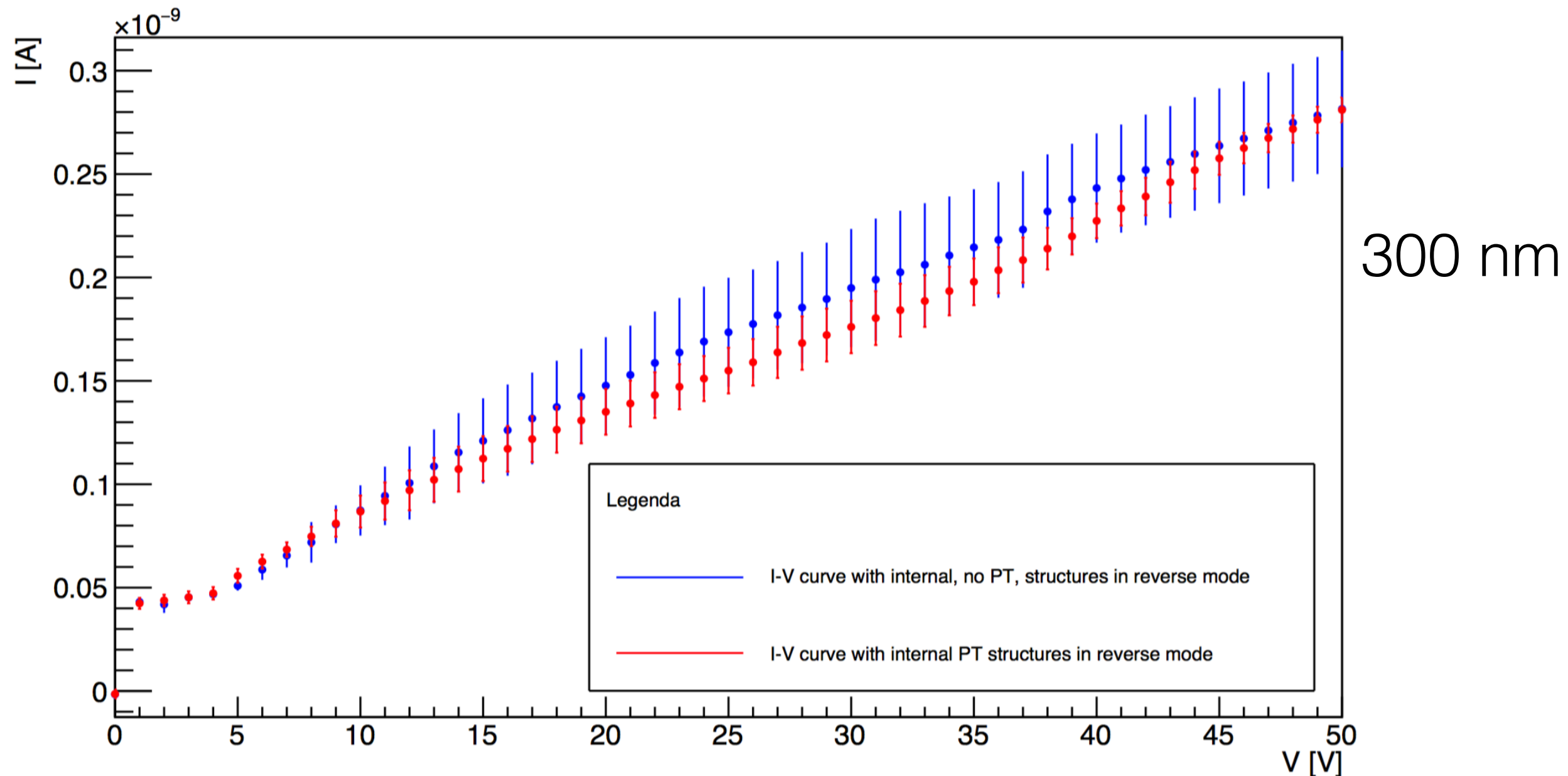


Sensor Structures



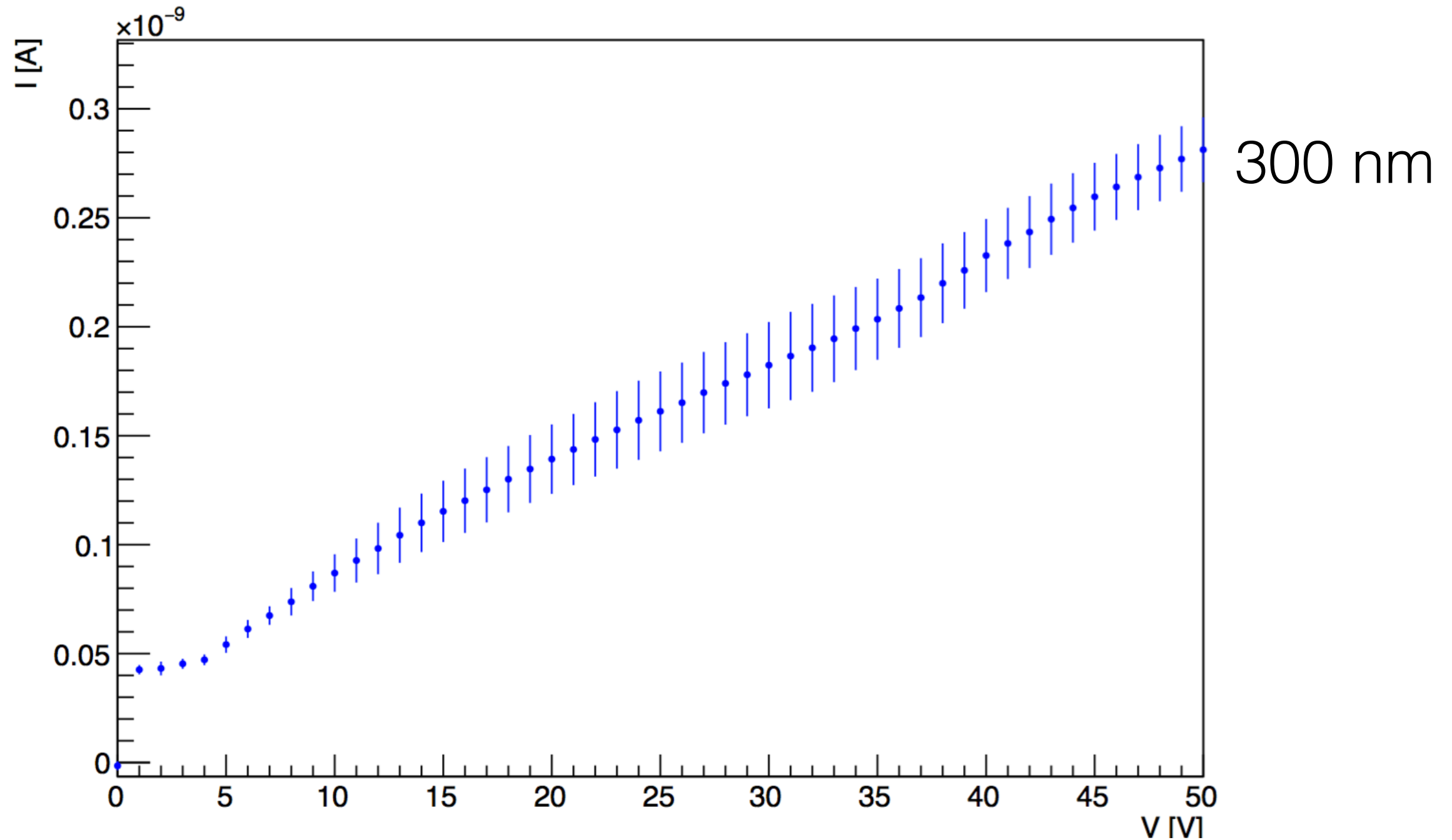
Sensor Structures

I-V curve with internal PT structures in reverse mode

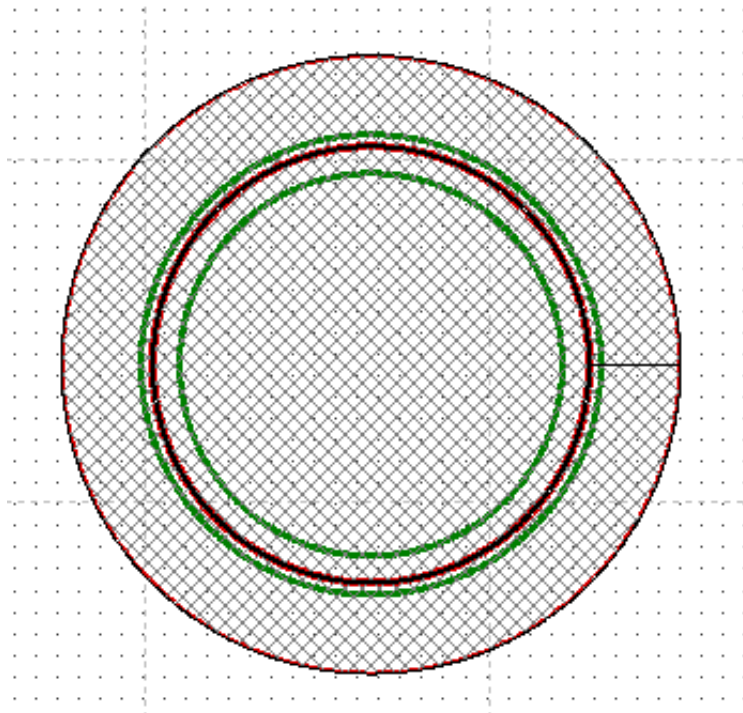


Sensor Structures

I-V curve with all internal structures in reverse mode



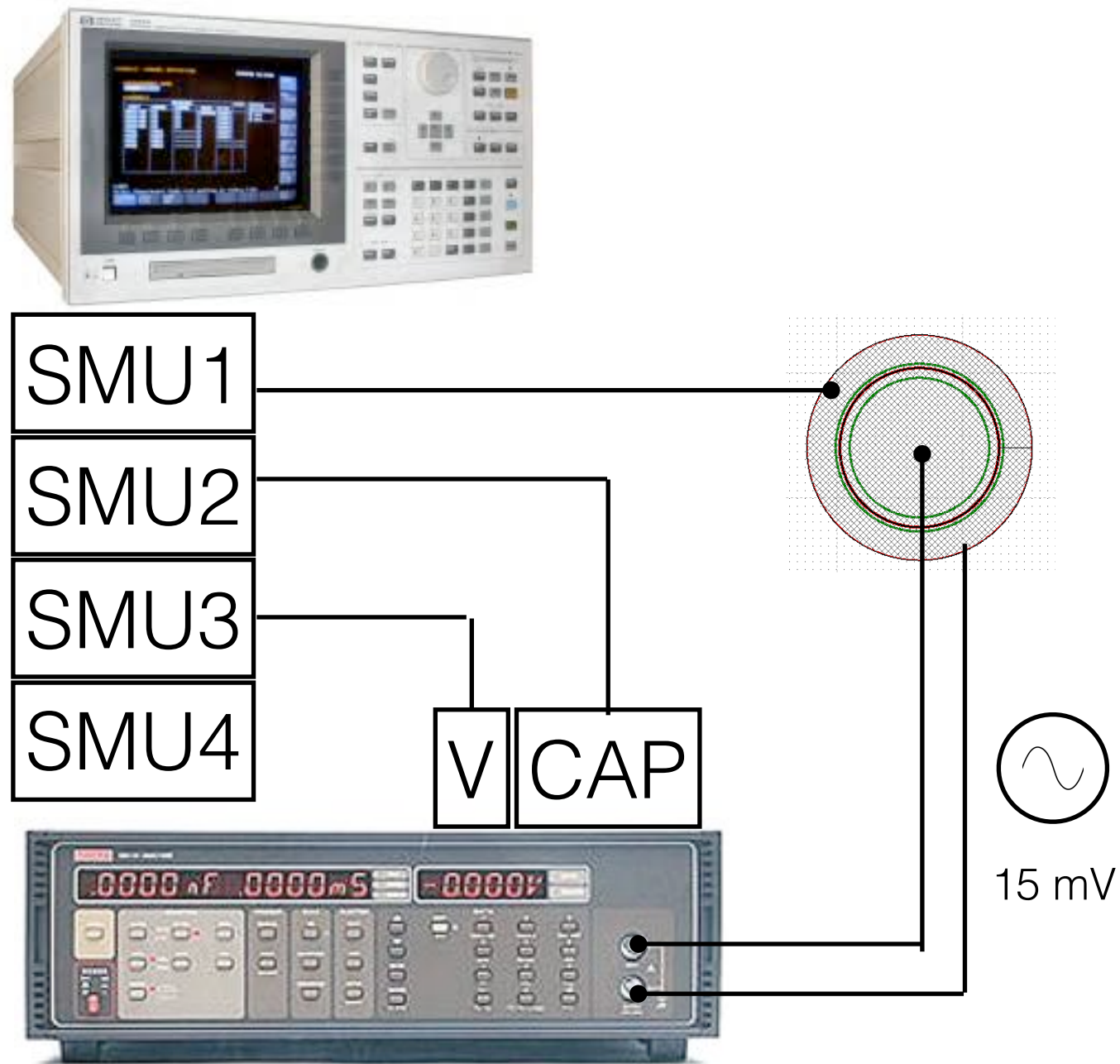
Test Structures



- Diode

- **$d = 1 \text{ mm}$, $A = 0.785 \text{ mm}^2$**
- C-V curves (100 kHz, 15 mV)
- I-V 0 V - 50 V

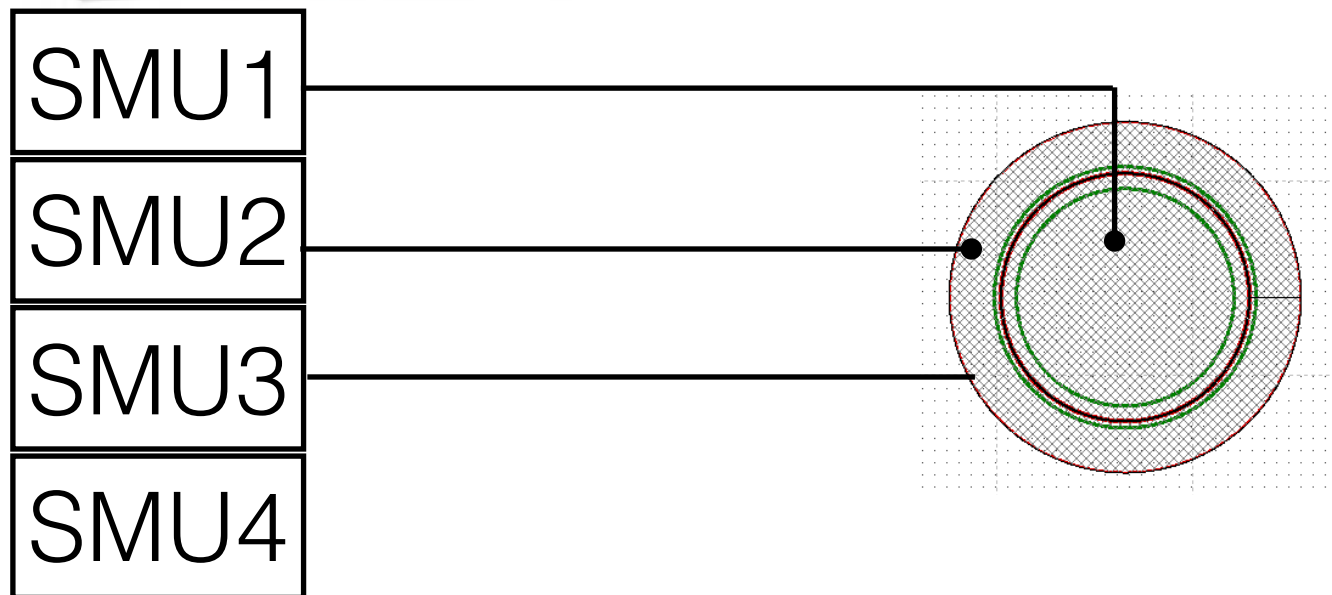
Test Structures



- Diode

- ▶ $d = 1 \text{ mm}$, $A = 0.785 \text{ mm}^2$
- ▶ **C-V curves (100 kHz, 15 mV)**
- ▶ I-V 0 V - 50 V

Test Structures



- Diode

- ▶ $d = 1 \text{ mm}$, $A = 0.785 \text{ mm}^2$
- ▶ C-V curves (100 kHz, 15 mV)
- ▶ **I-V (0 V - 50 V)**

$$(1) \quad w = \sqrt{\frac{2\epsilon_s \cdot (\phi_i - V)}{q \cdot N_d}} \quad N_d \ll N_a$$

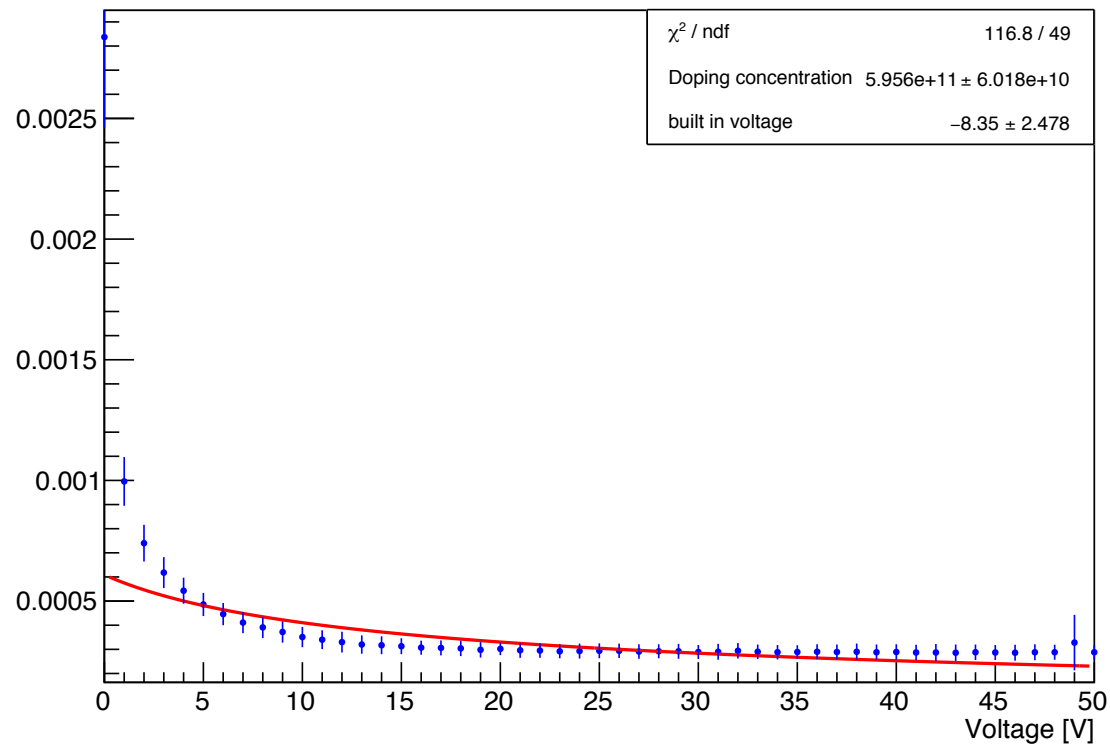
$$(2) \quad C = \frac{\epsilon_s \cdot A}{w}$$

$$(3) \quad \frac{1}{C^2} = \frac{2}{q \cdot \epsilon_s \cdot A^2 \cdot N_d} (\phi_i - V)$$

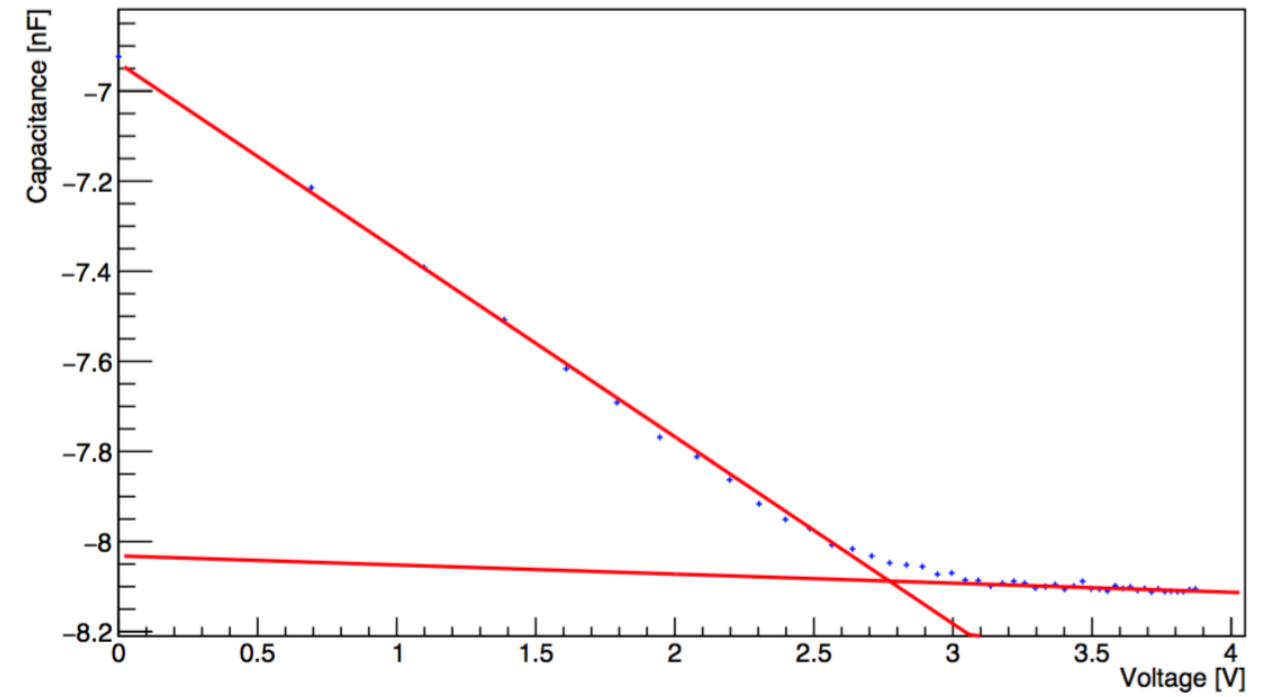
$$(3.1) \quad C = \sqrt{\frac{q \cdot \epsilon_s \cdot A^2 \cdot N_d}{2(\phi_i - V)}}$$

$$(4) \quad N_d = \frac{2}{q \epsilon_s A^2} \cdot \frac{1}{\Delta} \quad : \quad \Delta = \frac{\partial(\frac{1}{C^2})}{\partial V}$$

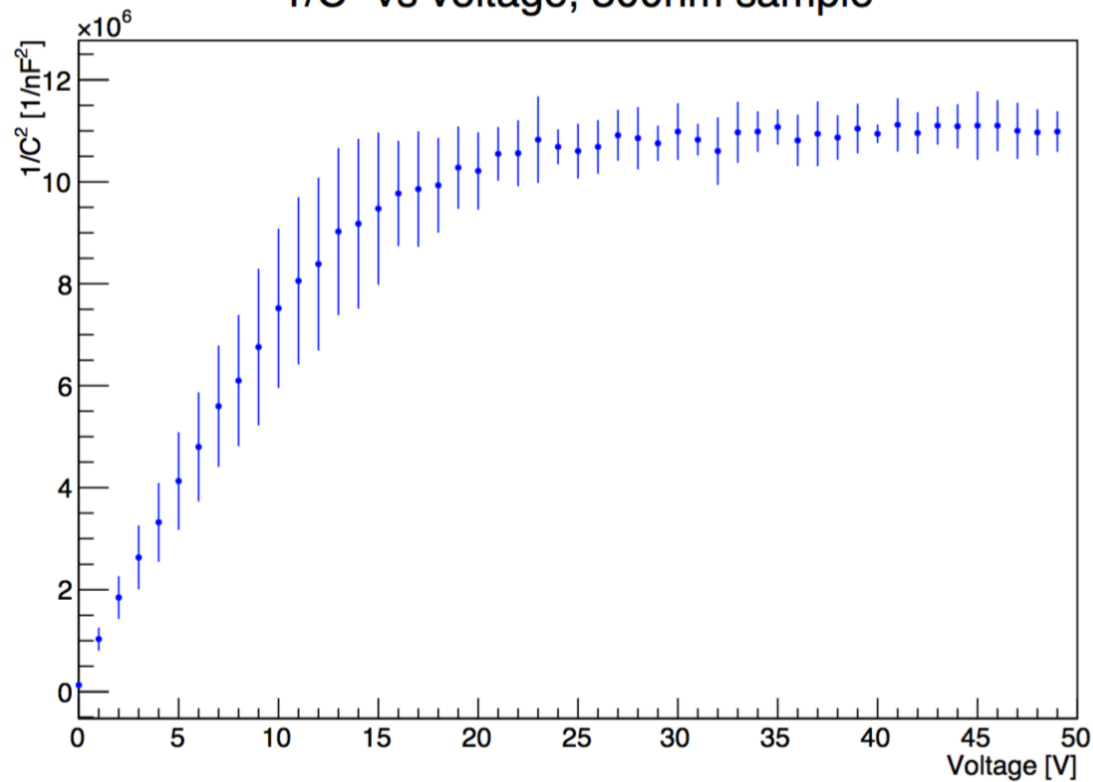
Average capacitance vs bias voltage, 300nm sample



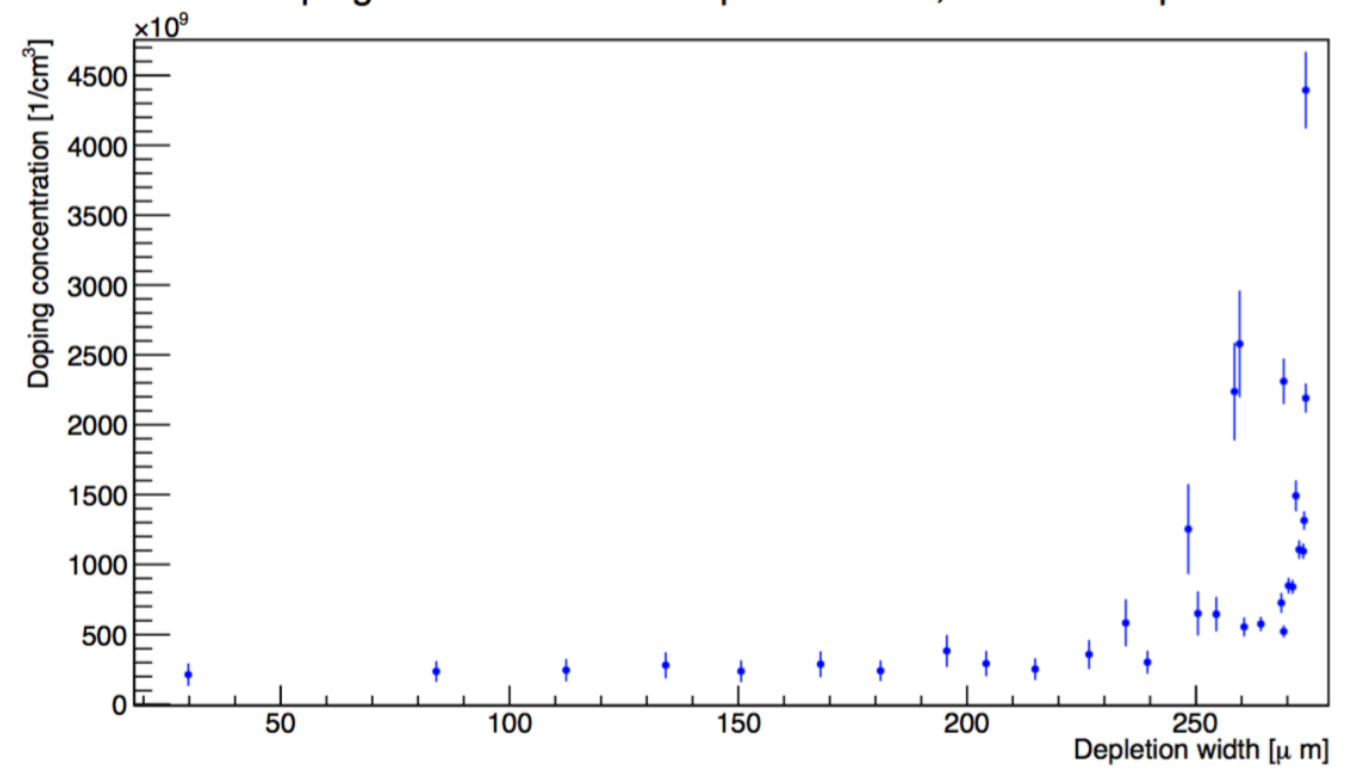
Capacitance vs voltage, 300nm sample



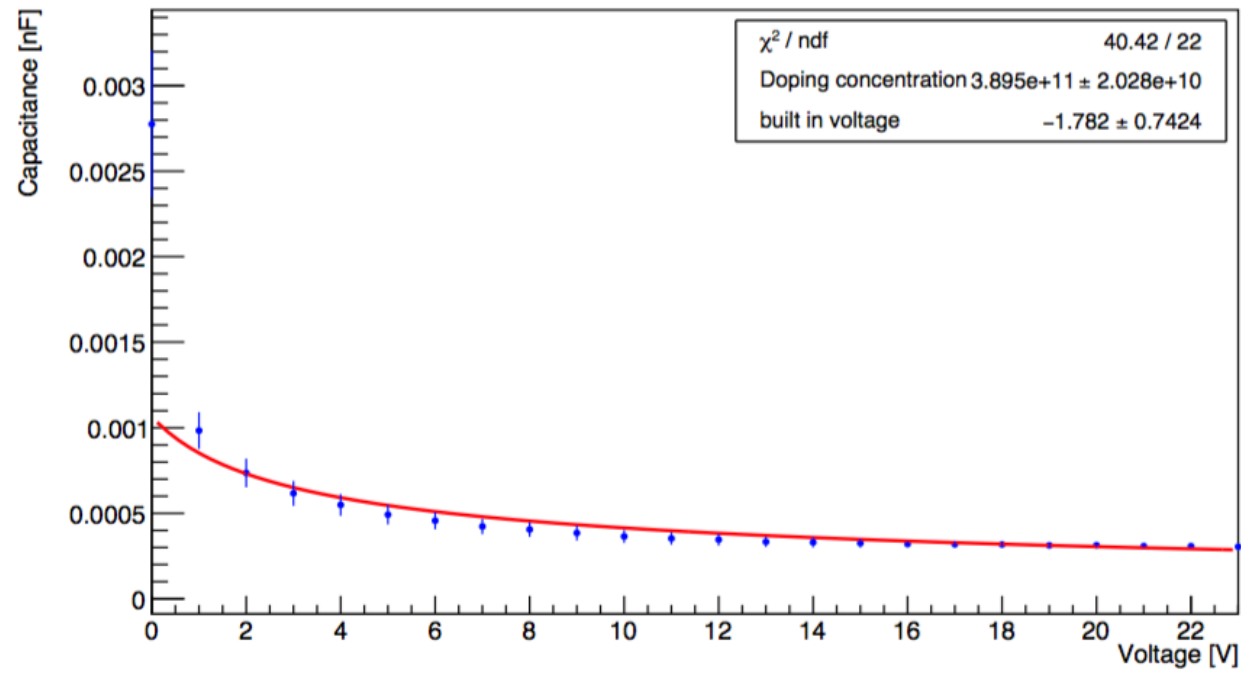
$1/C^2$ vs voltage, 300nm sample



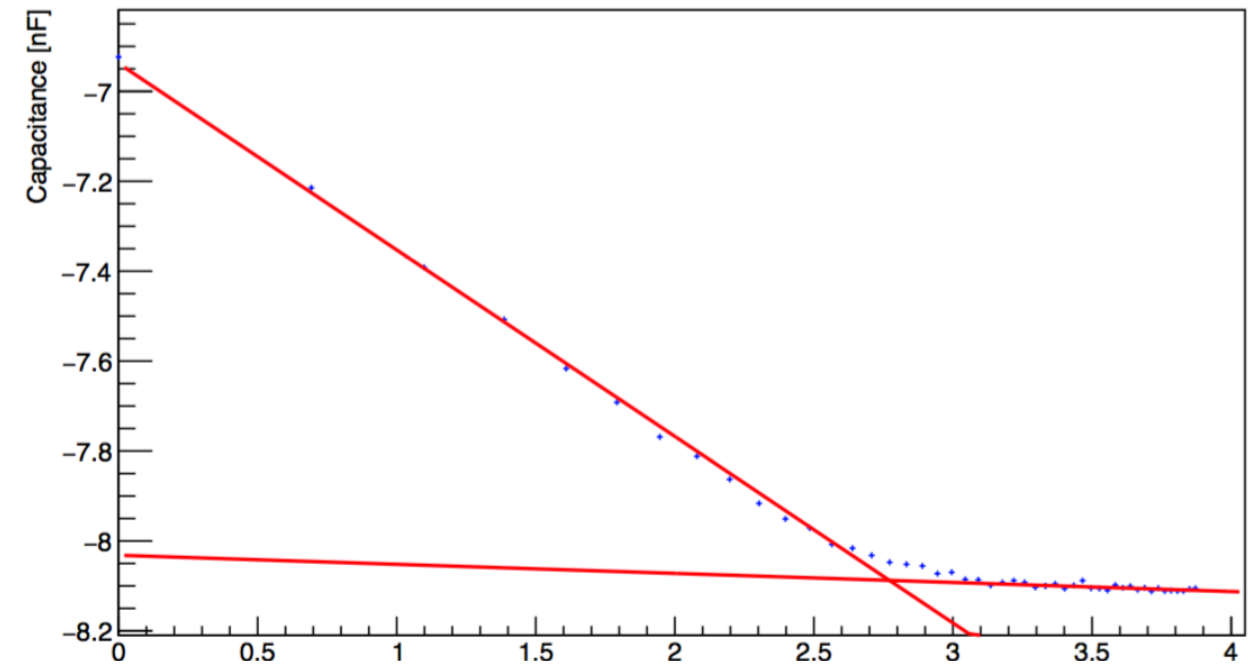
Doping concentration vs depletion width, 300nm sample



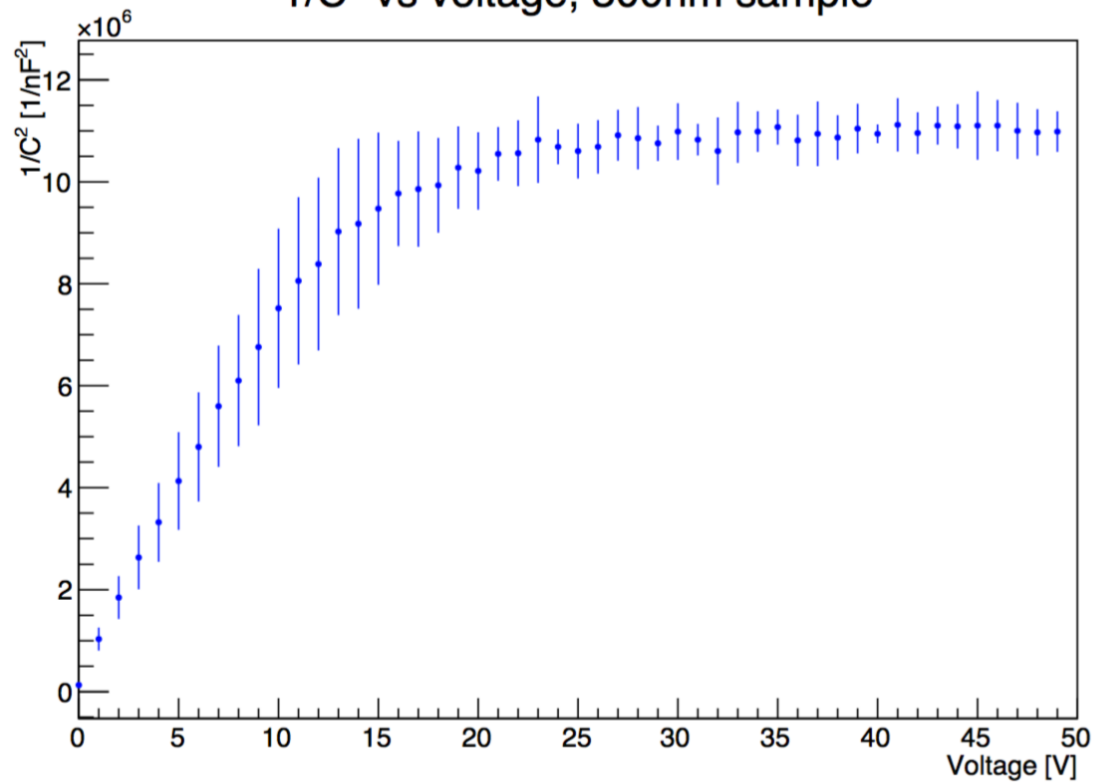
Capacitance vs voltage , 300nm sample



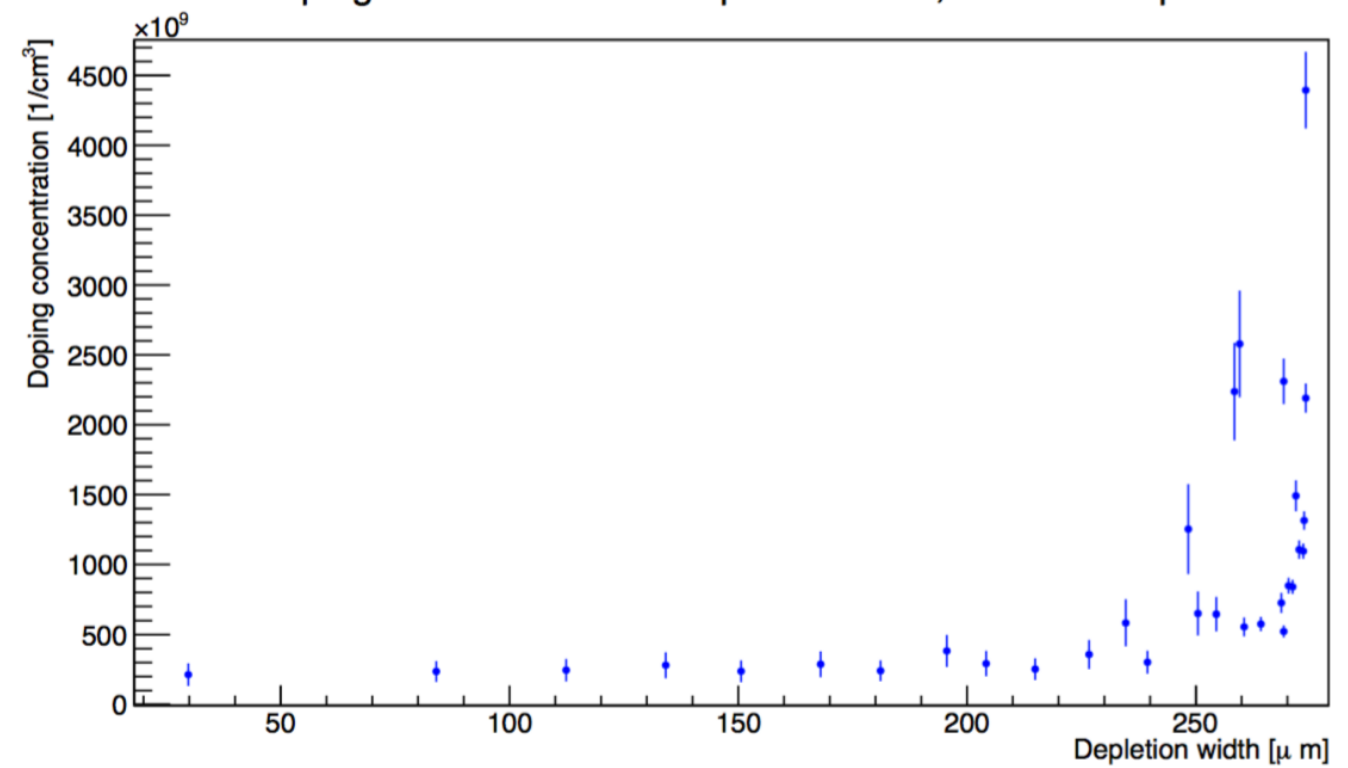
Capacitance vs voltage, 300nm sample



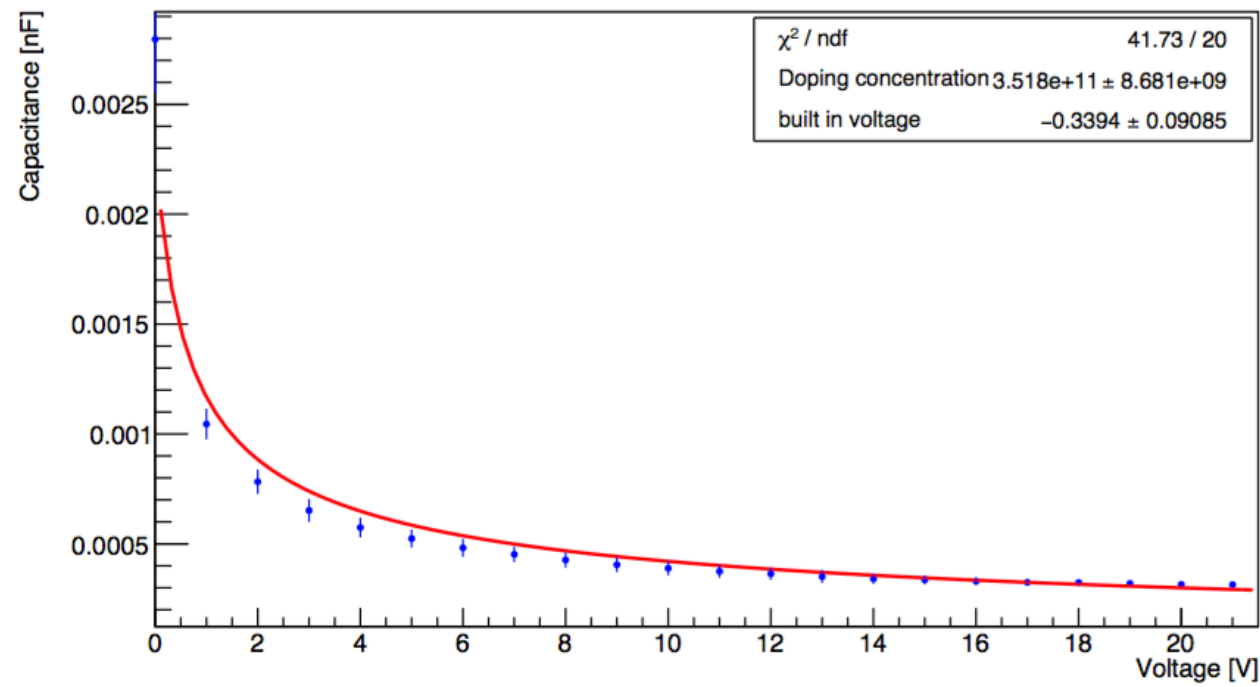
$1/C^2$ vs voltage, 300nm sample



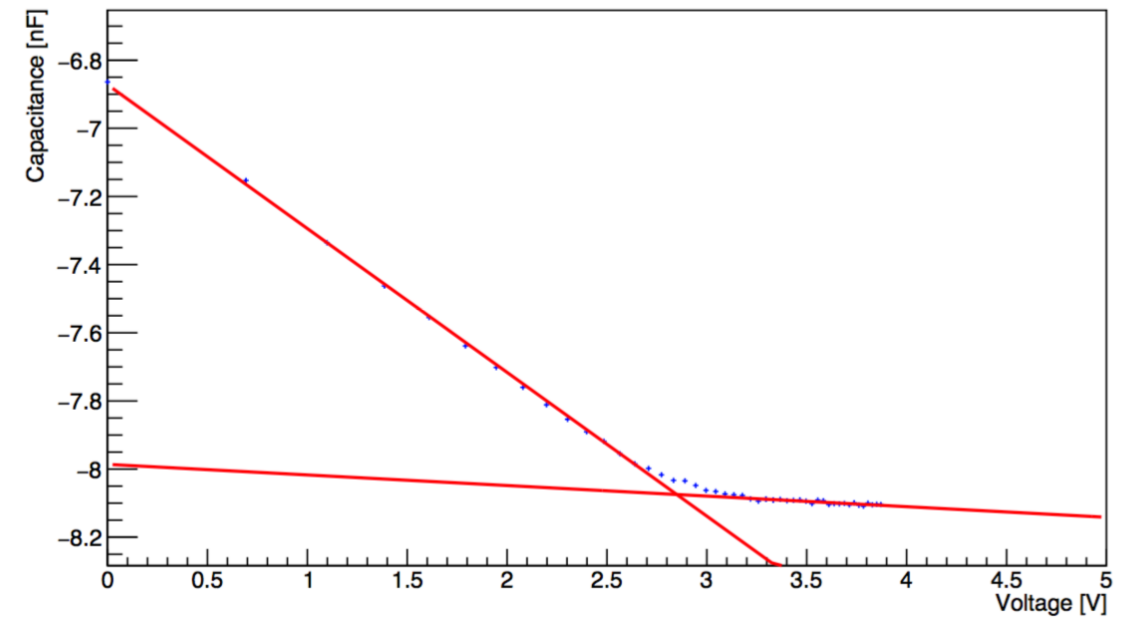
Doping concentration vs depletion width, 300nm sample



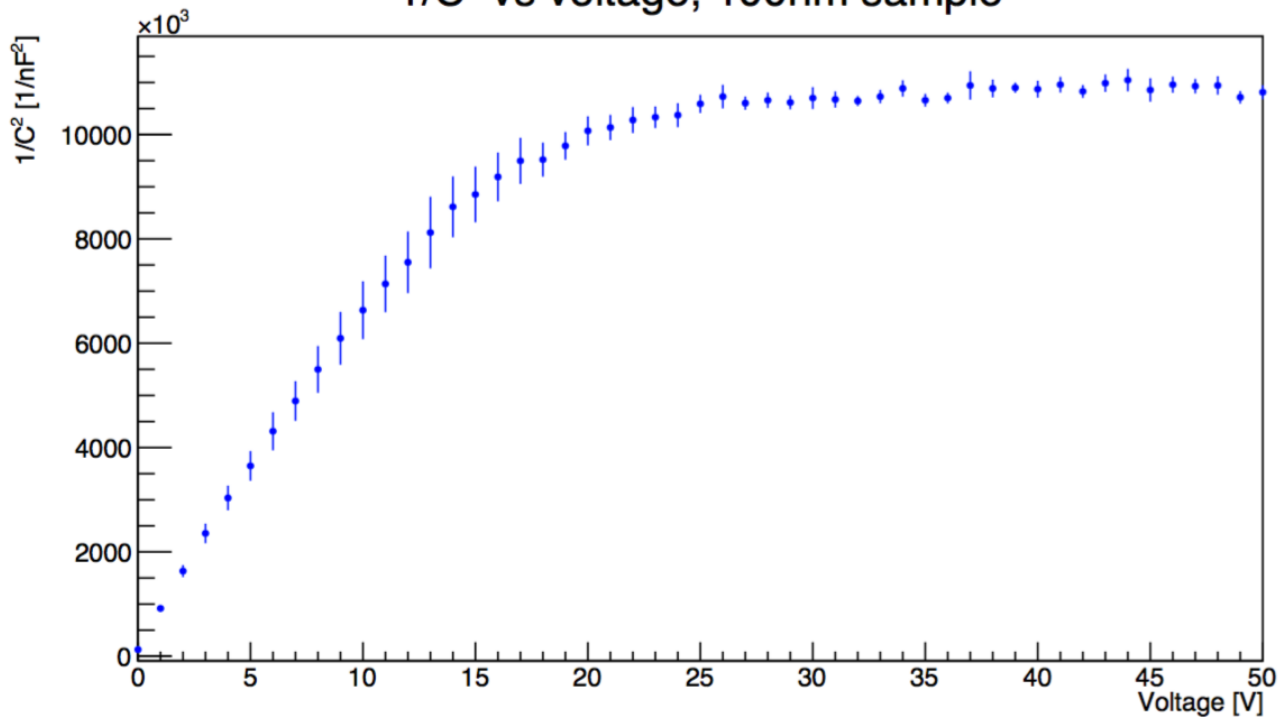
Average capacitance vs bias voltage, 100nm sample



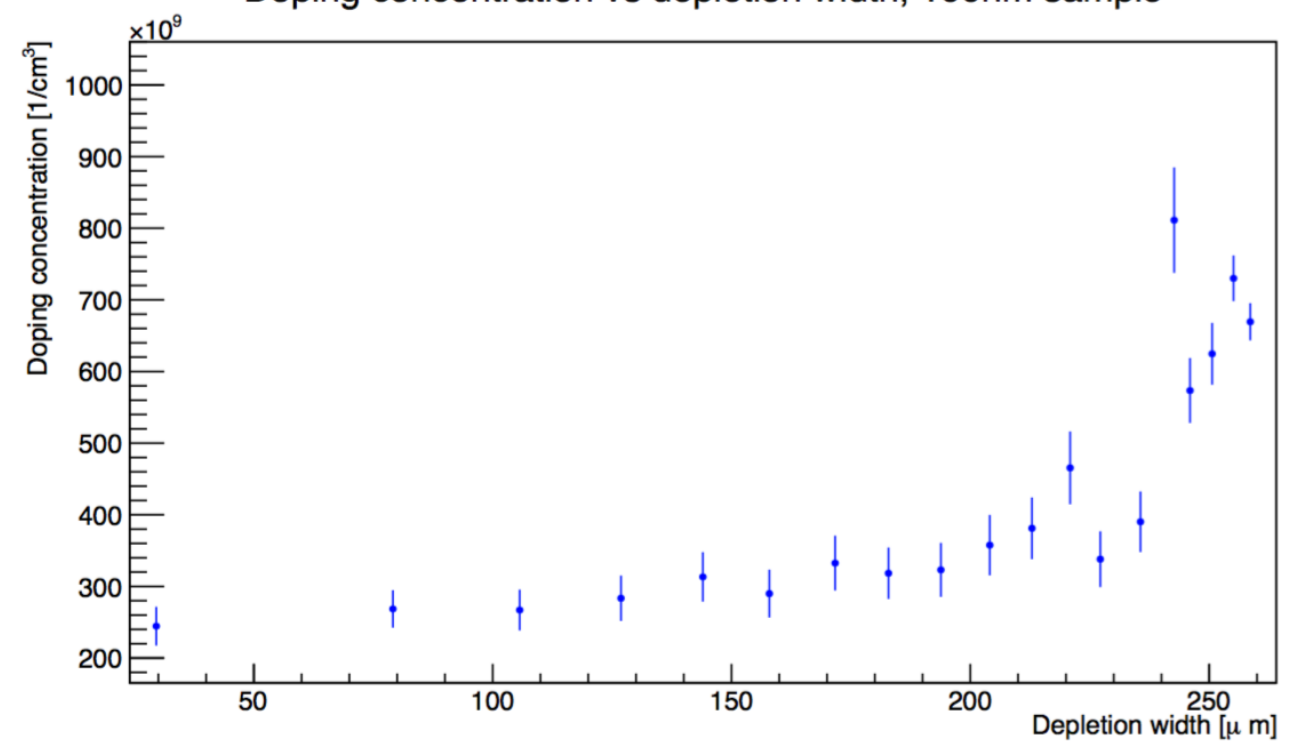
Capacitance vs voltage, 100nm sample



$1/C^2$ vs voltage, 100nm sample



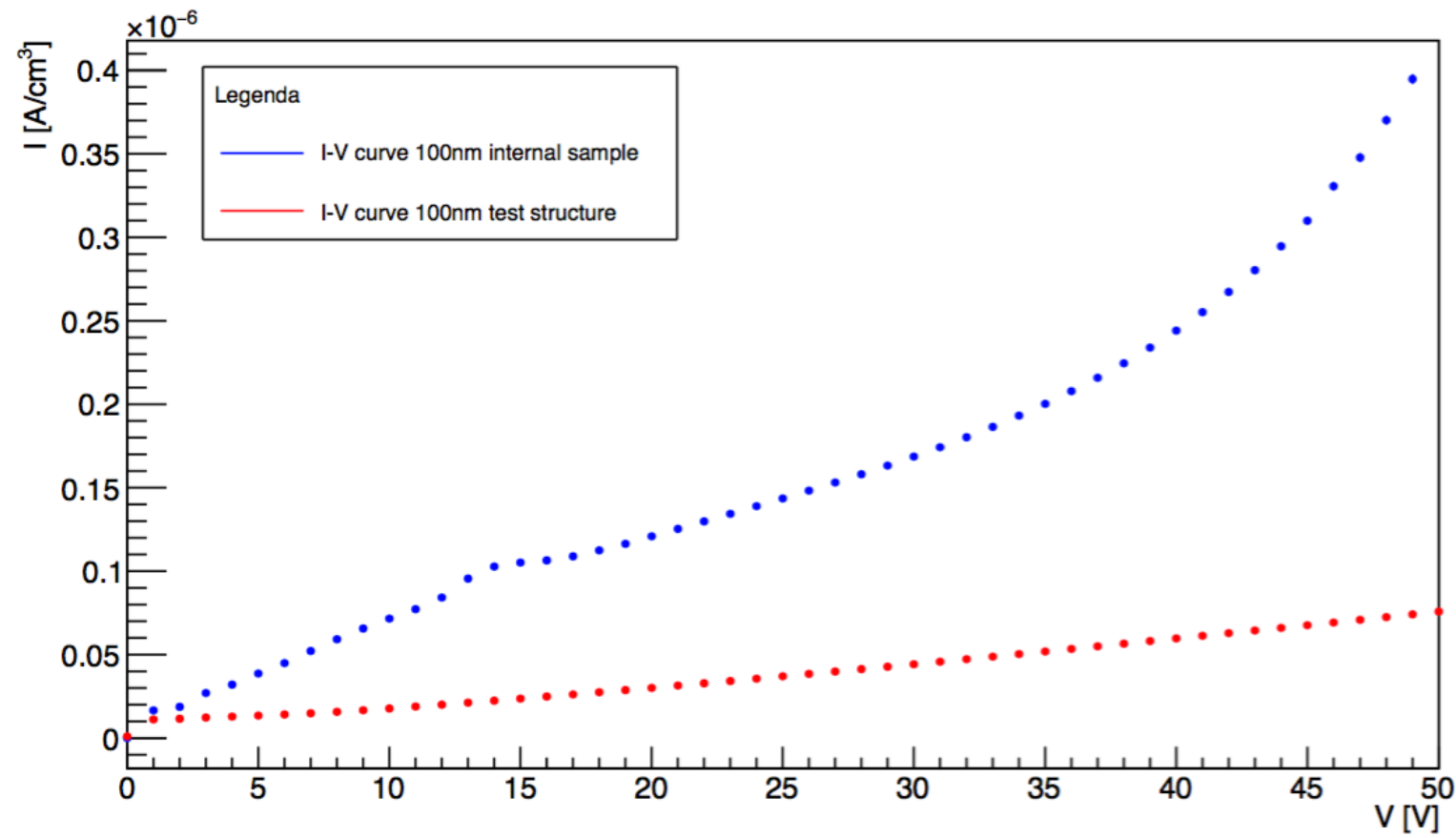
Doping concentration vs depletion width, 100nm sample



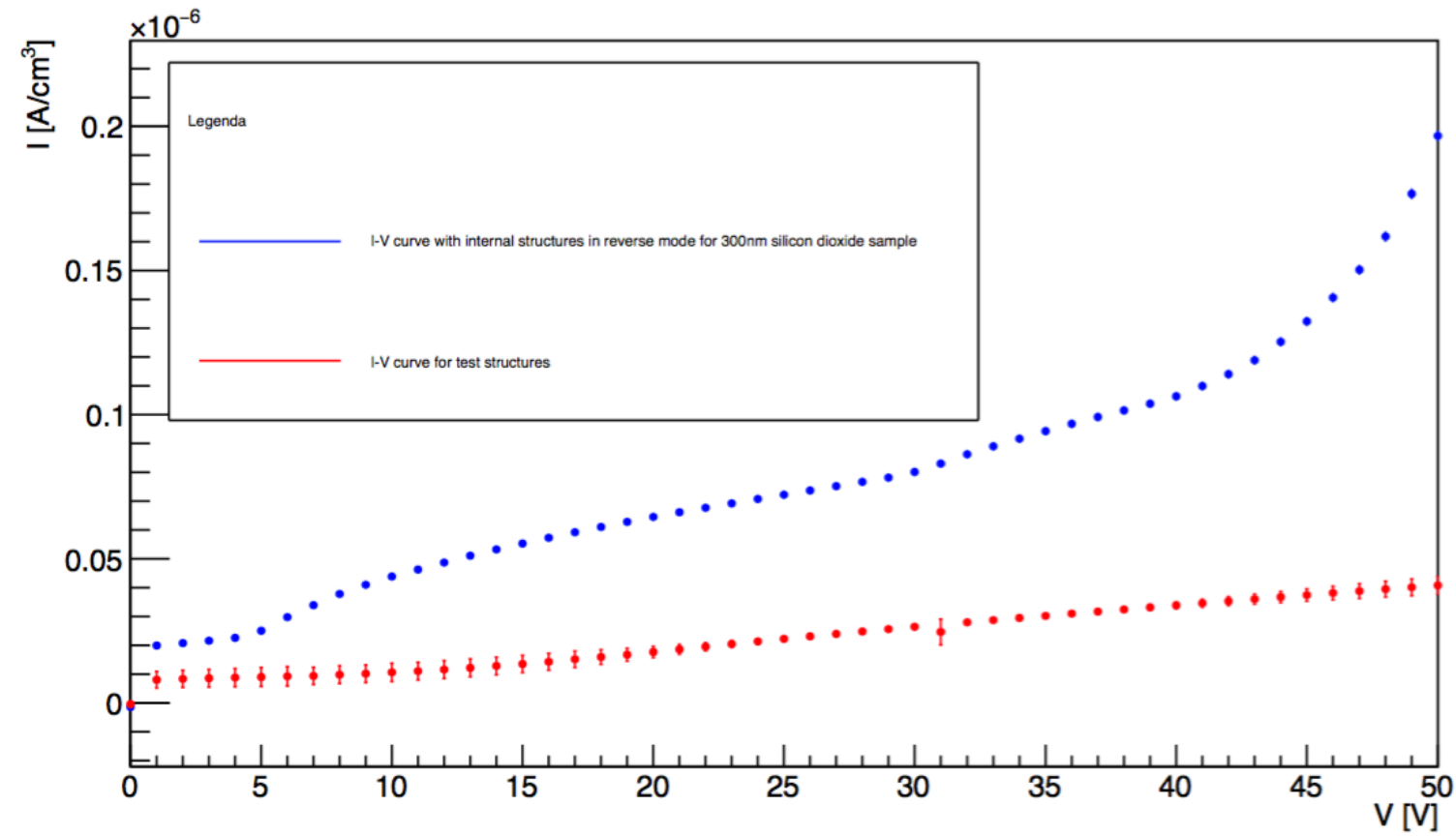
SiO ₂ width [nm]	300	100
Depletion width w [μm]	276 +- 7	271 +- 5
Depletion Voltage [V]	16.4+-1.7	17.5+-0.9
Doping Concentration from C-V [1/cm ³]	(3.9+-0.2)*10 ¹¹	(3.51+-0.09)*10 ¹¹
Doping Concentration from $\delta(1/C)/\delta$ [1/cm ³]	$\frac{(2.\pm0.1)*10^{11}}{(5.\pm0.6)*10^{11}}$	$\frac{(2.4\pm0.2)*10^{11}}{(4.2\pm0.6)*10^{11}}$

SiO ₂ width [nm]	300	100
Depletion width w [μm]	276 +- 7	271 +- 5
Depletion Voltage [V]	16.4+-1.7	17.5+-0.9
Doping Concentration from C ₁₁	(3.9+-0.2)*10 ¹¹	(3.51+-0.09)*10 ¹¹
Doping concentration 7*10¹¹ -> resistivity ρ = 6 kΩcm		
Doping Concentration from $\delta(1/C)/\delta$ [1/cm ³]	$\frac{(2.\pm0.1)*10^{11}}{(5.\pm0.6)*10^{11}}$	$\frac{(2.4\pm0.2)*10^{11}}{(4.2\pm0.6)*10^{11}}$

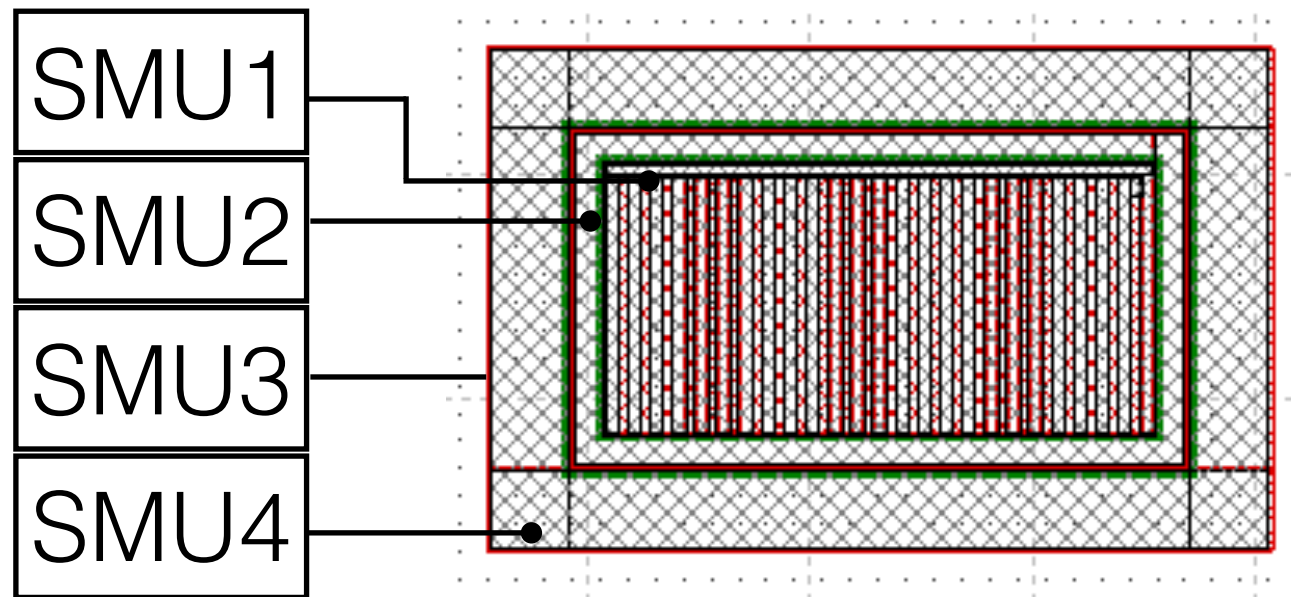
I-V curve with all internal structures in reverse mode



I-V curve with all internal structures in reverse mode



Test Structures



- Gate controlled Diode

- ▶ $l = 2 \text{ mm}$, $w = 1 \text{ mm}$, $A = 2 \text{ mm}^2$
- ▶ I-V curves
 - $V_{\text{gate}} (-10 \text{ V} - 6 \text{ V})$
 - Constant bias voltage (V_{back})

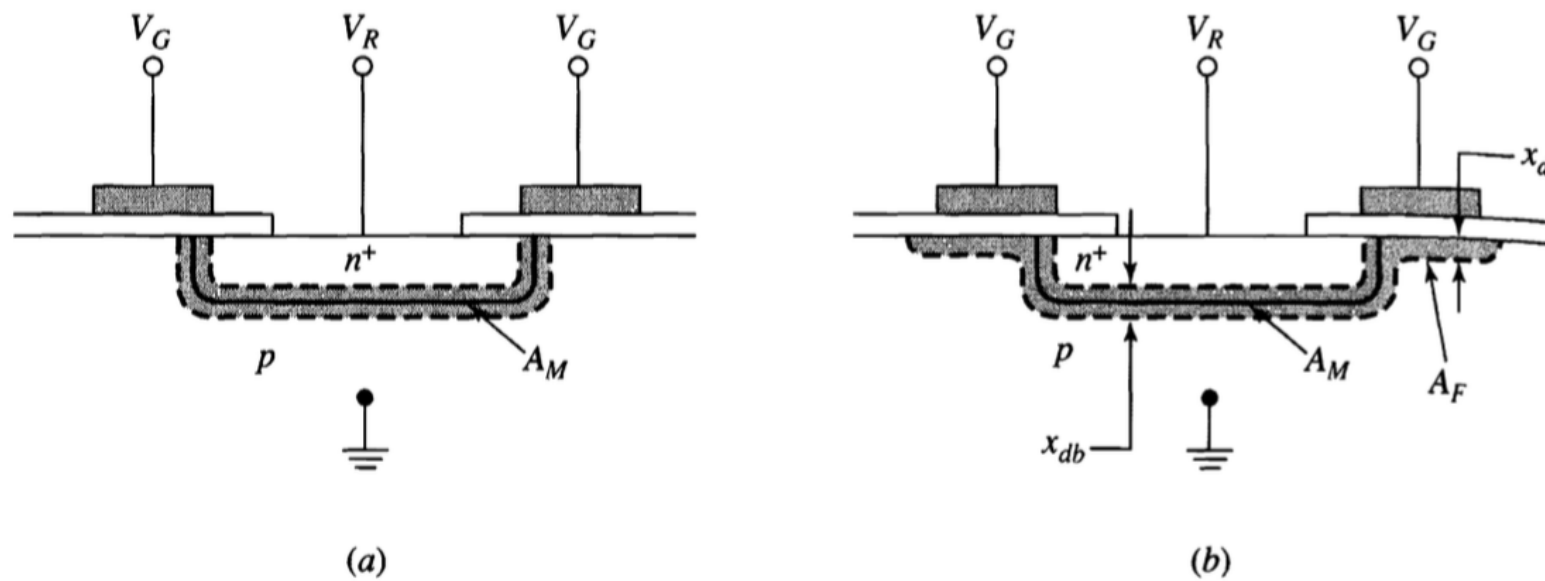


FIGURE 8.20 Gated-diode structure showing depletion regions: (a) when the gate voltage is V_{FB} for the p -region, and (b) when the gate causes a depletion region of width x_{ds} at the silicon surface.

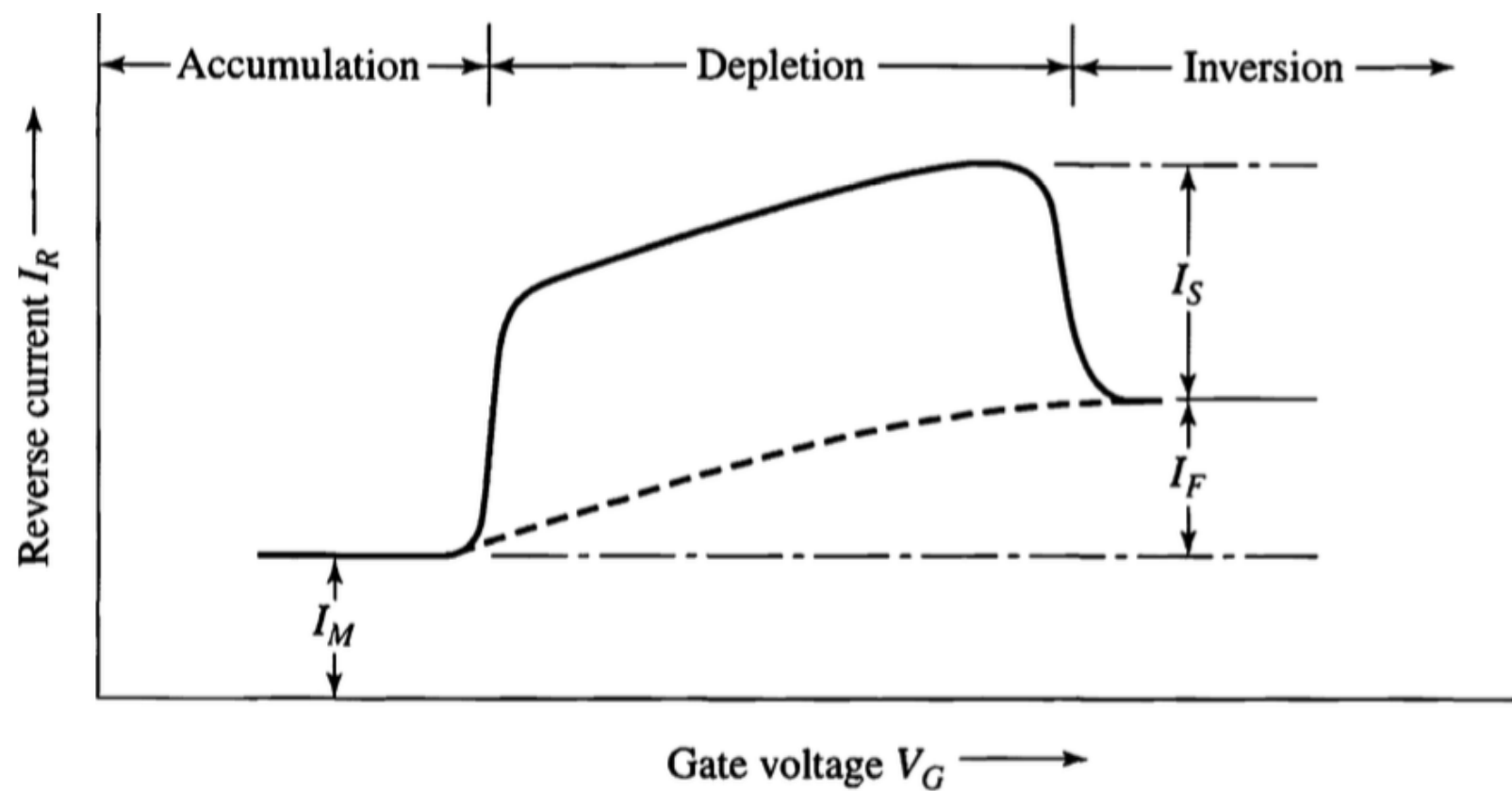


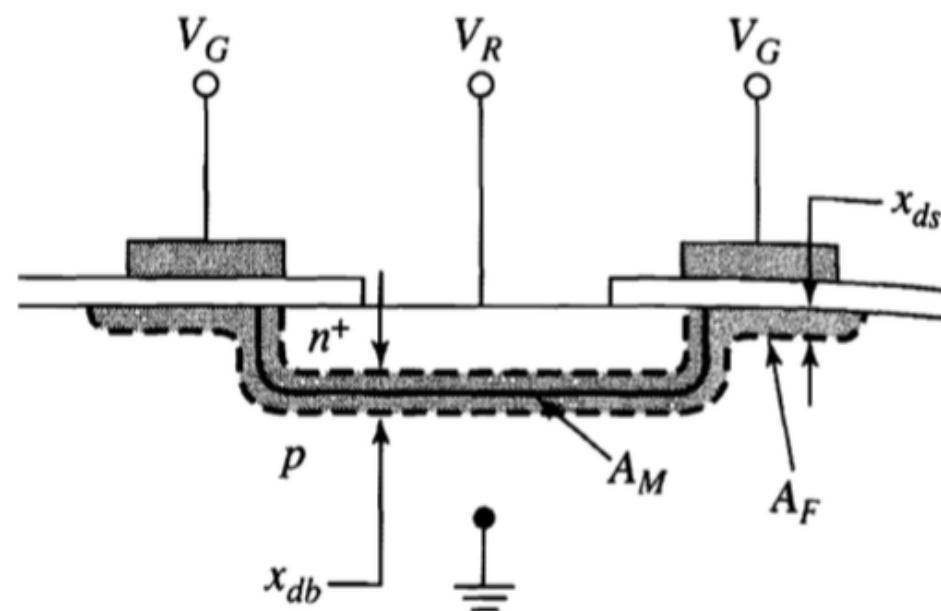
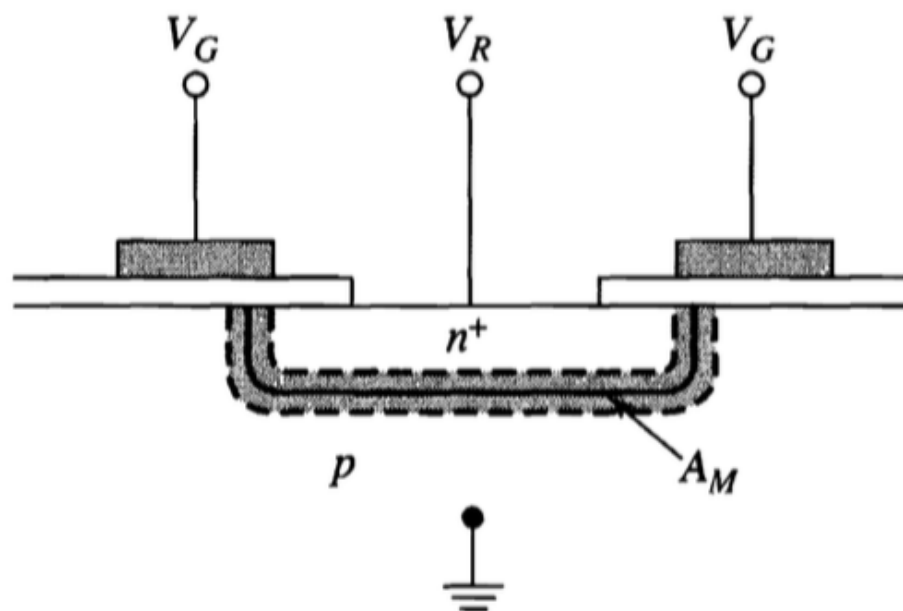
FIGURE 8.21 Reverse current in the gated diode as a function of V_G showing the marked increase in leakage when the surface is depleted.

$$I_R = I_M + I_F + I_S$$

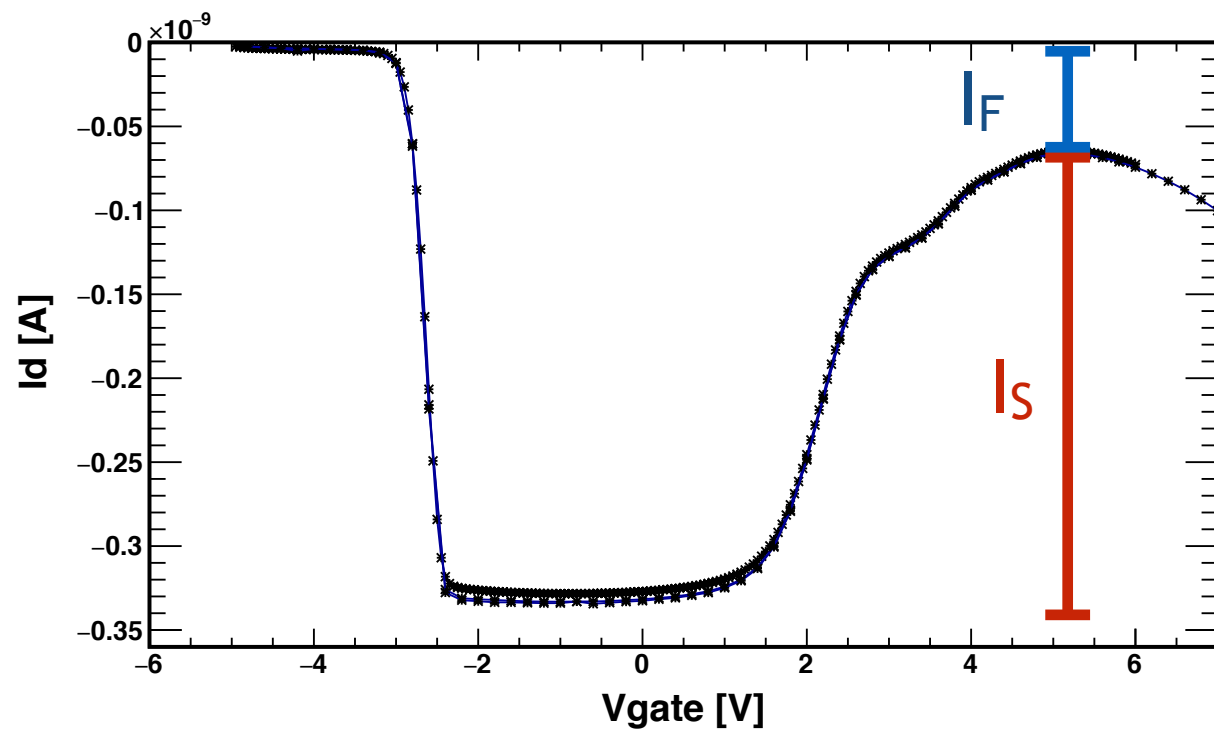
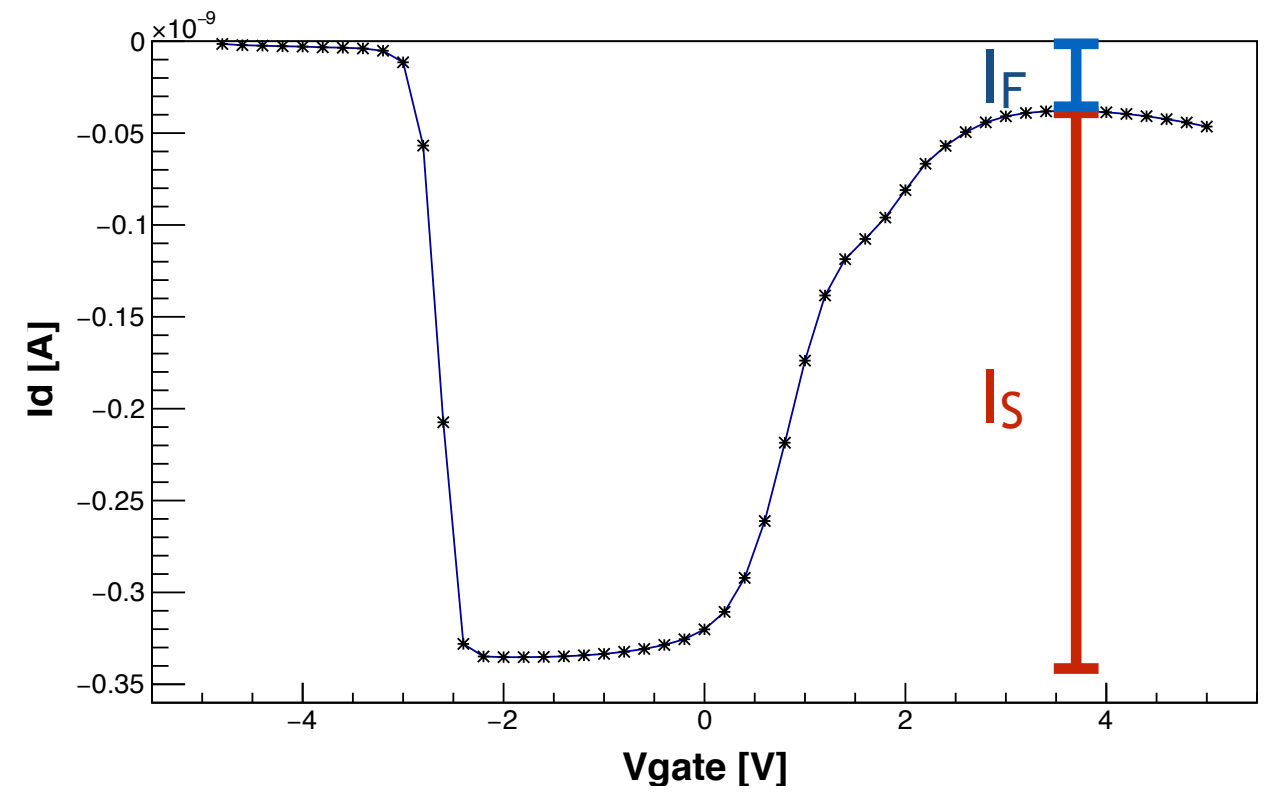
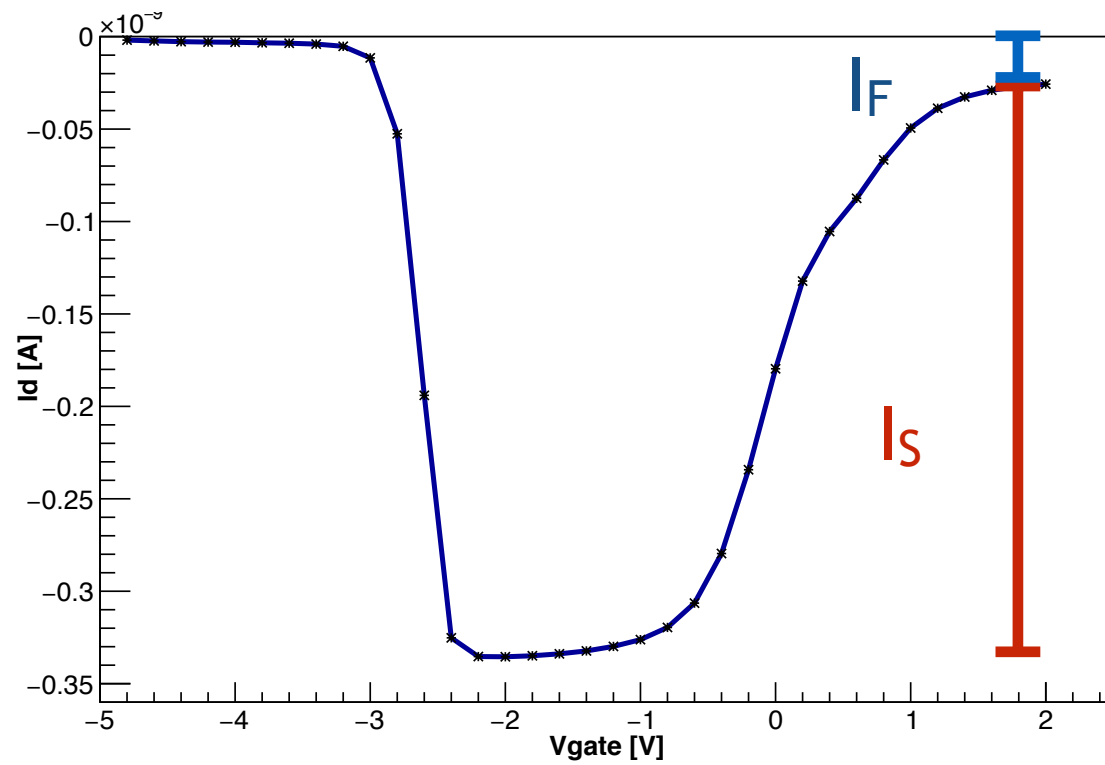
$$I_M = \frac{qn_i}{2\tau_0} x_i A_M \quad x_i \sim \sqrt{V_{back} - \phi_i}$$

$$I_F = \frac{qn_i}{2\tau_0} x_{ds} A_F$$

$$I_S = \frac{qn_i s_0 A_F}{2} \quad p_s/n_s \ll n_i$$

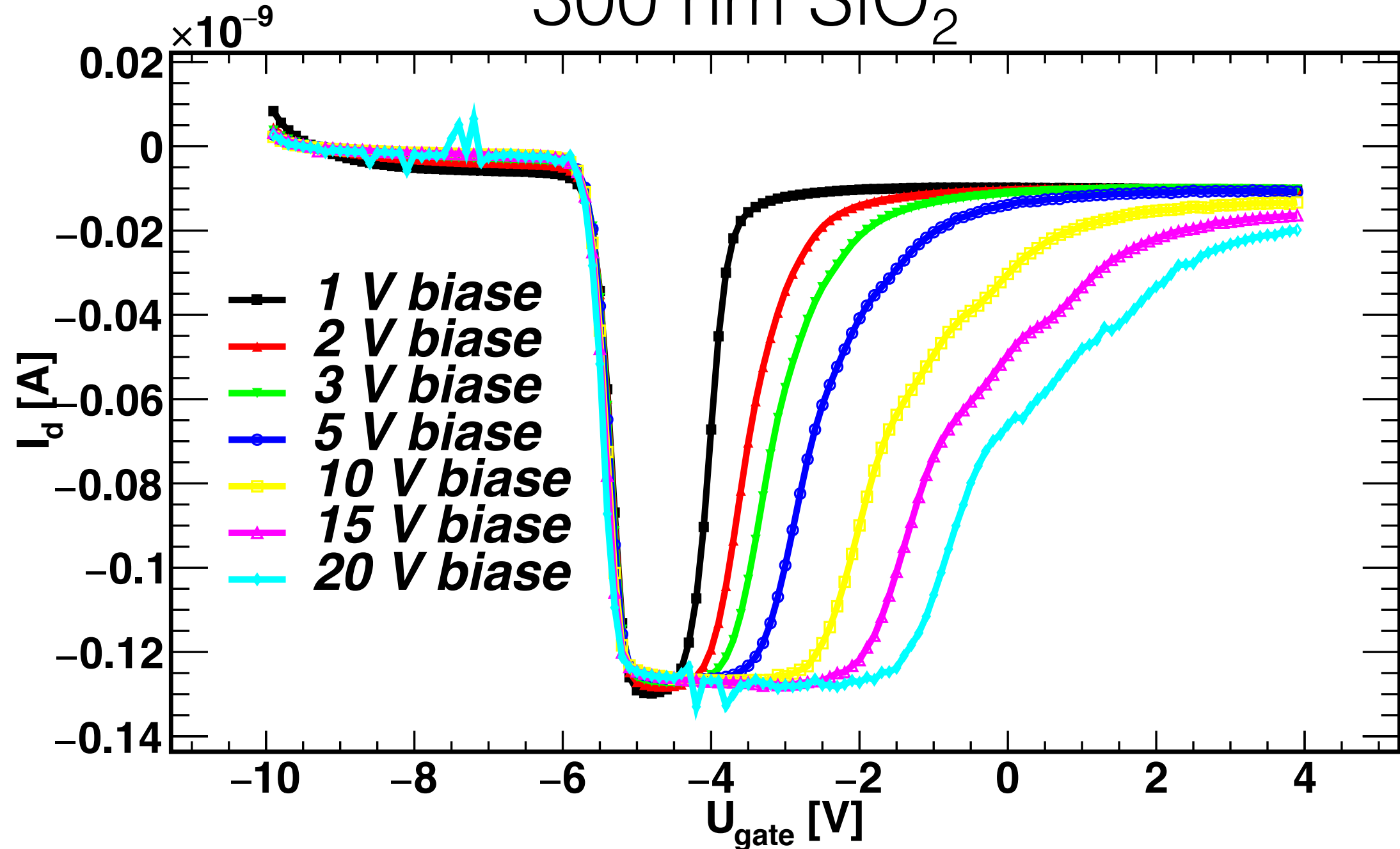


100 nm SiO₂



V_{biase}	5 V	10 V	20 V
I_s	0.304 nA	0.290 nA	0.259 nA
I_s/A	15.2 nA/ cm ²	14.5 nA/ cm ²	12.95 nA/cm²

300 nm SiO₂



V_{biase}	1 V	2 V	3 V	5 V	10 V	15 V	20 V
I_s	0.117 nA	0.117 nA	0.116 nA	0.116 nA	0.113 nA	0.110 nA	0.107 nA
I_s/A	5.85 nA/ cm ²	5.85 nA/ cm ²	5.8 nA/ cm ²	5.8 nA/ cm ²	5.65 nA/ cm ²	5.5 nA/ cm ²	5.35 nA/ cm²

