Thin Silicon detectors

MUonE meeting

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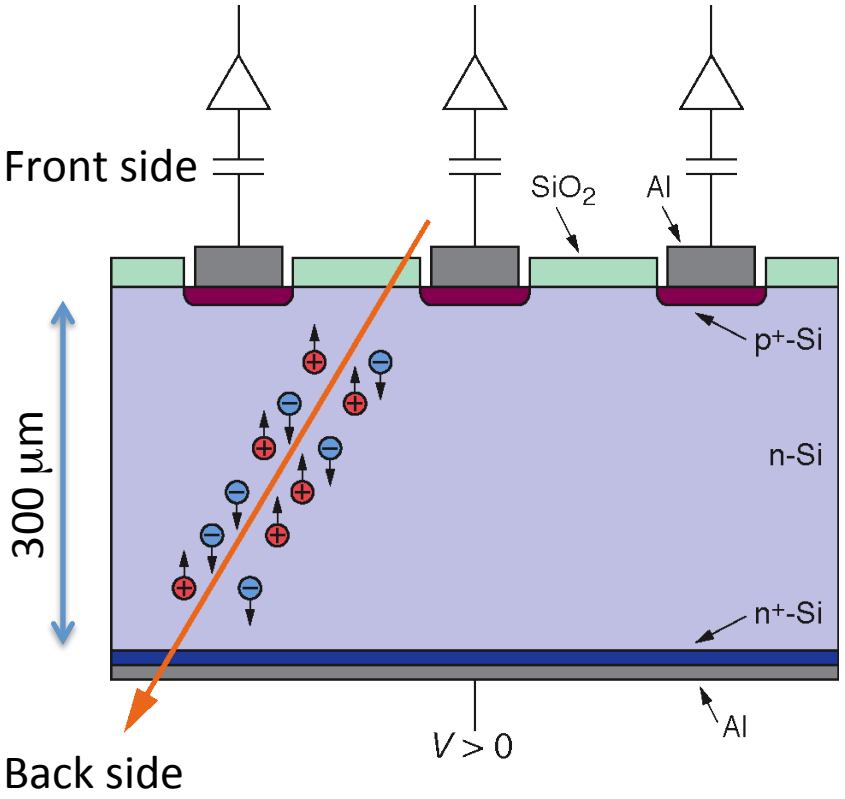
Talk Outline

- Introduction: segmented devices
- Wafers options for a reduced material budget
- Application on Strip/Pixel devices*
  - Geometry
  - Technology
  - Design rules constraints

*(focusing on today existing devices)

Strip Detector: Single sided device



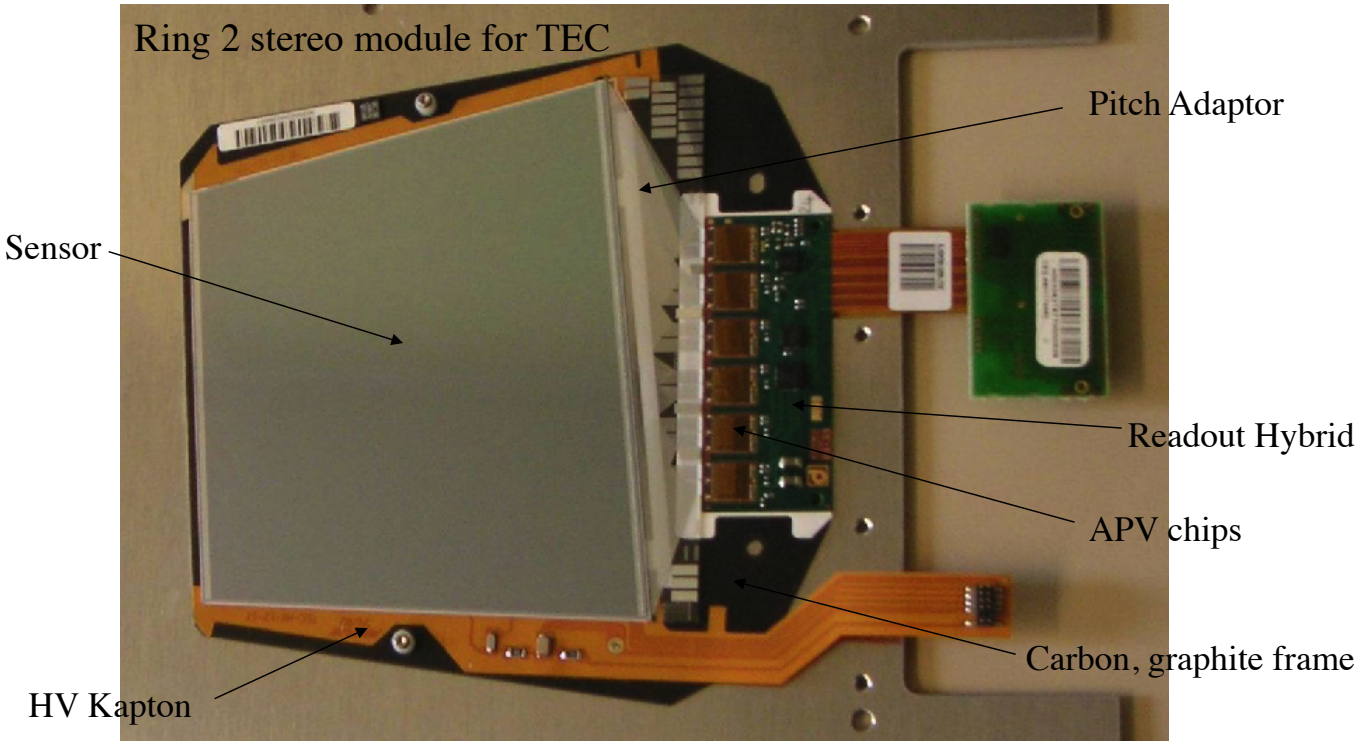
- Thin Silicon wafer (~300 µm) with implanted strips (e.g. p^+ in n-bulk).
- Each implant is connected to a readout electronics channel.
- Through going charged particles generate electron-hole pairs.
- Electron-hole pairs drift in electric field.

From the signals measured by the electronics the position of the particle can be deduced to a few micrometer precision.

Reconstruction of particles track.

- Pros:
  - Single sided technology: simpler, high production efficiency, cheaper.
  - Simple bias/readout scheme
  - Some freedom on the thickness value
- Cons:
  - One coordinate measurement per silicon layer

i.e. single sided CMS Tracker silicon strip detector



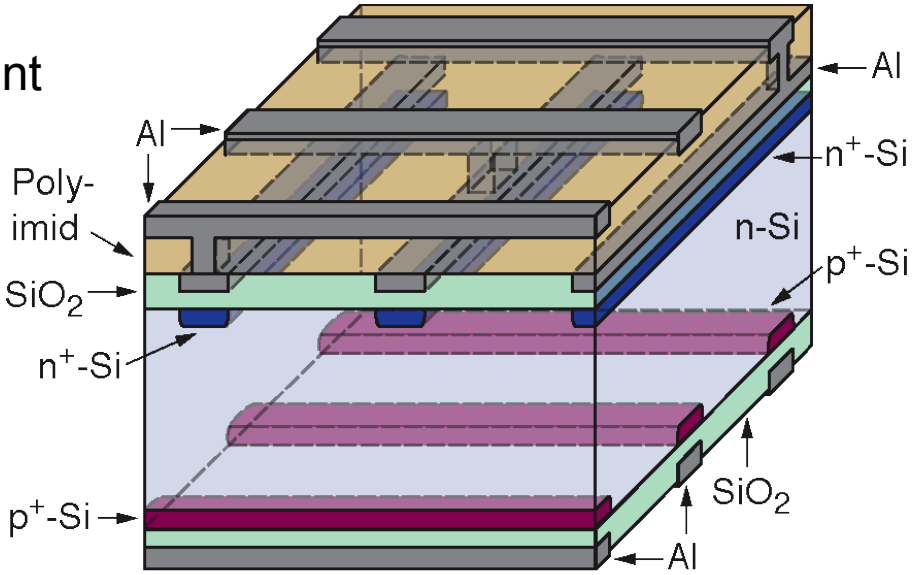
- Sensitive volume (Sensor) far from the read-out electronics (read-out chip + Hybrid)
- Detector cooling located underneath the Hybrid
  - Read-out circuitry dissipated the total power
  - Sensor (large area ~10 X 7 cm^2) in thermal equilibrium with surrounding gas

Strip Detector: double sided device

- AC coupled Silicon sensors with integrated bias resistors:
  SiO_2 layer forms integrated capacitors. Bias resistors realised with polysilicon structures or transistor devices (punch through).

- Double sided Silicon sensors:
  Backside implant structured, allows dimension measurement with one sensor ➔ very sophisticated production process.

- Double metal layers:
  2nd metal layer to route signal from strips to electronics.



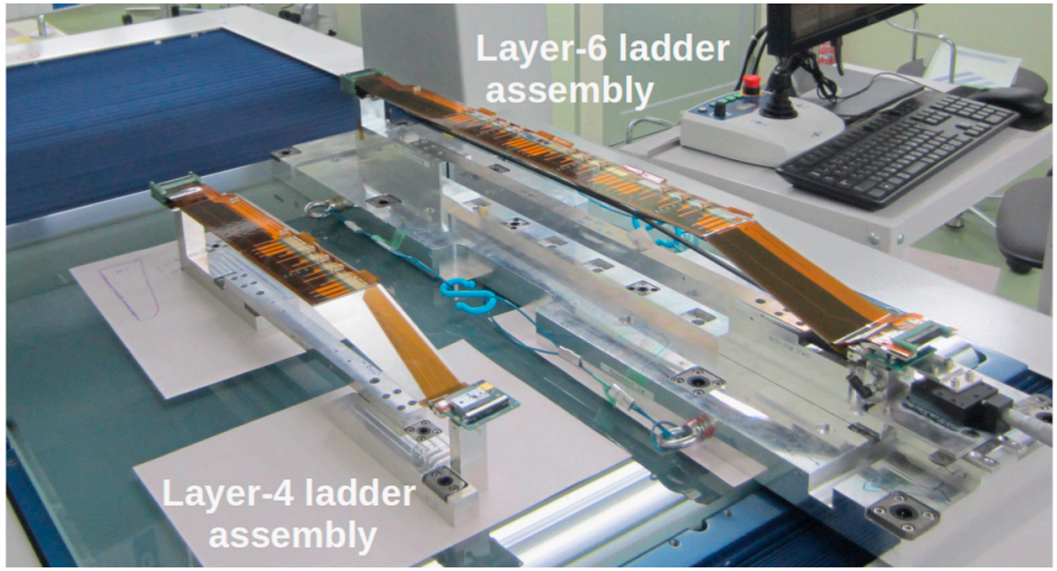
Double sided, AC coupled sensor with double metal layer

- Pros:
  - two coordinates in one silicon layer
- Cons:
  - Double sided technology: more processing steps (increase cost)
  - bit more complicate bias/readout scheme
  - Typical thickness ~250-320 μm, difficult to start from thinner wafers and cannot be thinned after processing

i.e. Double sided Belle2 strip tracker

- The SVD, consists of four layers of DSSD sensors *
  - Thickness: 300 or 320 µm
  - Two coordinates per Si layer, max area ~12 X 6 cm^2 (6-inch wafer)
  - excellent spatial (~ 20µm)
- The sensors are supported by carbon fiber reinforced ribs with AIREX core to decrease material budget.

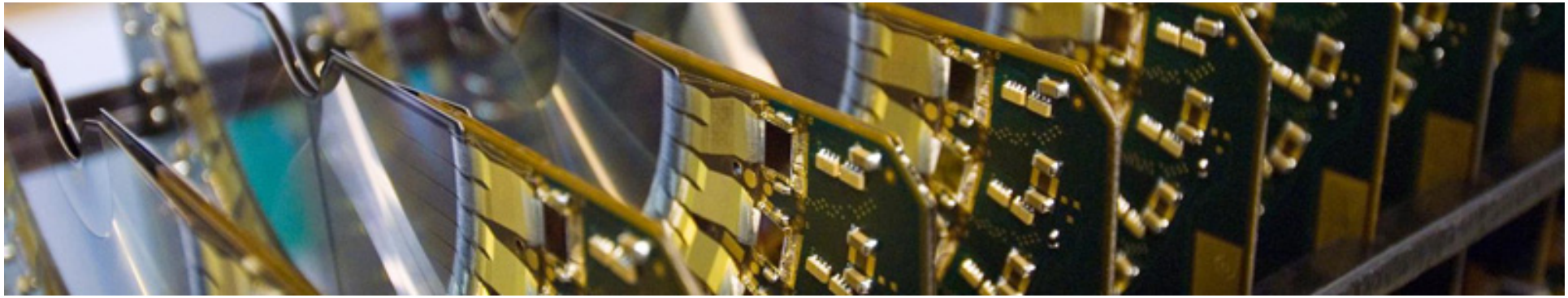
* Hamamatsu Photonics (Japan) and Micron Semiconductor (UK)



- Material budget:
  - Silicon sensor
  - Kapton circuits
  - Mechanical support
  - cooling

i.e. LHCb

- VeLo LHCb



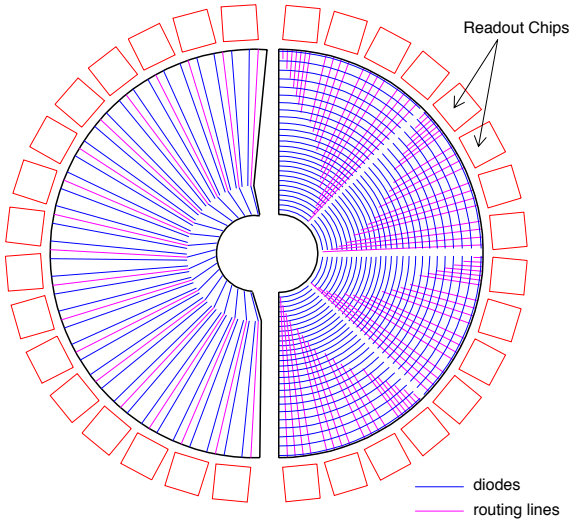


Fig. 2. Schematic diagram of the VELO sensor lay-outs (left: ϕ-measuring sensor, right: R-measuring sensor).

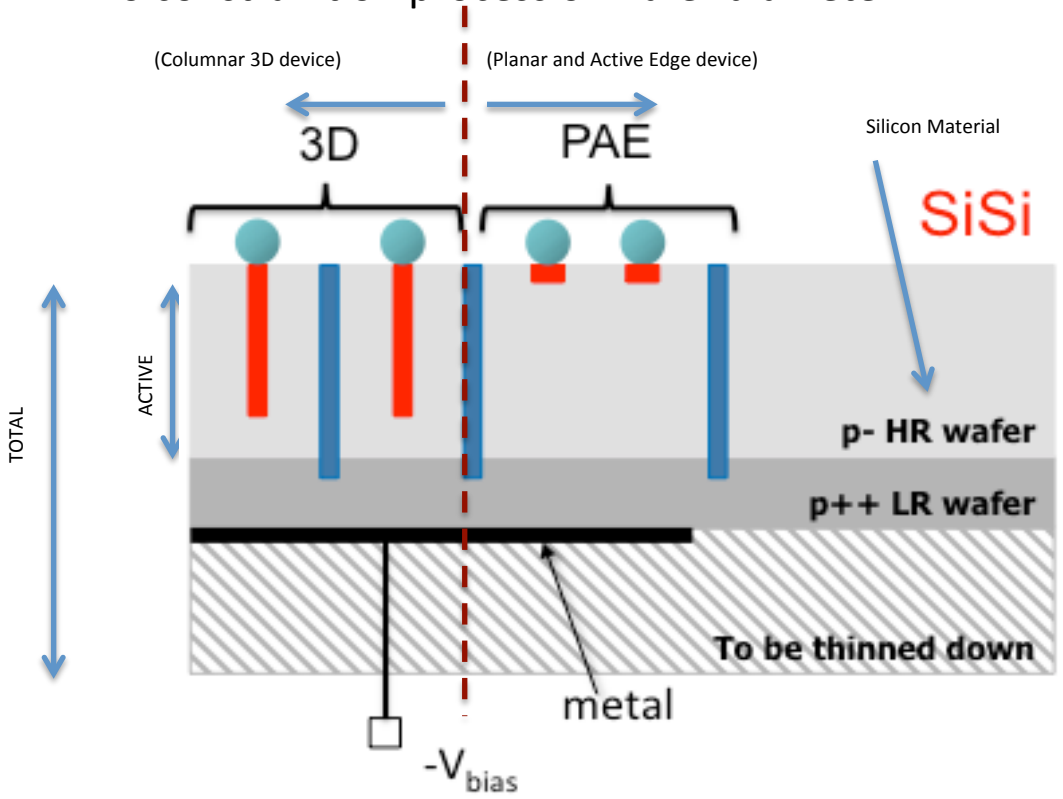
Wafer options for small material budget

1. "native" thin Float-zone wafer
   - Safe configuration: 6-inch wafer 200 μm thick
     - Hamamatsu is providing such a sensors, processed as single sided device, for the CMS tracker upgrade
       - » Thin implies single sided processing

2. "standard" thick Float-zone wafer
   - Typical thickness of 300-320 μm on 6-inch (on 8-inch) wafer
   - Thinning by mechanical grinding and/or chemical etching of the back side (after front side processing)
     - Minimum thickness limited by the "post thinning" processing steps on the back side:
       - High dose ohmic implant + metal sputtering
         - » Only single sided device

Wafer options for small material budget

3. Processed wafer build by an active wafer on top of a carrier wafer (mainly conductive),
   - no constraint on process or wafer diameter



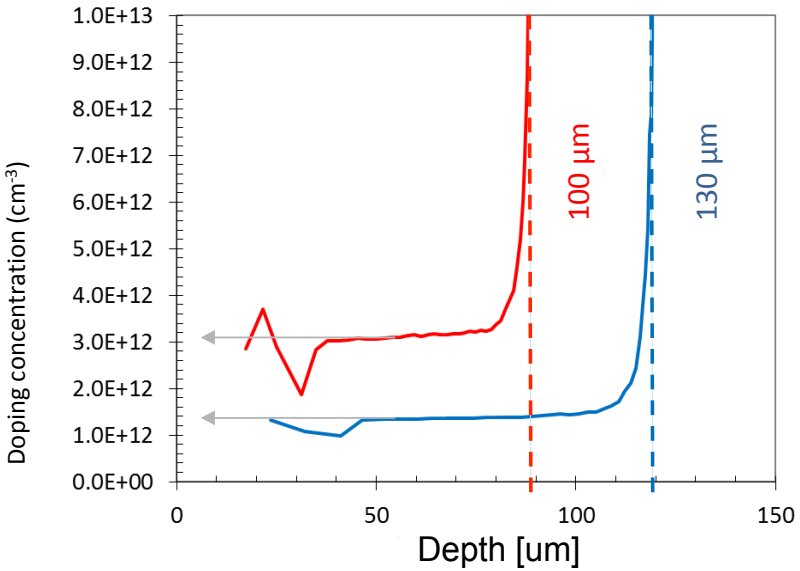
Typical material:
Float Zone high resistivity
Junction depleted at low bias

Typical material:
Czochralski low resistivity

- Active Thickness (Si-AT): primary charge generation
- Total thickness (Si-TT): material budget
  - Single sided device

Wafer options for small material budget

- Such raw material can be made available by using two technologies:
  a. Si-Si Direct Wafer Bond: starting from two single wafers, no constraint on the active thickness
     i. Si-Si DWB: common wafers interface melting
        – Active thickness electrically accessible from back side



- Active thickness not sharply defined:
  – Doping concentration profile measurement: effective thickness reduced by the Boron diffusion (for SiSi) from wafer carrier deep about 10 µm.

Wafer options for small material budget

- Such raw material can be made available by using two technologies:
  a. Starting from two single wafers: no constraint on the active thickness
     i. Si-Si Direct wafer bond: common wafers interface melting
        – Active thickness electrically accessible from back side
     ii. SOI: no melting at Si-Oxide interface
        – Active thickness well defined, however electrically isolated, solution as trench needed

Wafer options for small material budget

- Such raw material can be made available by using two technologies:
  a. Starting from separate wafers: no constraint on active thickness
     - Si-Si Direct wafer bond: common wafers interface melting
       - Active thickness electrically accessible from back side
     - SOI: no melting at Si-Oxide interface
       - Active thickness electrically isolated, solution as trench needed

  b. Epitaxial layer on handle wafer
     - small thickness available (< 100 μm) given the slow growth speed
       - Active thickness electrically accessible from back side
       - Constraint on wafer size

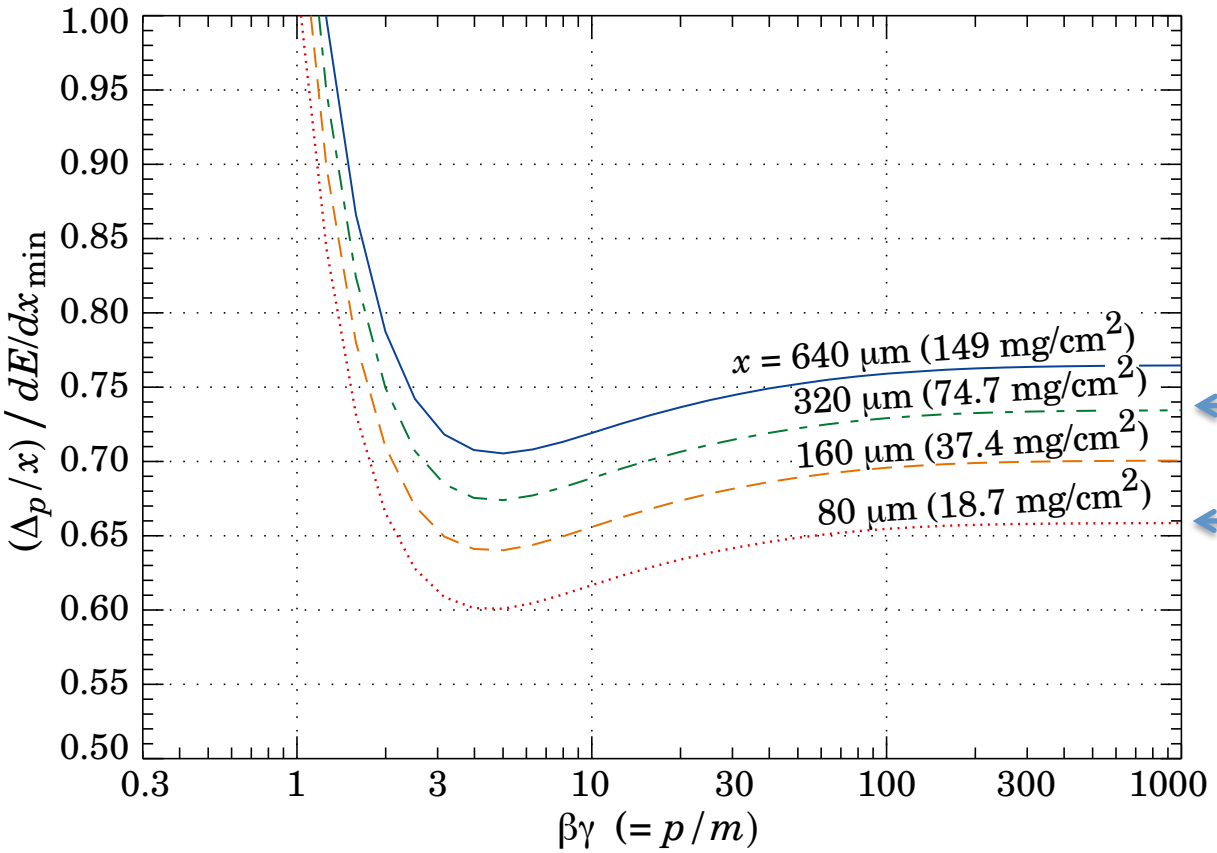
- For both (a. and b.) technologies:
  - Processing of single sided device
  - No high dose ohmic implant needed on the back side
  - Metal sputtering for uniform electrical contact after thinning

Thickness options and implications

- Silicon Material budget :
  - X_0 value: 21.82 g cm^{-2} or 9.37 cm
    - 300 μm corresponds to 0.32% X_0
- Thinning is a solution in order to decrease material budget
  - However there are implication on
    - Design rules
    - Devices technology
    - Wafer size and detector area
    - Manufacturer
    - Detector assembly steps

» Consider also mechanical support and services in the material budget.

Signal = charge produced in the Si-AT



At minimum βγ ~3

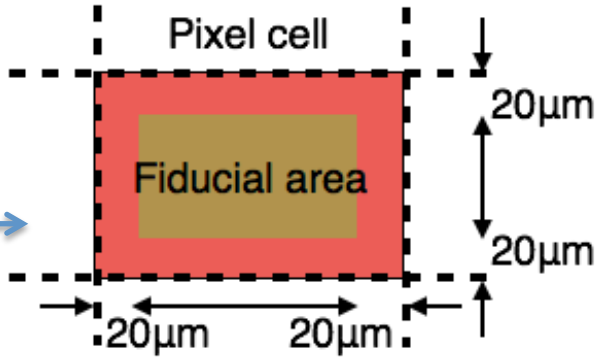
23k-24k (e-h) pairs

5k-6k (e-h) pairs

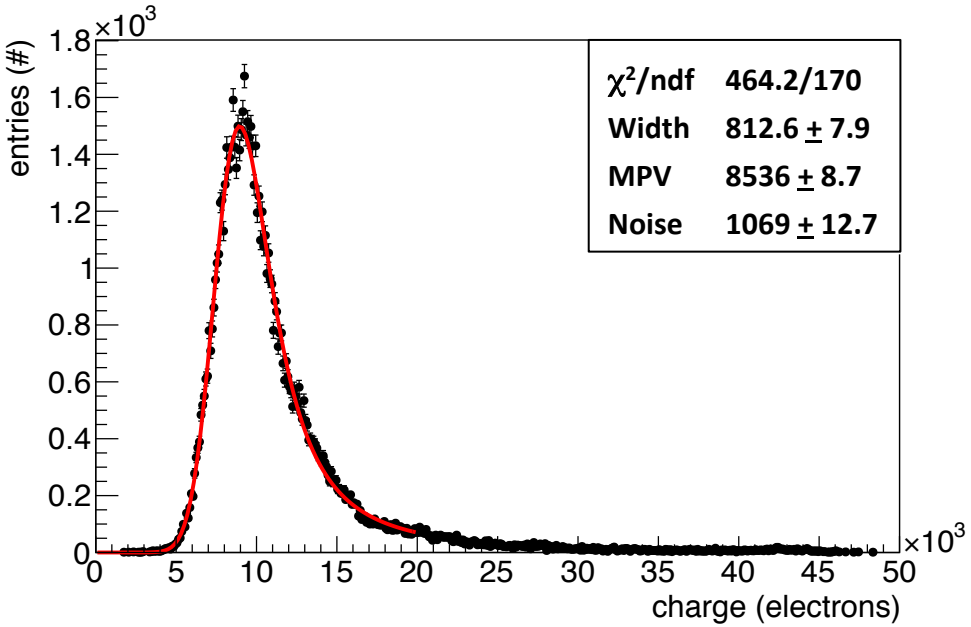
Figure 31.9: Most probable energy loss in silicon, scaled to the mean loss of a minimum ionizing particle, 388 eV/μm (1.66 MeV g^{-1}cm^2).

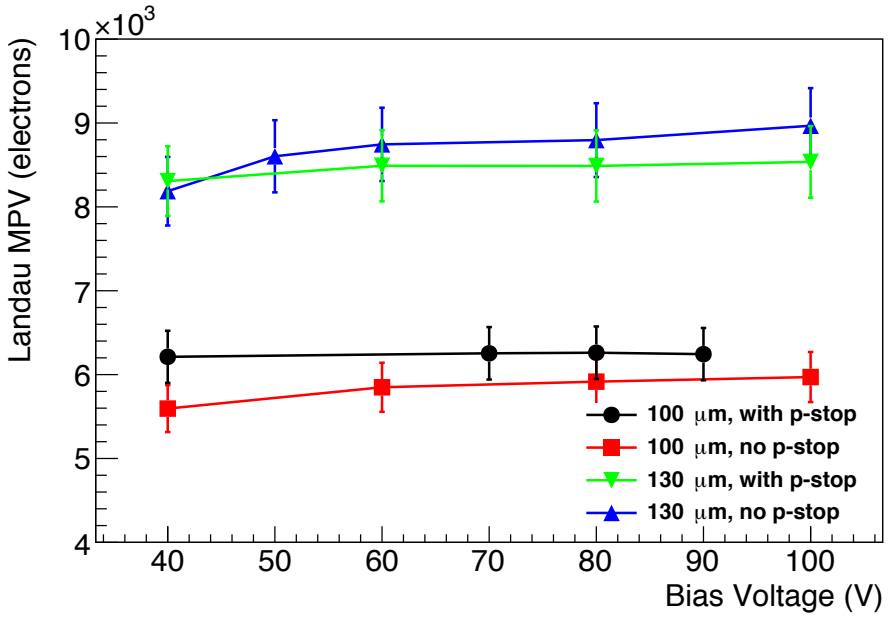
i.e. charge on thin hybrid pixel sensors (CMS)

- **Standard** pixel prototype ***SiSi DWB***
- Require single pixel clusters
- Tracking pixel telescope selection:
  - the predicted track impact point should be located ± 20 µm far from pixel cell edges (two sides)



Dev. 45C: 130 µm Active + 50 µm carrier, V_{bias}=100V



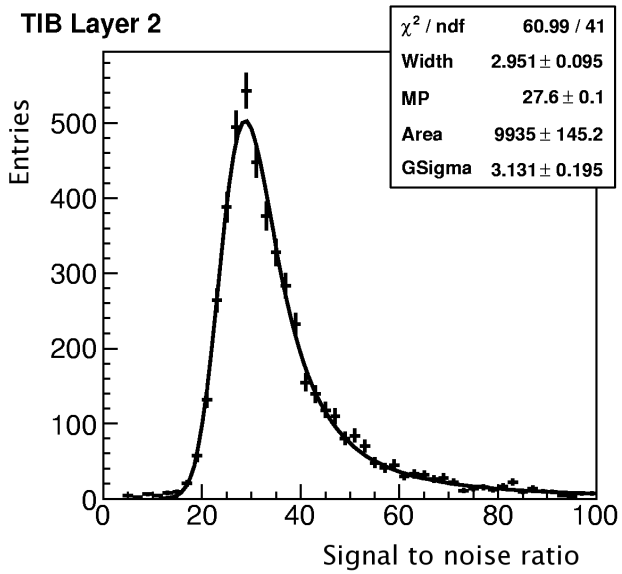


Averaging over full sample the Ratio MPV@130um / MPV@100 is ~1.38 , expected [1.2-1.44]
Detector material budget: silicon sensor 0.16 - 0.19 % X_0 + ROC 0.186 % X_0

Thin Silicon Strip sensor: design rules

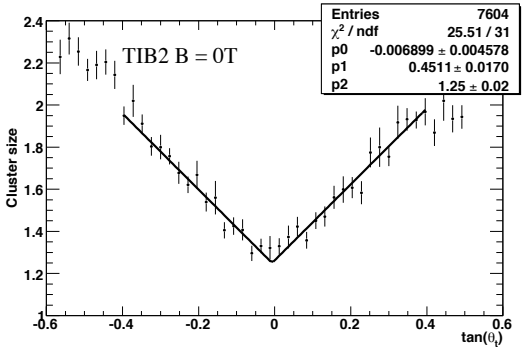
- Detector performance provided by the S/N ratio (SNR)
  - SNR affects:
    - Track detection efficiency
      - » ***SNR > 10-12 for a good detection efficiency***
    - Point resolution σ = pitch/SNR (charge sharing)
  - SNR ingredients:
    1. Signal S given by the collected charge
       - Depends on Si-AT, ionization charges (e-h) pairs
    2. Noise N given by C load and Read-Out speed
       - Depends on Si-AT
       - Segmentation geometry
         - width/pitch ratio ~ 0.25, compromise between:
           - high width/pitch ratio that reduces the field peak located at the p^+ edge
           - low value that reduces the total strip capacitance
         - strip length
       - i.e. noise parameterization for APV25 readout, fast shaping time
         - *noise*(e) = (427 ± 39) + (38.7 ± 3.0) x strip *length* (*cm*)

i.e. CMS Silicon Strip sensor

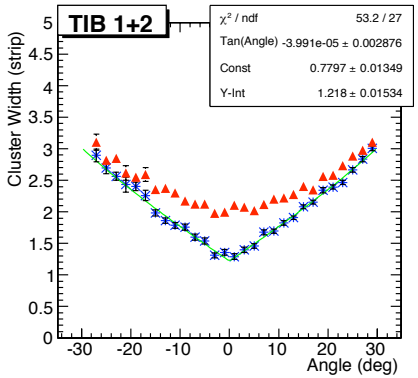


- i.e. CMS tracker silicon strip
  - 320 μm Si-AT
  - Strip geometry
    - Pitch 121 μm, w/p=0.25
    - length ~10 cm, width ~6 cm

- Cluster charge vs track incident angle:
  - Minimum size 1.2 strip (pitch = 80 μm)
  - Strip length ~10 cm

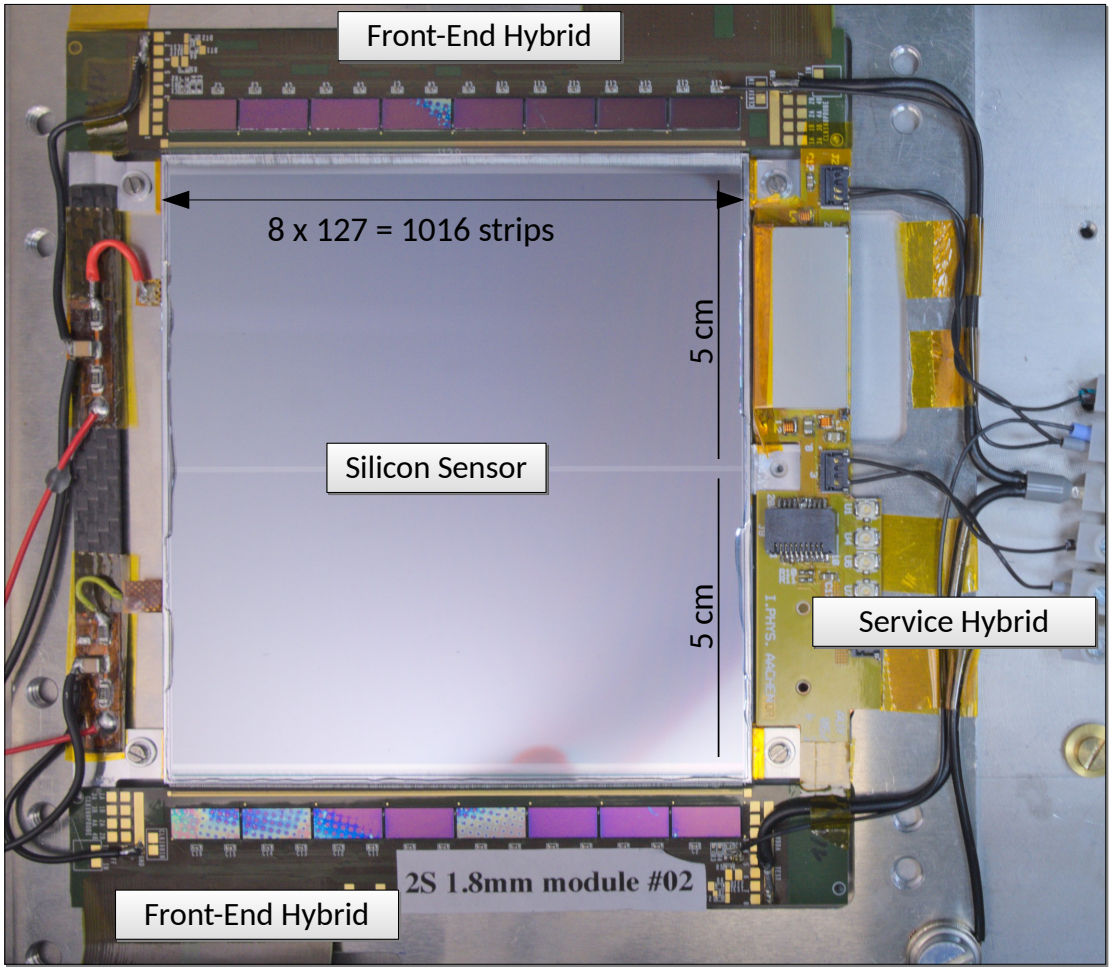


- Strip sharing increases with inter-strip coupling
  - Electrodes capacitance sensitive to design (pitch and width)
    - Blue 3%, Red 7%



i.e. thin strip detectors readout by CBC (CMS)

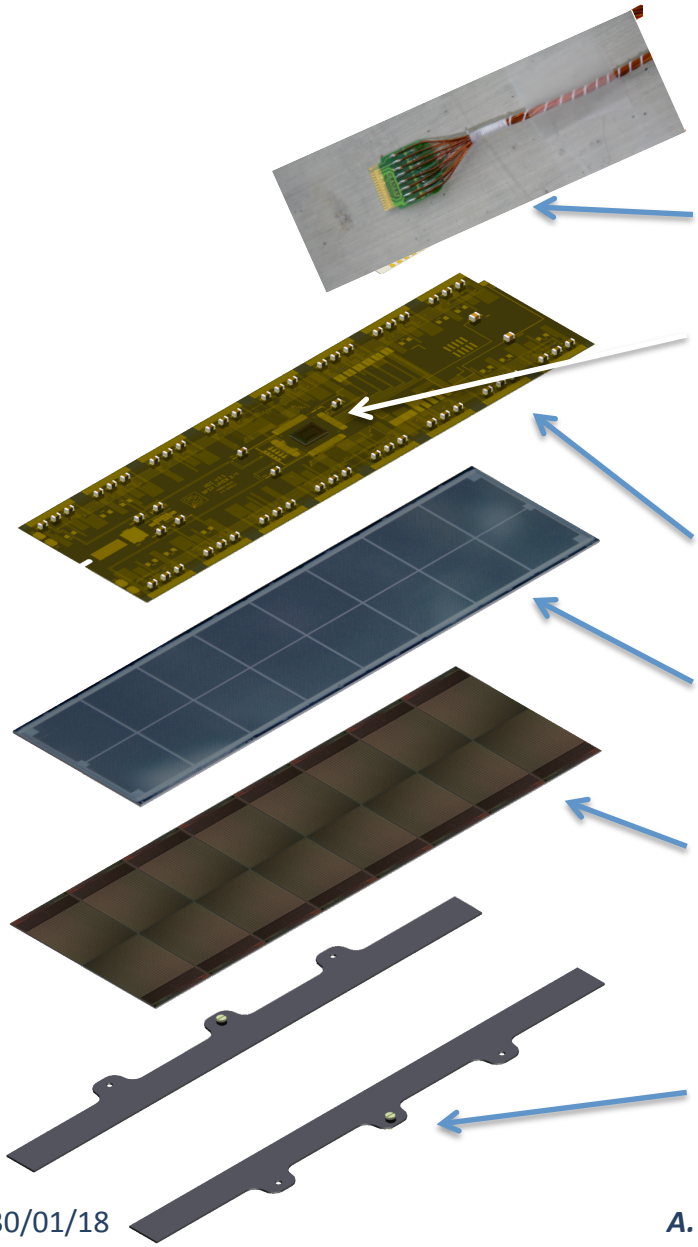
- Target thickness of 200 μm, Single sided device
  - Large area sensor processed on 6-inch wafer *



- 240 μm thick full size n-in-p type Sensors, each with 2x1016 strips (~8 pF strip capacitance)
- Thinner Si-AT implies less charge and shorter strips
  - A large area sensor is divided in two half readout independently
- Sensor width defined by
  - Read-Out chip pitch
  - Number of chip managed by the hybrid circuitry

*Hamamatsu

Pixel detectors: hybrid design. i.e. CMS BPIX



Cable & Connector
Twisted pairs ~ 1 mt long in order to move material far from IP.

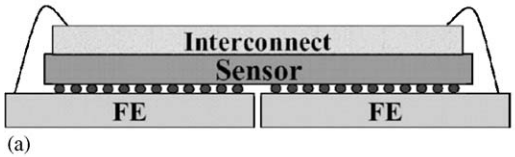
TBM
Data processor

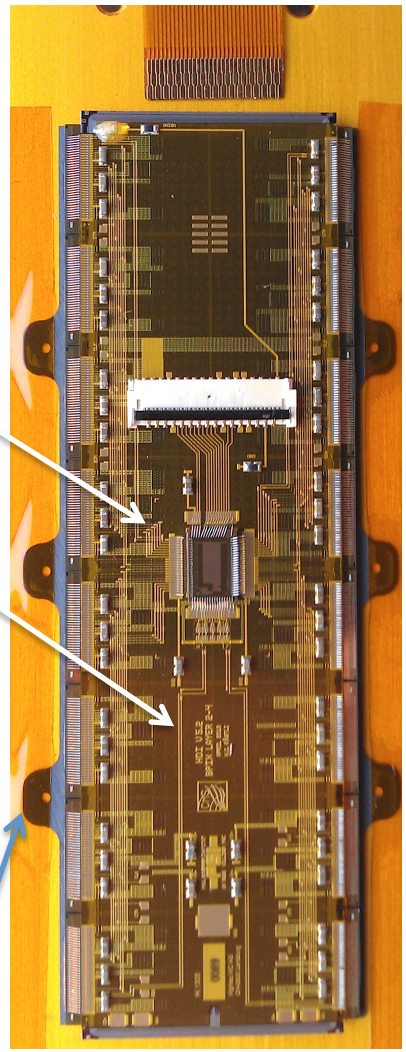
HDI multiple ROC pixel circuit

Silicon Sensor
2008 n+/n cell 100X150 μm
Full size 12 cm^2

16 ROCs Digital PSI46Dig
(5000ch/cm^2)
Charge digitized 8 bit, 40 MHz

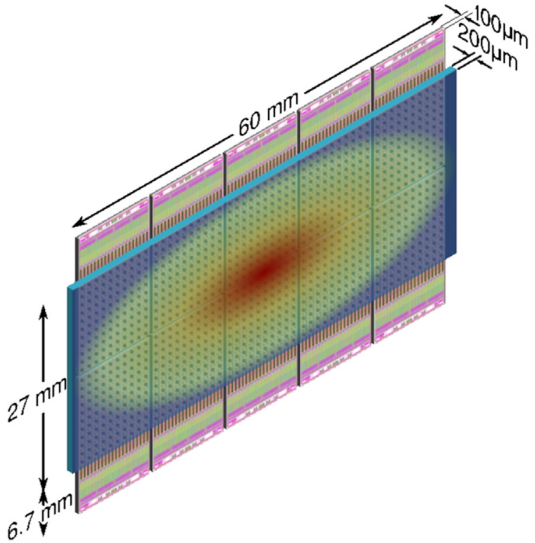
SiN Base strips
200 μm thick: support and cooling





i.e. Hybrid pixel: NA62 giga-tracker

- Total amount of silicon can be kept below 0.32% X_0 per station
  - Two coordinates measurement per layer
  - sensor thickness of 200 μm good compromise between
    - minimum material budget
    - fast charge collection
    - signal large enough for the electronics chain.
    - Pixel size/pitch 300 X 300 μm^2
  - The silicon on the ROC chip side thinned down to 100 μm.
  - Cooling and support by a single 125 μm thick carbon fiber structure, corresponding to about 0.06% X_0
- Module size defined by the ROC technology



i.e. thin Pixel detectors ILC/Belle2

- The basic building block of the Belle II PXD is a DEPFET module
  - sensor matrix with 250 columns and 768 rows
  - Pixel size in the inner layer r–ϕ is 50 µm X 55 µm
- A module is fabricated on special SOI silicon wafer, which allows a thinning of the sensitive area to 75µm.
  - Si-AT not relevant here for ionization charge (e-h) pair generation

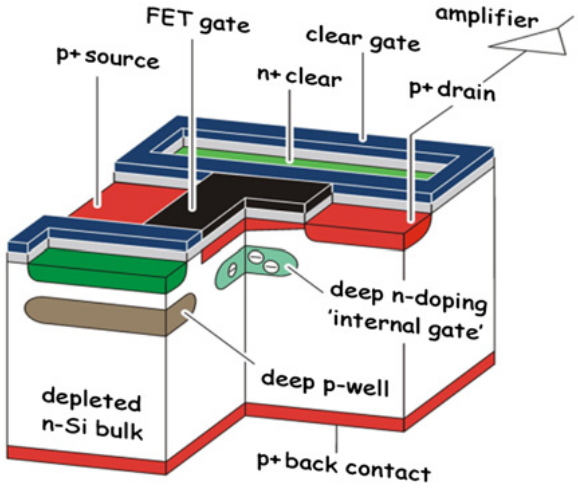


Fig. 1. The MOS-type DEPFET.

Table 1
Comparison between the requirements of ILC and the baseline design for SuperKEKB.

Parameter	ILC	SuperKEKB
Number of layers	5	2
Number of pixels (inner layer)	512×4096	215×1024
Pixel size	25×25 µm^2	50×75 µm^2
Material budget	$0.1\% X_0$	$0.1–0.15\% X_0$
Ionizing radiation	10–50 kRad/a	~1 MRad/a
Row processing time	20–50 ns (two-fold readout)	~100 ns (four-fold readout)
Frame time	25–50 µs (inner layer)	10–20 µs

i.e. thin Pixel detectors ILC/Belle2

- Including the frame and the SWITCHER chips the average radiation length of a module within the Belle II acceptance is only 0.21% X_0

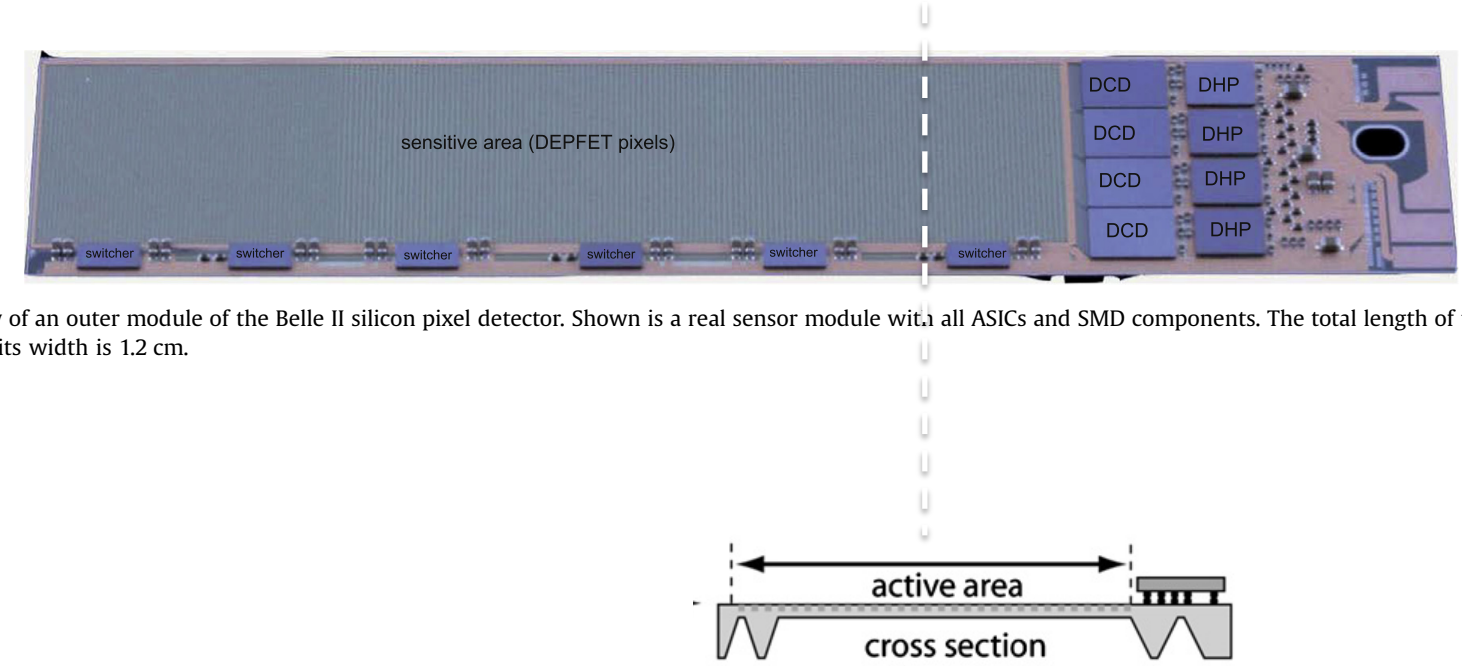


Fig. 2. View of an outer module of the Belle II silicon pixel detector. Shown is a real sensor module with all ASICs and SMD components. The total length of this module is 8.5 cm and its width is 1.2 cm.