# TimeSPOT WP3 Workshop: Introduction to 28 nm CMOS

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UNIVERSITÀ
DEGLI STUDI
DI MILANO

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# TimeSPOT WP3 Target: MiniASIC in 28 nm

We plan to use the **mini@asic** fabrication service, provided by Europractice/IMEC.

Advantage:

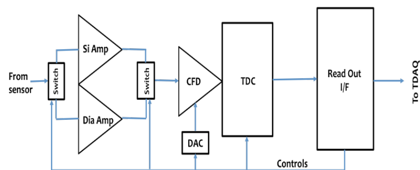
- LOW COST: 2017 Price 23 kEUR per block of 1570x1570 microns

Disadvantage:

- Fixed area; pad-limited chip
- Few submission dates (in April and in October)

Our target: **First submission in Oct. 2018** (submission dates do be confirmed for the second half of 2018)

# TimeSPOT WP3 Activities




| | Cagliari | Milano | Torino |
|---:|---|---|---|
| **CSA** | | | × |
| **Discriminator** | | | × |
| **TDC** | × | | |
| **DAC** | × | × | |
| **BandGap** | | ×(+BG) | |
| **LVDS** | | ×(+BG) | |
| **OpAmp (Voltage Buffer)** | × | × | |
| **Standard cells** | | × | |
| **[Digital I/F]** | | | |

Preliminary meeting held in Milano on Nov. 23, 2017; Kick-off meeting held in Cagliari on Dec. 1, 2017.

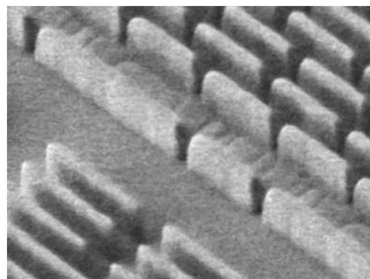
# Technology choice: 28 nm

28 nm is a common and mature technology
(Xilinx Kintex-7, Nvidia 600-700-900 series)

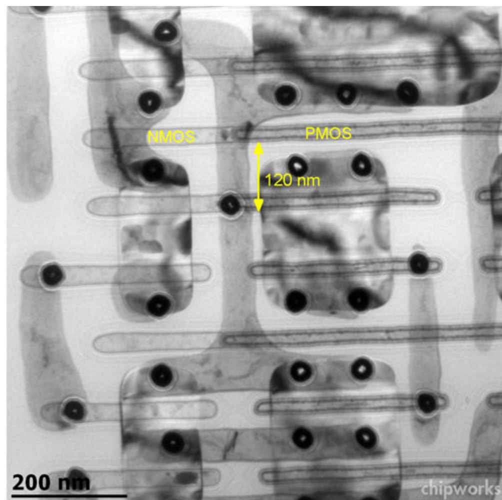
- Minimum gate length 28 nm
- Minimum gate pitch 120 nm

- UV $\lambda >$ gate length

- Interference figure needed to fabricate transistors
- "REGULAR FABRICS"
- More (and complex) design rules

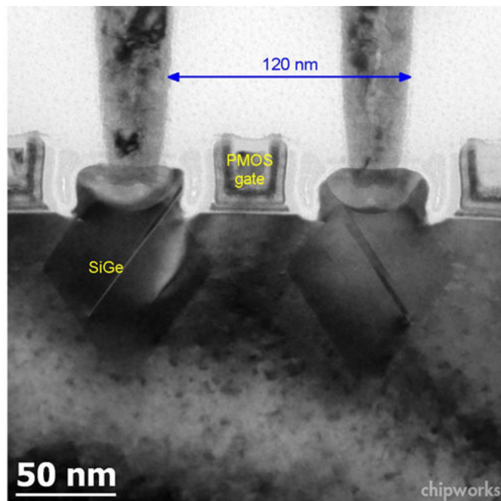


# Images (1)




Xilinx XC7K325T Kintex-7 TSMC 28 nm HPL - Plan View TEM
(from https://www.chipworks.com/about-chipworks/overview/blog/ /review-tsmc-28-nm-process-technology)

# Images (2)




Altera 5SGXEA7K2F40C2 Stratix V 28 nm HP PMOS - TEM
(from https://www.chipworks.com/about-chipworks/overview/blog/ /review-tsmc-28-nm-process-technology)

# Example: TSMC 28 nm 'flavors'

(from https://www.semiwiki.com/forum/content/ /4530-tsmc-unleashes-aggressive-28nm-strategy-e.html)

28 nm technologies from TSMC

| | |
|---|---|
| **HP** | (high performance) |
| **HPM** | (high performance mobile) |
| **HPC** | (high performance computing) |
| **HPC+** | (faster version of HPC) |
| **HPL** | (high performance low power) |
| **LP** | (low power) |
| **ULP** | (ultra-low power for IoT and other battery powered applications) |

# Big differences in 28 nm 'flavors'

**Low power** versions use conventional **poly gate with ONO dielectric**
⟶ low gate capacitance, low on-current, low leakage
⟶ SUITABLE FOR PORTABLE DEVICES WITH **STAND-BY OPERATION**

**High performance** versions use **high-k metal gate (HKMG) transistors**
⟶ high gate capacitance, high on-current, high leakage
⟶ **HIGHER SPEED, HIGHER POWER CONSUMPTION**

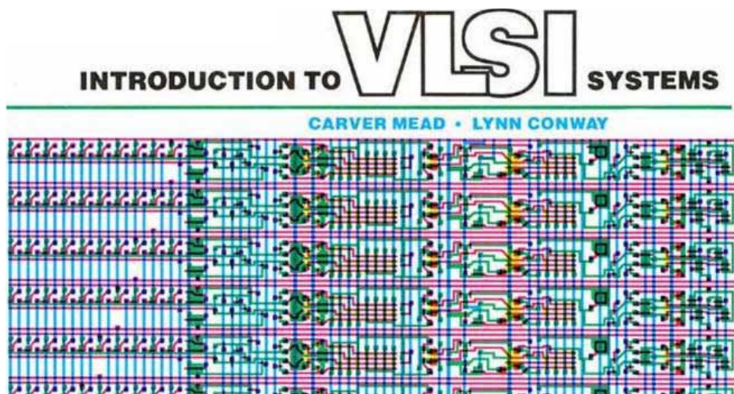
We are focussing on 28 nm HPC with 10 metal layers (needed for interconnections in high-density logic)

# 28 nm technology features

TWO key factors:

1. **NEW MATERIALS**: silicon dioxide is replaced by high-$\kappa$ dielectrics, not compatible with polysislicon gate
2. **SMALL SIZE**: larger process variation and mismatch

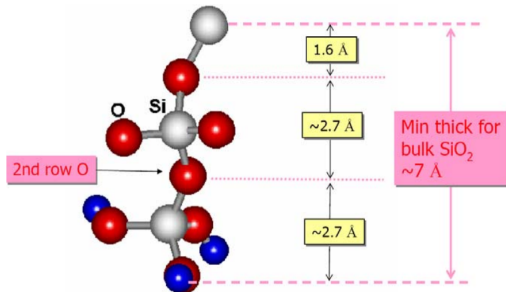
# 28 nm new materials – why?

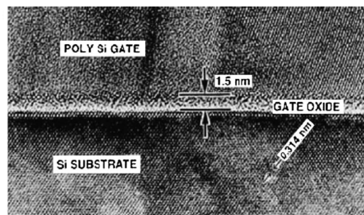


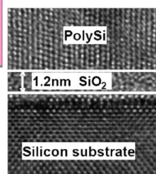

A famous textbook published in 1979 predicted that 0.25 µm would have been the scaling 'limit' for CMOS, due to the tunneling current through the thin gate oxide.
**Silicon dioxide 'survived' until 65 nm CMOS.**
Now $SiO_2$ is being replaced by exotic materials.

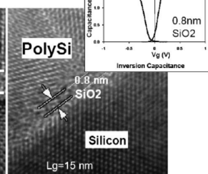
# Minimum oxide thickness

Minimum gate oxide thickness: 0.7 nm (theoretical) / 0.8 nm (demostrated)



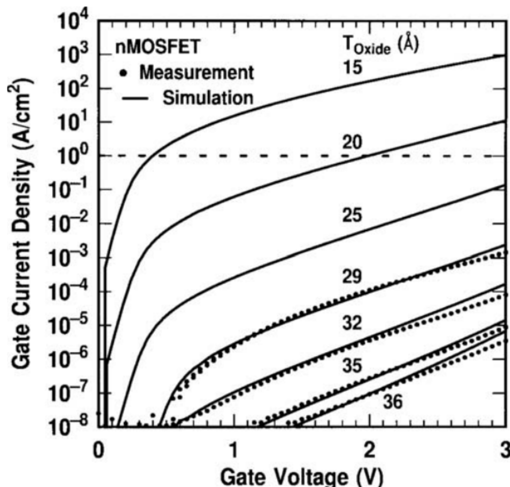




H. Wong, H. Iwai, "On the scaling issues and high-$\kappa$ replacement of ultrathin gate dielectrics for nanoscale MOS transistors", *Microelectronic Engineering* **83** (2006) 1867–1904.

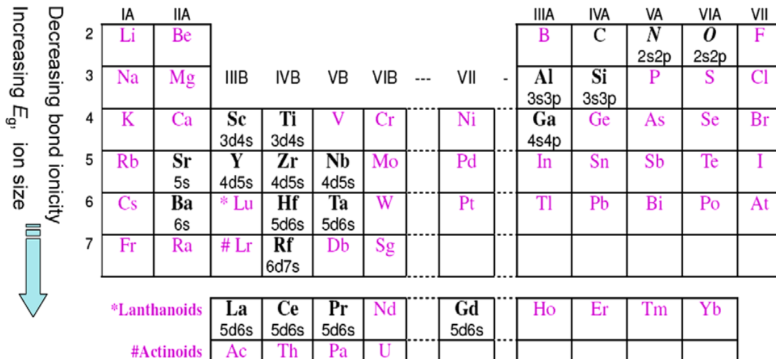
# Direct tunneling current




S.-H. Lo, D.A. Buchanan, Y. Taur, W. Wang, "Quantum-Mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's", *IEEE Electron Device Letters* **18** (1997) 209-211.

# Candidate materials for insulating gate

Part of the periodic table. Elements in **bold** (cations) can be combined with elements in *italic* (anions) to form an insulator.




H. Wong, H. Iwai, "On the scaling issues and high-$\kappa$ replacement of ultrathin gate dielectrics for nanoscale MOS transistors", *Microelectronic Engineering* **83** (2006) 1867–1904.

# HK dielectrics

**HK** = high-$\kappa$
$\kappa = \epsilon_r$ is the (relative) dielectric constant of the insulator

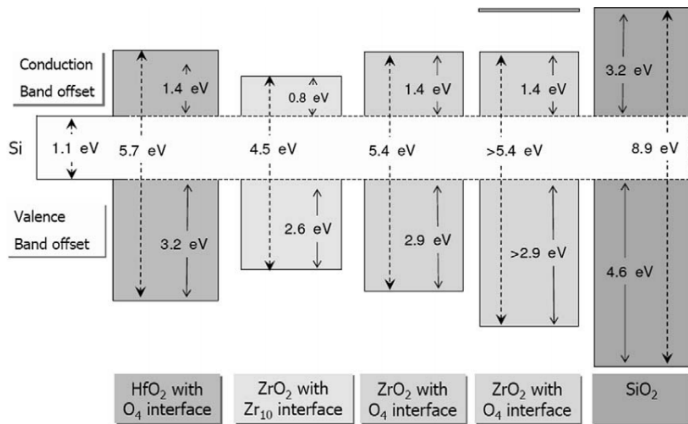
- Air has $\epsilon_r = 1$ (like 'vacuum')
- $SiO_2$ has $\epsilon_r = 3.9$
  - but tunneling occurs for $t_{ox} < 3$ nm
  - and $t_{ox}$ must be very thin to achieve high gate capacitance

Higher dielectric constant is required, together with other properties:

- the material must be an insulator (both for electrons and for holes)
- must be compatible with silicon and stable over time at operating temperature
- must be compatible with the gate electrode material

# Energy gap

Examples of “good” insulators for both NMOS and PMOS transistors:




H. Wong, H. Iwai, “On the scaling issues and high-$\kappa$ replacement of ultrathin gate dielectrics for nanoscale MOS transistors”, *Microelectronic Engineering* **83** (2006) 1867–1904.

# Properties of insulators

Table 4
Comparison of various characteristics and main features of existing and potentially high-$\kappa$ gate dielectrics

| Dielectric | Dielectric constant (bulk) | Bandgap (eV) | Conduction band offset (eV) | Merits | Drawbacks |
|---|---|---|---|---|---|
| Silicon dioxide ($SiO_2$) | 3.9 | 8.9 | 3.15 | Excellent Si interface, low $Q_{ox}$ and $D_{it}$ | Low-$\kappa$, EOT > 0.8 nm |
| Silicon nitride ($Si_3N_4$) | 7–7.8 | 5.3 | 2.1 | Good interface and bulk properties, medium $Q_{ox}$ and $D_{it}$ | Low-$\kappa$, EOT > 0.5 nm |
| Aluminum oxide ($Al_2O_3$) | 9–10 | 8.8 | | $E_g$ comparable to $SiO_2$, amorphous Good thermal stability | Medium $Q_{ox}$ and $D_{it}$, medium $\kappa$ |
| Tantulum pentoxide ($Ta_2O_5$) | 25 | 4.4 | 0.36 | High-$\kappa$ | Unacceptable $\Delta E_C$, not stable on Si, |
| Lanthana ($La_2O_3$) | ~27 | 5.8 | 2.3 | High-$\kappa$, better thermal stability Low $D_{it}$ | Moisture absorption, instable with Si High $Q_{oxt}$ |
| Gadolinium oxide ($Gd_2O_3$) | ~12 | ~5 | –[a] | –[a] | Crystallization |
| Yttrium oxide ($Y_2O_3$) | ~15 | 6 | 2.3 | Large $E_g$ | Low crystallization temperature, hight $D_{it}$, silicide formation |
| Hafnia ($HfO_2$) | ~20 | 5.6–5.7 | 1.3–1.5 | Most suitable compared to other candidates | Crystallization, silicate and silicide formation, |
| Zirconia ($ZrO_2$) | ~23 | 4.7–5.7 | 0.8–1.4 | Similar to hafnia | High $Q_{ox}$ and $D_{it}$ Marginal stable with Si, crystallization, silicide formation |
| Strontium titanate ($SrTiO_3$) | ~300 | 3.3 | −0.1 | High-$\kappa$ | Unacceptable $E_g$ and $\Delta E_C$, field fringing effect |

Data from Robertson [131], Gusev et al. [132], Hubbard and Schlom [133], and other sources. Slightly different values of those parameters were report time to time.

H. Wong, H. Iwai, "On the scaling issues and high-$\kappa$ replacement of ultrathin gate dielectrics for nanoscale MOS transistors", *Microelectronic Engineering* **83** (2006) 1867–1904

# The insulating layer: HfSiON

"Best" option for today's MOS transistors:

**HfSiON**: hafnium-silicon oxinitride ($Hf_wSi_xO_yN_z$)

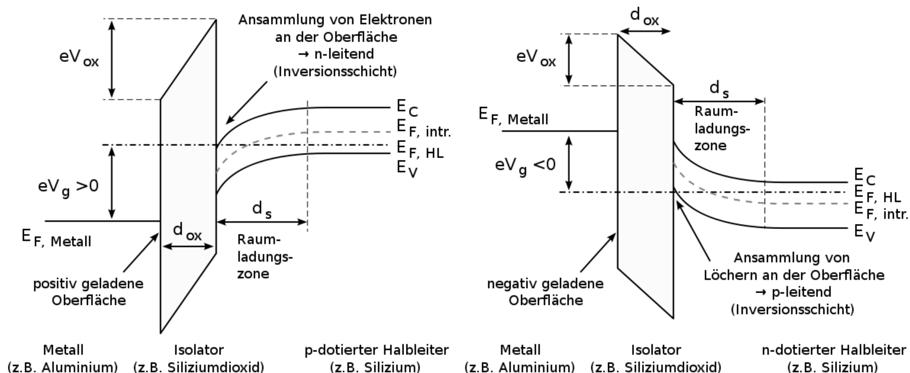
with $\approx 50\,\%$ Hf $+$ $50\,\%$ Si, and $\approx 80\,\%$ O $+$ $20\,\%$ N

obtained by ALD (Atomic Layer Deposition), which is a variant of CVD (Chemical Vapour Deposition)

For the future: $La_2O_3$ is a very promising insulator, but it is more diffcult to process

# Gate electrode compatibility

We need both NMOS and PMOS transistors with the correct energy bands (NMOS with positive threshold voltage and PMOS with negative threshold voltage): the gate electrode material must have a workfunction in a "good" range




from de.wikipedia.org

HfSiON is not compatible with polysilicon gate!

# “Metal gate”

TiN (titanium nitride) can be used as gate electrode of PMOS transistors (TiN gate).
TiN is a ceramic material with very high mechanical hardness, and high electrical conductivity (unusual for a ceramic); it is used as a protective coating for edge retention in tools (drill bits, cutters).

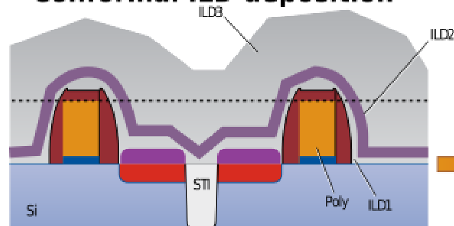
from `en.wikipedia.org`

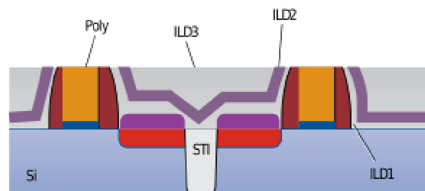
By adding aluminium, the workfunction of Tin can be made suitable also for NMOS transistors (TiAlN gate).

L.P.B. Lima, H.F.W. Dekkers, J.G. Lisoni, J.A. Diniz, S. Van Elshocht, “Metal gate work function tuning by Al incorporation in TiN”, *Journal of Applied Physics* **115**, 074504 (2014)

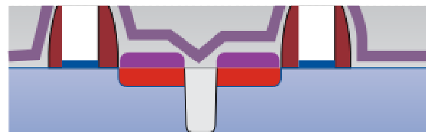
# TiN gate deposition

TiN / TiAlN gate fabrication ("GATE LAST"):

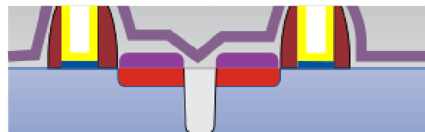



Sacrificial Poly removal



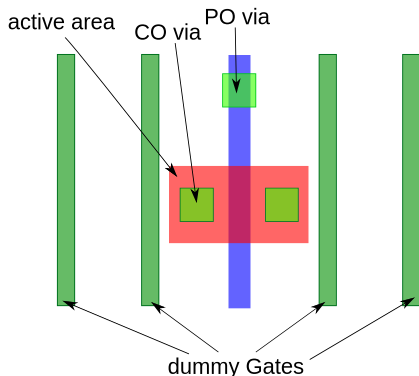
TiN (or TiAlN) Gate deposition



The CMP (Chemical-Mechanical Polishing) is critical!

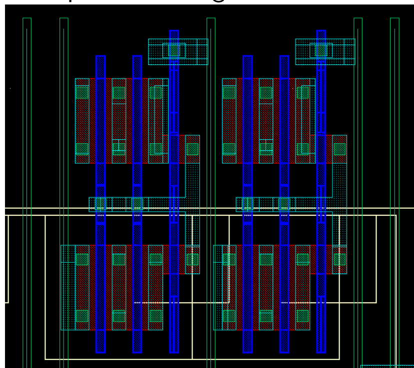
# Dummy gates for planarization

Dummy gates are required **for both lithography and planarization**




- Two dummy gates per side
- Fixed space between gates
- No L-, T-, U-shaped gates
- Contact larger than min. gate

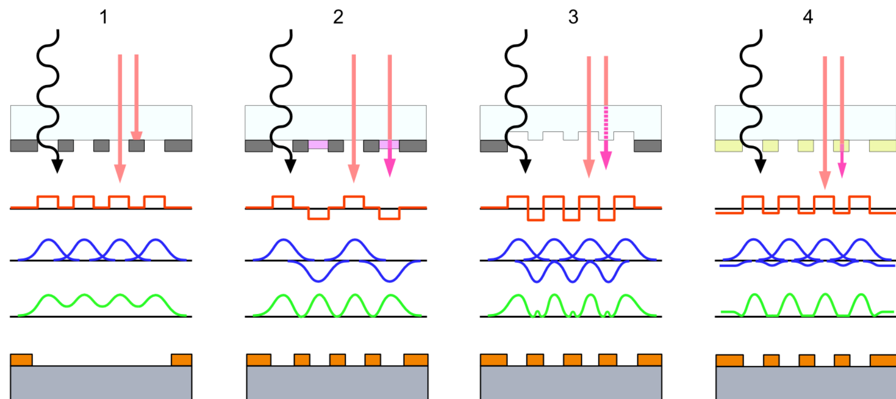
Example: multi-finger transistors



- Different width is possible

# Phase Shift Masks

Conventional masks are "binary" masks (0 = opaque, 1 = transparent)
Phase Shift Masks are "ternary" masks (0 = opaque, 1 = transparent with 0°, −1 = transparent with 180°)




from en.wikipedia.org

The photoresist reaction occurs only above a given intensity threshold

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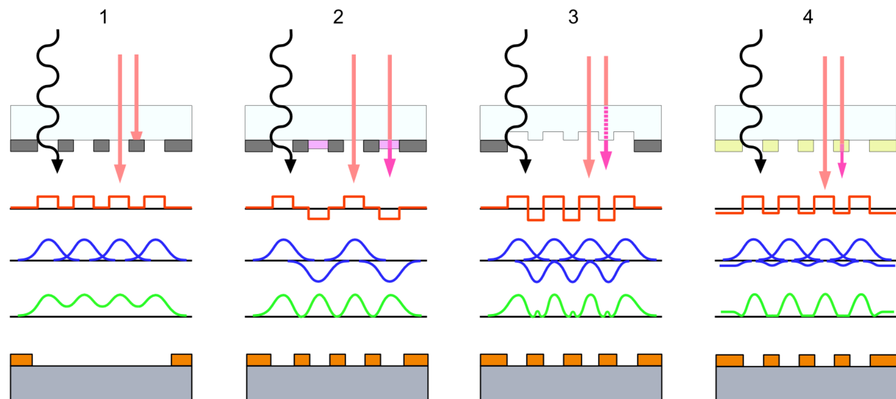
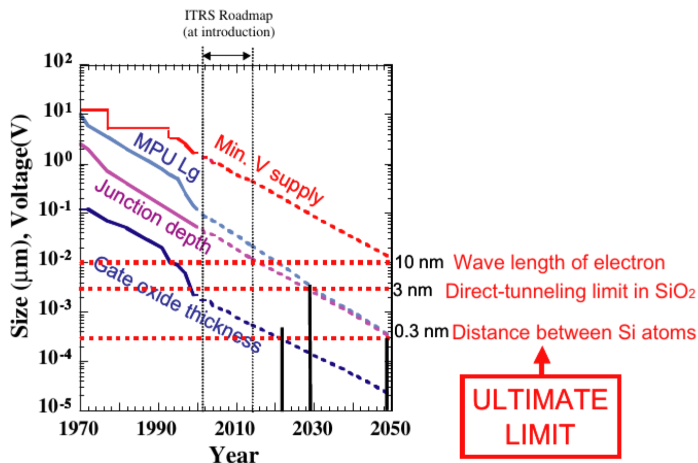



from en.wikipedia.org

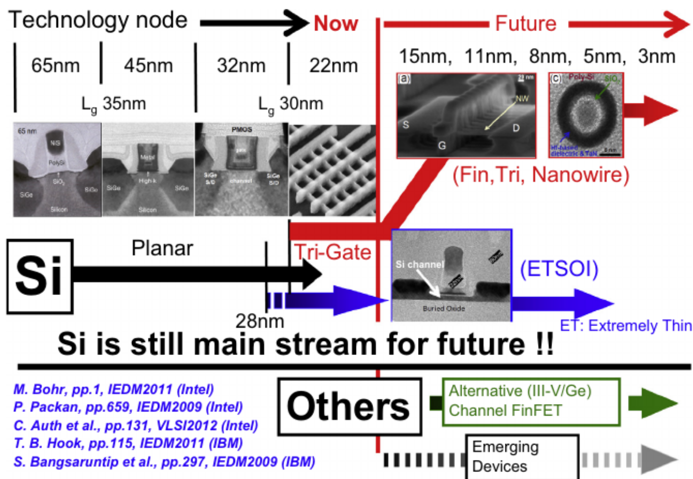
The photoresist reaction occurs only above a given intensity threshold

# The ultimate limit of silicon?



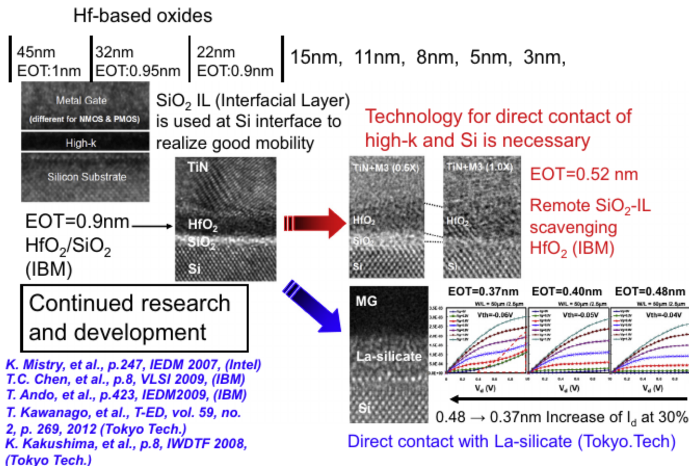

Hiroshi Iwai, "CMOS downsizing toward sub-10 nm", *Solid-State Electronics* **48** (2004) 497–503.

# The future of silicon (1)




Hiroshi Iwai, “Future of nano CMOS technology”, *Solid-State Electronics* **112** (2015) 56–67.

# The future of silicon (2)




Hiroshi Iwai, "Future of nano CMOS technology", *Solid-State Electronics* **112** (2015) 56–67.

# The future of silicon (3)

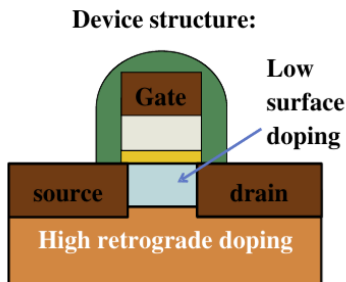
**Table 1**
Parameters for future logic CMOS LSIs predicted by ITRS 2013 for high-performance devices. Commercial name is the technology name used for semiconductor companies. $L_g$ is physical gate length. $V_{dd}$ is the supply voltage. Values for the ITRS 2007 are shown in parenthesis.

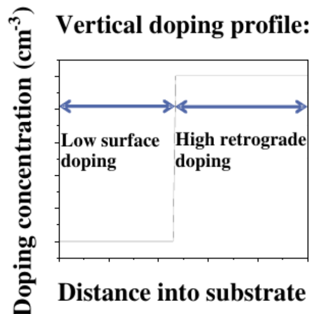
| Year | 2013 | 2015 | 2017 | 2019 | 2021 | 2023 | 2025 | 2027 |
|---|---|---|---|---|---|---|---|---|
| Commercial name (nm) | 14 | 10 | 7 | 5 | 3.5 | 2.5 | 1.8 | 1.3 |
| Metal half pitch (nm) | 40 | 32 | 25.3 | 20 | 15.9 | 12.6 | 10 | 8 |
| $L_g$ (nm) | 20.2 | 16.8 | 14.0 | 11.7 | 9.7 | 8.1 | 6.7 | 5.6 |
| ($L_g$ for ITRS 2007) | (13) | (10) | (8) | (6) | (5) | (4.5 in 2022) | | |
| $L_g$ for low stand by power (nm) | 23 | 19 | 16 | 13.3 | 11.1 | 9.3 | 7.7 | 6.4 |
| $V_{dd}$ (V) | 0.86 | 0.83 | 0.80 | 0.77 | 0.74 | 0.71 | 0.68 | 0.65 |
| ($V_{dd}$ (V) for ITRS 2007) | (0.90) | (0.80) | (0.70) | (0.70) | (0.65) | (0.65 in 2022) | | |

Hiroshi Iwai, "Future of nano CMOS technology", *Solid-State Electronics* **112** (2015) 56–67.

# Variability

Small size devices are more prone to random variability of parameters
Mitigation: "retrograde" doping profile

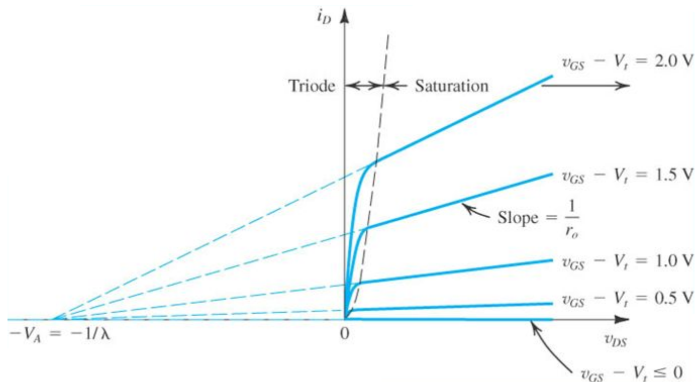



Low doping at the surface: $N_A = 10^{22}$ m$^{-3}$, $d \approx 10$ nm
High retrograde doping: $N_A = 5 \cdot 10^{25}$ m$^{-3}$
(compare with $N_{\mathrm{Si}} = 5 \cdot 10^{28}$ m$^{-3}$)
J. Woo, P.Y. Chien, F. Yang, S.C. Song, C. Chidambaram, J. Wang, G. Yeap, "Improved device variability in scaled MOSFETs with deeply retrograde channel profile", *Microelectronics Reliability* **54** (2014) 1090–1095.

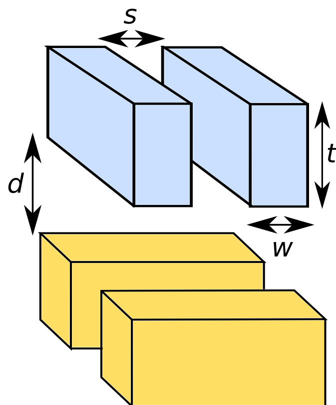
# Short channel effects

Channel length modulation becomes a severe limit for analog transistors




- Avoid minimum size transistors in analog blocks (analog design requires LARGE area)
- Use digital techniques, whenever possible

# Interconnection capacitances




- $s < d$
- $t \approx 2 \cdot w$

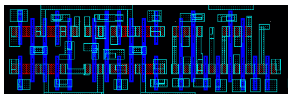
Frequency performance and power consumption are affected by the capacitance of interconnections

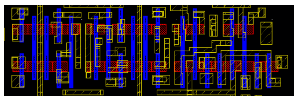
Lateral capacitance is dominant

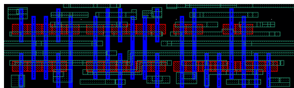
Maximum operation frequency and dynamic power consumption in digital circuits can be optained ONLY after parasitic extraction from layout!

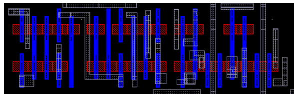
# Metals (10 layers)

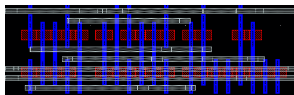
M1: local; M2-6: thin; M7-8: medium; M9-10: large (VDD and VSS)

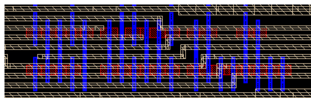
M1


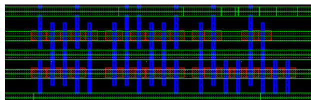
M2


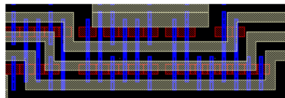
M3


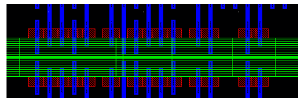
M4


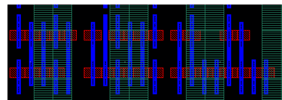
M5


M6


M7


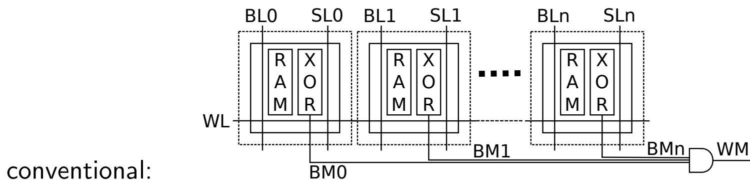
M8


M9


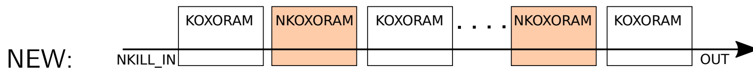
M10


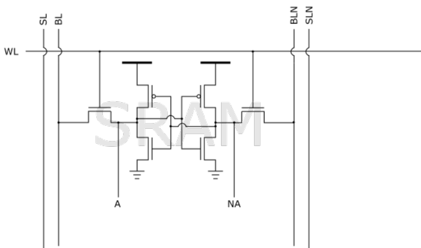
# Example: Associative memory for TrackTrigger

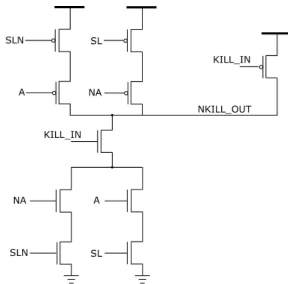
conventional:



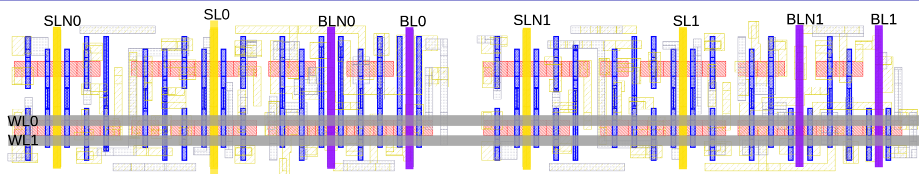

NEW:



# KOXORAM cell




M2 SL and SLN, M4 BL and BLN, M5 WLs

## Design goals:

- Reduce as much as possible the capacitance on SLs without increasing the cell area
- Reduce the switching activity of the transistors during comparison

## Results

- The capacitance associated to the search lines is 0.27 fF for two cells (0.20 fF due to gate capacitances, and 0.07 fF due to metal-metal capacitances)
- The average energy per comparison is 0.3 fJ/bit

# THANK YOU !