OMEGA ReadOut ASICs for High Granularity Calorimeters

CepC Workshop, Univ Roma III, Italy

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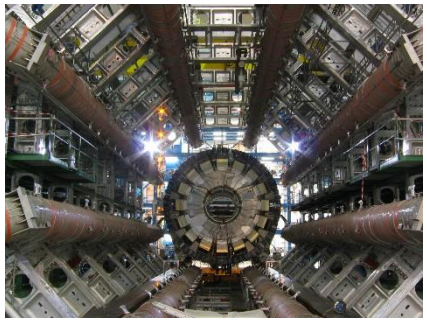
Ecole Polytechnique CNRS/IN2P3 , Palaiseau (France)

Organization for Micro-Electronics desiGn and Applications

Omega microelectronics lab

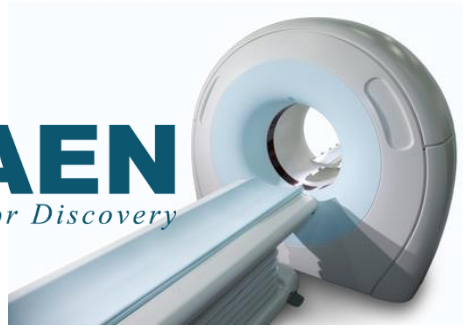
- Mutualized ASIC design team created in 2006, UMS in 2013
- 11 research engineers (3 IR0, 1 IR1, 5 IR2, 1 IE2, 2 AI)
- Importance of critical mass for more and more complex circuits
- Cross-fertilization between projects
- Projets selection by IN2P3 management
- Technology transfer via startup WEEROC



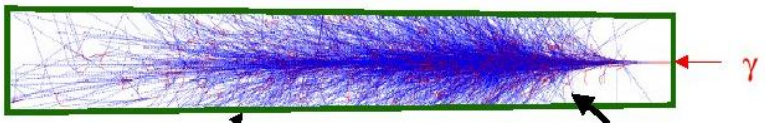
Research, Institute

Education, School

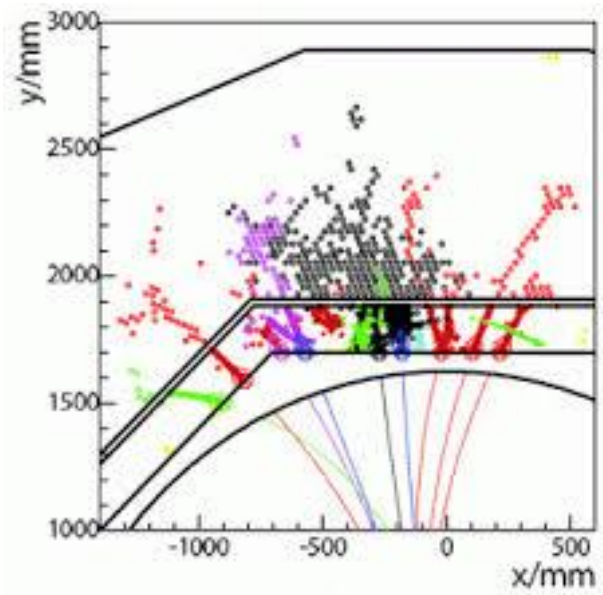
Industry, company

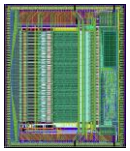


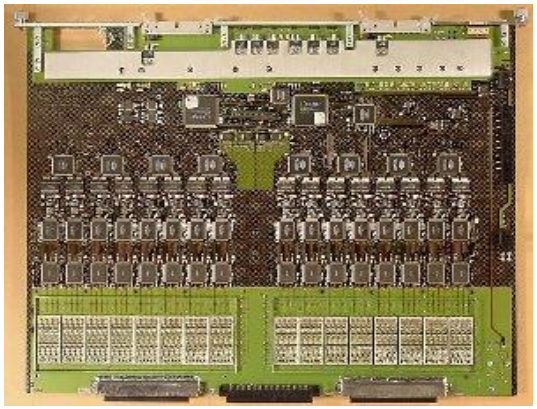
Evolution of calorimetry

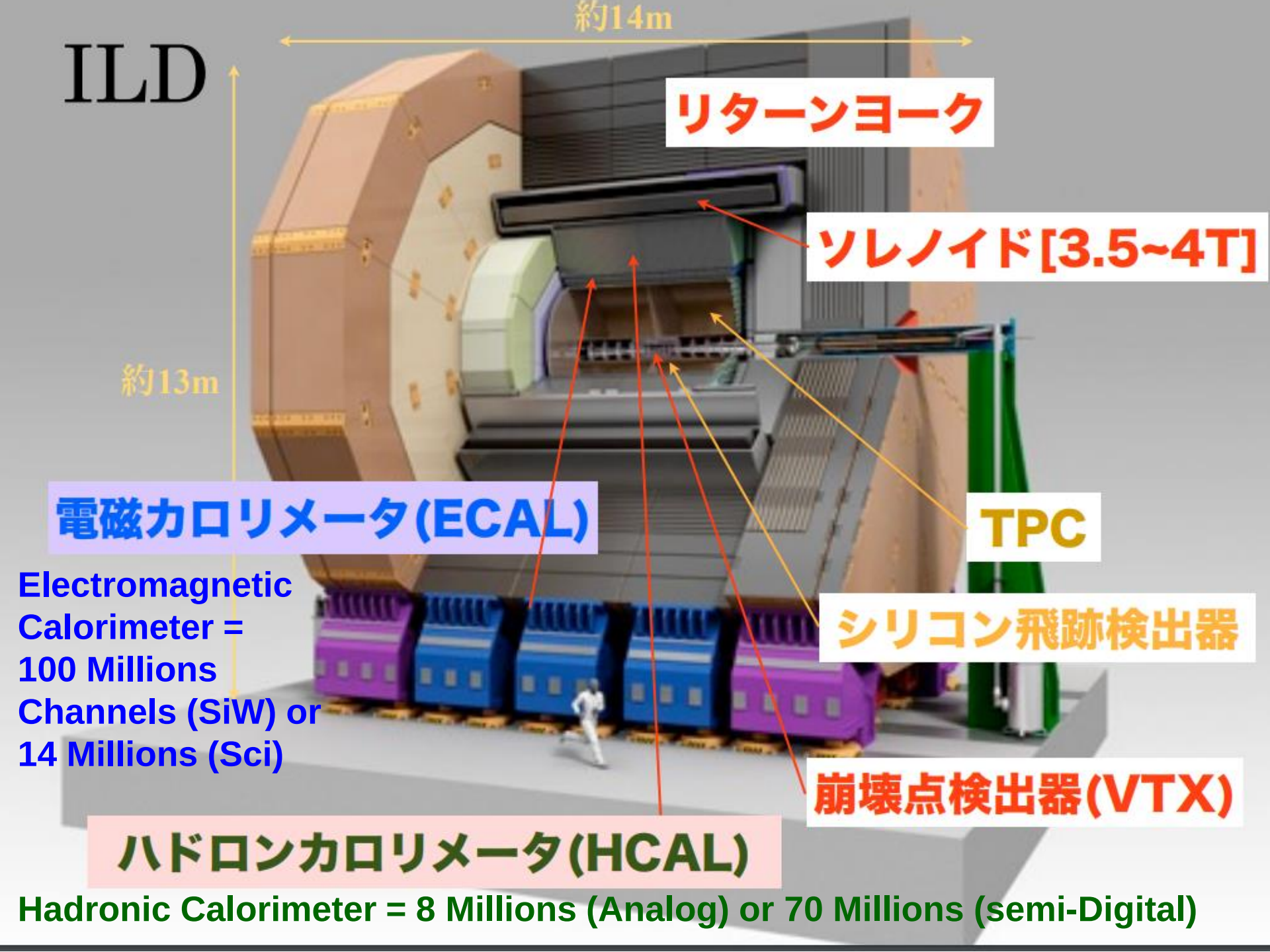


- 3D calorimetry : eta, phi, Energy
- 4D calorimetry : x,y,z,E
- 5D calorimetry : x,y,z,E,t
  - High granularity=> Millions of channels = > Low power !
    - Power pulsing ~1% for ILC
    - Low power + C02 cooling for HL-LHC
  - Energy measurement : Large dynamic range
    - MIP sensitivity => low noise (~0.1 fC)
    - Up to thousands of MIPs (~10 pC)
  - Timing information
    - Nice addition for ILC for PID : few ns is enough
    - Crucial for HL-LHC : pileup mitigation, need few tens of ps
  - Embedded electronics vs data out
    - Daisy chain and low power busses for ILC
    - High speed e/optical links for HL-LHC
  - Radiation levels
    - Negligible at ILC
    - Daunting at HL-LHC : >100 Mrad 1^{E}16N



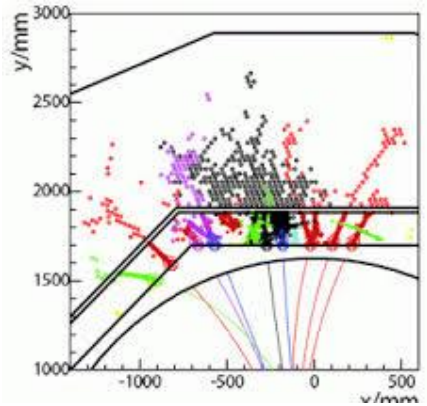




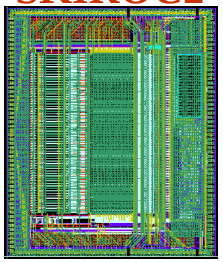

ILD
約14m
約13m
リターンヨーク
ソレノイド[3.5~4T]
電磁カロリメータ(ECAL)
Electromagnetic Calorimeter = 100 Millions Channels (SiW) or 14 Millions (Sci)
TPC
シリコン飛跡検出器
崩壊点検出器(VTX)
ハドロンカロリメータ(HCAL)
Hadronic Calorimeter = 8 Millions (Analog) or 70 Millions (semi-Digital)

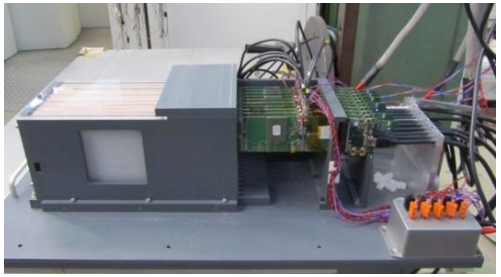
CALICE technological prototypes

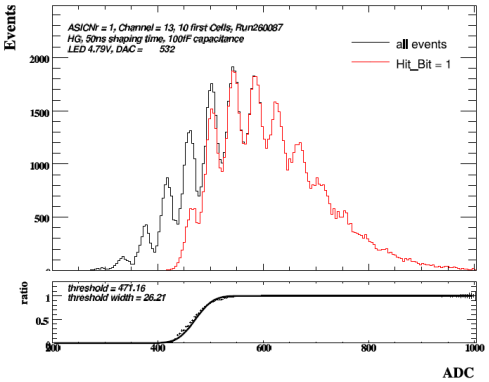
- R&D on imaging calorimetry
  - Particle Flow Algorithms
  - Electronics crucial (low noise, ultra low power, fully integrated, large dynamic range, zero suppress)
  - Several innovative features (power pulsing, SiPM…)
  - Validation of technological prototypes
  - Common R/O features
  - Worldwide collaboration



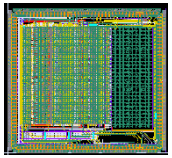
SKIROC2



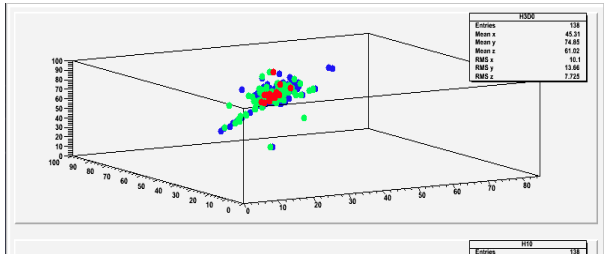




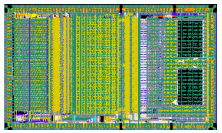
SPIROC2



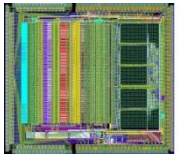
AIDA



HARDROC2

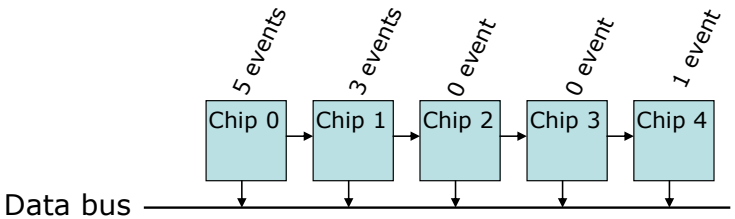


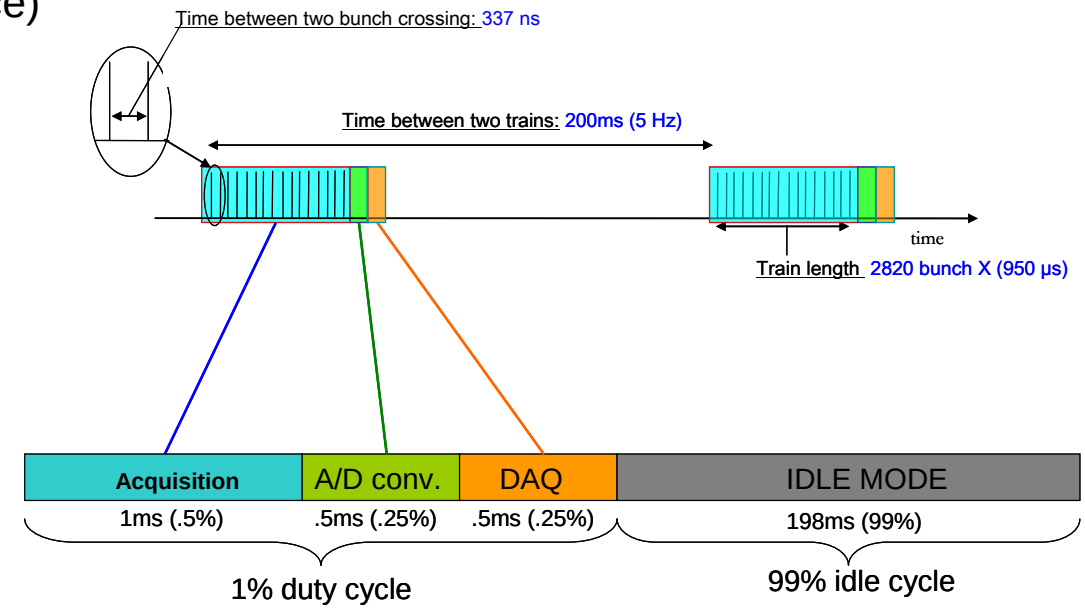
MICROROC

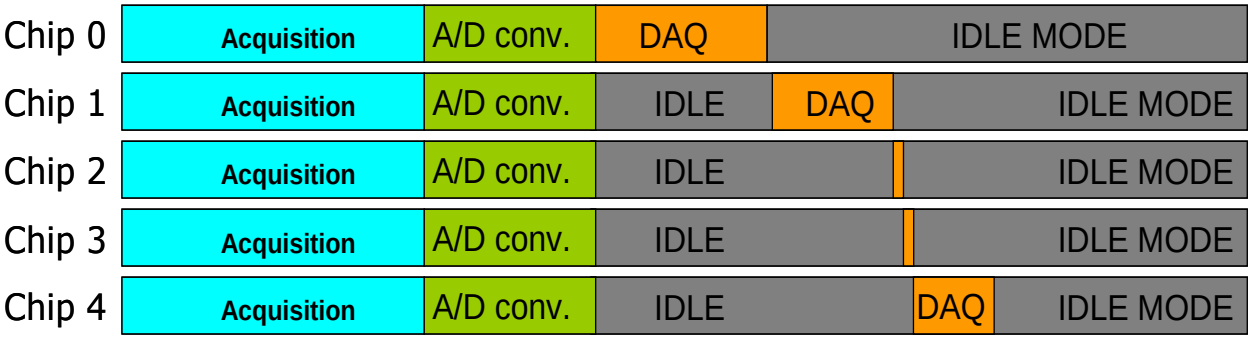


From 2nd generation…

- **2nd generation chips for ILD**
  - Auto-trigger, analog storage and/or digitization
  - Token-ring readout (one data line activated by each chip sequentially)
  - Common DAQ (common interface)
  - Power pulsing : <1 % duty cycle







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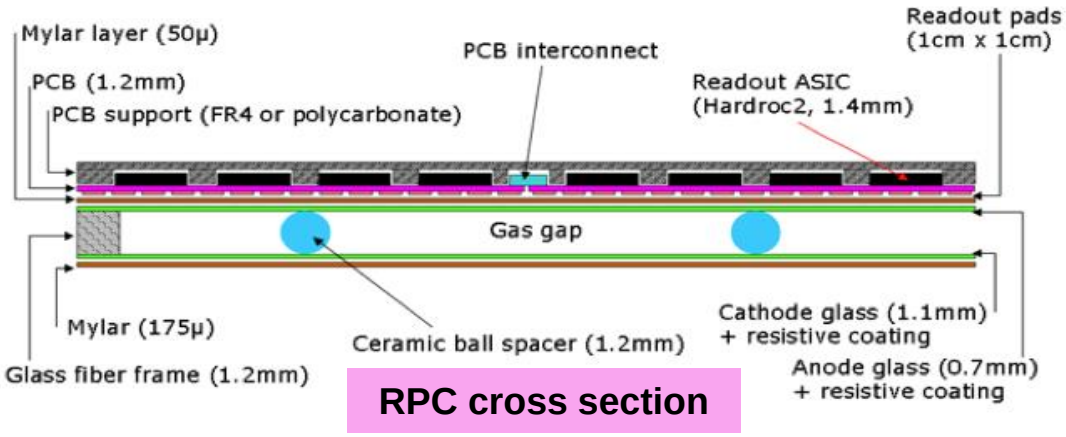
…To 3rd generation

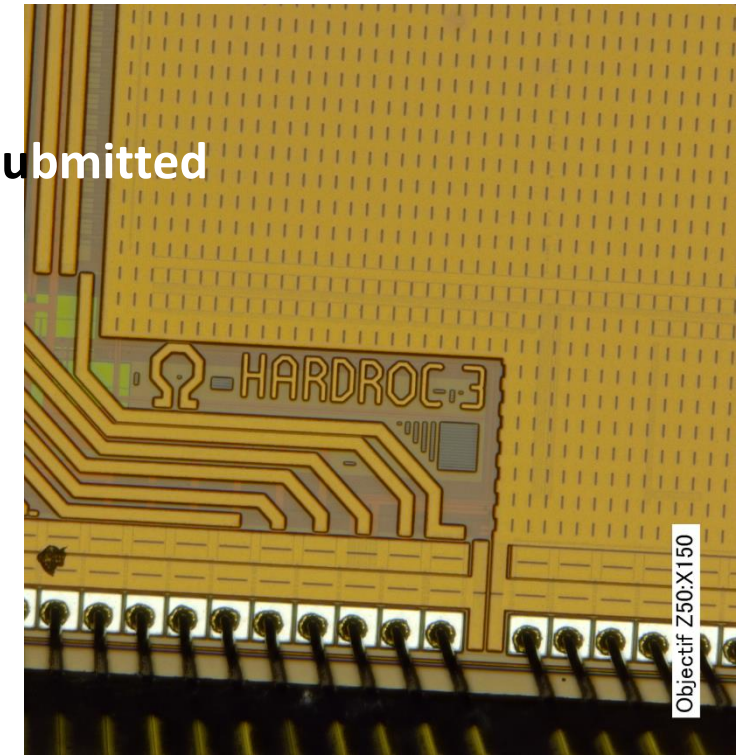
- **3rd generation chips for ILD**
  - **Independent channels (zero suppress)**
    - Huge change in digital part !!
    - Digital part power consumption and size (+30 to 50%)
  - **I2C link (@IPNL)** for Slow Control parameters and **triple voting**
    - configuration broadcasting
    - geographical addressing
  - **PLL** provides the Fast Clock (mainly used for digitization) from the Slow Clock
    - No Fast Clock to be provided to the ASICs !

- **HARDROC3: 1st of the 3rd generation chip to be submitted**

  But all ILC R&D stopped since 2016, waiting for ILC decision

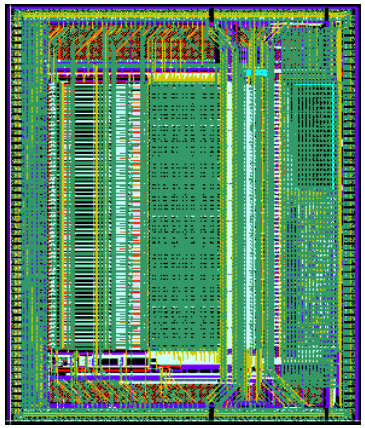


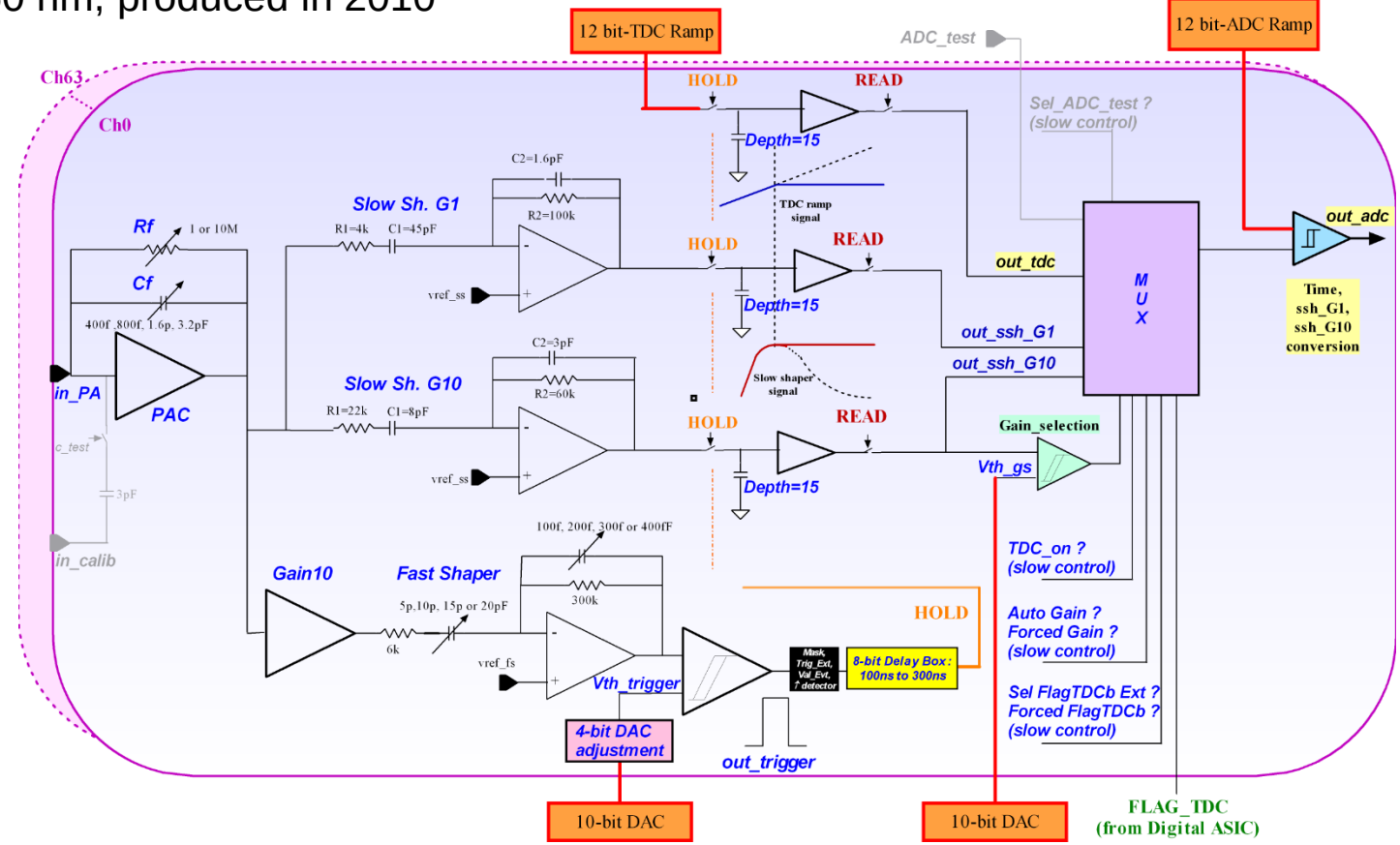
RPC cross section



SKIROC2 readout ASIC

- 64-channel Silicon Kalorimeter Integrated Read-Out Chip
  - Autotrigger @ ½ MIP = 2 fC
  - Charge measurement 15 bits in two gains
  - 16-deep Analog memory
  - Low power 25µW/Ch with power pulsing
  - Embedded readout
  - SiGe 350 nm, produced in 2010

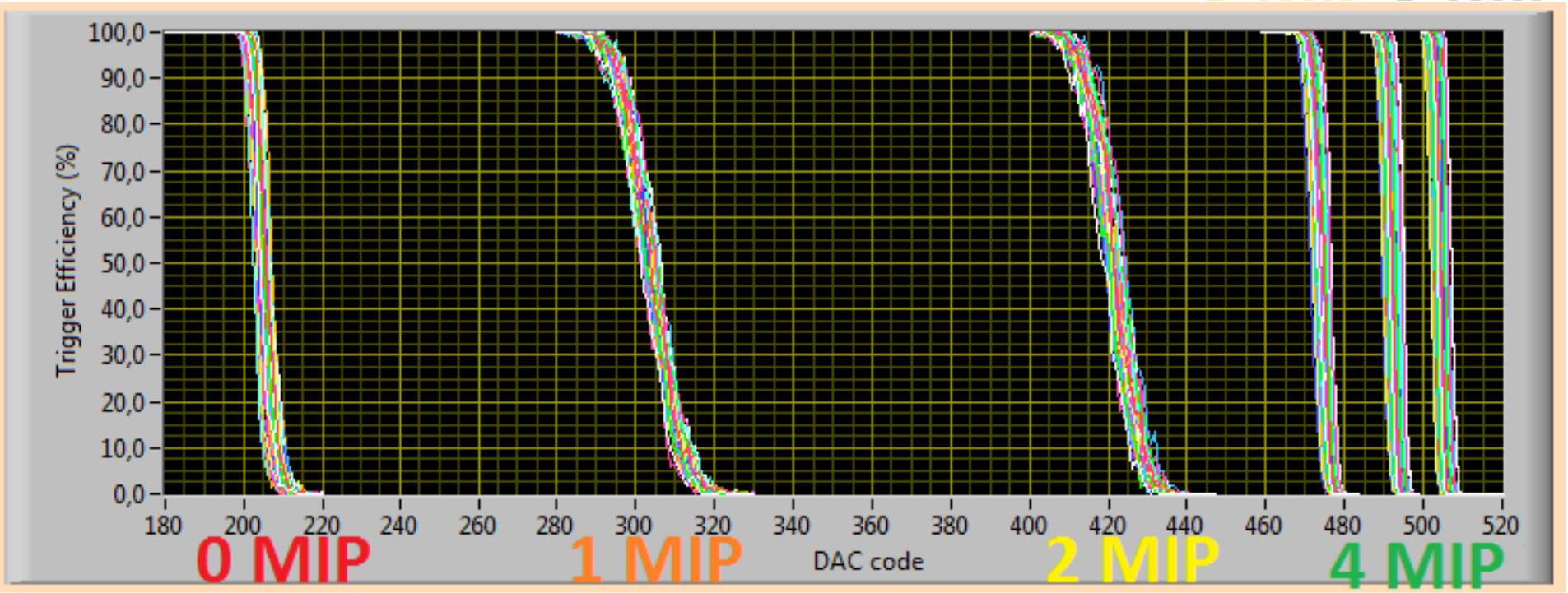




SKIROC2A : S-Curves (trigger efficiency)

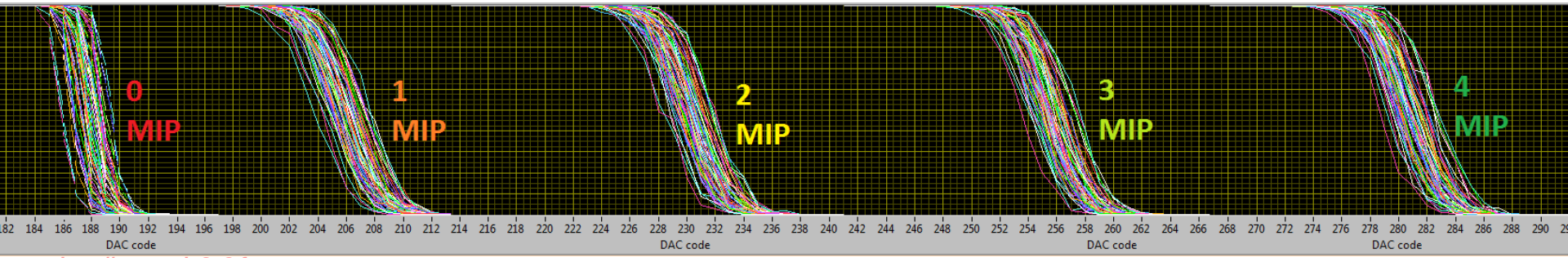
PA Gain = 1.2pF

3 MIP 5 MIP



S/N > 9

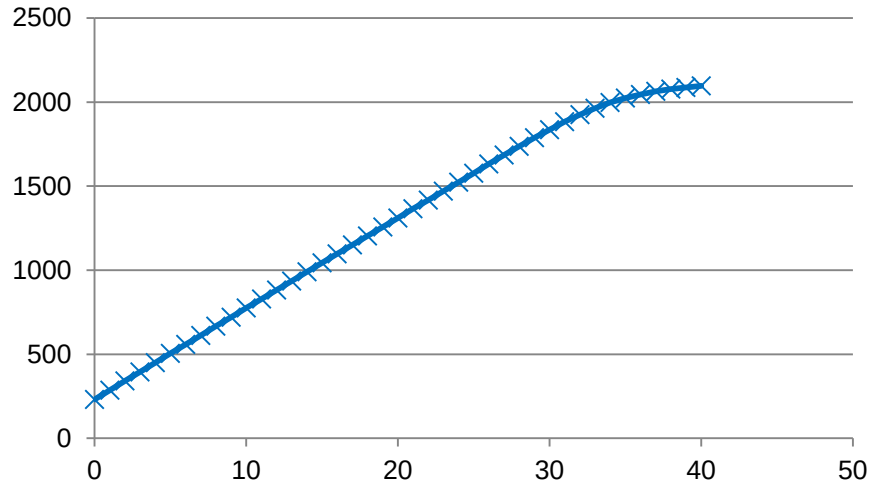
PA Gain = 6 pF



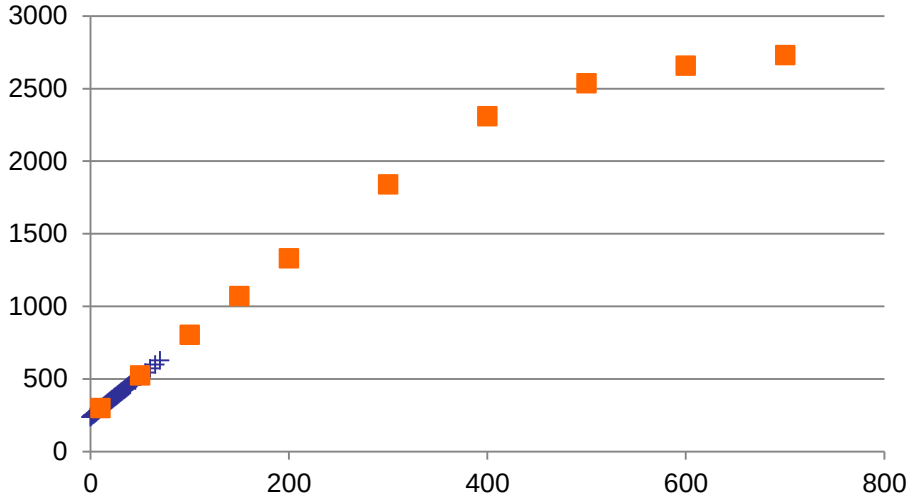
SKIROC2A Linearity

PA Gain @ 1.2pF

HG

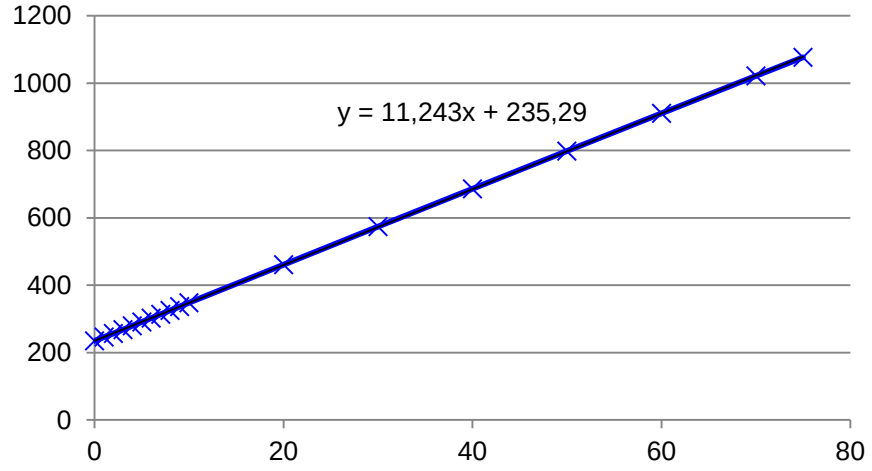


LG

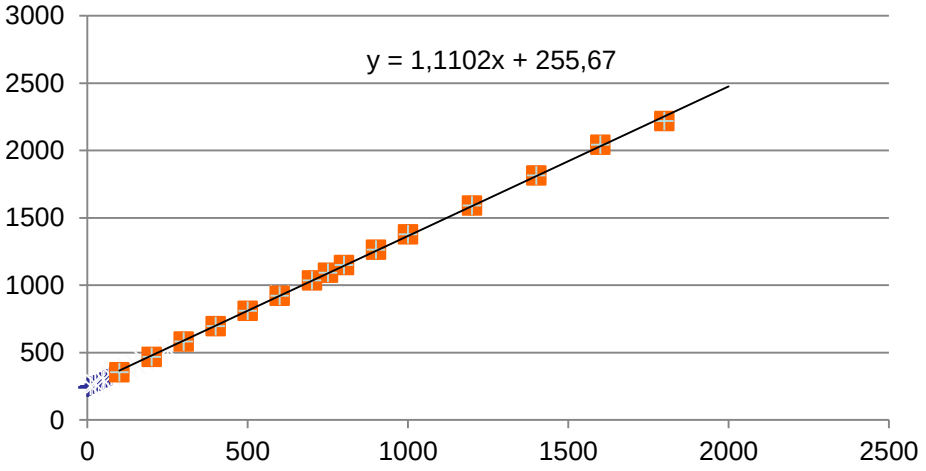


PA Gain @ 6pF (ILC request)

HG



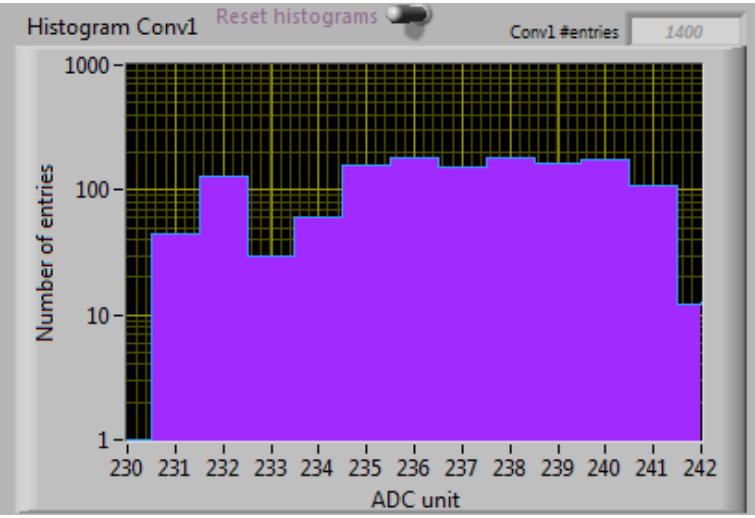
LG

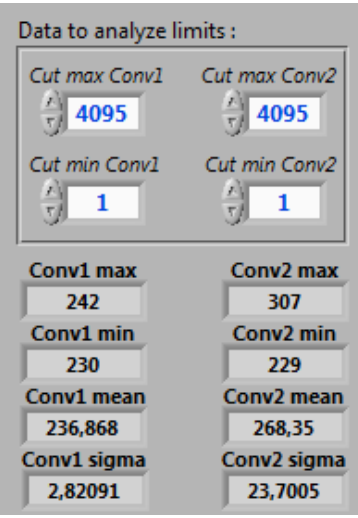


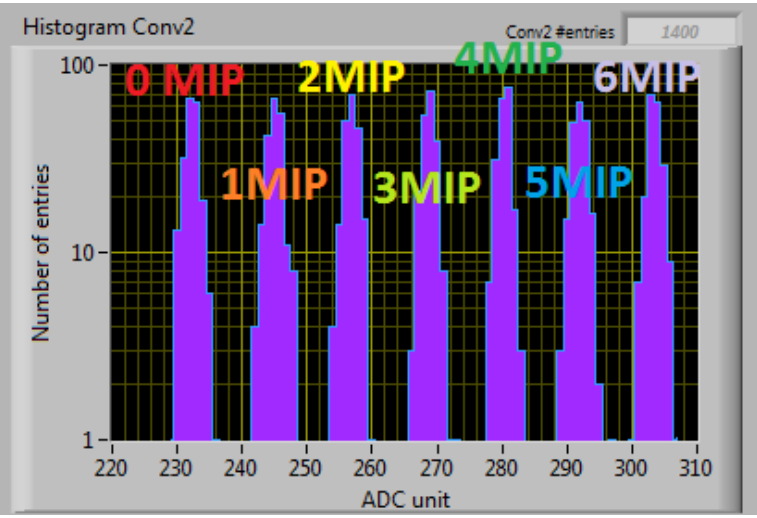
SKIROC2A : histogram

PA Gain @ 6pF

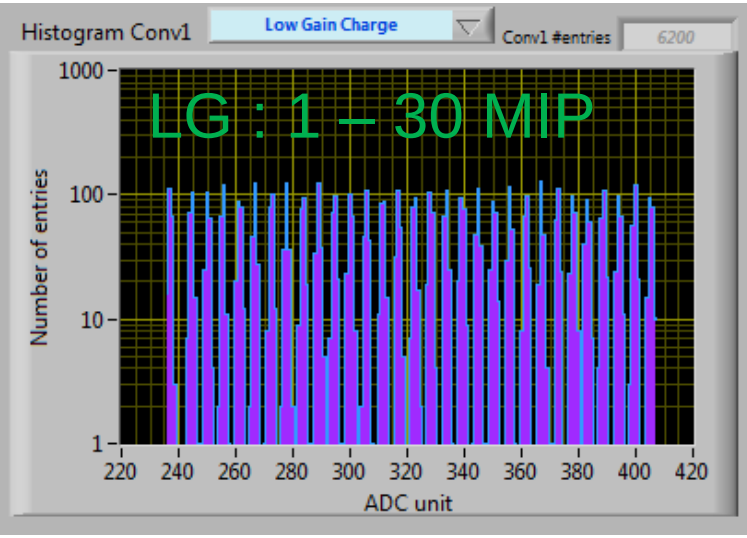
S/N > 10

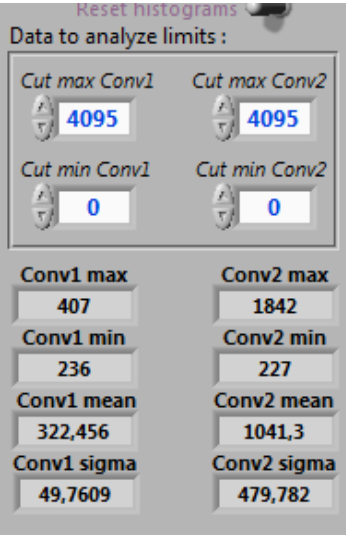


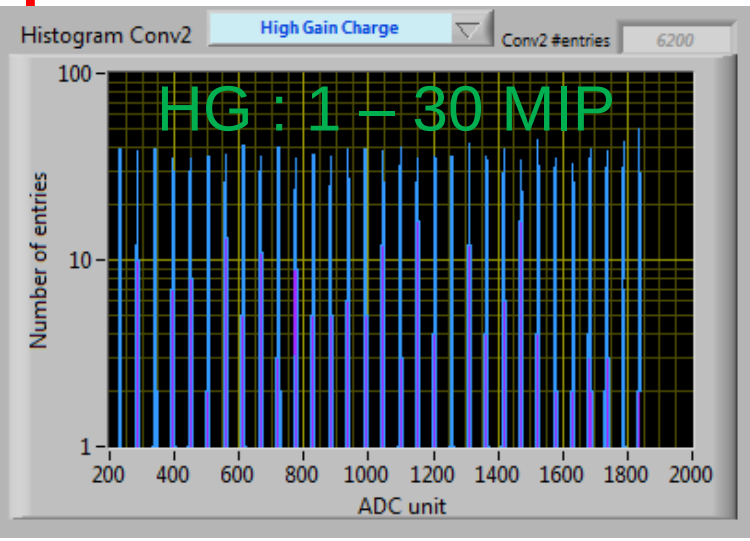




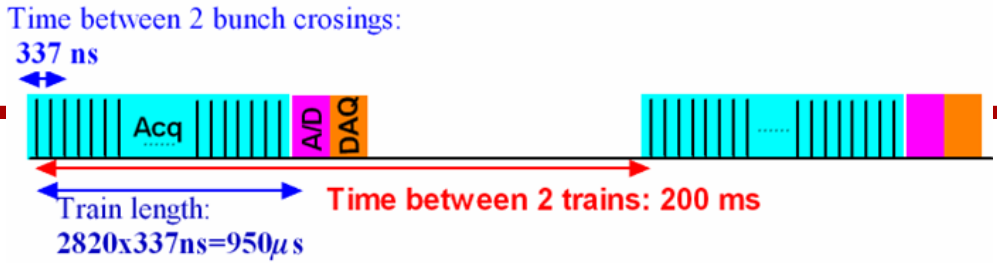
PA Gain @ 1.2pF



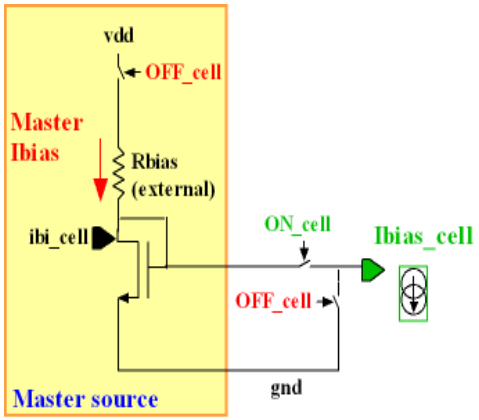




POWER PULSING in SK2



- **Requirement:**
  - **25 µW/ch with 0.5% duty cycle**
  - **500 µA for the entire chip**



- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**
- **SK2 power consumption measurement:**
  - 123 mA x 3.3V ≈ 40 mW => **0.6 mW/ch**

- **4 Power pulsing lines** : analog, conversion, dac, digital
- Each chip can be forced **on/off by slow control**

Measurements		
Acquisition	88 mA , 290 mW	Duty Cycle =0.5%, 1.45 mW
Conversion	27.3 mA, 90 mW	Duty Cycle =0.25%, 0.225 mW
Readout	8.0 mA, 26.4 mW	Duty Cycle =0.25%, 0.066 mW

Skiroc2 power consumption with Power pulsing: 1.7 mW ie 27 µW/ch

Si-W ECAL

- 25 mm² Si pads 300 µm thick
- 4 wafers per ASU 18x18 cm
- Readout 16 SKIROC2 chips 64ch
- Chip on board or BGA package
- Daisy-chain readout
- MIP/noise ~18

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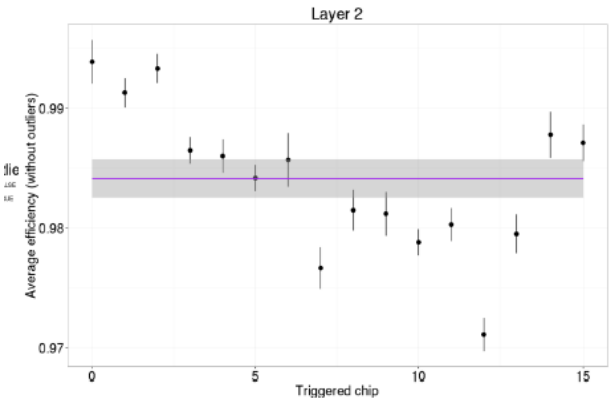
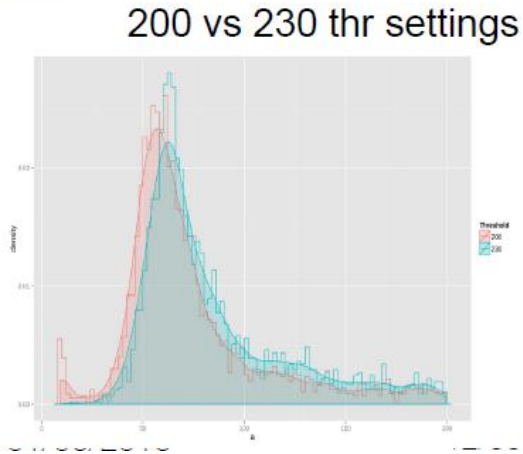
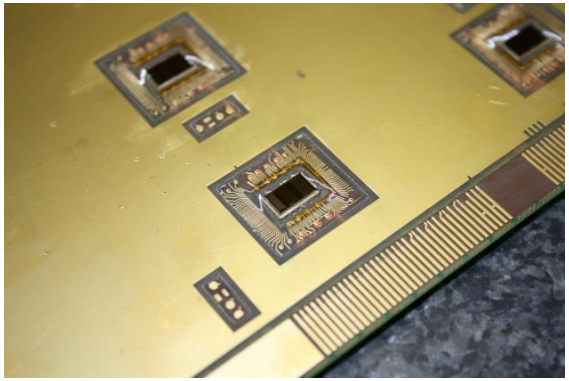
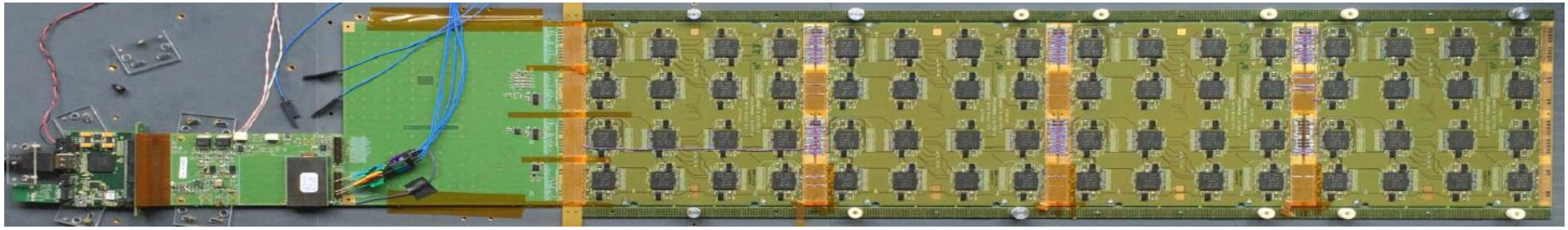
https://agenda.linearcollider.org/event/7014/contributions/34685/

$\langle\varepsilon\rangle_{CHIP} > 97\%$; $\langle\varepsilon\rangle_{LAYER} \geq 98.3\ \%$

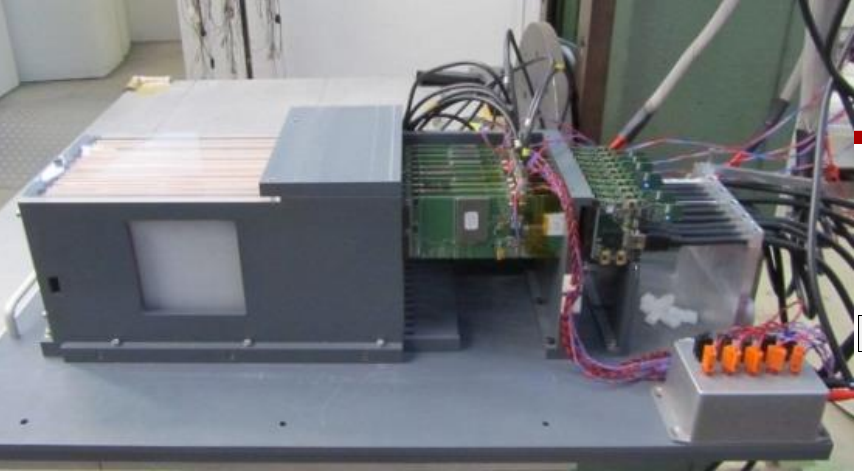




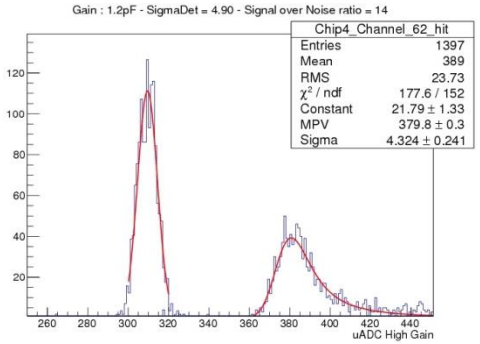




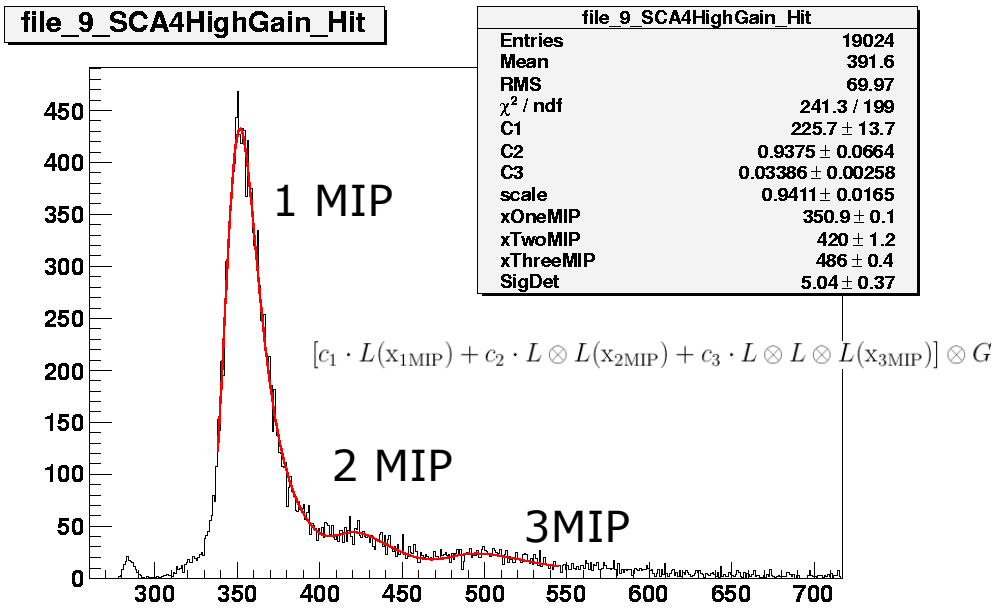
Skiroc2 in Test Beam

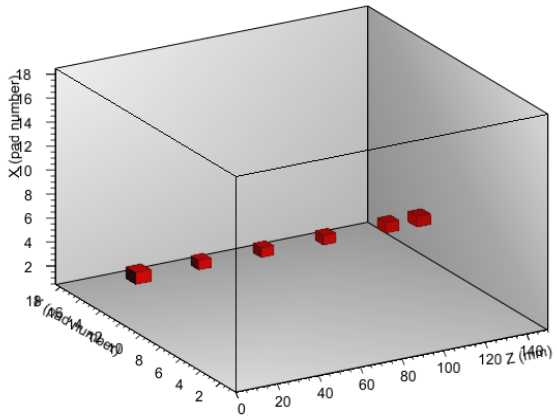


- Fit of the energy distribution (without W): expected result (physics studies)

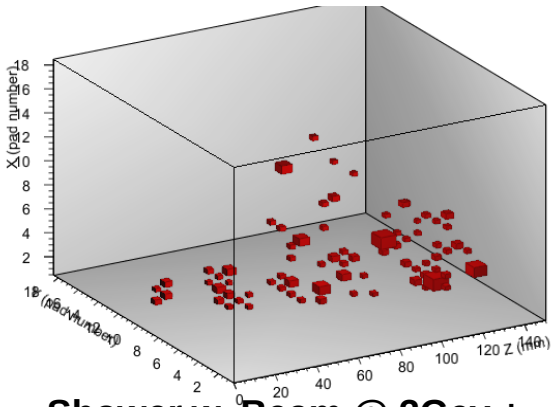


Pedestal 1 MIP

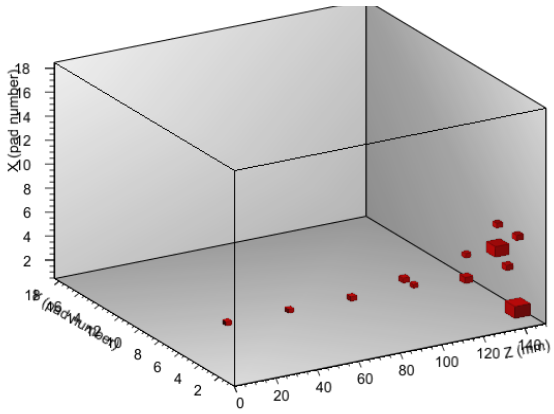




1 MIP (Beam without W)



Shower w. Beam @ 3Gev + 3x$_0$ W + W enclosed



Shower w. Beam @ 1Gev + W enclosed

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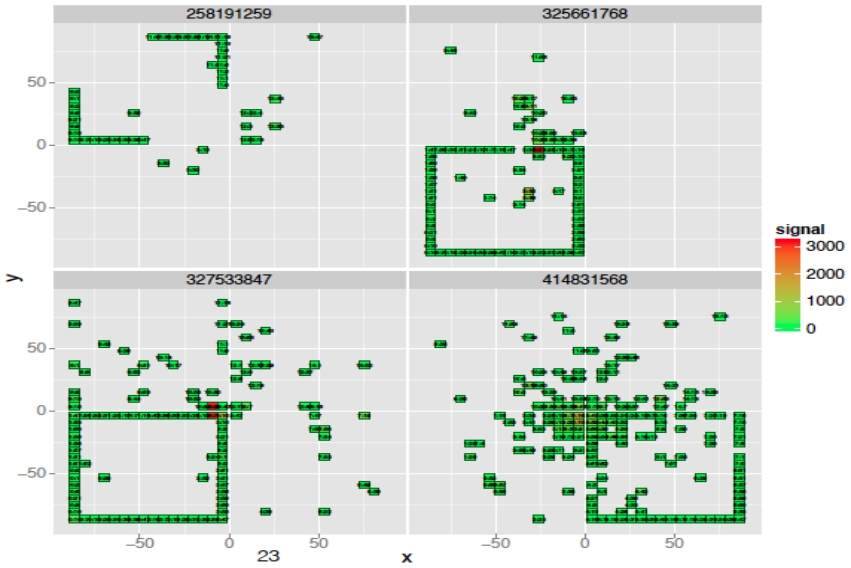
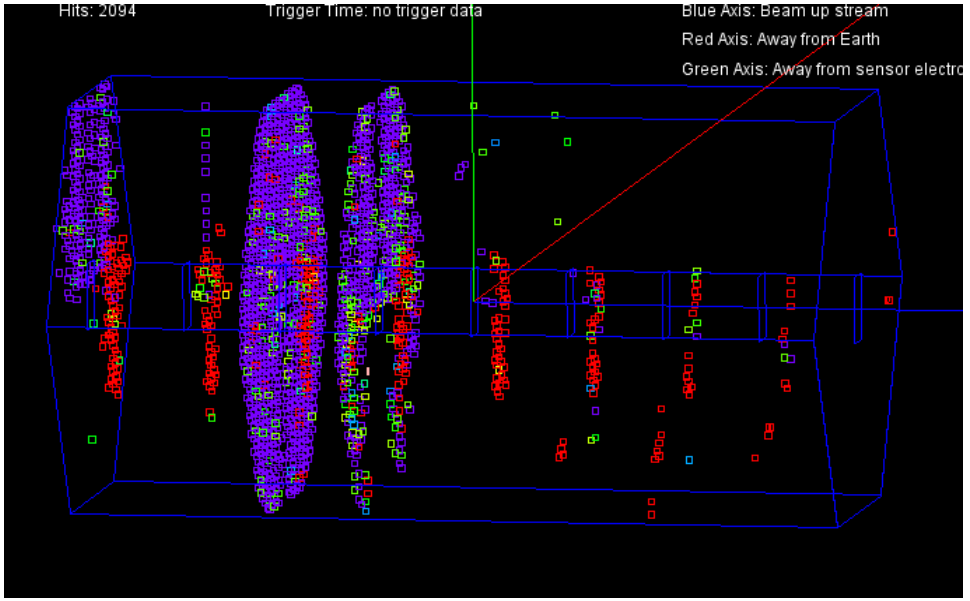
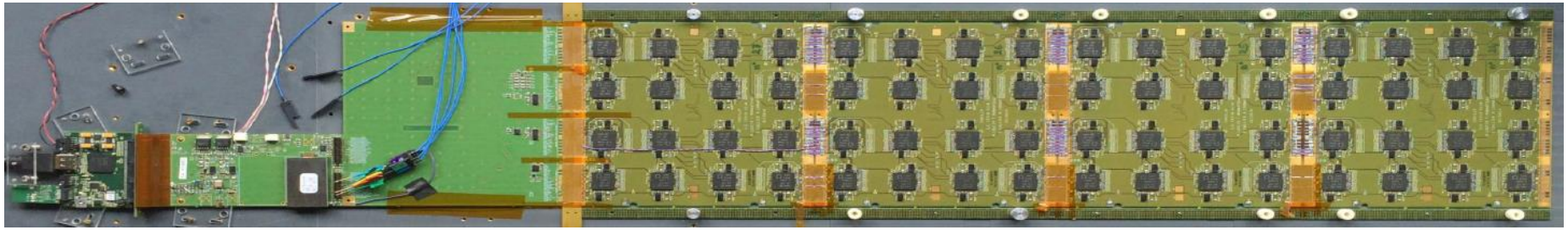
Issues (system issues)

- Noise, crosstalk, « square events » « monster events »
- Retriggering, digital noise
- Connectors and power supplies





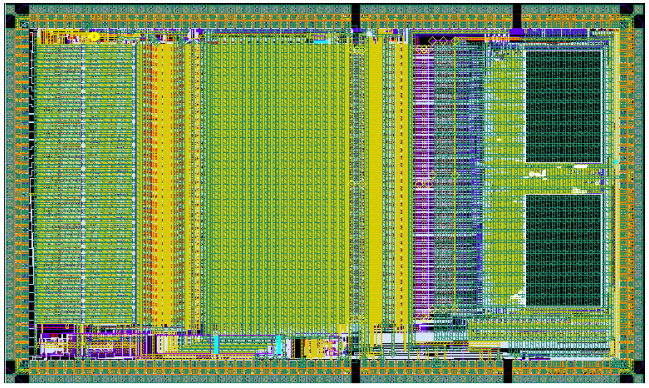


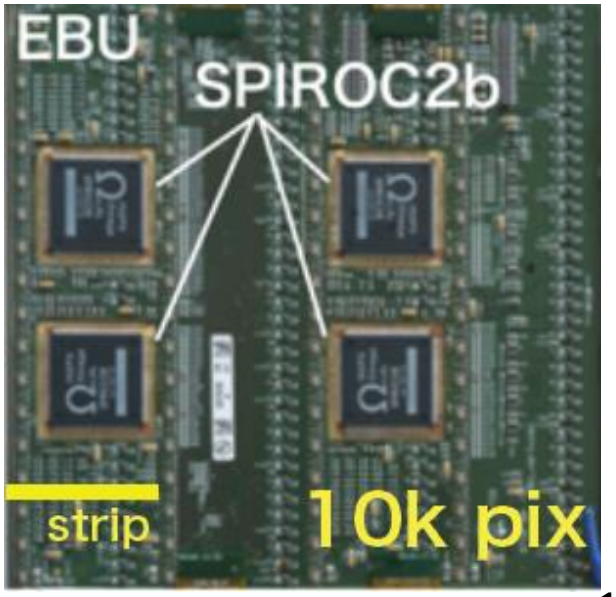
AHCAL/ScECAL : SiPM readout

- Scintillating tiles and SiPM
  - Pioneered by DESY (EUDET/AIDA)
  - Chip embedded in detector : low power !

(0.36m)² Tiles + SiPM + SPIROC (144ch)

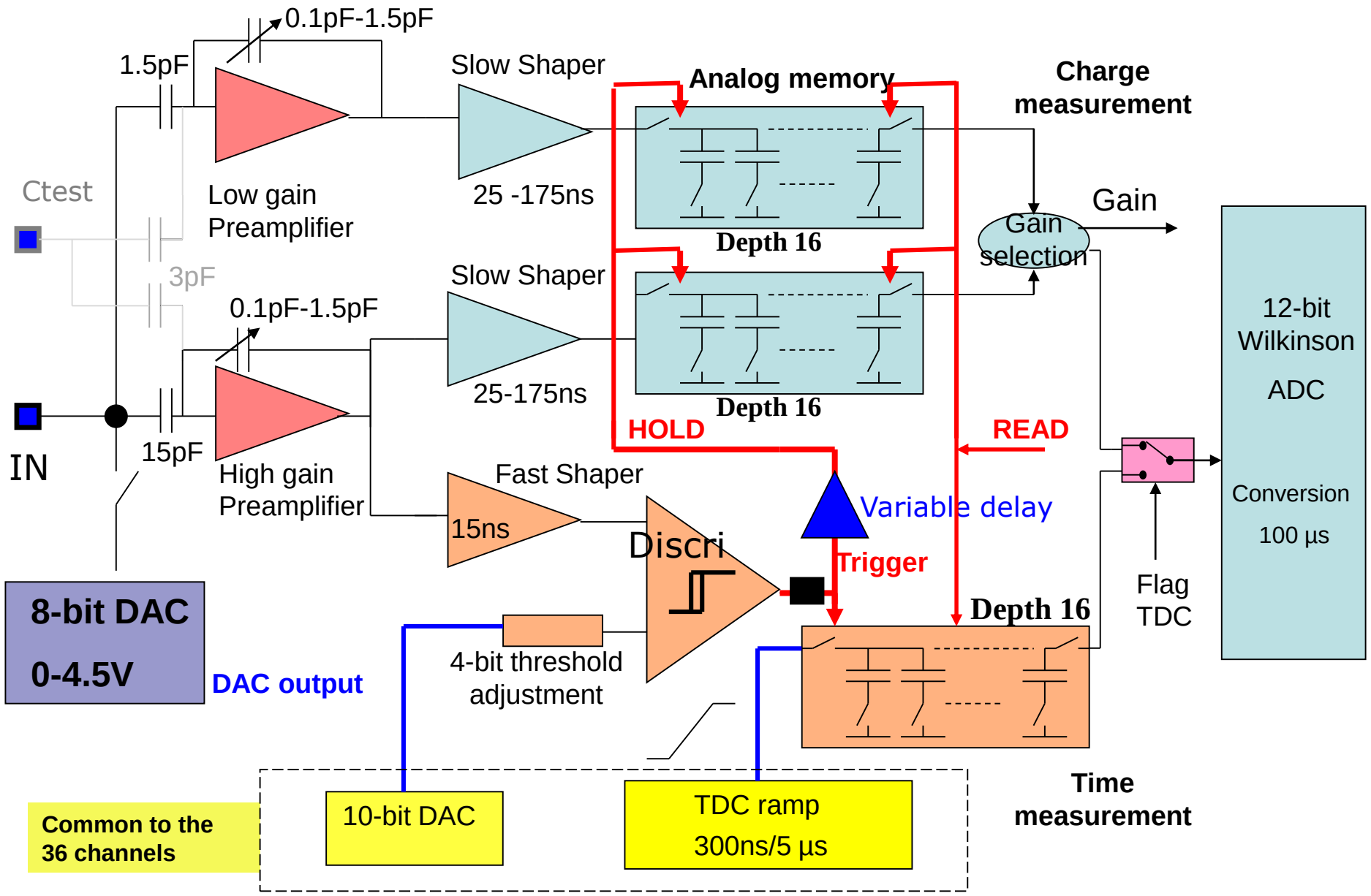
- SPIROC : Silicon Photomultiplier Integrated Readout Chip
  - Variant of skiroc
  - 36 channels autotrigger 15bit readout
  - Energy measurement : 15 bits in 2 gains
  - Autotrigger down to ½ p.e. (80 fC)
  - Time measurement to ~1 ns
  - Power dissipation : 25µW/ch (power pulsed)



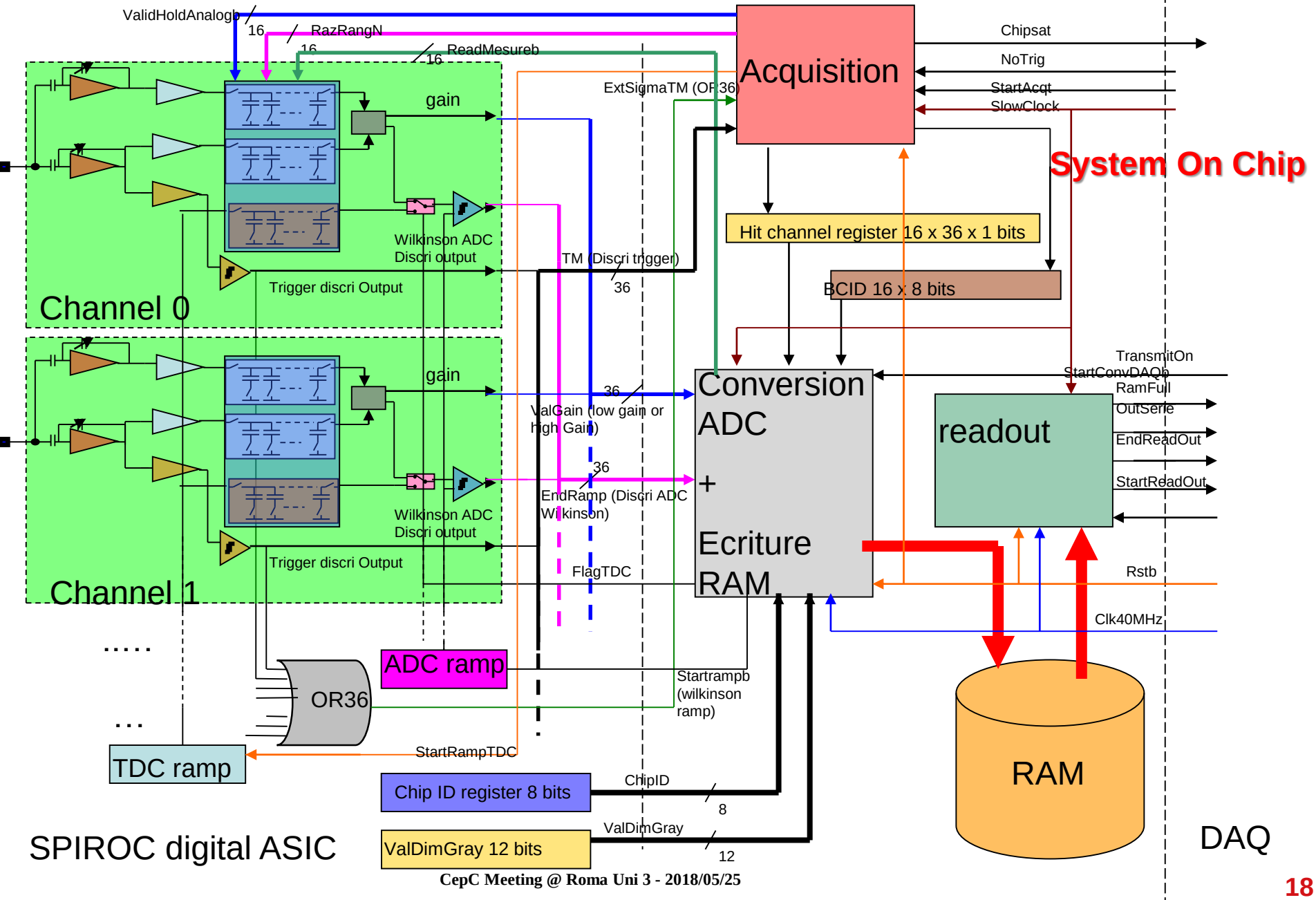


SHINSHU UNIVERSITY

SPIROC : One channel schematic

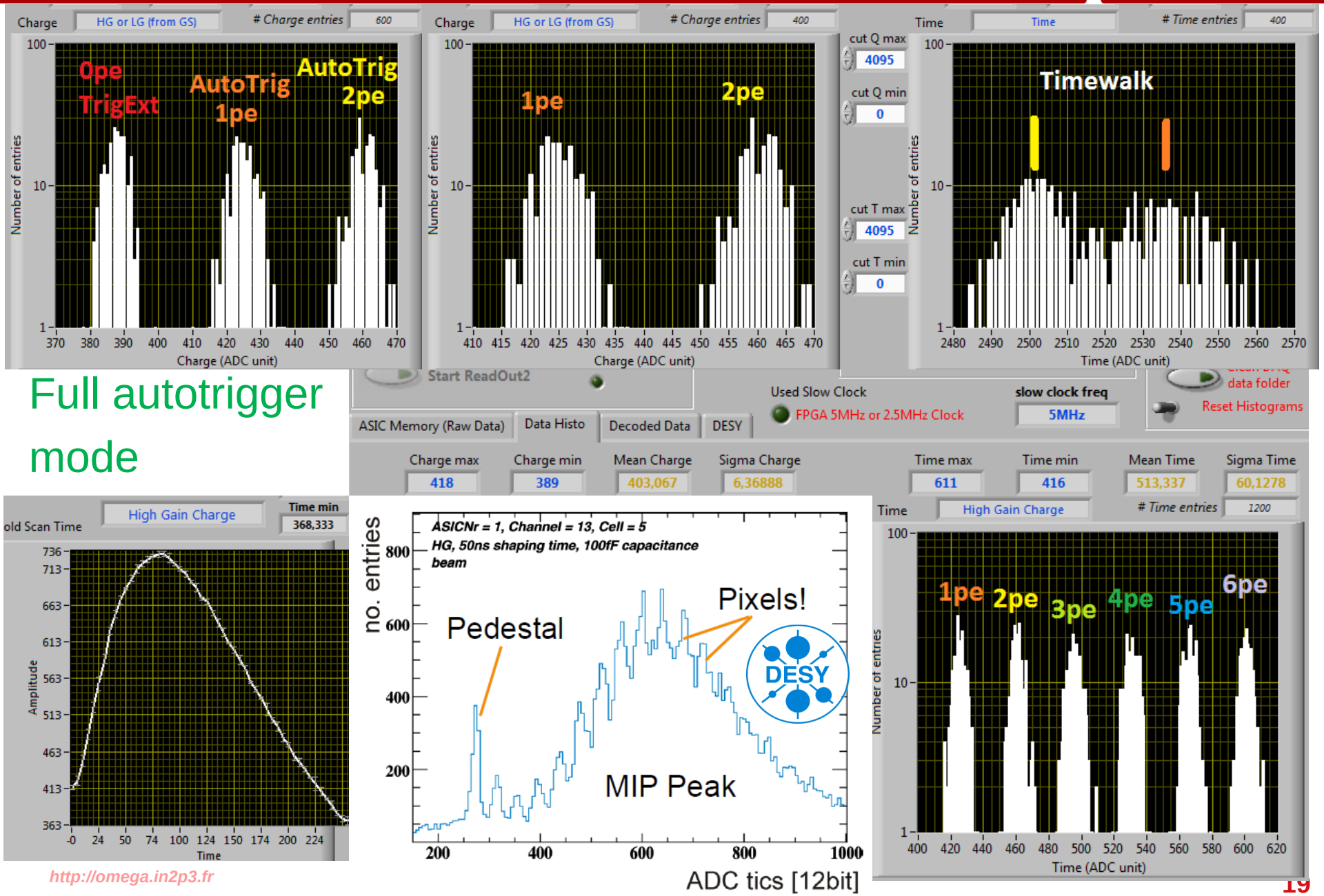


SPIROC : System On Chip

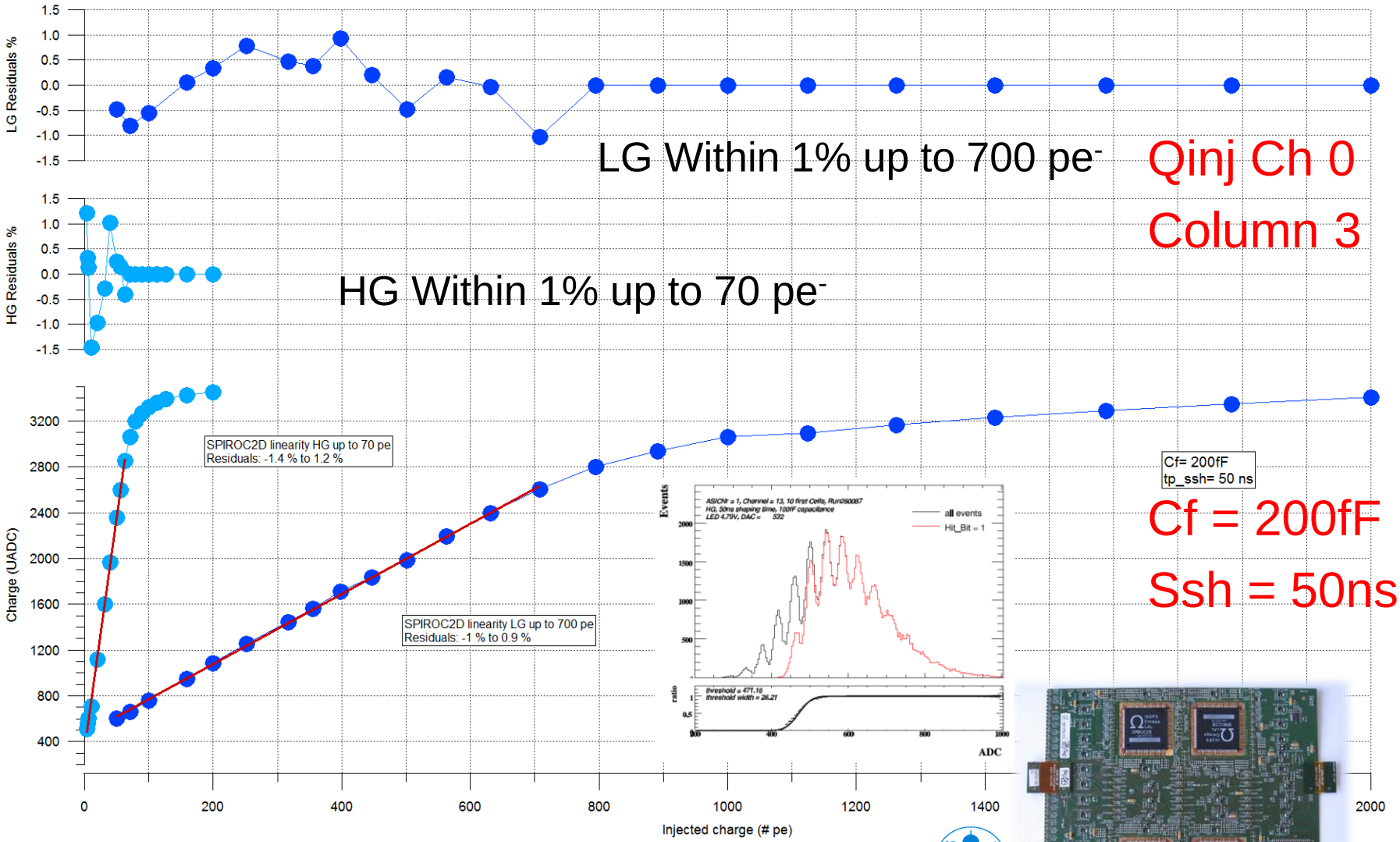


SPIROC2E : Auto-trigger

Full autotrigger mode

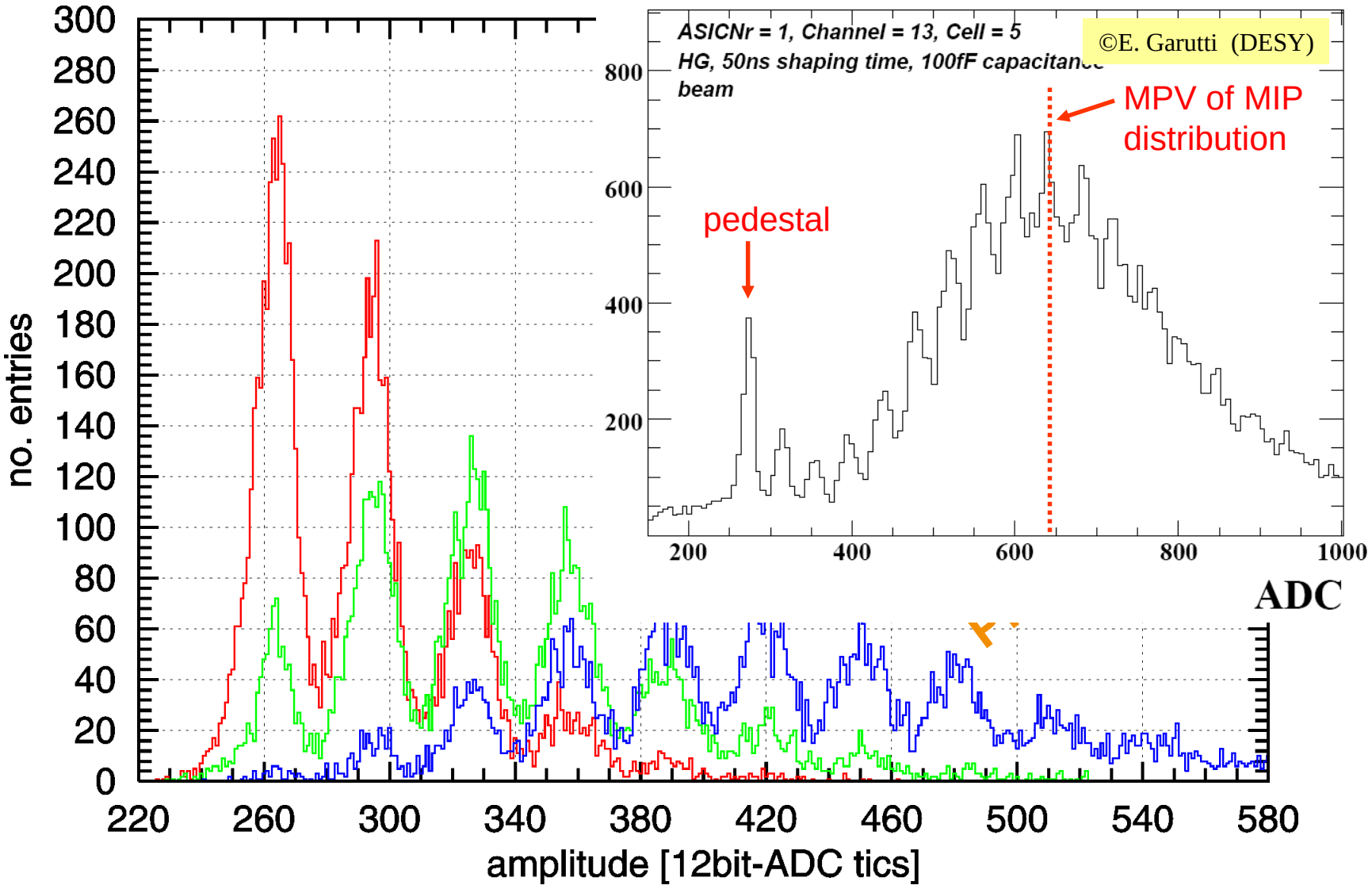


SPIROC2 : Linearity of Charge Measurement



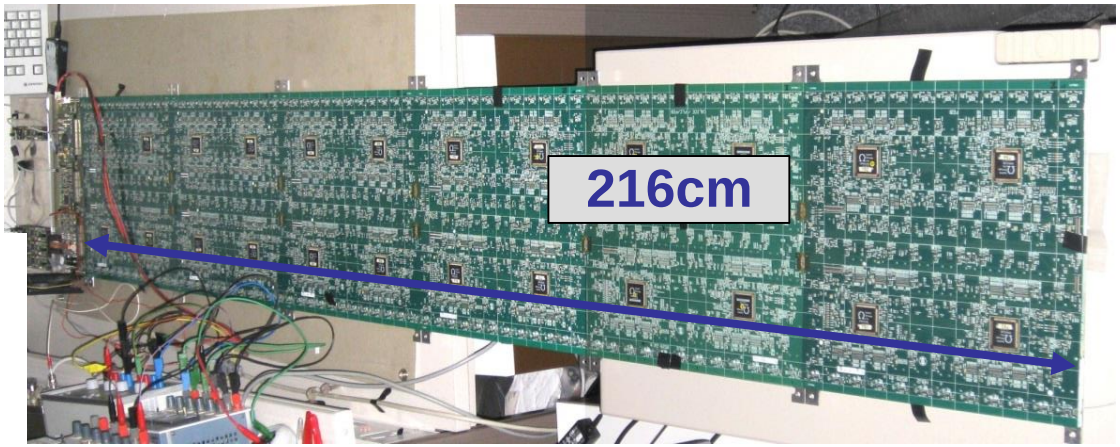
1 EBU : 18 cm x 18 cm
4 Spiroc2 , 144 SiPMs

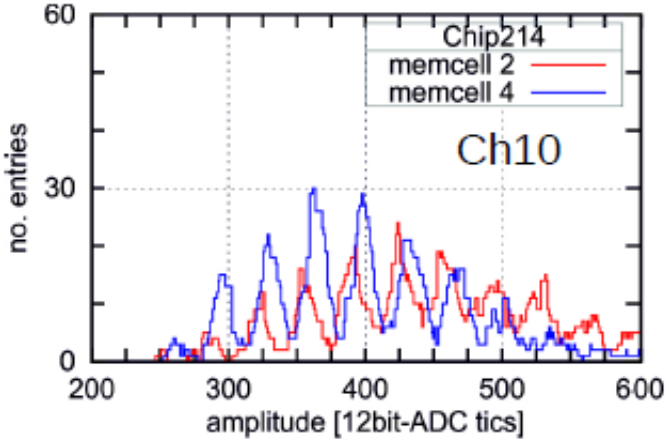
Single-Photon Peaks I

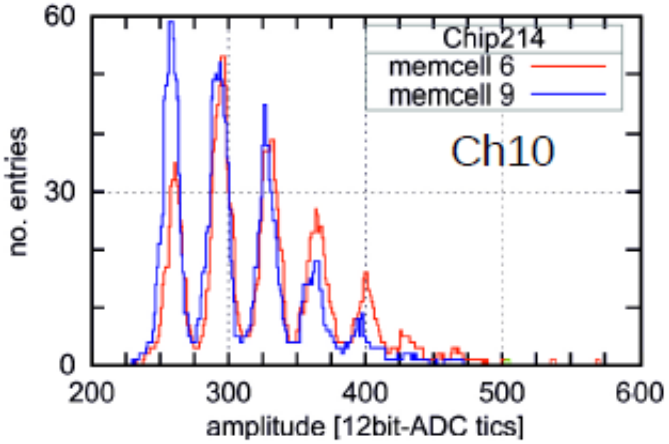


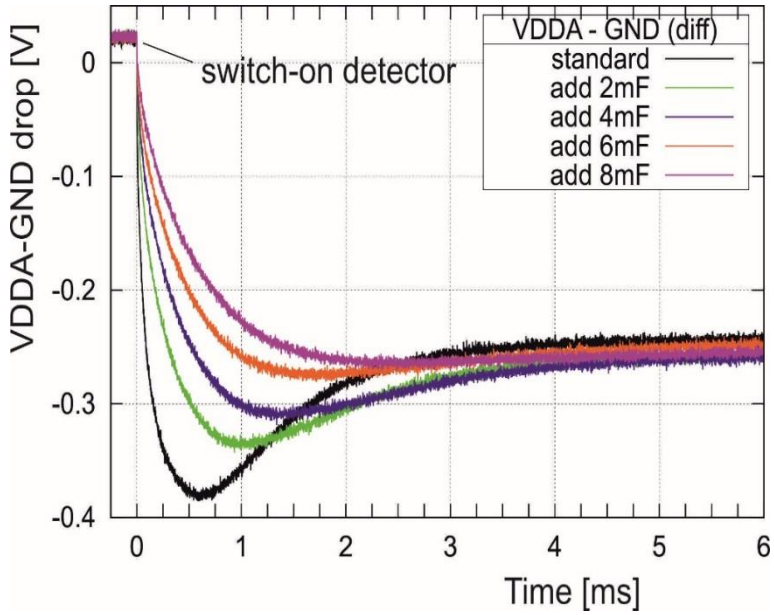
Power pulsing studies

- 2.5 A switched at 5 Hz
- 150 µs settling time

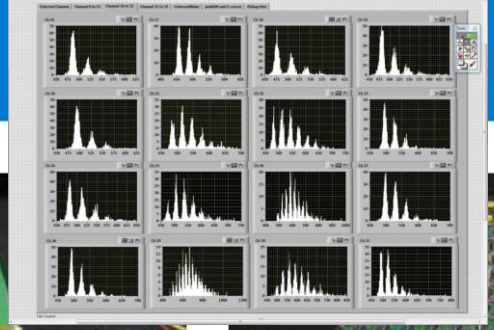


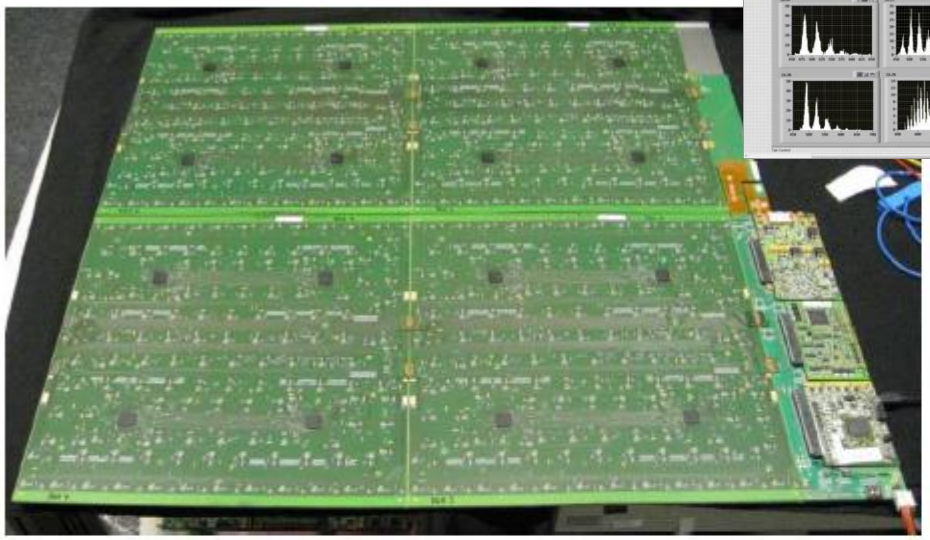


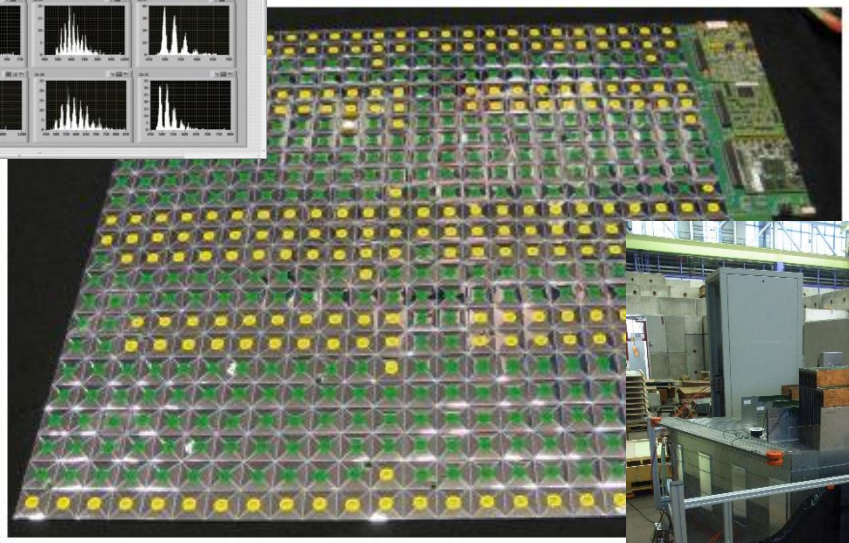


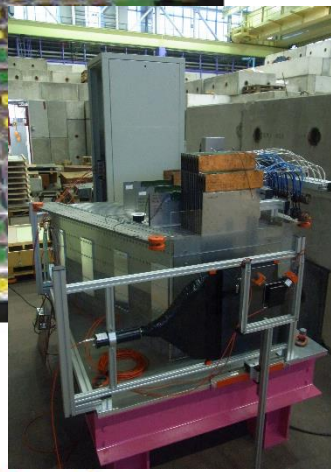


Testbeam Modules



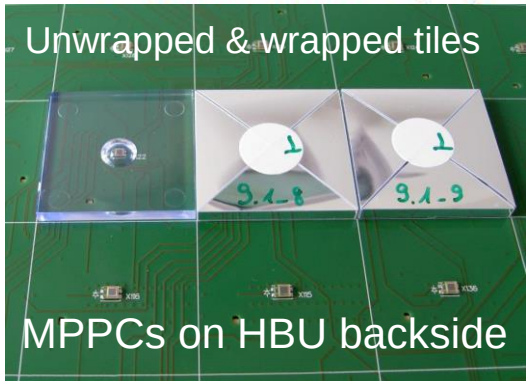


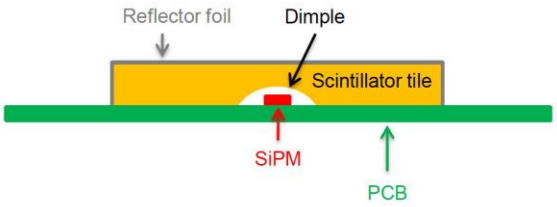


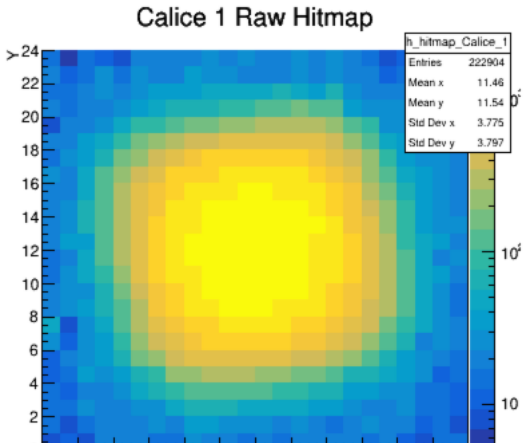


Front- and back side of an AHCAL testbeam detector module

- 24 of 39 detector modules completed. All modules expected end March.
- Detector modules are tested with LED (ET), cosmics and at DESY electron testbeam facility (16 modules already tested).

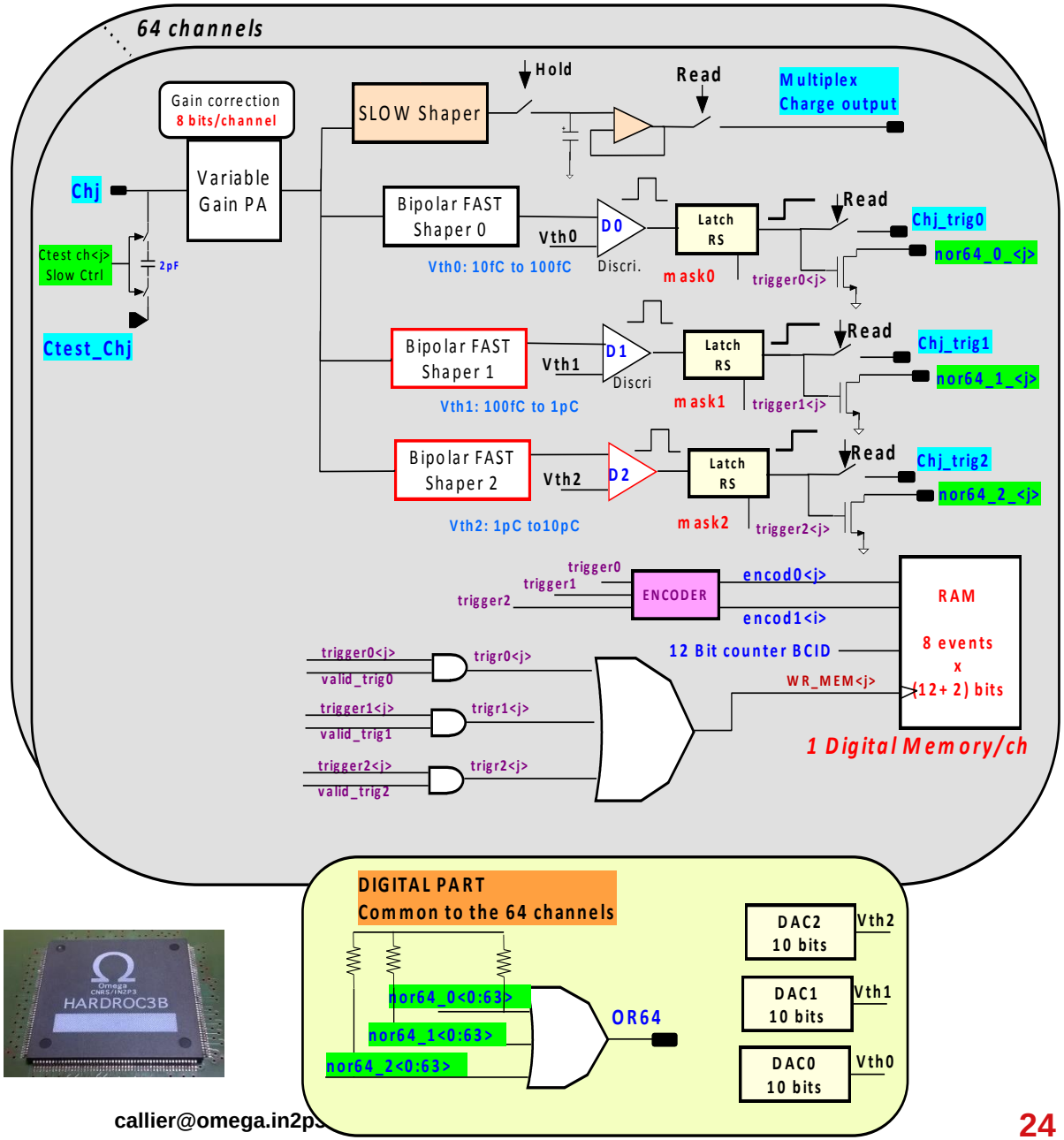






RPC sDHCAL : HARDROC3

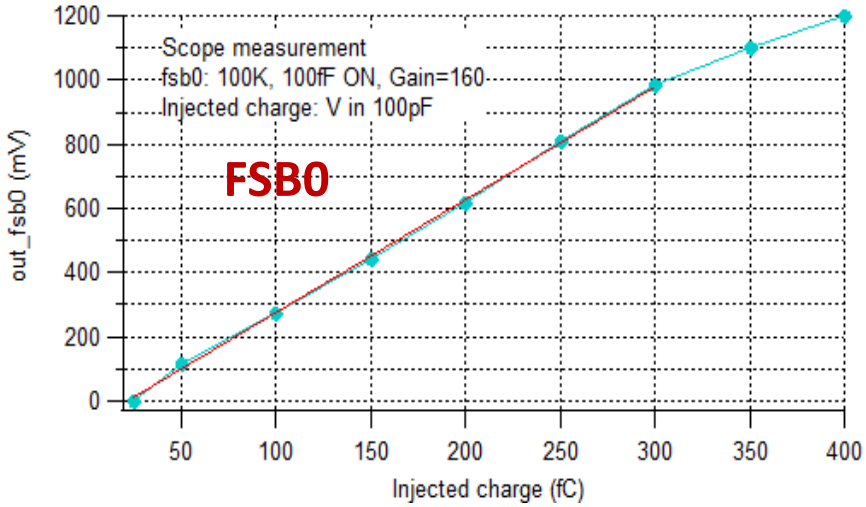
- 64 channels with current preamplifiers
- Trigger less mode (auto trigger 15fC up to 50pC)
- Gain correction (max factor 2)
- 3 shapers + 3 discriminators (encoded in 2 bits for readout)
- I2C link with triple voting for Slow Control Parameters
- 64 Independent channels with zero suppress
- Max 8 events / channel with 12-b time stamping
- Integrated clock generator: PLL
- All bias and reference voltage internal (with power pulsing)
  - No decoupling capacitances required on bias and references voltages
- Token Ring ReadOut

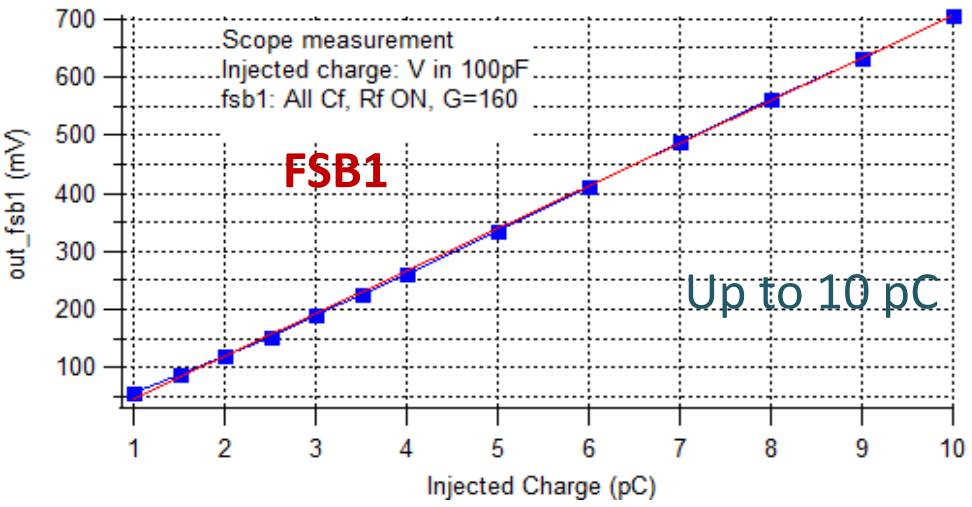


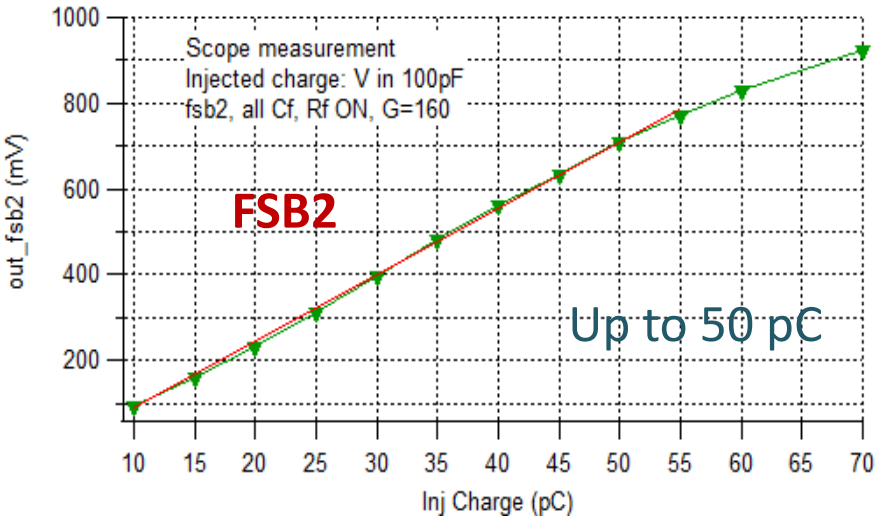
callier@omega.in2p3

HR3: Analog linearity

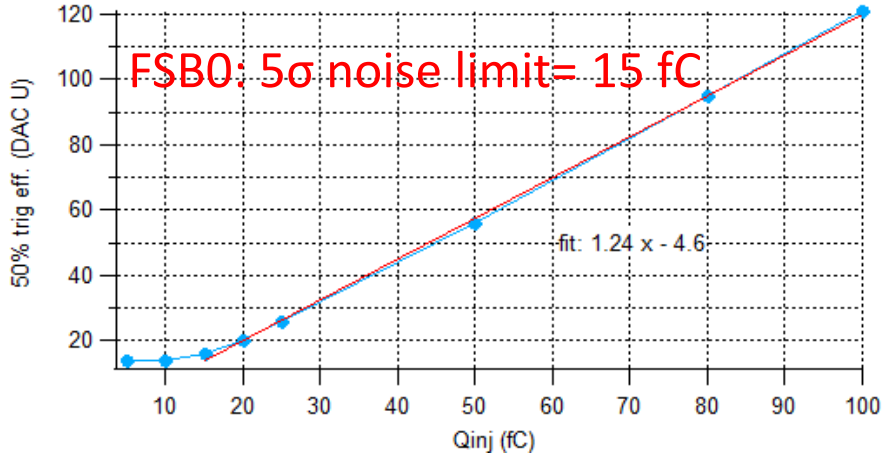
Fast shaper outputs (mV) vs Qinj (fC)







50% trig. Eff. (DAC units) vs Qinj (fC)



Dynamic range: 15fC - 50 pC

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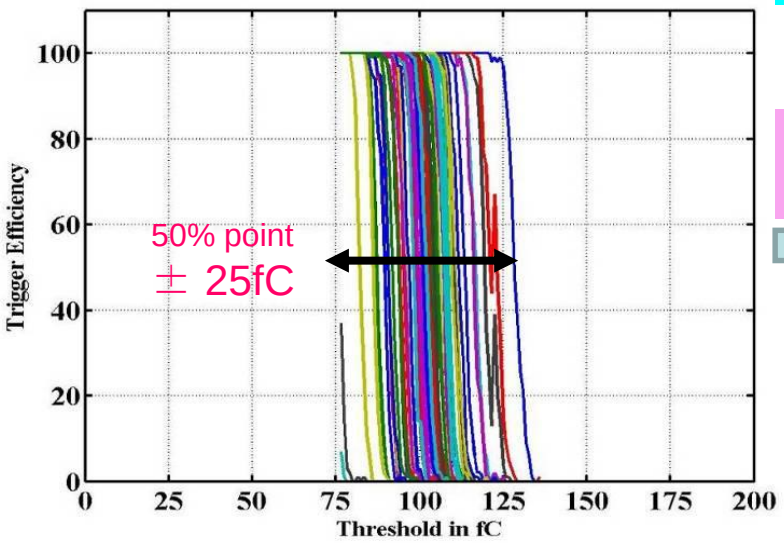
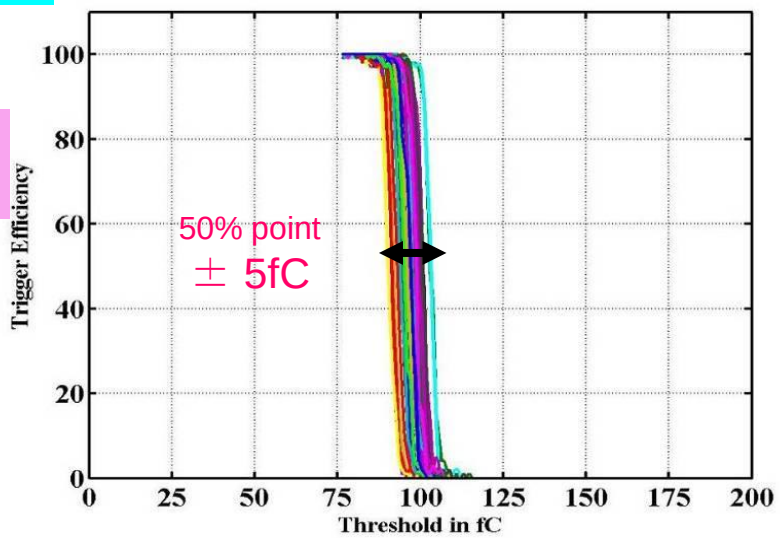
Gain correction / Scurves

Qinj=100fC



HR2 gain correction

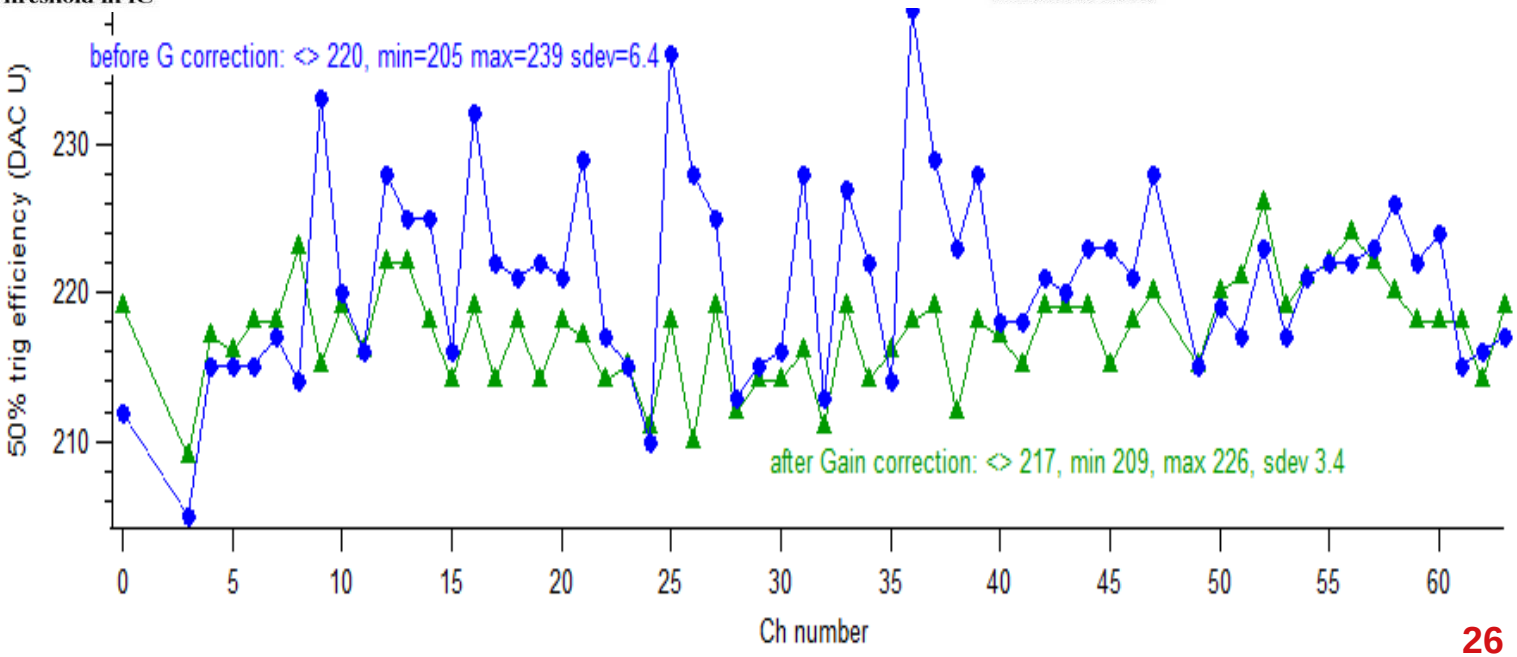


HR3: extracted 50% S-curves point vs Channel number

Before: ± 17 DACU

After: ± 8 DACU

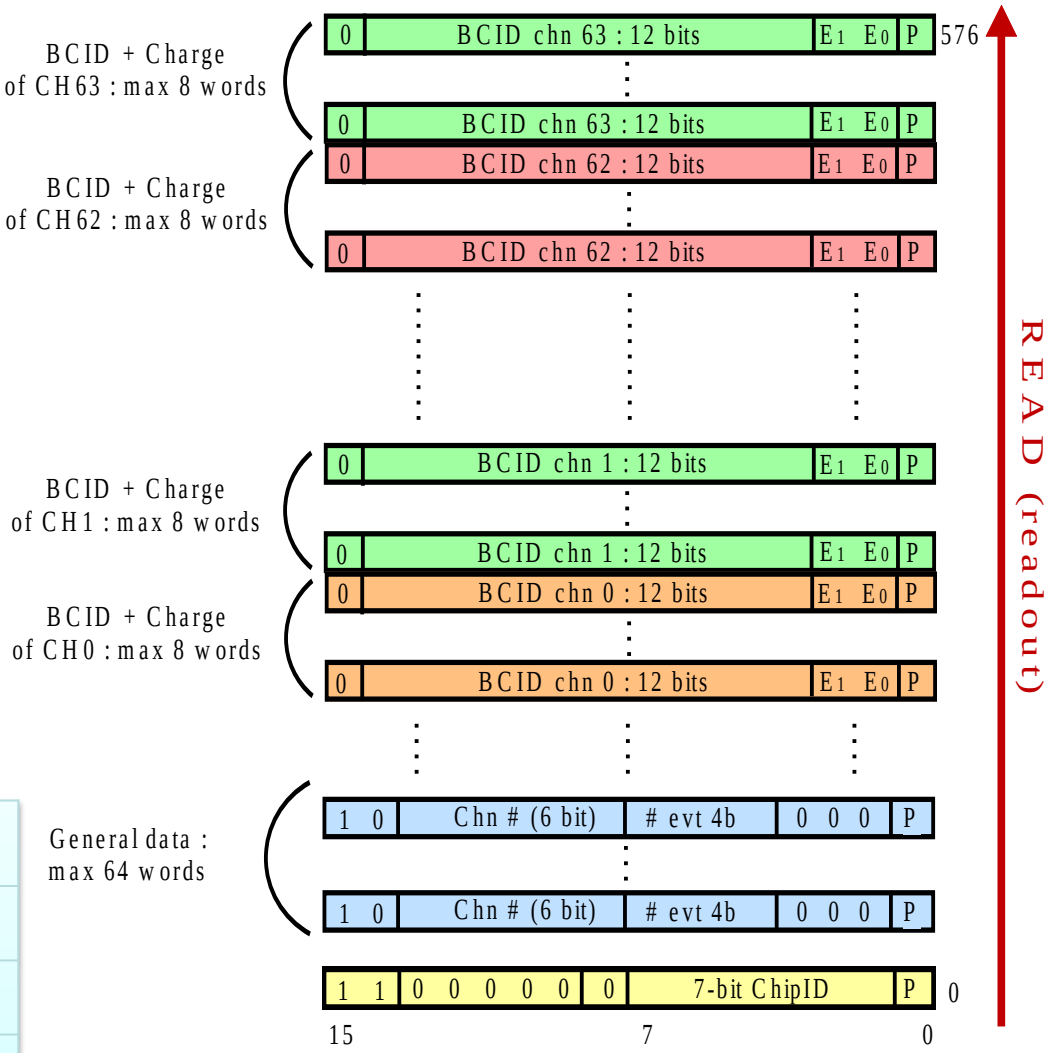
(± 6 fC)



Zero suppress: Memory mapping

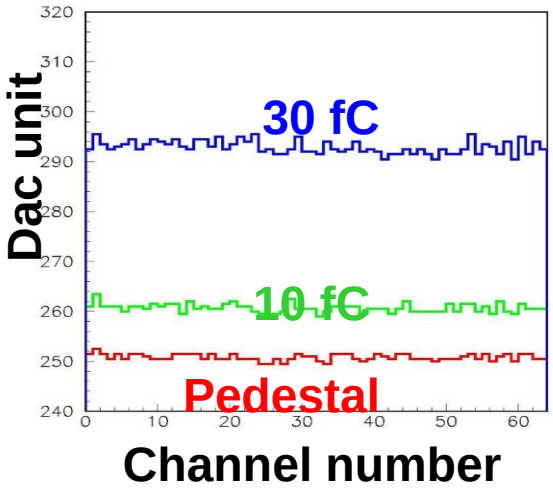
- Chip ID is the first to be outputted during readout (MSB first)
- MSB of each word indicates type of data:
  - "1": general data (Hit ch. number and number of events)
  - "0": BCID + encoded data
- A parity bit/word
- Up to 9232 bits (577x16) during readout
- Example of number of bits during readout:

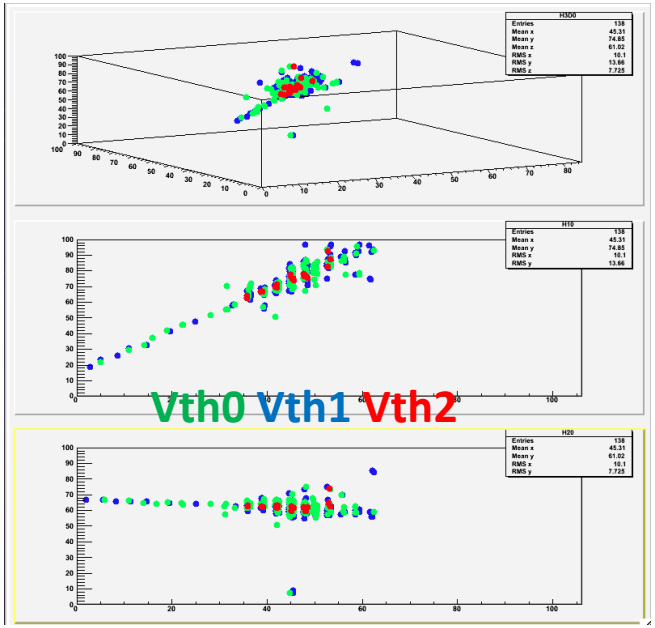
	HR2	HR3
1 chn hit	160	48
8 chn hit	1280	272
4 chn hit @ same time	160	144
10 chn hit @ same time	160	336



RPC sDHCAL calorimeter : HARDROC

- Semi-digital Hadronic calorimeter (SDHCAL) technological proto with up to **50 layers** built in 2010-2011.
- Scalable readout scheme successfully tested
- 10 fC threshold on 1 m²
- Complete system in TB with **460 000 channels**, **AUTOTRIGGER** mode and **power pulsing (5%)**





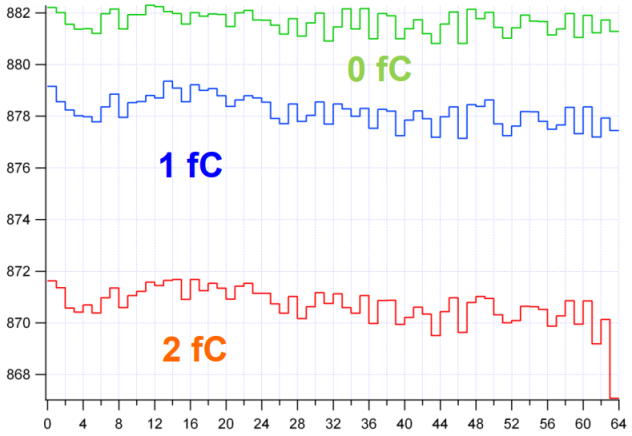
Micromegas sDHCAL : MICROROC

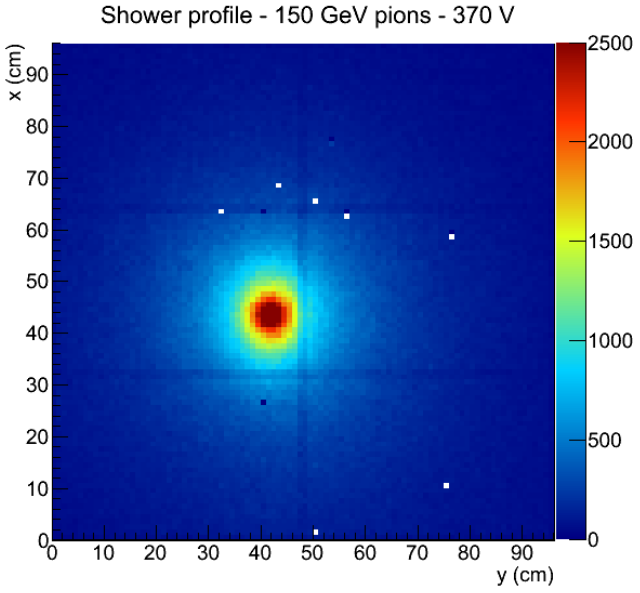
64 channels for µMegas (sDHCAL)

- Very similar to HARDROC except :
  - Input (charge) preamp
  - Slower shapers (100-150 ns)
  - HV Spark protections
- Noise: **0.2fC (Cd=80 pF). Auto trigger on 1fC** up to 500fC
- Pulsed power: **10 µW/ch** (0.5 % duty cycle)
- 4 Micromegas prototypes of 1x1 m2 were constructed in 2011-2012 and tested in particle beams inside the DHCAL steel structure in 2012

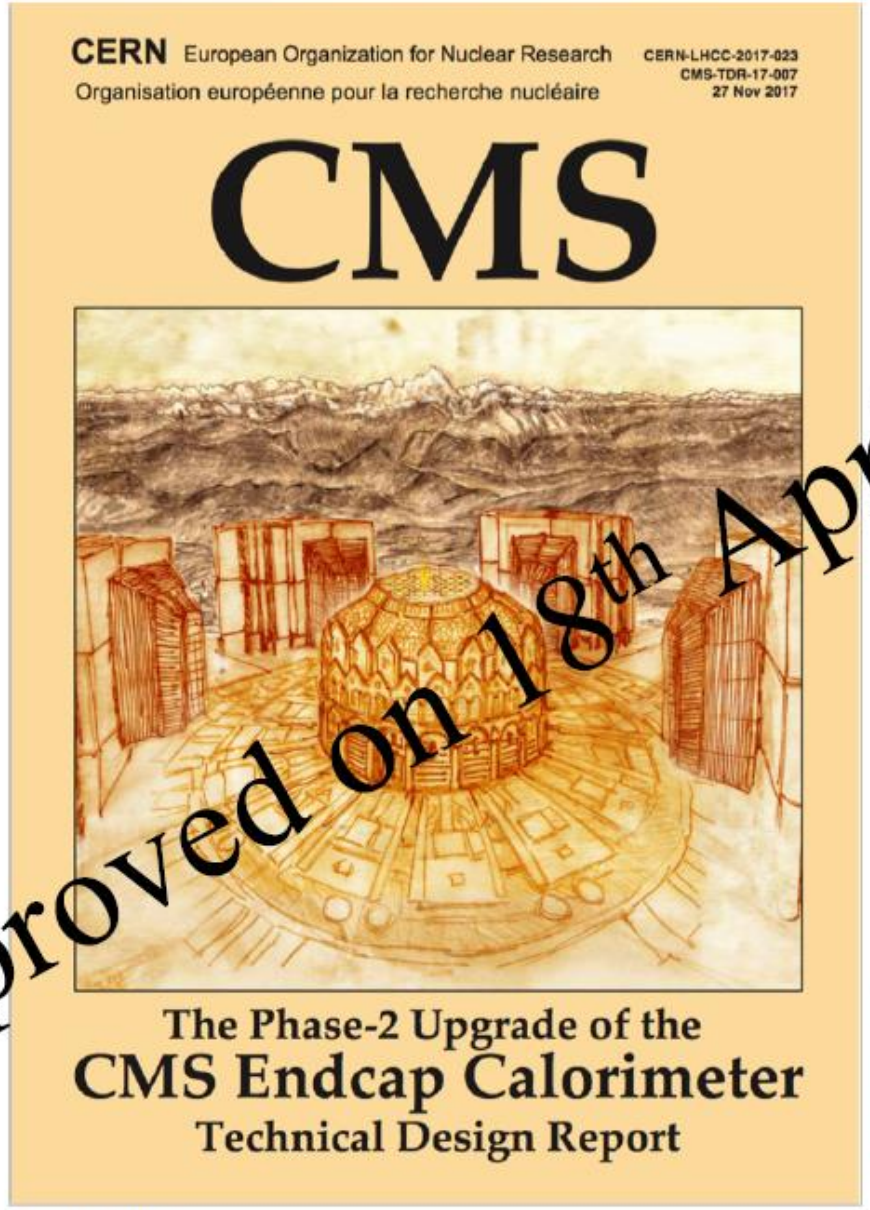
1m² Micromegas detector
Microroc : 10 000 channels

Very good performance of the electronics and detector (Threshold set to 1fC)





HGCAL TDR was submitted in Nov. 2017
R&D continues; construction starts in 2020

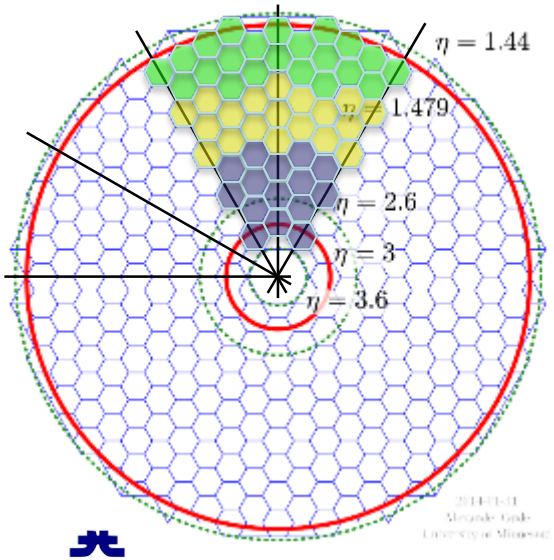


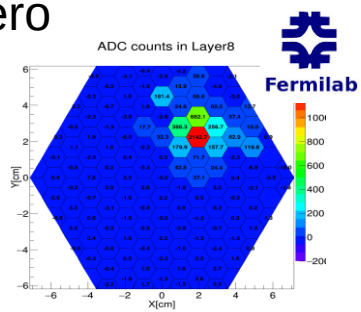
Approved on 18th April 2018!

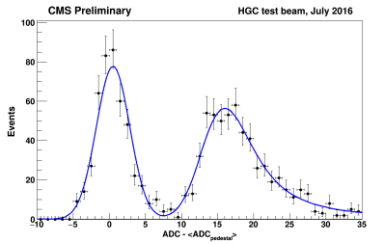
CMS-TDR-17-007
http://cds.cern.ch/record/2293646

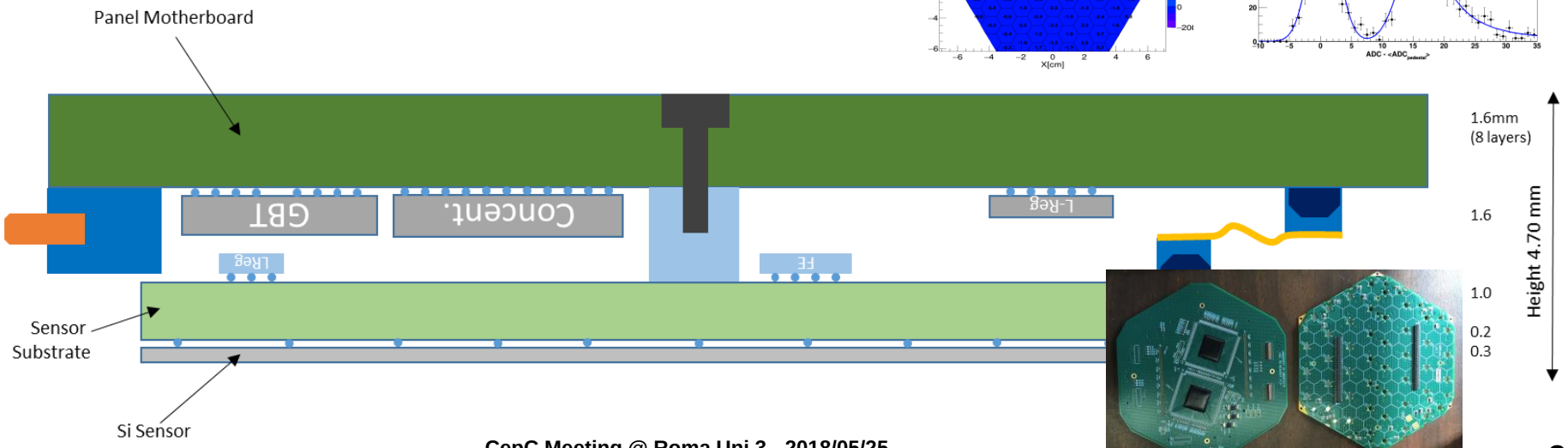
CMS HGCAL Detector overview

- Stringent requirements for Front-End Electronics
  - Low power (< 10 mW), [and dual polarity !]
  - Low noise (< 2000 e-) (MIP ~ 1-4 fC with S/N>2)
  - High radiation (200 Mrad, $10^{E}16$ N)
  - High dynamic range (0,2fC to 10pC)
  - Fast shaping time (<20ns to avoid pile up)
  - Timing information (tens of ps)
  - System on chip (digitization, processing : zero suppression, trigger sum on chip)
  - High speed readout (5-10 Gb/s)
  - ~ 10 million channels



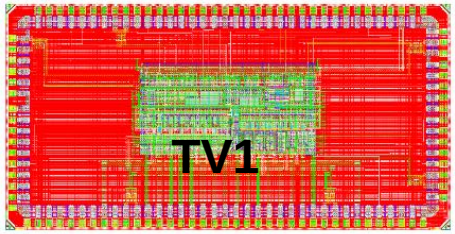


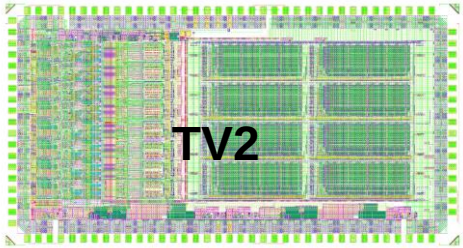




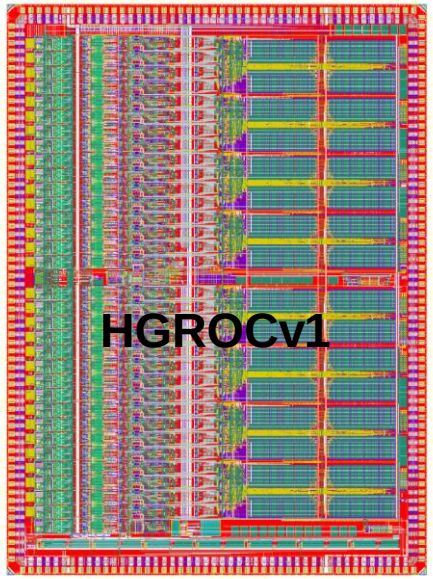
4 ASICs submitted in the past two years

- **SKIROC2_CMS**
  - SiGe 350 nm
  - Submitted in January 2016
  - Dedicated to test beam



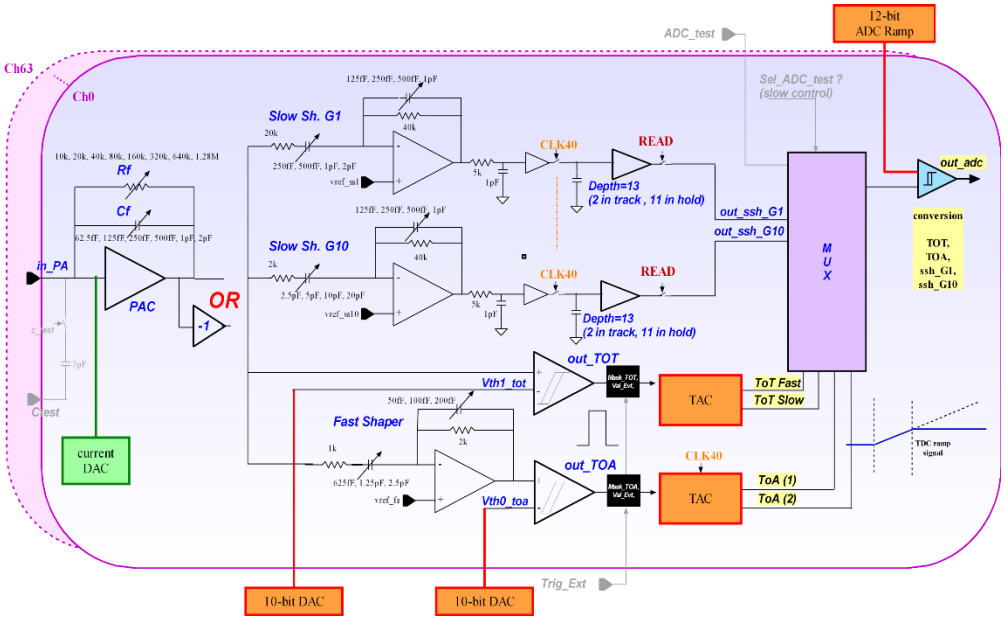


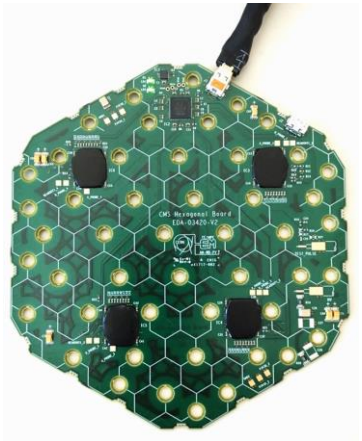
- 1st test vehicle: **TV1**
  - CMOS 130 nm
  - Submitted in May 2016, received in august 2016
  - Dedicated to preamplifier studies
- 2nd test vehicle: **TV2**
  - CMOS 130 nm
  - Submitted in December 2016, received in may 2017
  - Dedicated to technical proposal' analog channel study
- **HGROCv1**
  - CMOS 130 nm
  - Submitted in July 2017, expected in October 2017
  - all analog and mixed blocks; large part, but not complete, digital blocks



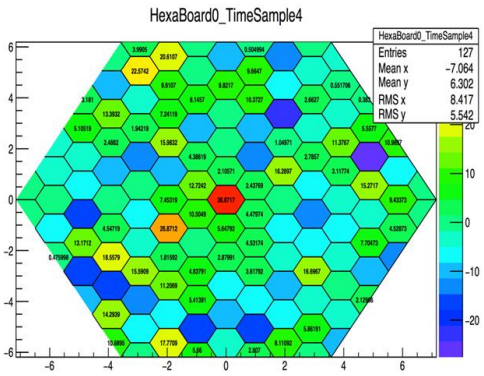
SKIROC2_CMS for HGCAL

- new SKIROC2 for CMS
  - Optimized version for CMS testbeam, pin to pin compatible
  - Dual polarity charge preamplifier
  - Faster shapers (25 ns instead of 200 ns)
  - 40 MHz circular analog memory, depth= 300 ns
  - TDC (TAC) for ToA and ToT , accuracy : ~50 ps
  - Submitted jan 2016 SiGe 350nm
- Tests :
  - First tests on BGA testboards
  - 4-5 boards equipped





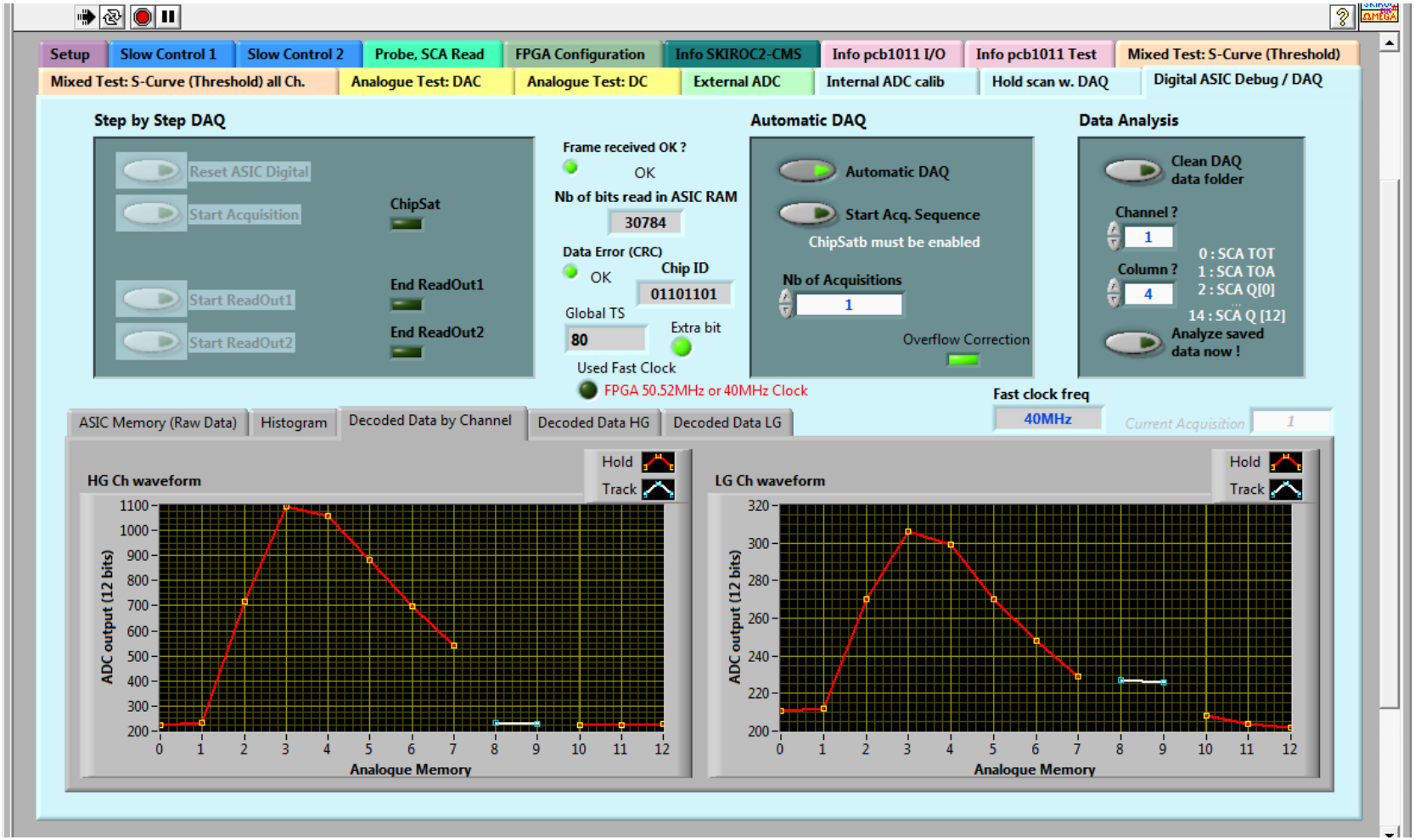
Hexaboard designed at CERN



Electron and pions signals seen In testbeam

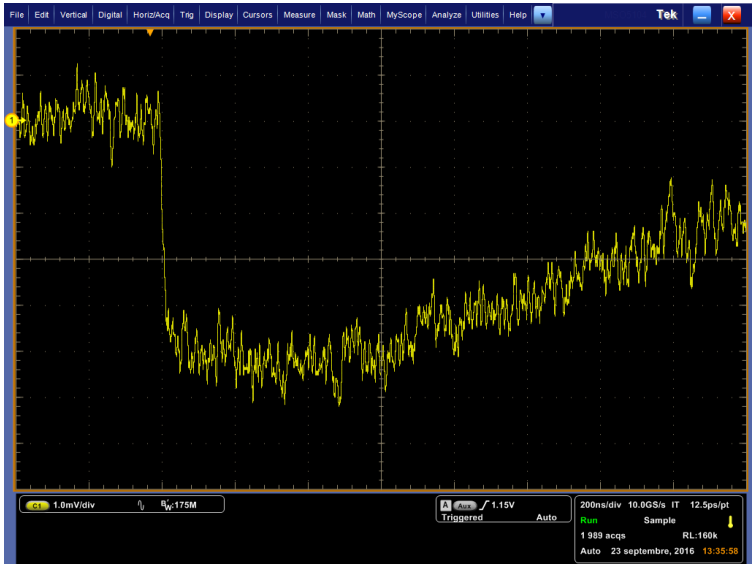
SCA operation

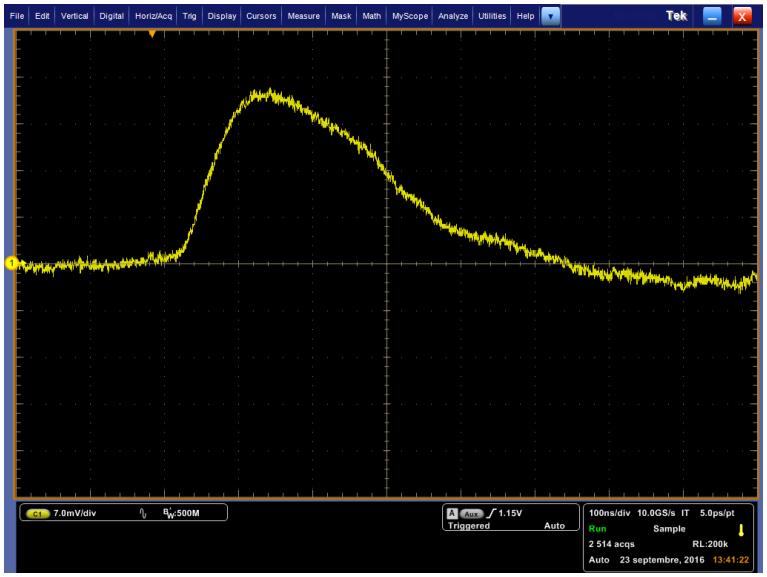
- 40 MHz circular analog memory. 13 cells in store and 2 in track
- Allows ~300 ns trigger latency

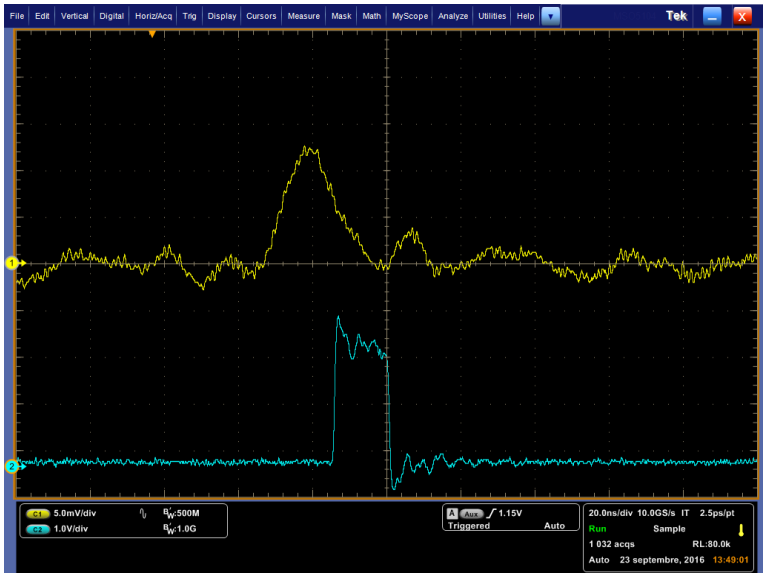


Waveforms with 1 MIP injection

- 3 fC test pulse injection ~1 MIP
- Preamp Cf = 0.5 pF Rf = 2.5MΩ Cd=0
  - Vout = 5 mV N = 0.4 mV
- HG shaper tau = 20 ns
  - Vout = 15 mV N = 1.2 mV =>0.25 fC
- Fast shaper tau = 5 ns
  - Vout = 12 mV N = 1.4 mV =>0.35 fC







Reconstructed waveforms CSA config

- Charge sensitive configuration : Rf = 2.5 MΩ Cf = 0.5pF
- Hi Gain / Lo Gain positive/negative configurations

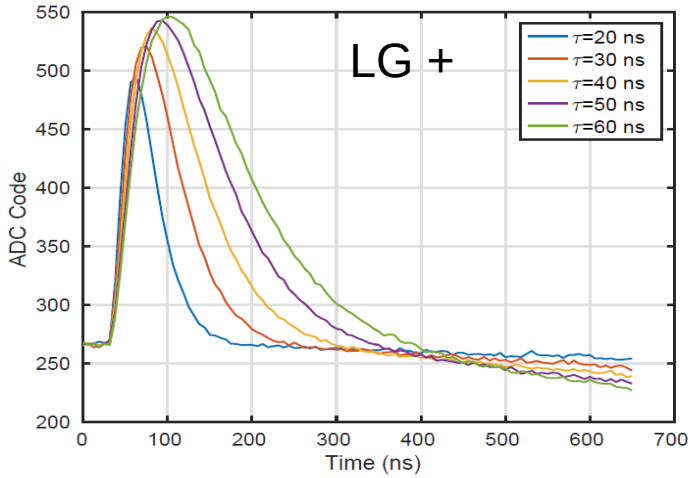
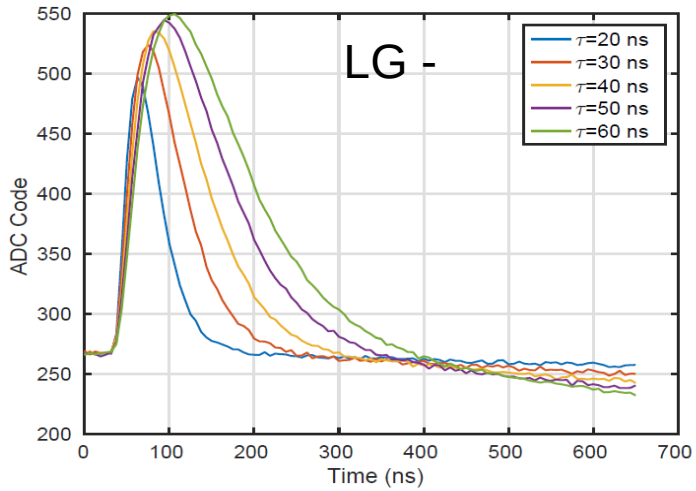


Figure 29: Shaper response for different tau, Low-gain, positive polarity



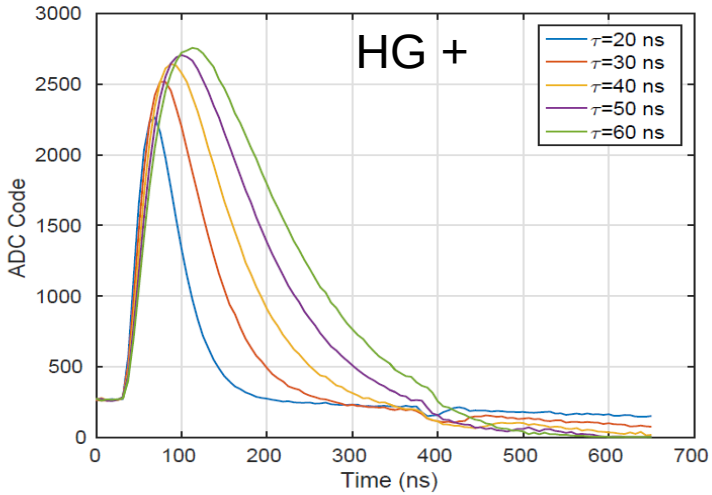


Figure 30: Shaper response for different tau, High-gain, positive polarity

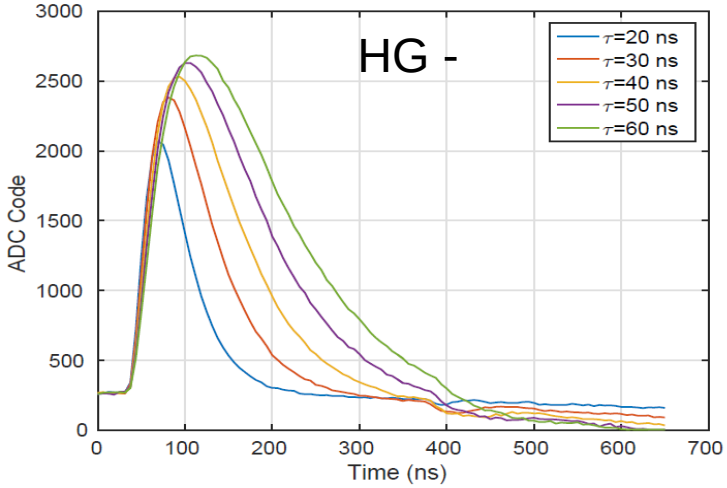
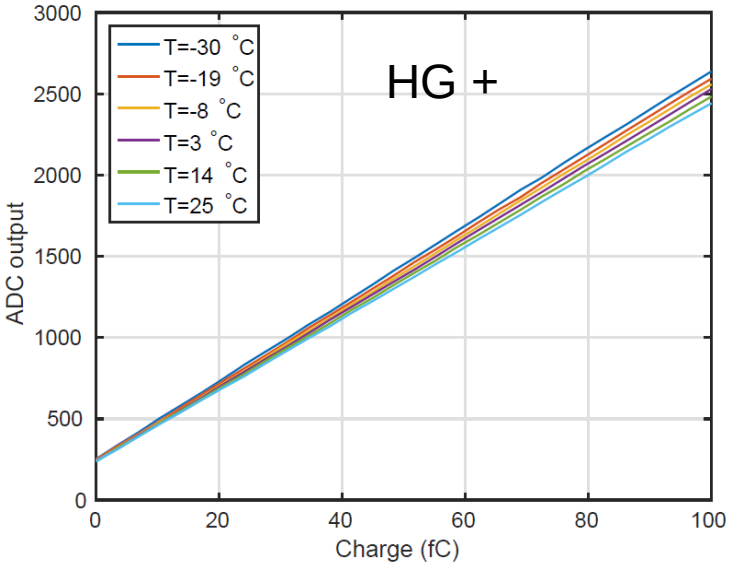


Figure 32: Shaper response for different tau, High-gain, negative polarity

Linearity

- Linearity < 1%, temperature sensitivity ~0.1%/K



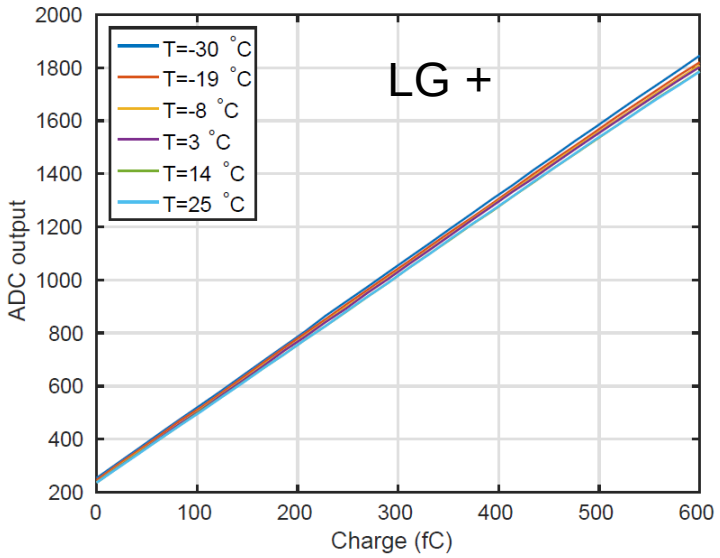
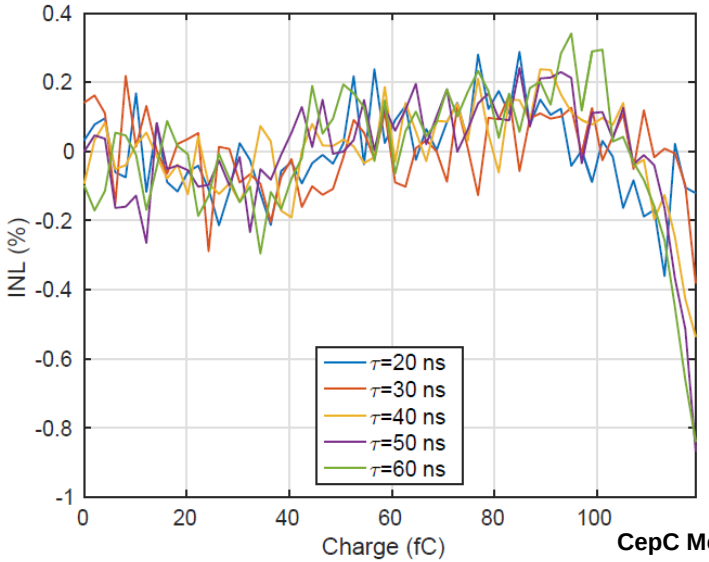
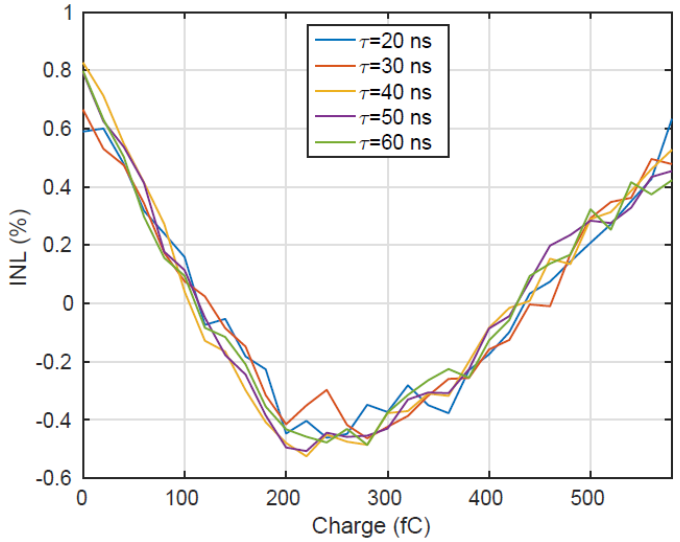


Figure 3: High-gain transfer function for different T, positive polarity, $\tau = 40ns$

Fig ns





Noise vs capacitance

- Linear fit of series noise gives e_n = 1.0 nV/√Hz
- Parasitic capacitance : Ca = 34 pF (10 pF chip 20 pF board)

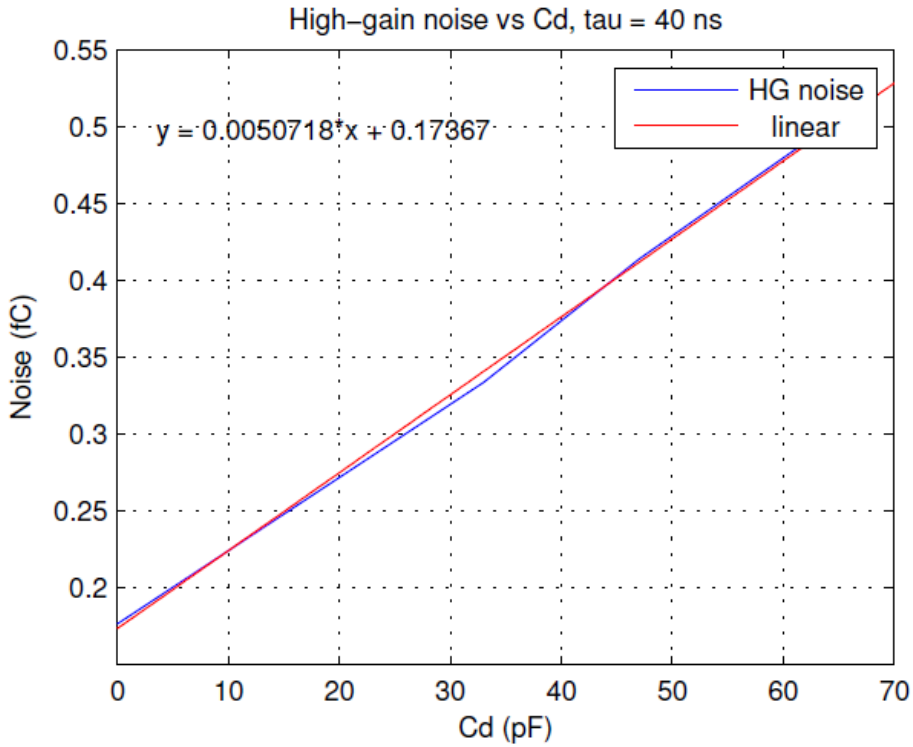


Figure 8: High-gain noise vs Cd, positive polarity, $\tau = 40$ ns. Least-squares linear fit: $y = 0.17367 + 50.718 \times 10^{-3}x$ (fC, pF), $y = 0$ yields $C = 34$ pF.

Waveforms : ISA configuration

- Current sensitive configuration : Rf = 20 kΩ Cf = 0.5pF
- Hi Gain / Lo Gain positive/negative

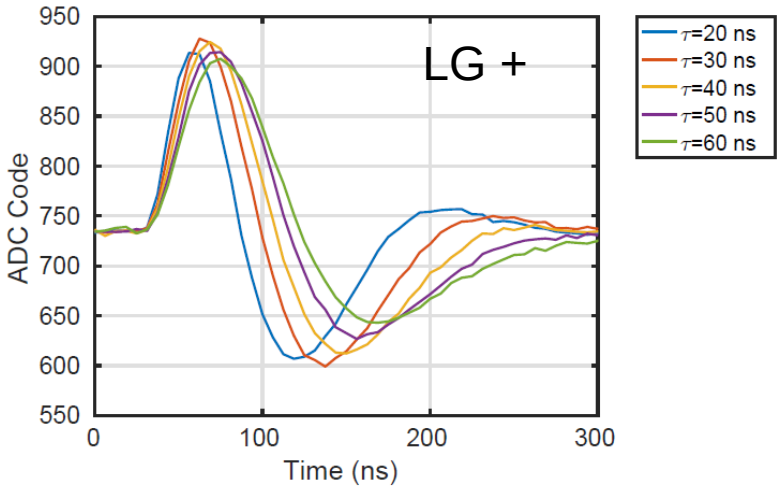


Figure 33: Shaper response for different tau, Low-gain, positive polarity

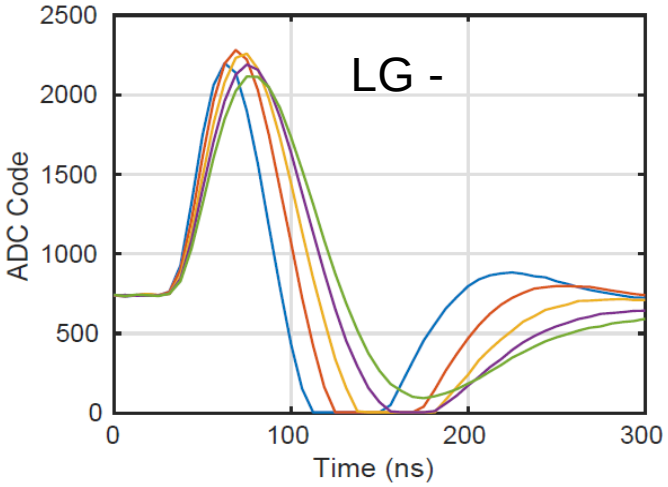


Figure 34: Shaper response for different tau, High-gain, positive polarity

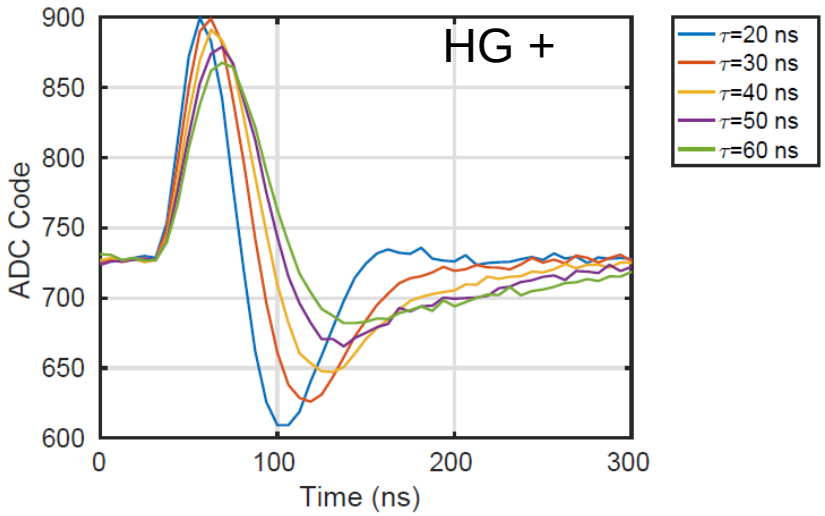


Figure 35: Shaper response for different tau, Low-gain, negative polarity

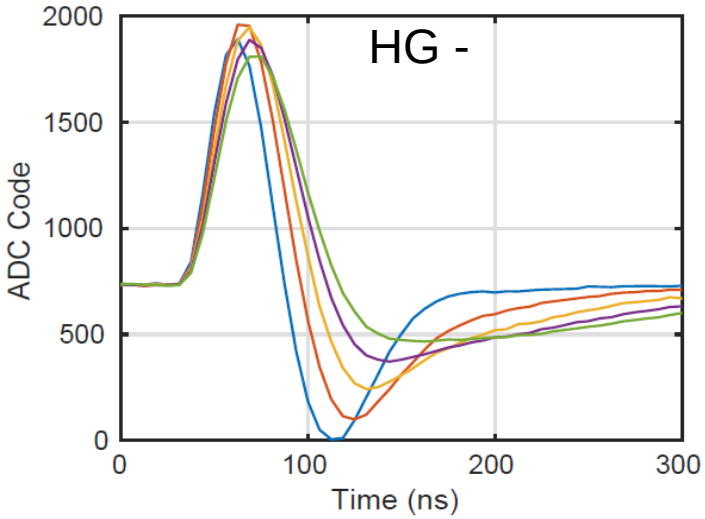
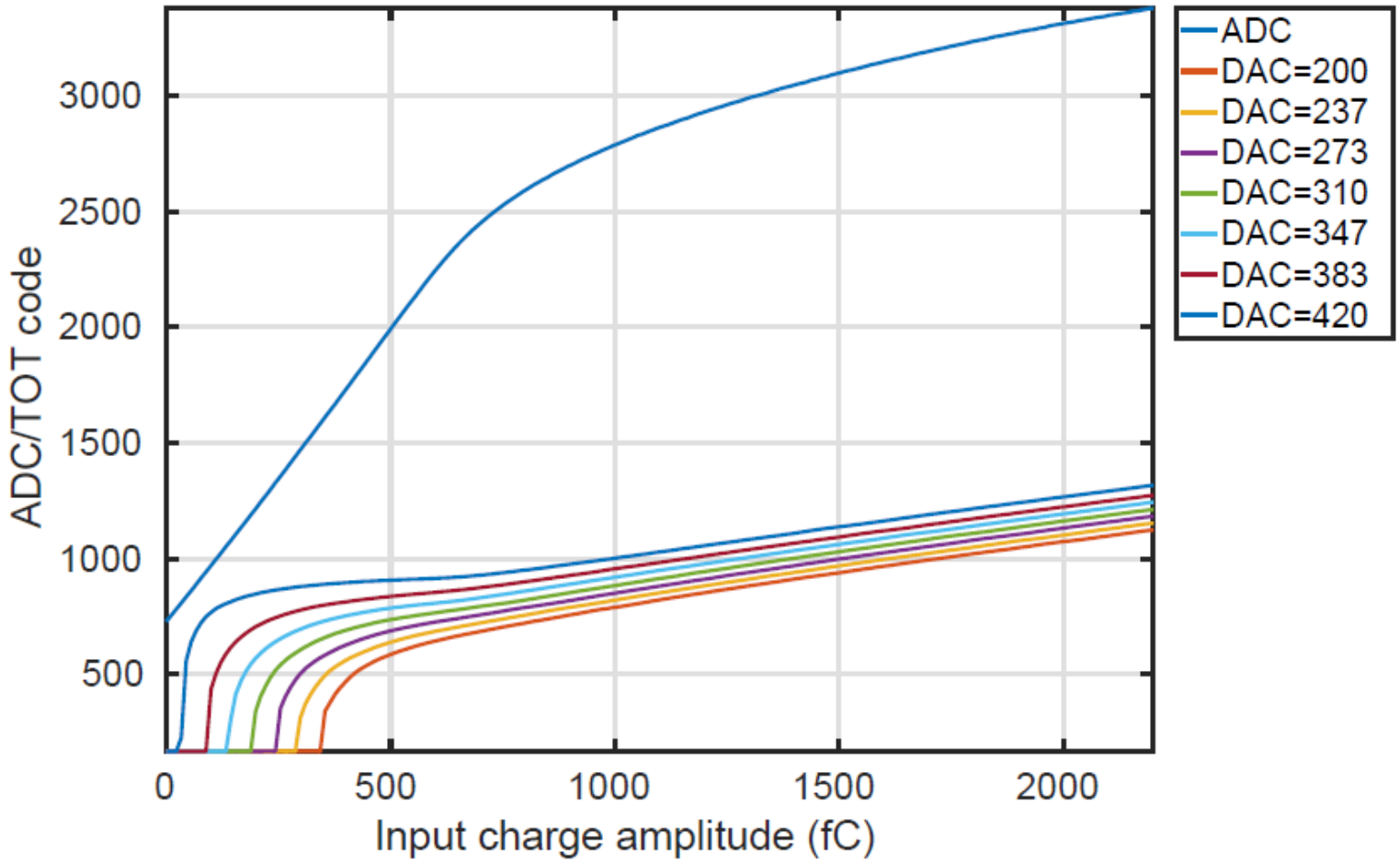


Figure 36: Shaper response for different tau, High-gain, negative polarity

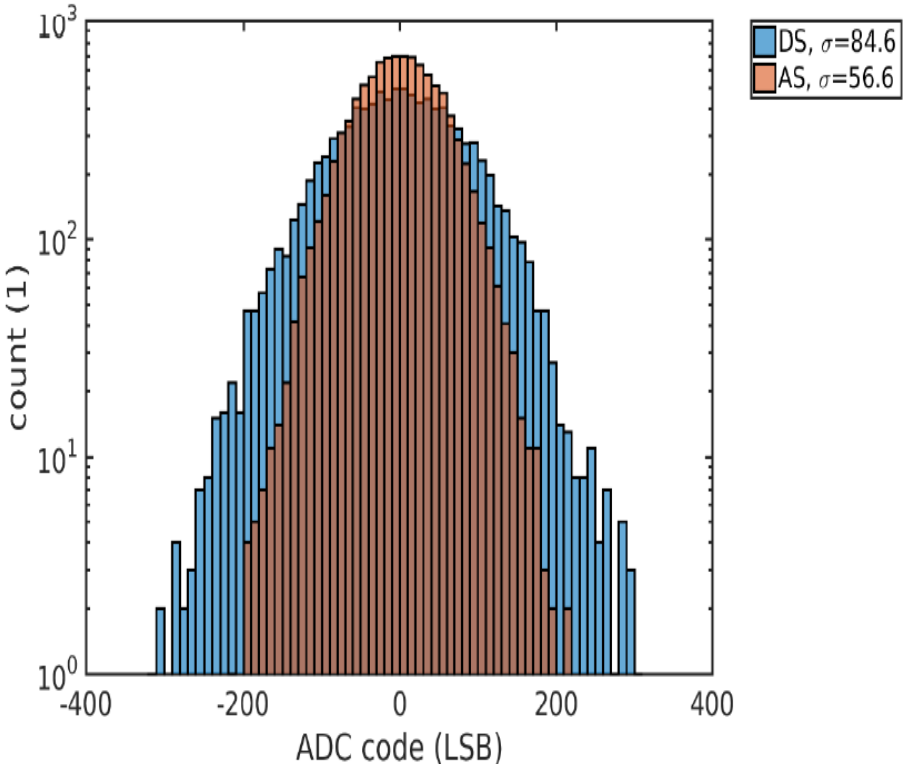
Time over Threshold (ToT)

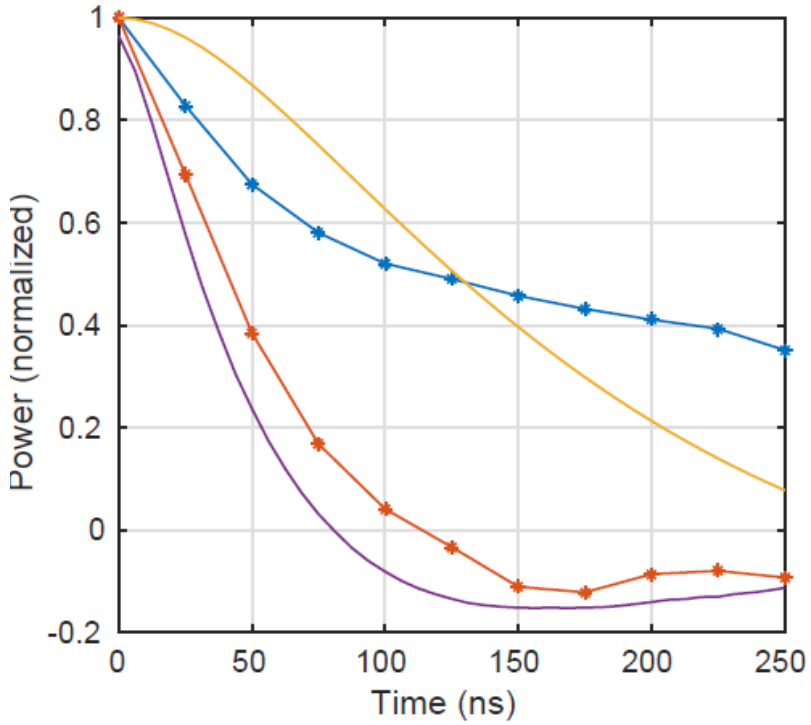
- TOT measured in current sensitive config : Rf=20k Cf=300f
- ADC range : 0-500 fC TOT above
- energy reconstruction around 500 fC, calibration, pedestal evaluation



Coherent and incoherent noise

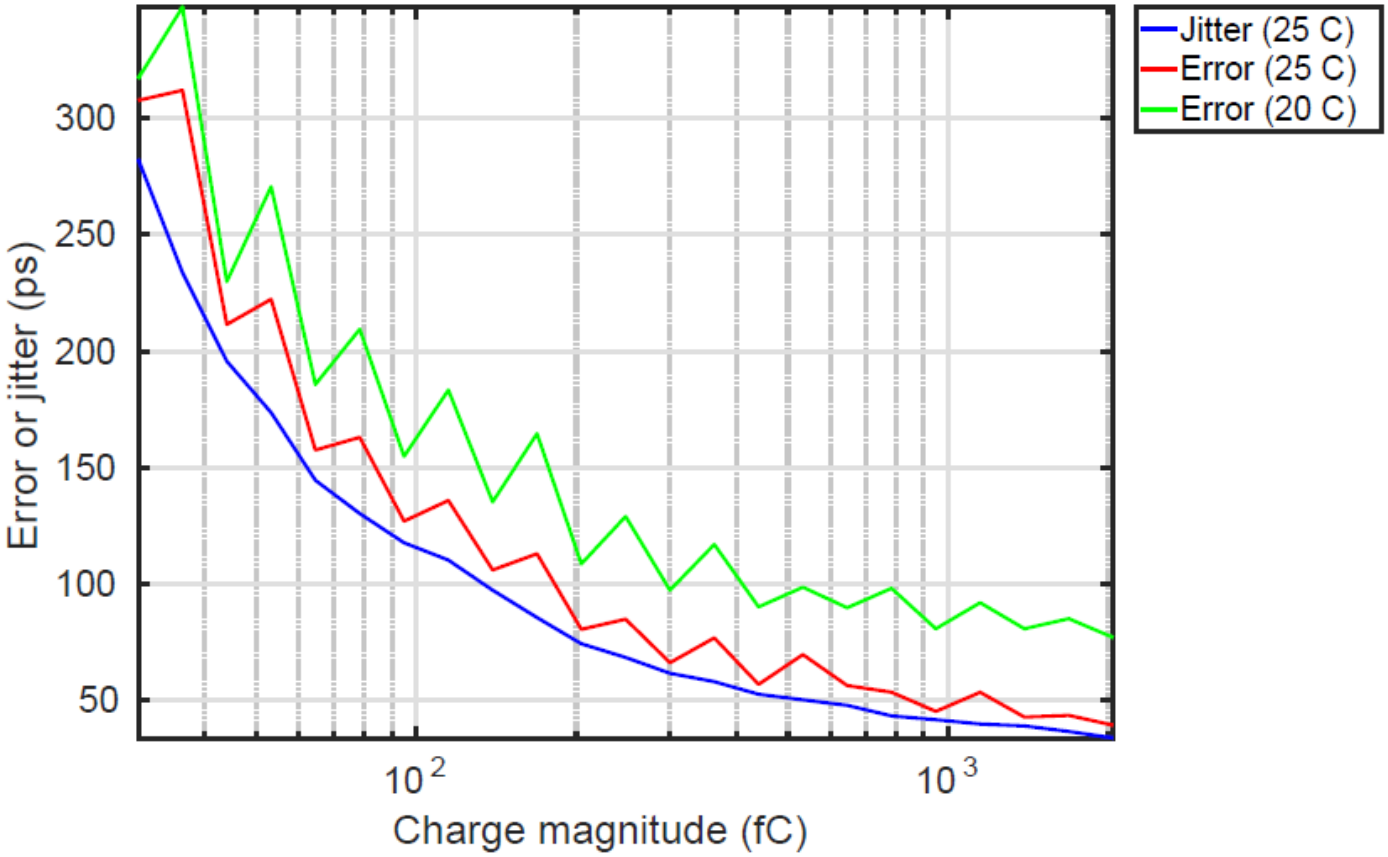
- A constant concern in calorimetry
  - Coherent noise extracted by comparing direct and alternate sums on n channels (n=64) : DS = ∑ ped[i] ; AS = ∑ $(-1)^i$ ped[i]
  - Incoherent noise IN = rms(AS) / √n
  - Coherent noise : CN = $\sqrt{var(DS) - var(AS)}$ / n
- Need to show that CN / IN ~ 10% can be obtained at system level



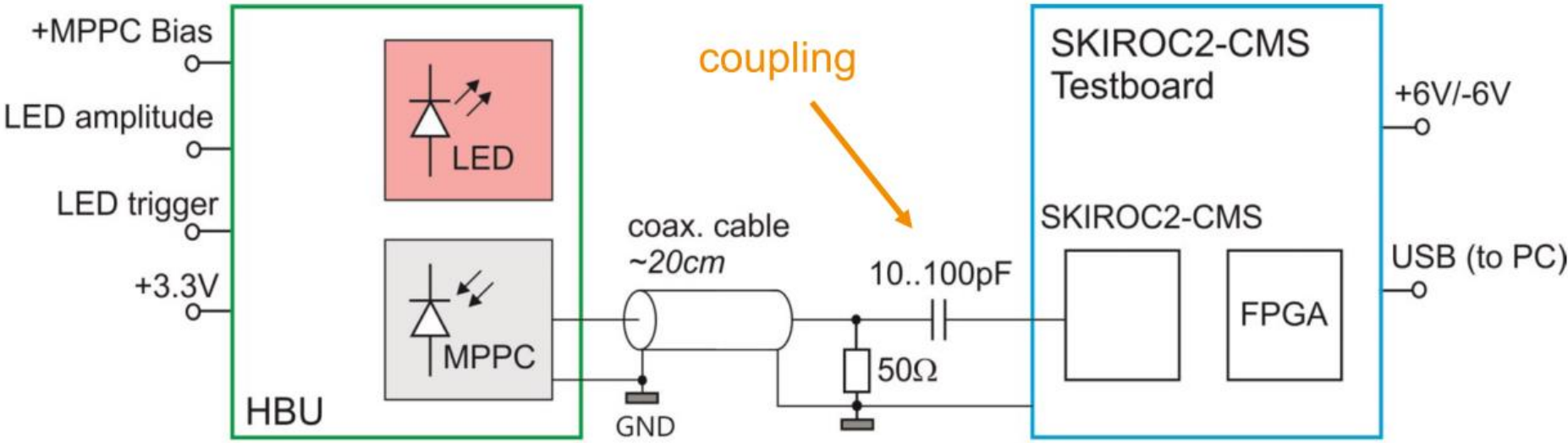


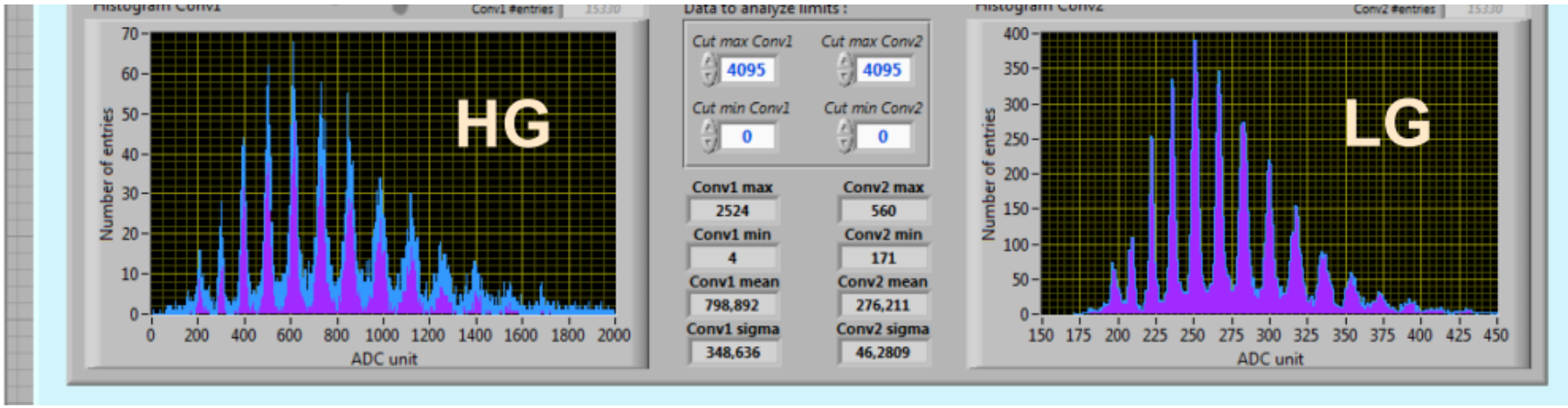
Time of arrival (ToA)

- TOA measured with internal TDC and corrected for time walk
- Constant term = 50 ps
- Noise term = 10 ns / Q(fC) (~4 ns/Q expected)
- What can be obtained at system level ?



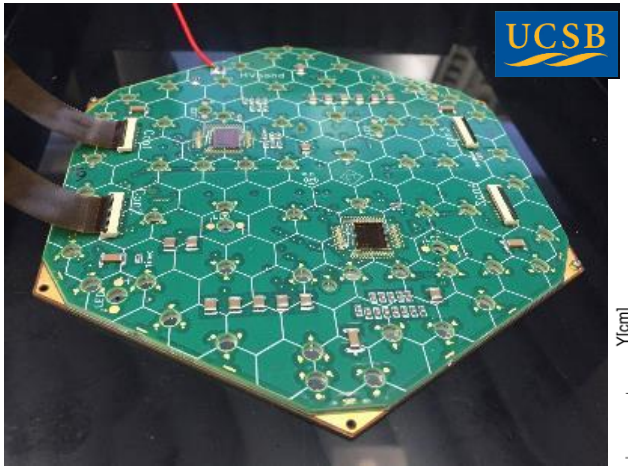
- Tests with SK2_CMS with DESY

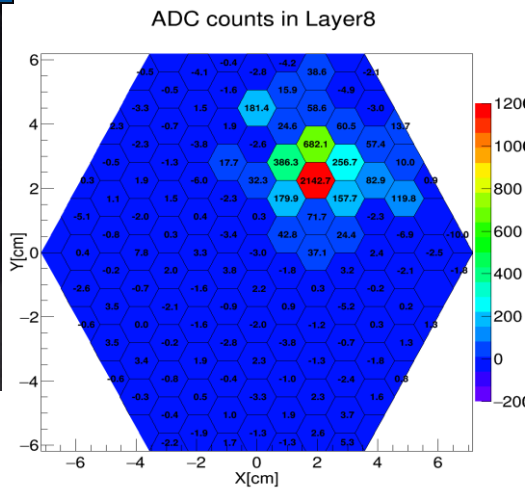


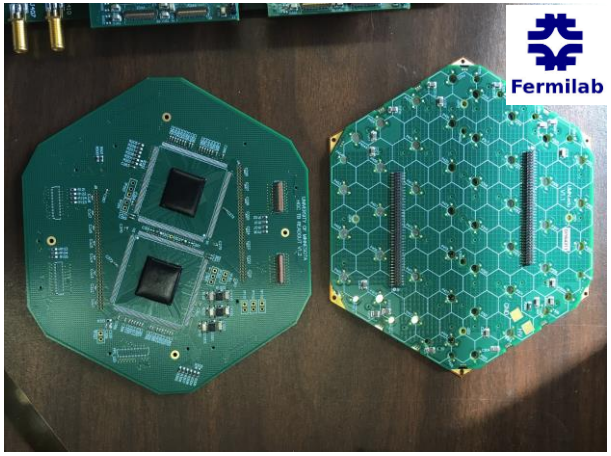


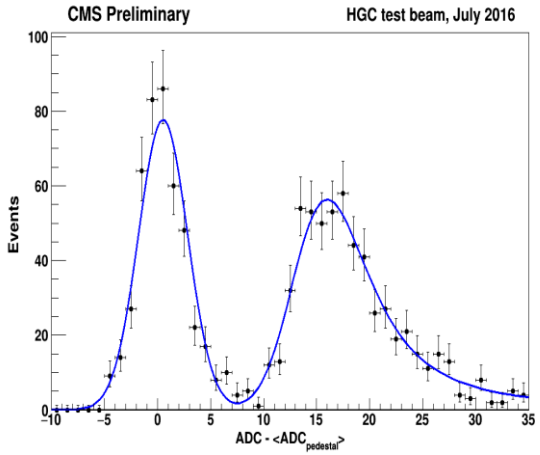
Testbeam setup(s)

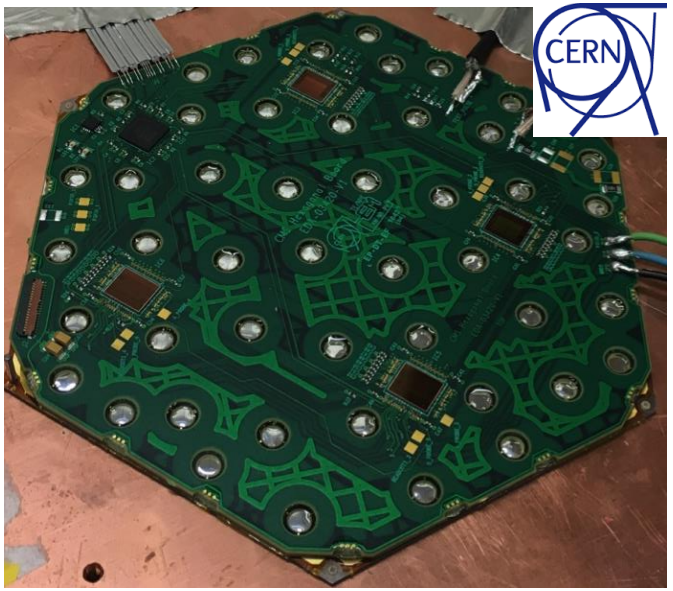
- Boards with SKIROC2 used in 2016 [UCSB, FNAL,UM]
- Hexaboards with SK2_CMS in 2017 [CERN]

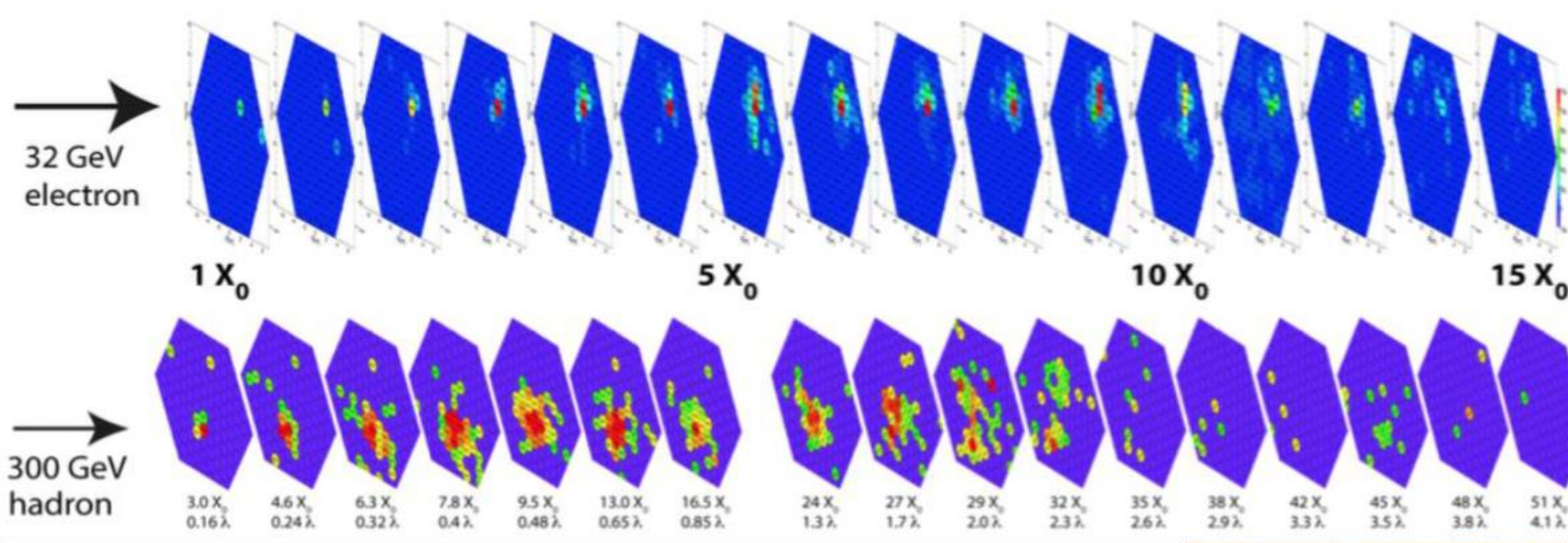






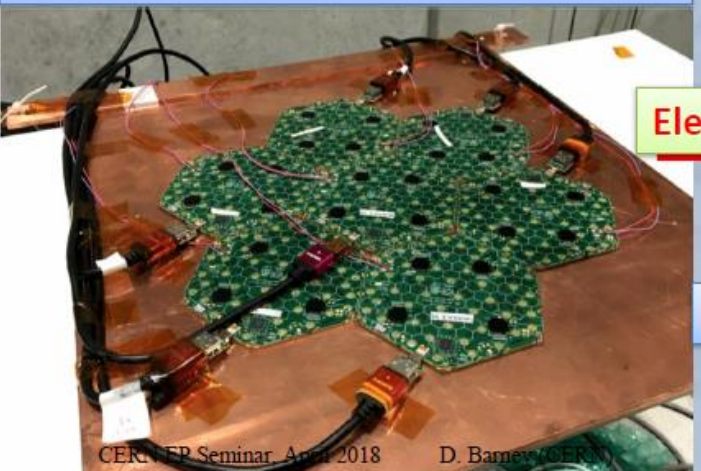


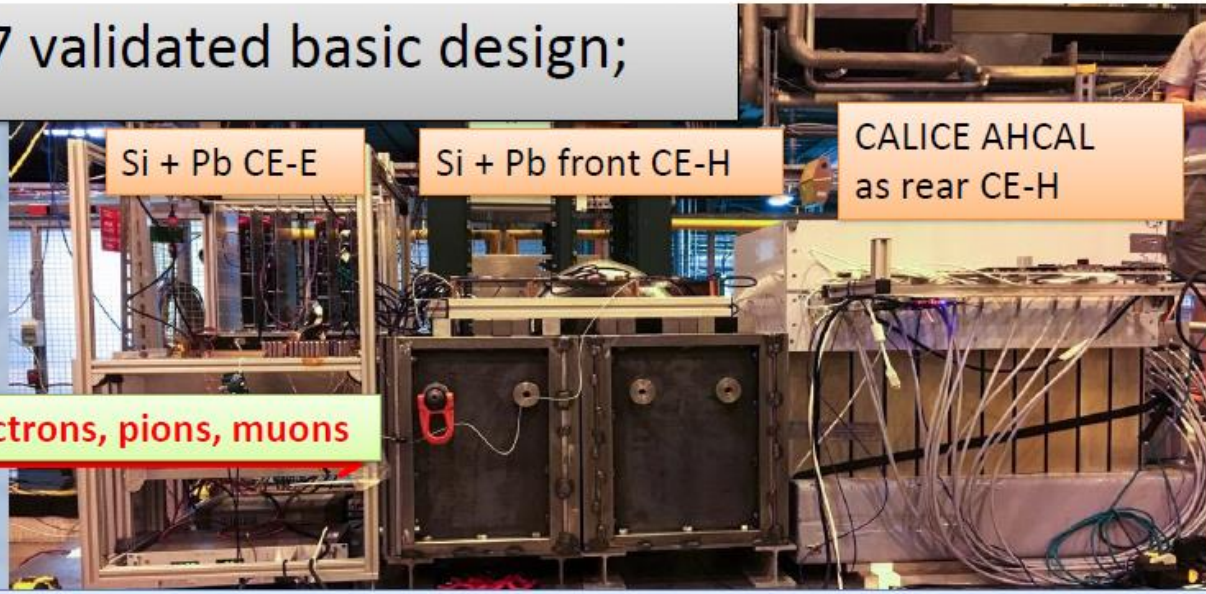




Beam tests in 2016 & 2017 validated basic design;

Mips (for calibration) seen from muons and also single particles within hadronic showers



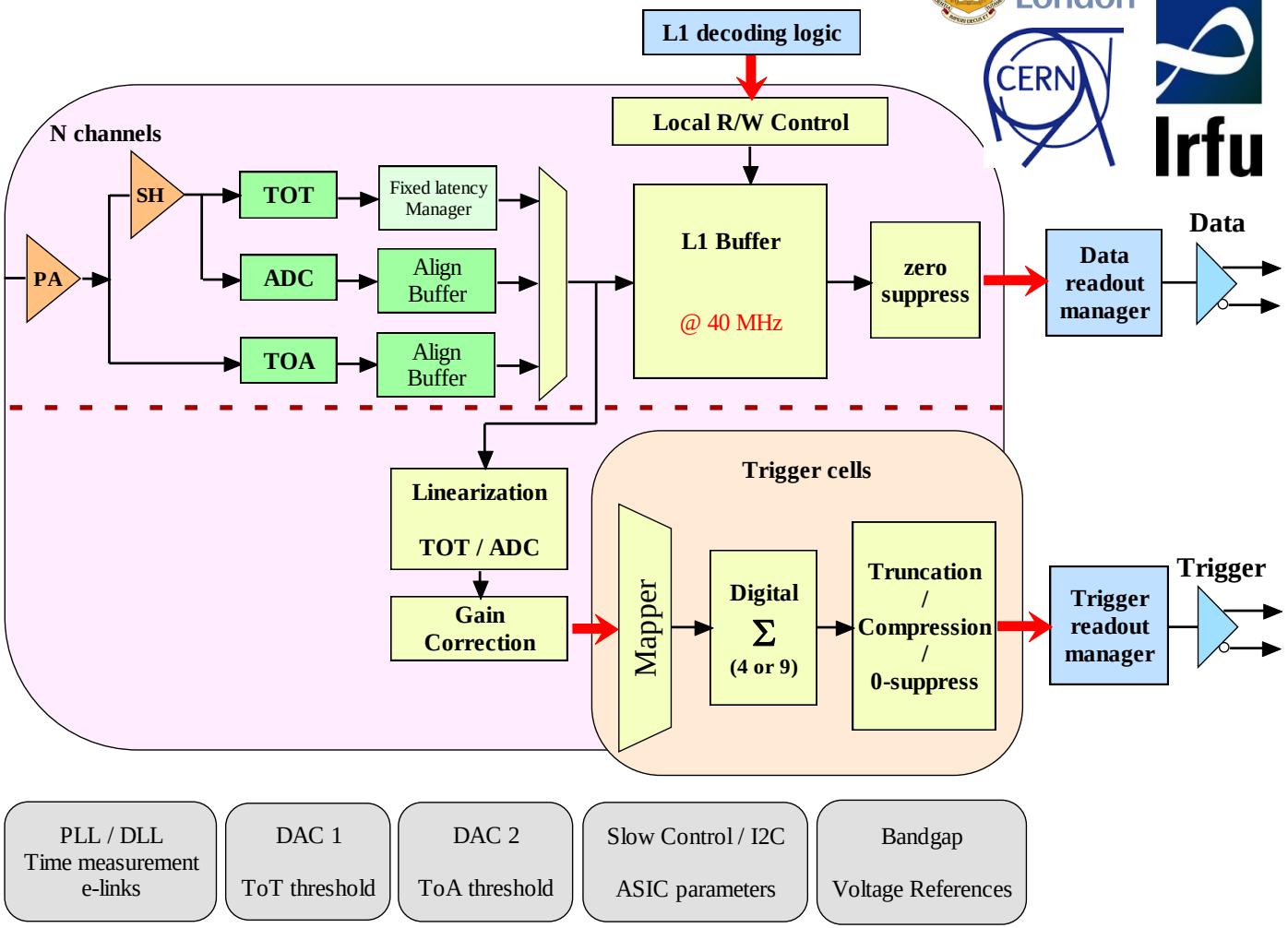


Existing ASIC (Skiroc2) used in 2016; evolution (Skiroc2-CMS) used in 2017/18

HGCAL readout ASIC

HGROCv1 features:

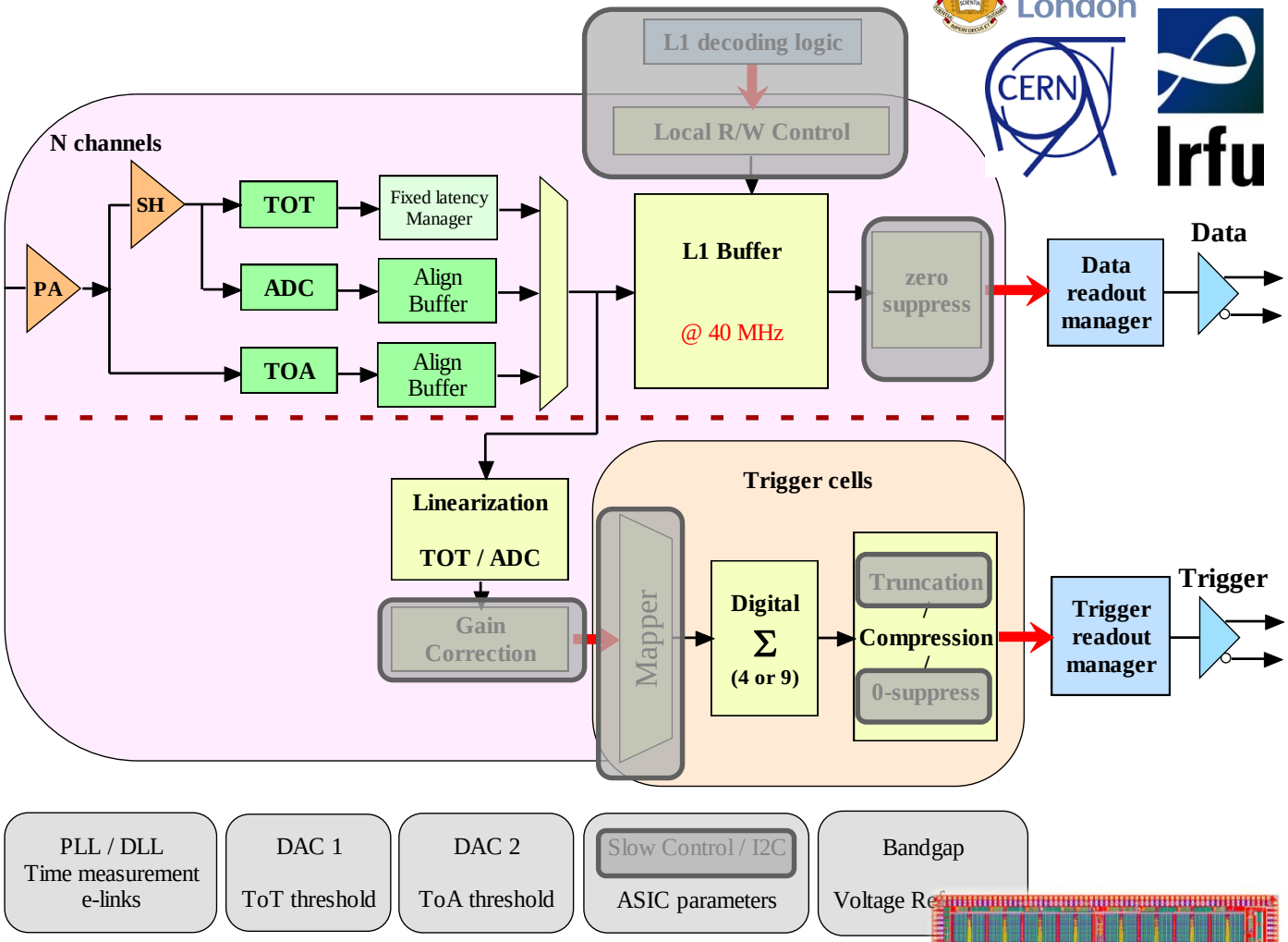
- 32 channels
- Dual polarity
- TOT with 2 variants:
  - Low power @ Imperial
  - DLL @ OMEGA (CERN based)
- TOA (CEA)
- 11-bit SAR ADC (OMEGA)
- Simplified Trigger path
  - Only sum by 4
  - No 0-suppress (4+4 log)
- Data readout to be defined
- SC with triple voting (shift register like SK2-CMS)
- Many digital block with simplified architecture
- Services
  - Bandgap from CERN
  - PLL from CEA-IRFU
  - 10b DAC from TV2

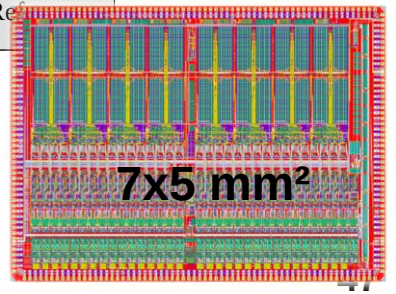


HGROC block diagram vs HGROCv1

HGROCv1 features:

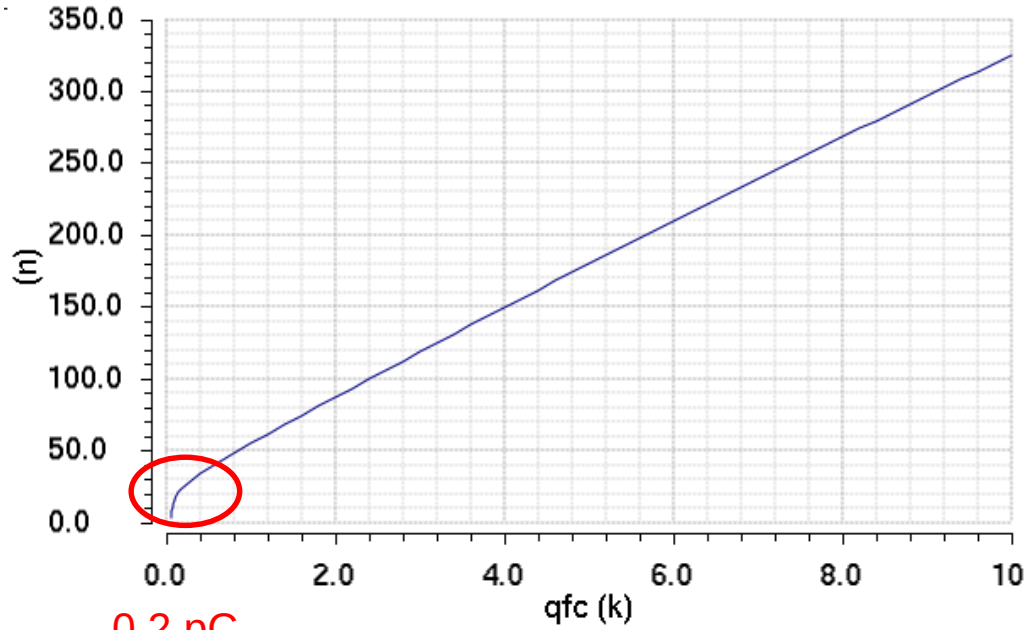
- 32 channels
- Dual polarity
- TOT with 2 variants:
  - Low power @ Imperial
  - DLL @ OMEGA (CERN based)
- TOA (CEA)
- 11-bit SAR ADC (OMEGA)
- Simplified Trigger path
  - Only sum by 4
  - No 0-suppress (4+4 log)
- Data readout to be defined
- SC with triple voting (shift register like SK2-CMS)
- Many digital block with simplified architecture
- Services
  - Bandgap from CERN
  - PLL from CEA-IRFU
  - 10b DAC from TV2



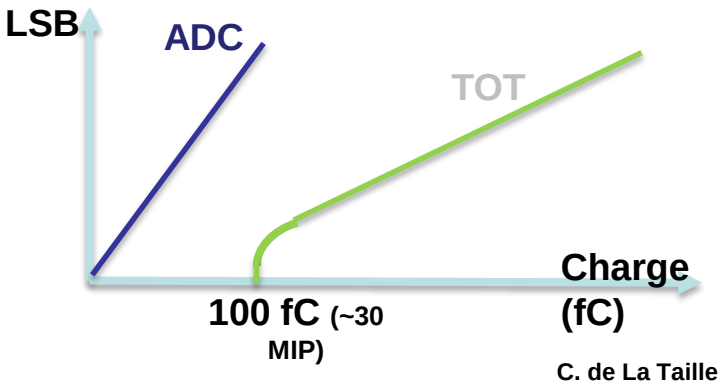


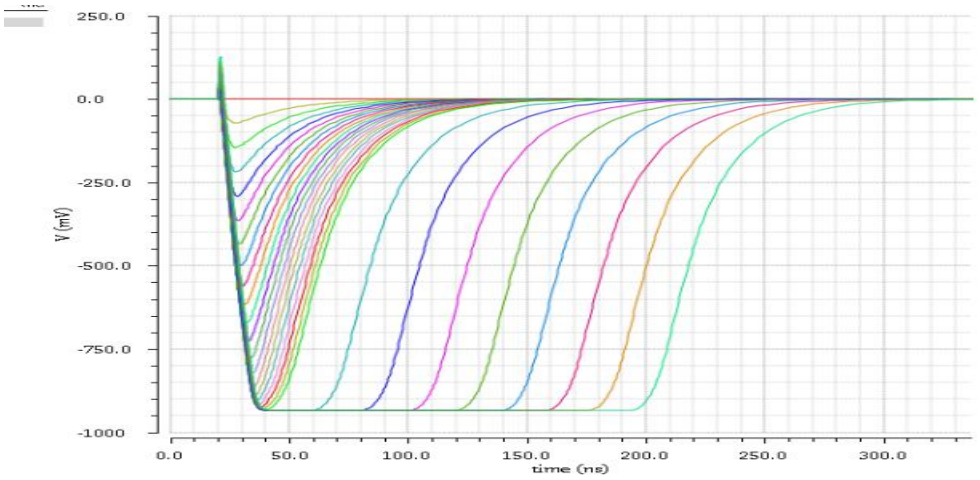
VFE architectural issues

- key issues to be studied :
  - Noise
  - Resolution
  - Stability
  - Linearity
  - Accuracy
  - Calibration
  - crosstalk
  - Radiation
  - Timing
  - Systematic effects



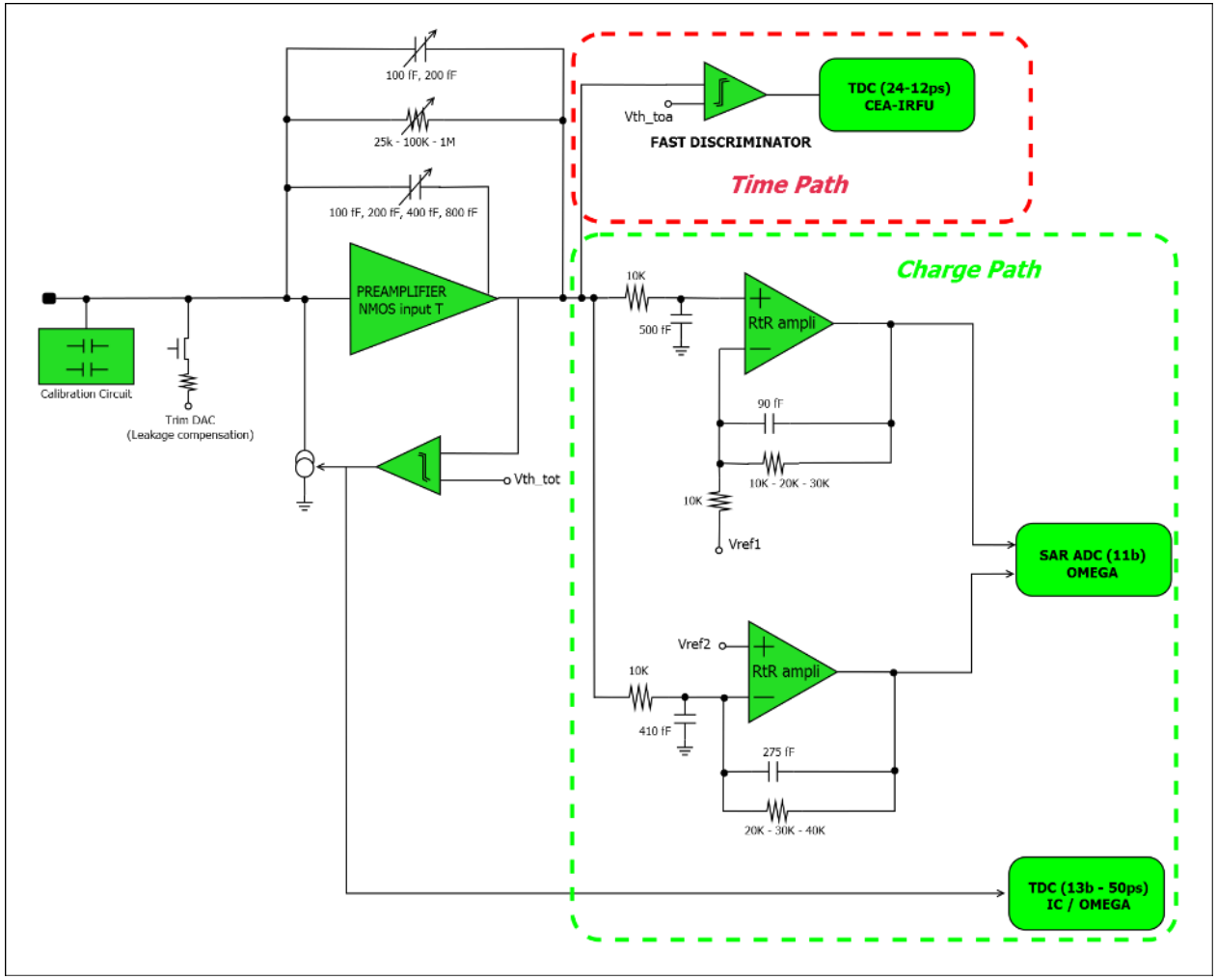
0.2 pC
~100 MIPS





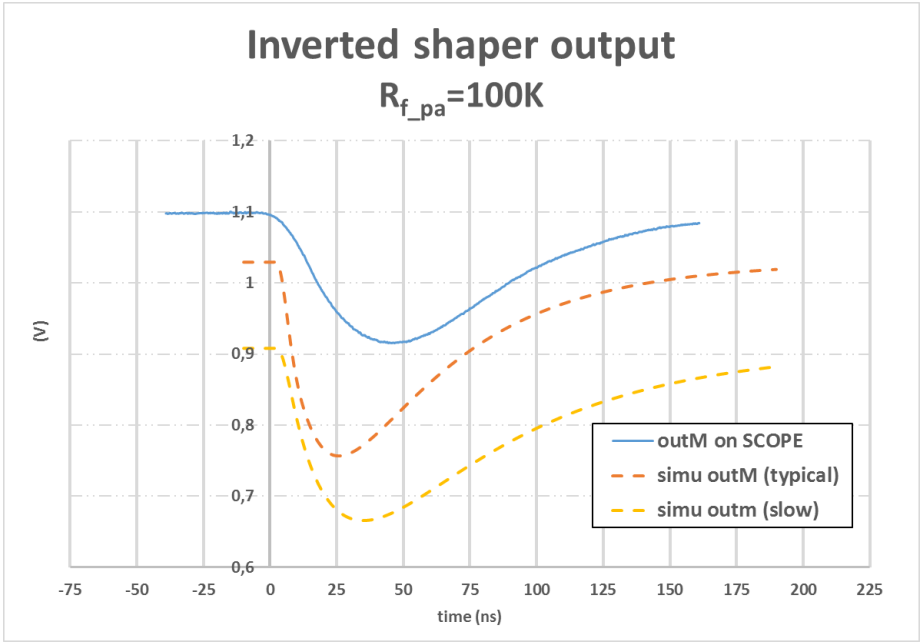
Analog and Mixed channel

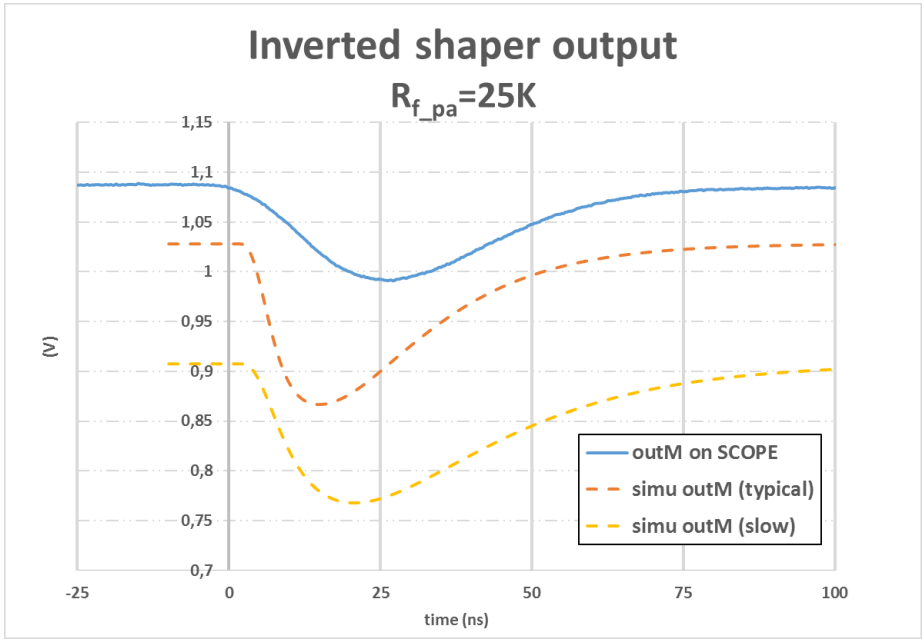
- Preamplifier gain adjustable on 4bit
- New shaper without SK
  - In a next version, with SK and tunable shaping time and gain
- Decay time given by R_{f_pa}
  - 25K
  - 100K
- New TOT architecture
  - Gain adjustable by SC
  - Undershoot ➔ dead time
  - In a next version, find a way to remove/reduce it (dynamic reset)
- New TOA fast discriminator
  - In a next version, higher preamp bias current and fast output to improve the time measurement
- Local 5bit DAC to adjust the Vrefs and the thresholds
- Local input current DAC to compensate the leakage
- Internal calibration circuit
  - Low range up to 600 fC
  - High range up to 12 pC

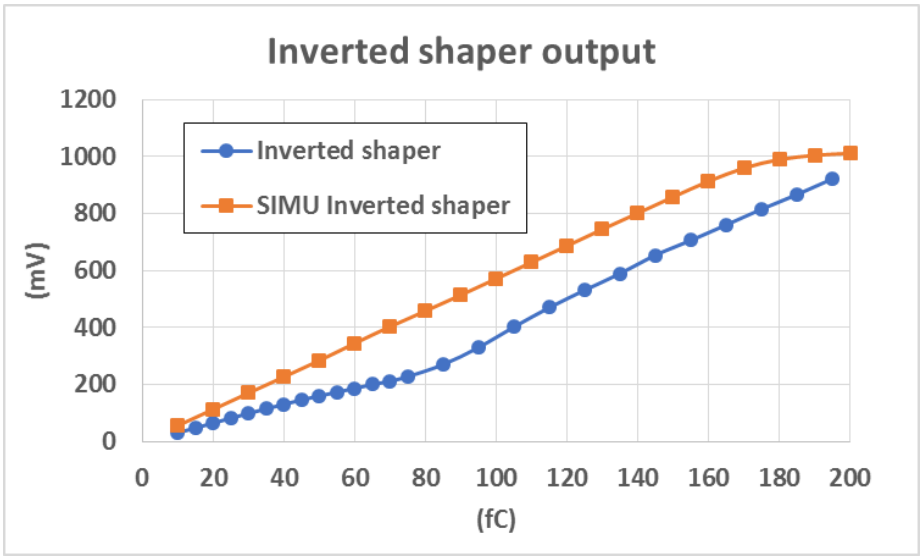


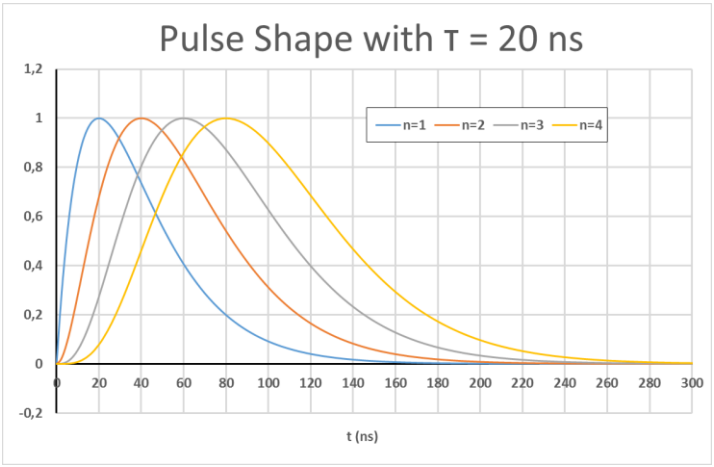
Power dissipation @ 1,5V supply
- Vdda (preamp): 1,6mA
- Vdd (tot): 160µA
- Vdd(shaper, toa): 1,1mA

Waveforms and linearity on scope

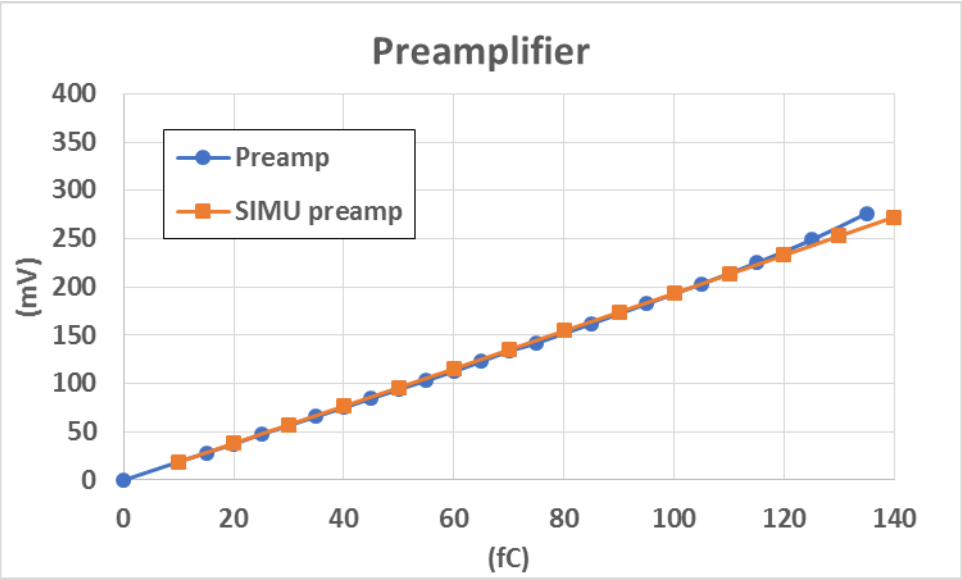


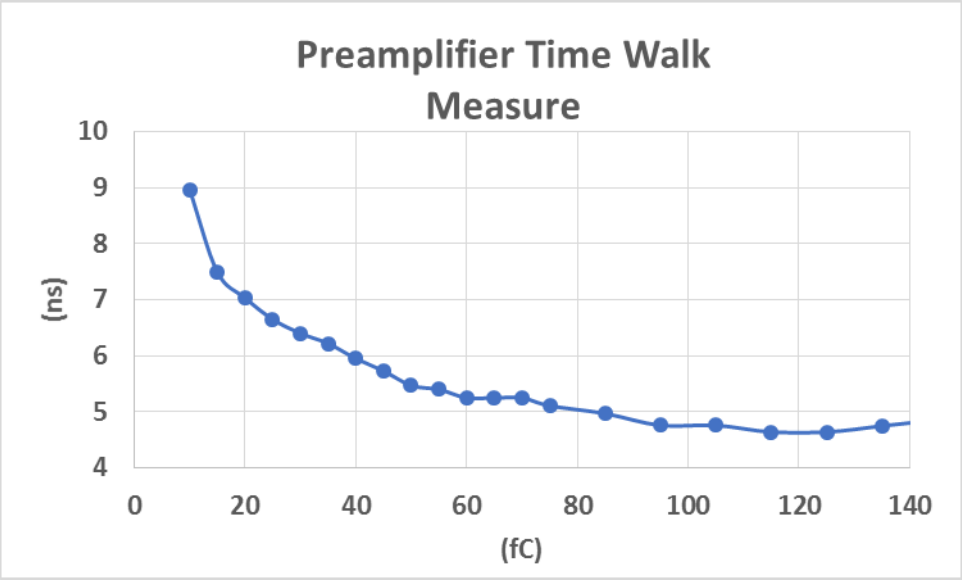




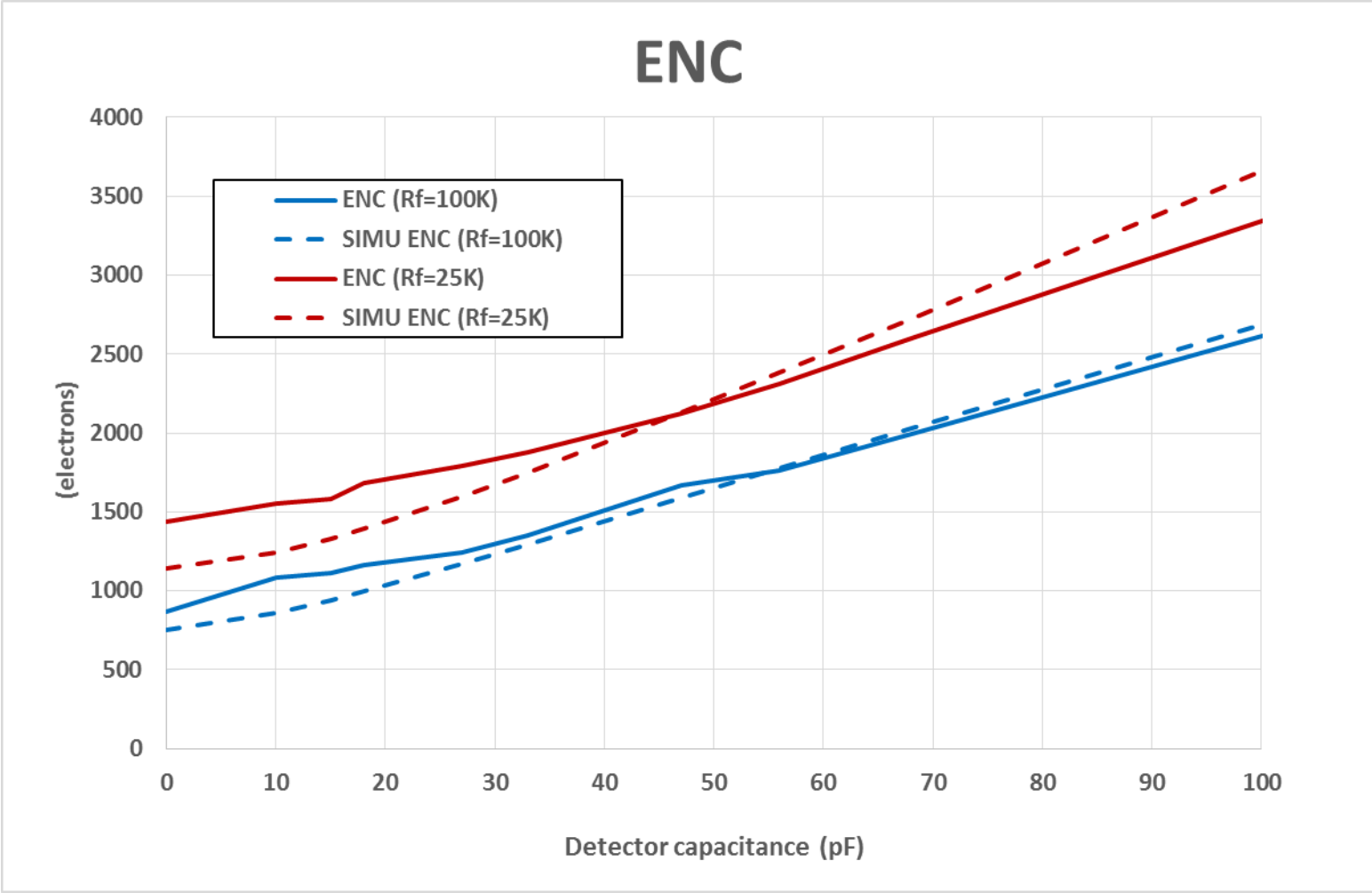


Preamplifier output



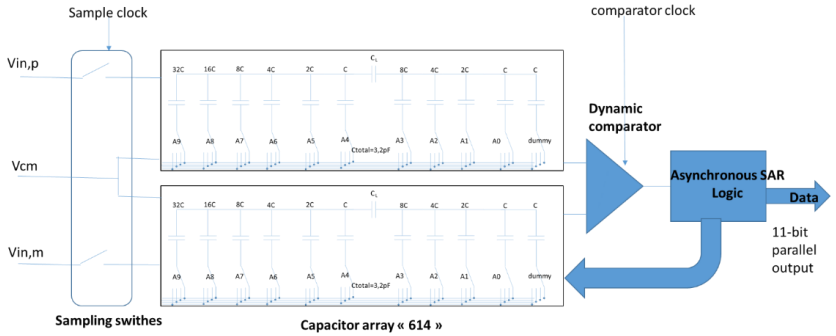


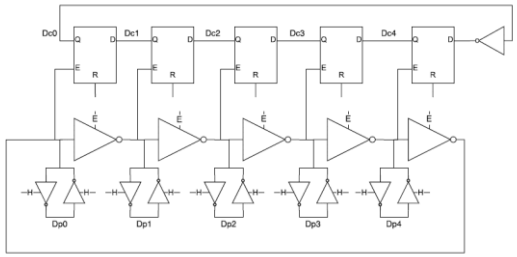
Equivalent Noise Charge

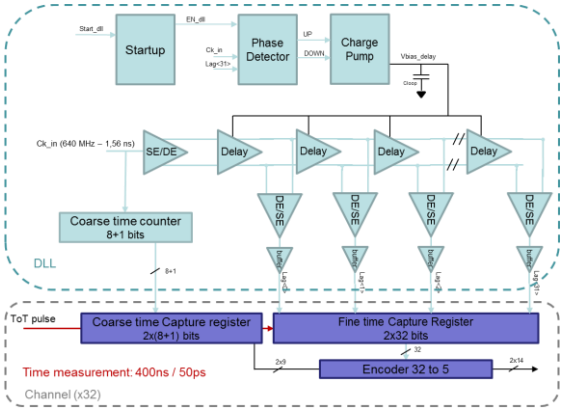


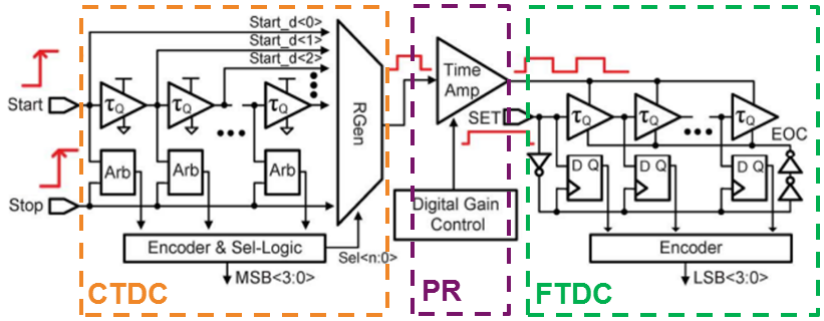
New mixed-signal circuits

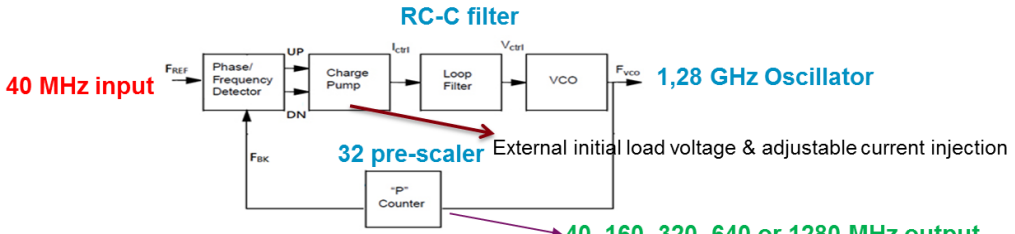
- ADC SAR
  - Inspired from Krakow design, 11 bit
- 2 TDCs for TOT
  - IC design, 50ps/200ns, based on a ring oscillator
  - OMEGA design, 50ps/400ns, based on a global DLL running at 640MHz
- TDC for TOA
  - CEA-IRFU design
  - 10/11 bit
- PLL
  - CEA-IRFU design
  - 40MHz input clock
  - 1,28GHz running frequency





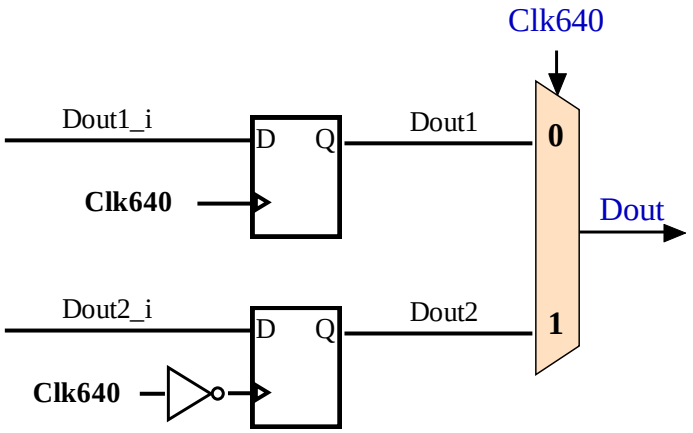






Serializer and Elink for trigger path

- The chip integrates 2 elink transmitter to handle the 64 bits from the trigger path
  - 4 channels are encoded into 8 bits (with 4+4 encoding)
  - 2 variants (fully digital or mixed ➔ way the last mux is done)
  - Possibility to readout a known frame (set by SC)
  - Default is 1,28 Gb/s (640 Mb/s possible)

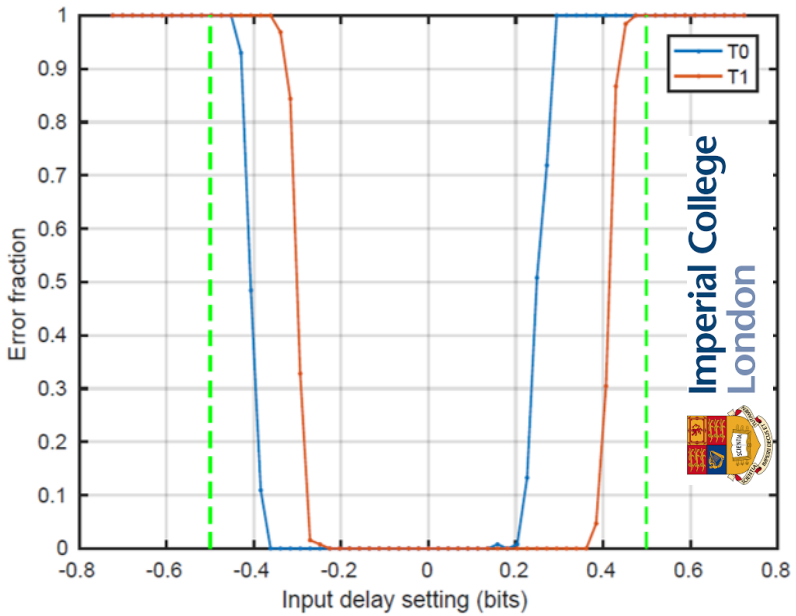


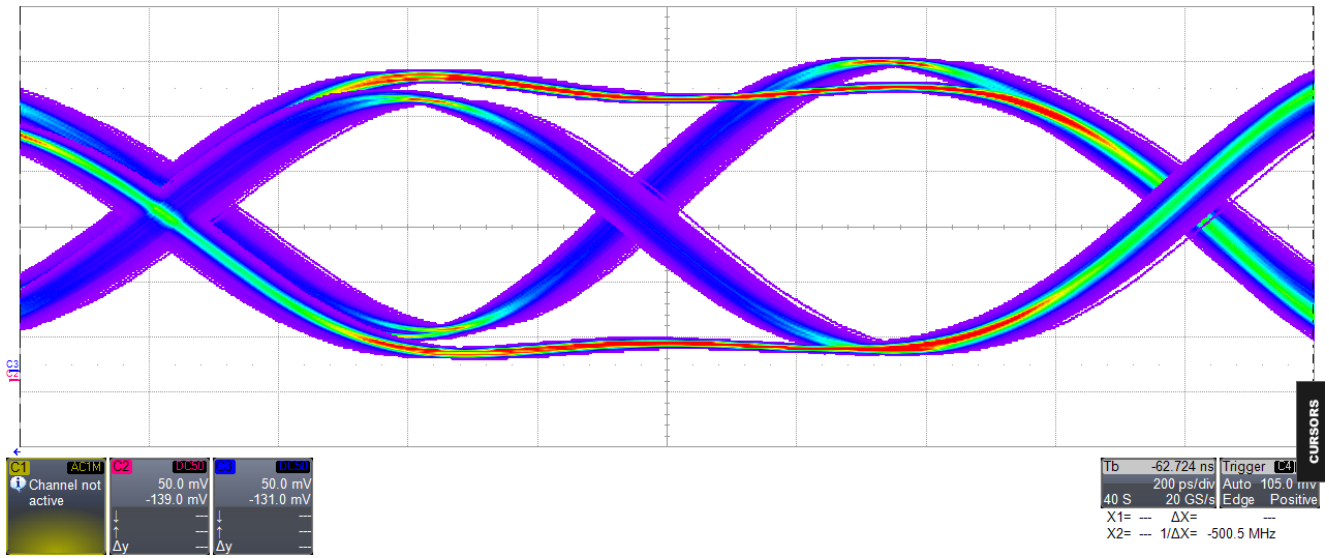
- Main specifications:
  - Data rate 1,28 Gb/s (internally 640M DDR)
  - Compatible with LpGBT protocol
  - Programmable Pre-emphasis (based on Paulo Moreira scheme)
  - Synchronization pattern on request (in place of trigger data)

Specification description	Value
Vcm (common voltage)	0,6 V
Vdiff (differential voltage)	100 to 200 mV
Pre-emphasis current	0,5 to 4 mA
Termination load	100 Ω

E-links

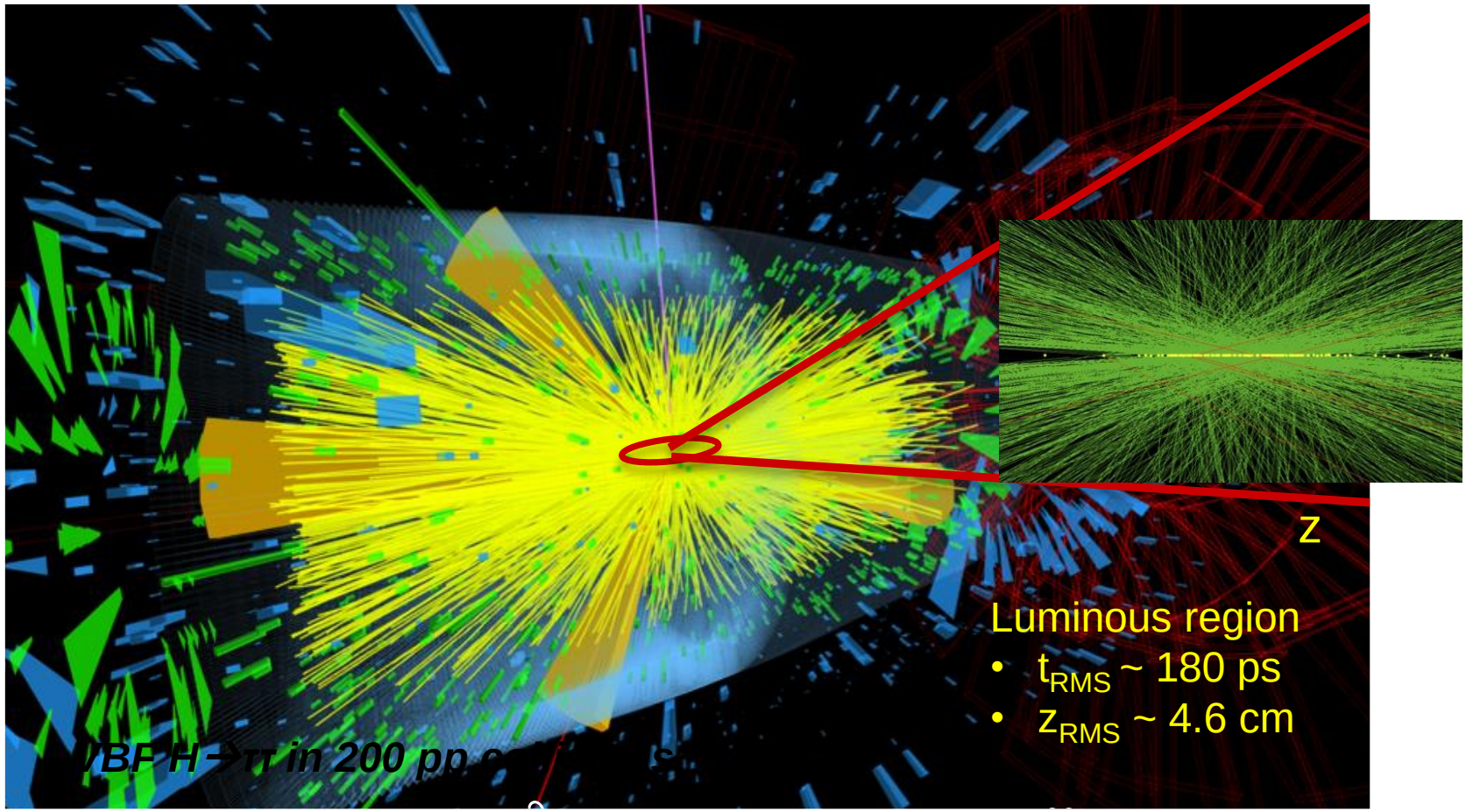
- Data path running at 320MHz
  - No difficulty to send out data from the SRAM
- Trigger path running at 1,28GHz
  - For now, I only look at the eye diagram and Johan provides the plot of error rate vs sampling delay





Timing at High-Luminosity LHC

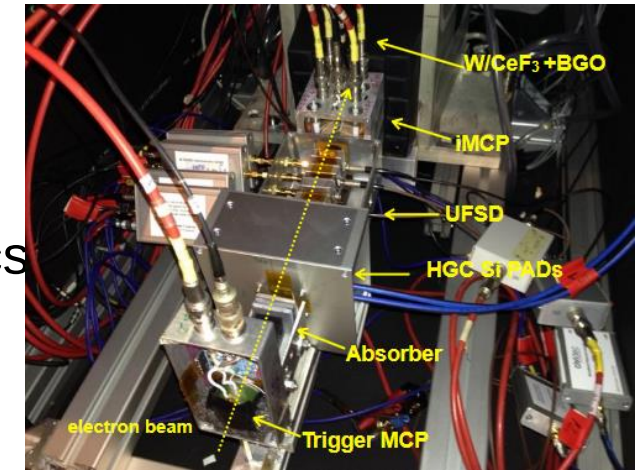
- Pileup mitigation with fine time information (~25 ps)

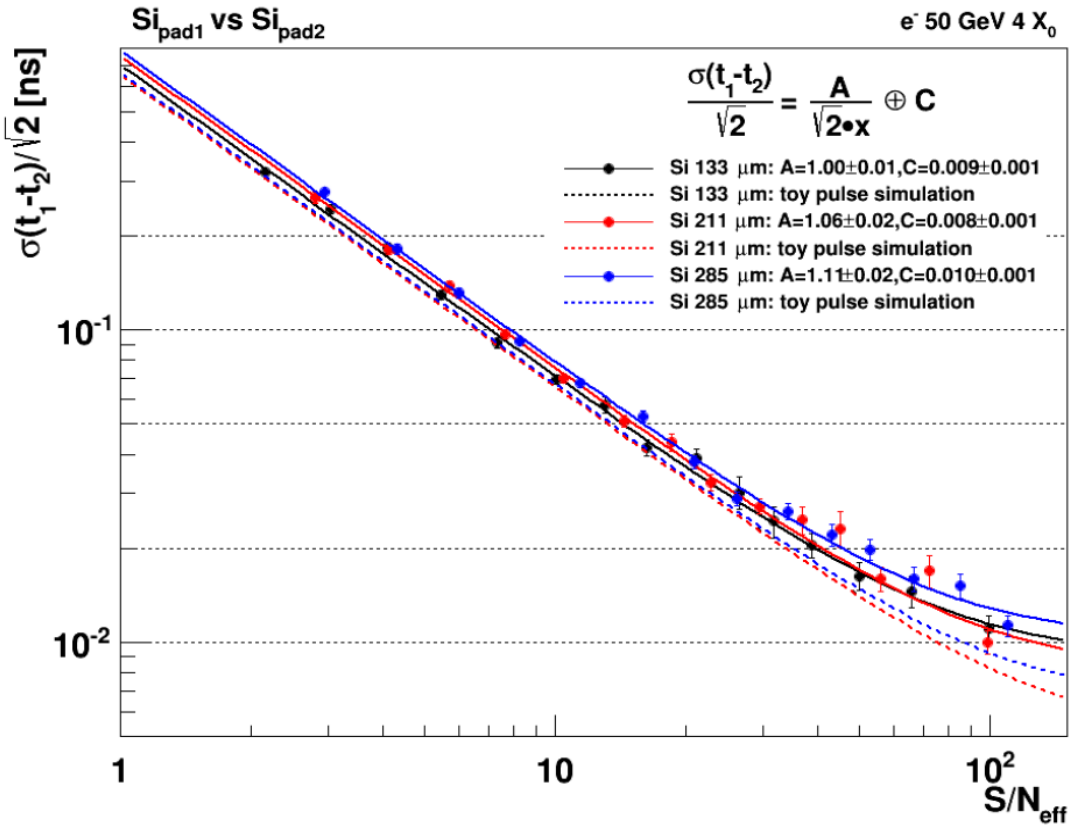


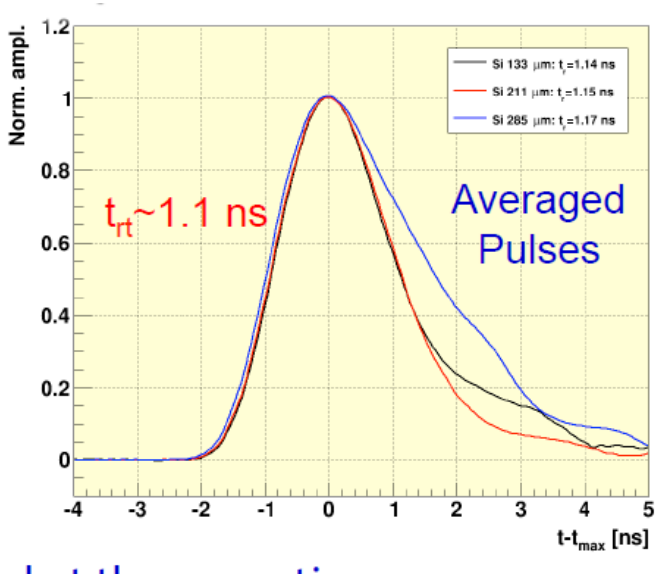
© G. tully CERN seminar on timing
/https://indico.cern.ch/event/633341/

HGCAL timing performance

- CMS HGCAL testbeam measurements
- Jitter : j ~1 ns / S/N
  - But S and N depend on BW…
  - Parts come from detector and from electronics



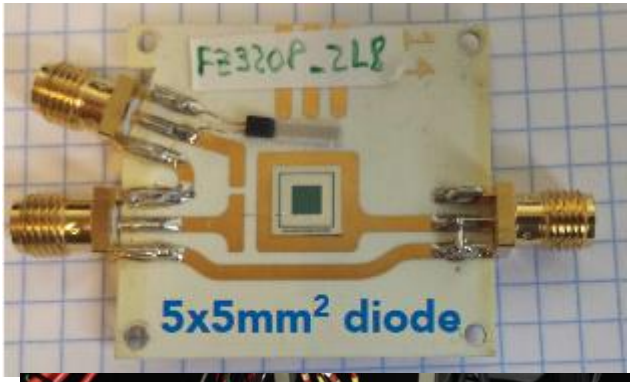


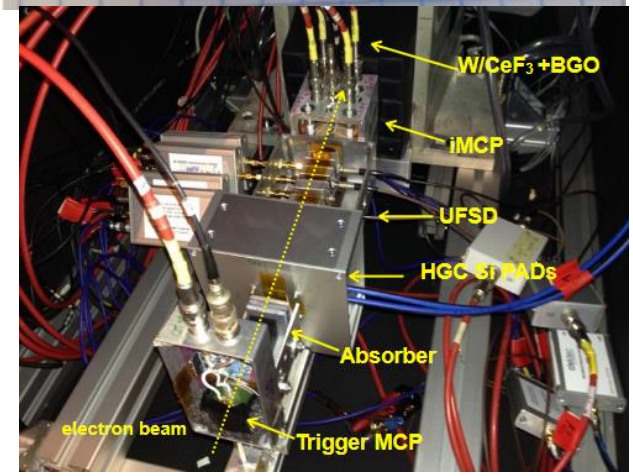


© *M. Mannelli et al. ACES 2016*
https://indico.cern.ch/event/468486

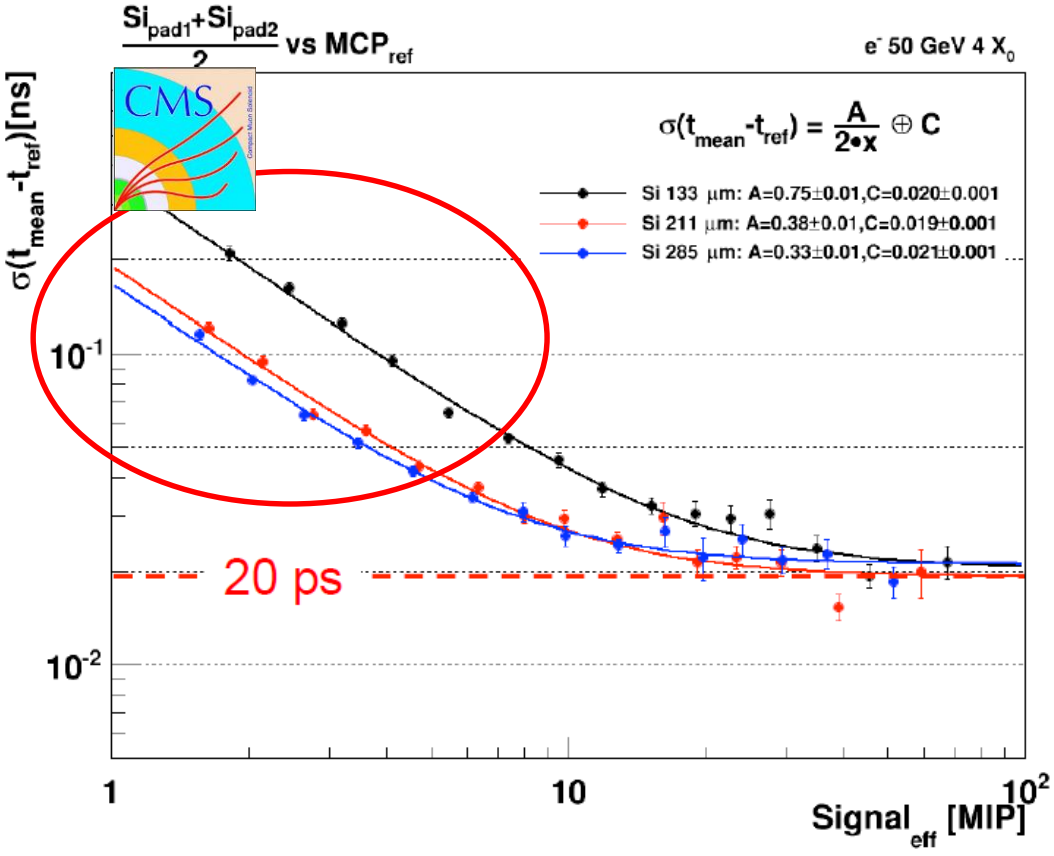
Results : CMS pin diodes caracterization

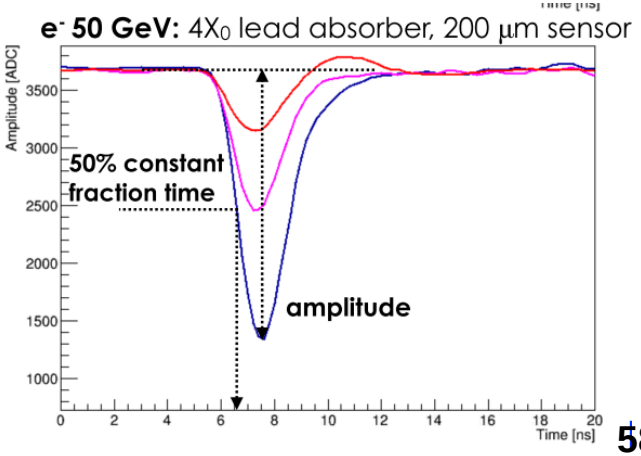
- Measured jitter In testbeam [A. Martelli et al.] :
  - jitter ~ 1 ns/Q(fC) (+) 20 ps





Timing Resolution (Mean Silicon - MCP) *vs* Mean Sensor Effective Signal



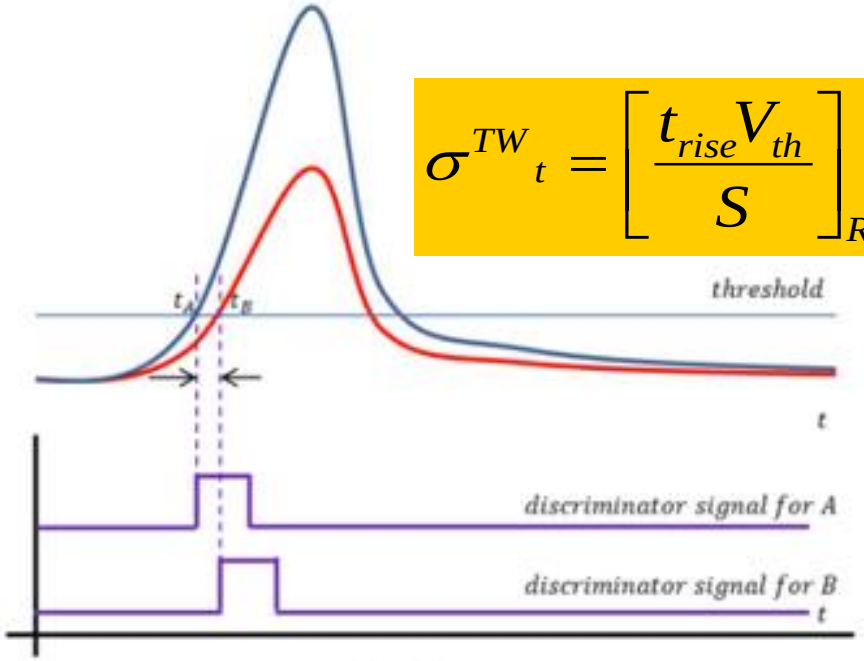


Time walk and Time jitter

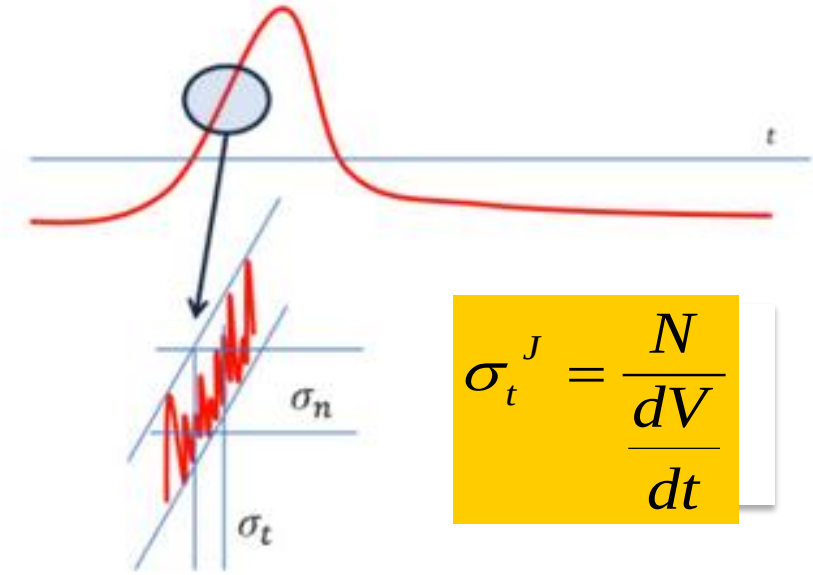
Time walk: the voltage value Vo is reached at different time for signal of different

Jitter: the noise is summed to the signal, causing amplitude variations

$$\sigma^{TW}{}_t = \left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}$$



Time walk effect



$$\sigma_t{}^J = \frac{N}{\frac{dV}{dt}}$$

Jitter effect

Due to the physics of signal formation

Mostly due to electronic noise

$$\sigma_t{}^2 = \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2$$

Jitter

Time Walk

TDC

© N. Cartiglia Trento workshop 2016
https://indico.cern.ch/event/485239/overview/

Examples

$$\sigma_t^{\ J} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

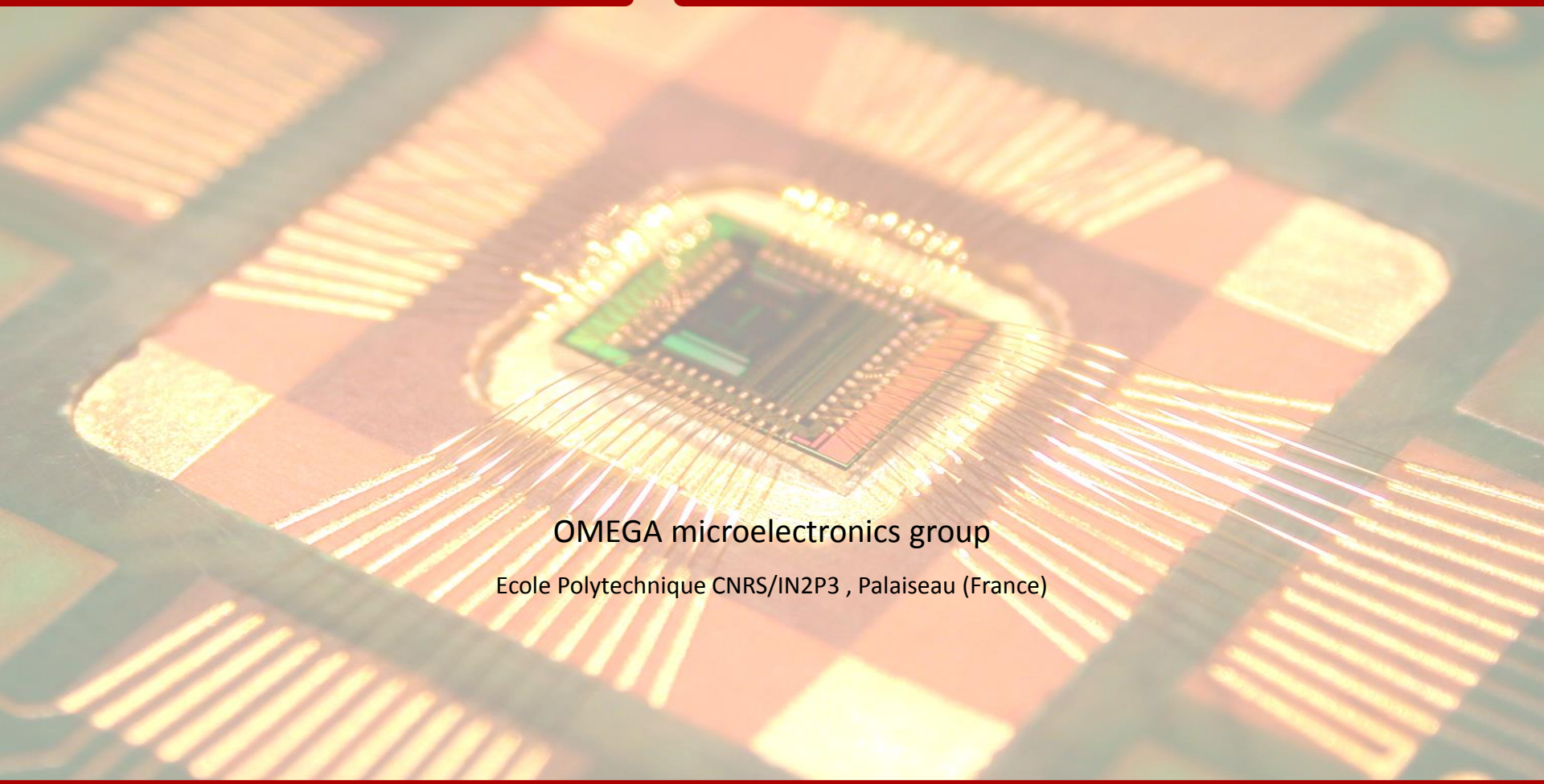
- CMS HGCAL : PIN diode thickness 300 µm A=25 mm²
  - C_d = 8 pF e_n = 1 nV/√Hz t_d = 3 ns σ = 420 ps/Q(fC)
  - 1 MIP = 3.8 fC => σ = 110 ps/#MIP (~200 ps measured)
- NA62 tracker : PIN diode thickness 300 µm A=0.09 mm²
  - C_d = 0.1 pF e_n = 11 nV/√Hz t_d = 3 ns σ = 60 ps/Q(fC)
  - 1 MIP = 3 fC => σ = 20 ps/#MIP (~60 ps measured)
- ATLAS HGTD : LGAD diode thickness 50 µm A= 2 mm² G = 10
  - C_d = 2 pF e_n = 2 nV/√Hz t_d = 0.5 ns σ = 50 ps/Q(fC)
  - 1 MIP = 5 fC (G=10) => σ = 10 ps/#MIP (~30 ps measured)
- SiPM G = 1^E6
  - C_d = 300 pF e_n = 1 nV/√Hz t_d = 100 ps σ = 3 ns/Q(fC)
  - 1 pe = 160 fC => σ = 20 ps/#pe (~60 ps measured)

Summary

- OMEGA has long history in FEE design
  - Started with ILC/Calice now lead by CMS/HGCAL
- Imaging calorimeters ramping up !
  - Require highly integrated R/O electronics : System On Chip
  - Low power, low noise, high speed, large dynamic range
  - Timing capability down to a few tens of ps
  - Lots of system issues
  - CepC requirements for FEE are similar to CMS HGCAL specs
- Timing performance dominated by sensor characteristics
  - Capacitance, duration, MIP charge
- Work getting organized towards 10 ps (1 ps ?) timing

OMEGA ILC chip

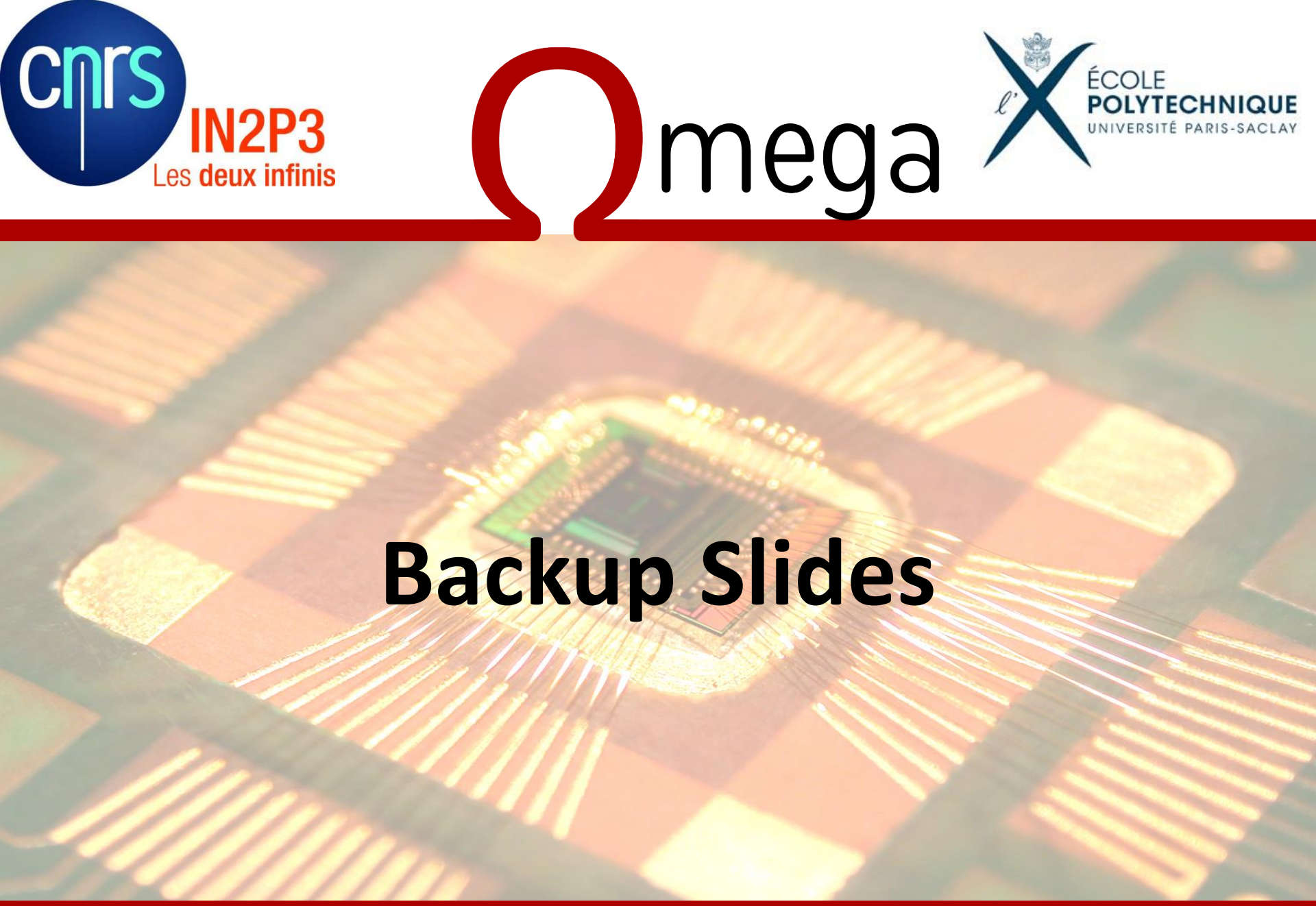
Omega



OMEGA microelectronics group

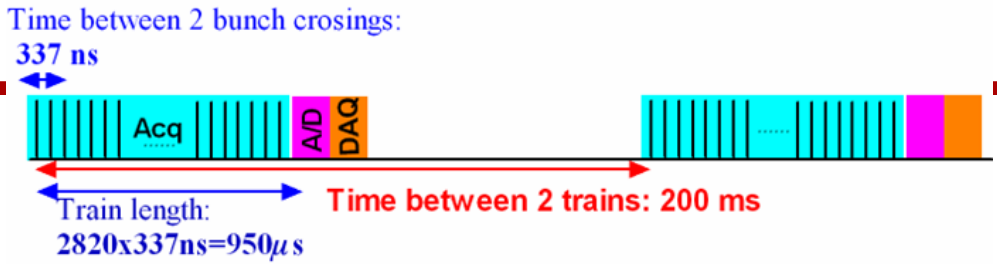
Ecole Polytechnique CNRS/IN2P3 , Palaiseau (France)

Organization for Micro-Electronics desiGn and Applications

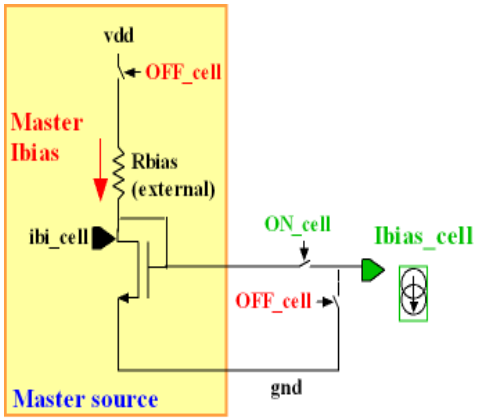


Organization for Micro-Electronics desiGn and Applications

POWER PULSING in SK2



- **Requirement:**
  - **25 µW/ch with 0.5% duty cycle**
  - **500 µA for the entire chip**



- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**
- **SK2 power consumption measurement:**
  - 123 mA x 3.3V ≈ 40 mW => **0.6 mW/ch**

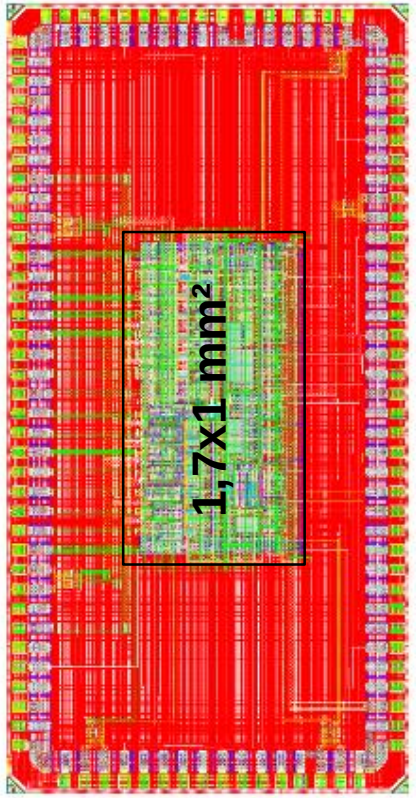
- **4 Power pulsing lines** : analog, conversion, dac, digital
- Each chip can be forced **on/off by slow control**

Measurements		
Acquisition	88 mA , 290 mW	Duty Cycle =0.5%, 1.45 mW
Conversion	27.3 mA, 90 mW	Duty Cycle =0.25%, 0.225 mW
Readout	8.0 mA, 26.4 mW	Duty Cycle =0.25%, 0.066 mW

Skiroc2 power consumption with Power pulsing: 1.7 mW ie 27 µW/ch

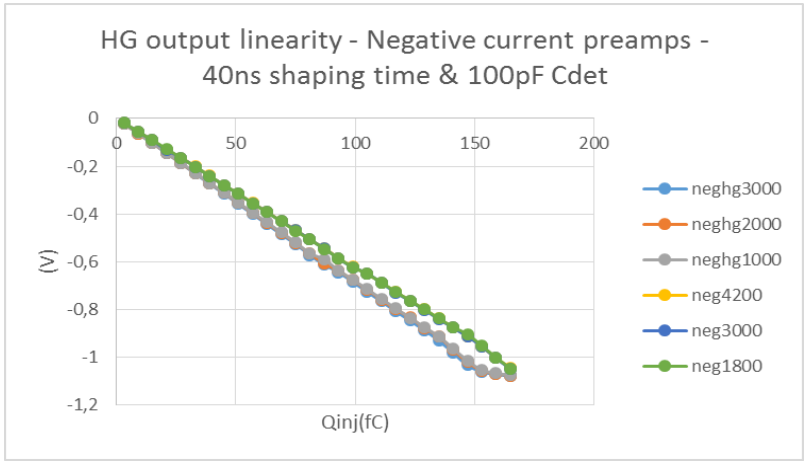
1st test vehicle: TV1

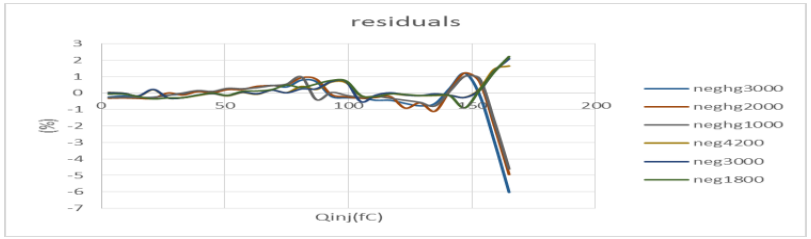
- Analog blocks for preamp characterization:
  - 6 positive & 6 negative input preamps
    - Use different transistor size ant type (lvt, typ, hvt)
    - 60dB and 90 dB OL gain architecture
    - Variable Rf and Cf: charge sensitive or current sensitive
    - CRRC shapers: HG and LG, 5 to 75 ns shaping time, => noise studies
  - 1 baseline channel from TP (CERN schematic)
  - 4 discriminators for TOT studies
  - Digital part for noise coupling tests



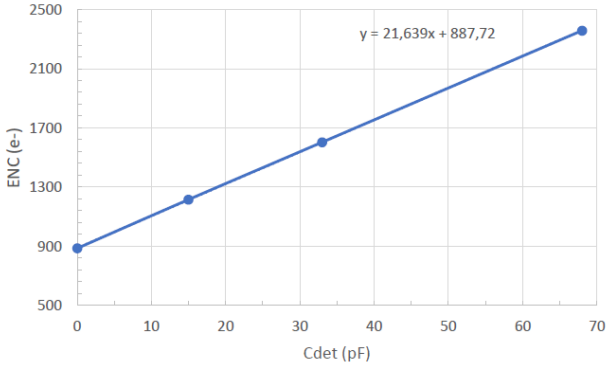
TV1 test results

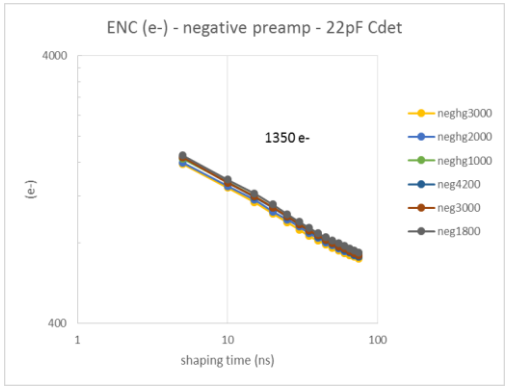
- "90dB" preamps, for both polarities, achieve the best performances in terms of open loop gain, linearity, speed and noise
- Issues found
  - Large parasitic capacitance (Cpa = 40pF)
  - Stability issues with R2R shapers
  - Poor modelization of Crtmom capacitors

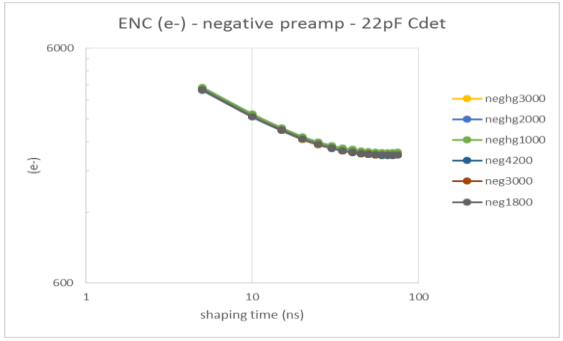




ENC noise vs detector capacitance

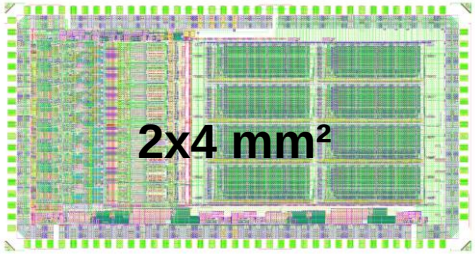


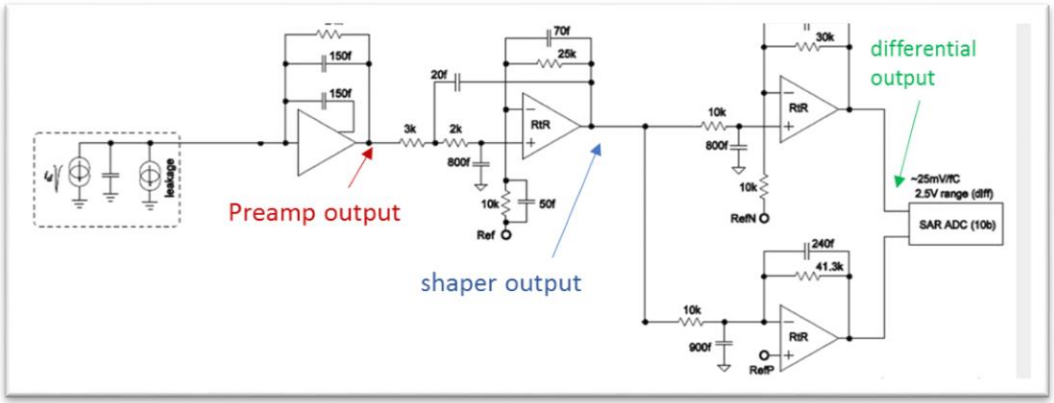




2nd test vehicle: TV2

- Negative input preamp
  - High OL gain (90dB)
  - Variable Cf: 0,1fF – 1,5pF
  - Two selectable Rf: 24K & 1M
  - Cf_comp for high gain setting
  - Different versions: baseline, low parasitics cap (custom layout)
- Baseline shapers
  - Tunable bias
  - Tunable miller comp
  - Global 10b DAC and 5b DAC in order to tune the Reference voltages
- 11b 40 MHz SAR ADC based on Krakow design
- ToT: No TDC but discri output on a PAD
- ToA: not implemented (high speed TDC still not available)
- 32x512 SRAM (CERN)



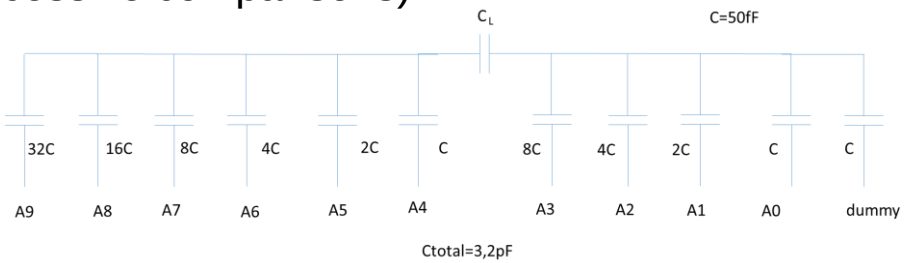


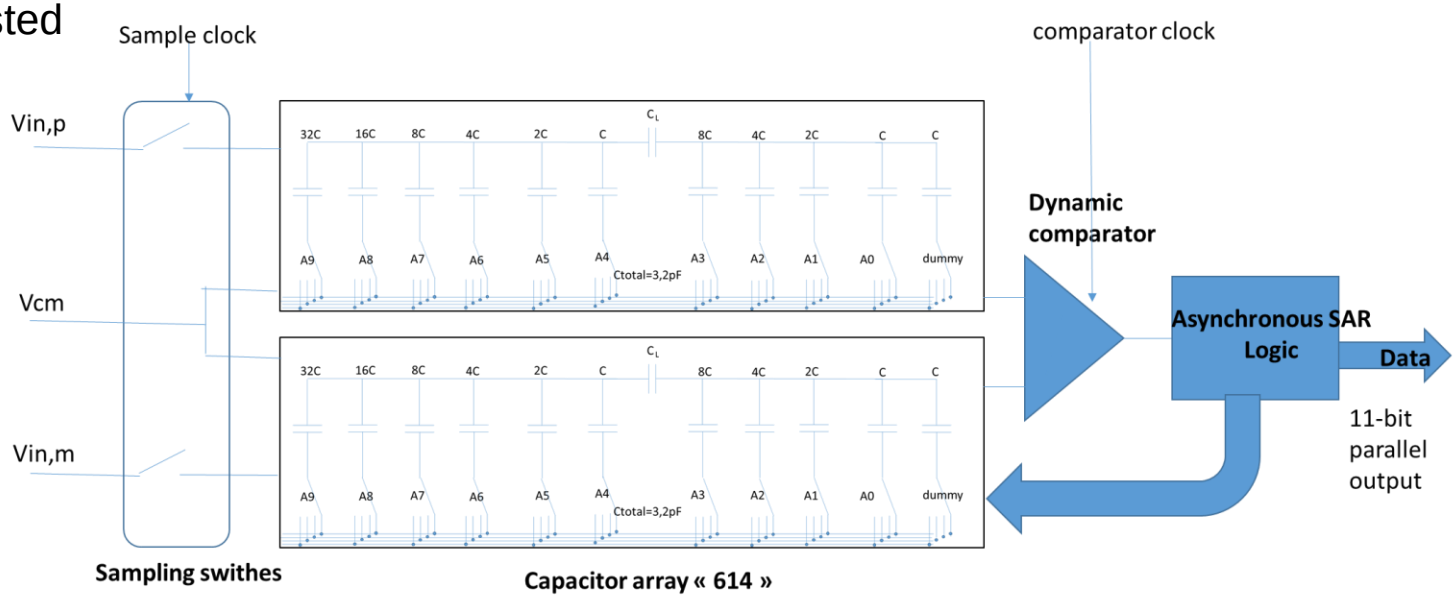
Different versions:

- Preamp: baseline, low parasitics cap (custom layout)
- 11b ADC: asynchronous and synchronous ADC, with and without bootstrap

TV2: ADC SAR

- 11-bit ADC SAR (MSB signal sign + 10 successive comparisons)
- Designed for 20 MSamples/second
- Design of 11-bit SAR ADC
  - Differential input signal
  - Based on a capacitive DAC architecture (« 614 » :Split 6b/4b DAC)
  - Based on a asynchronous SAR logic and tunable settling delay
- Power consumption ~3mW @ 20MHz (~50% capa array;~50% digital)
- 4 ADC SAR architectures in TV2 (w and w/o bootstrap; asynchronous/synchronous) to be tested





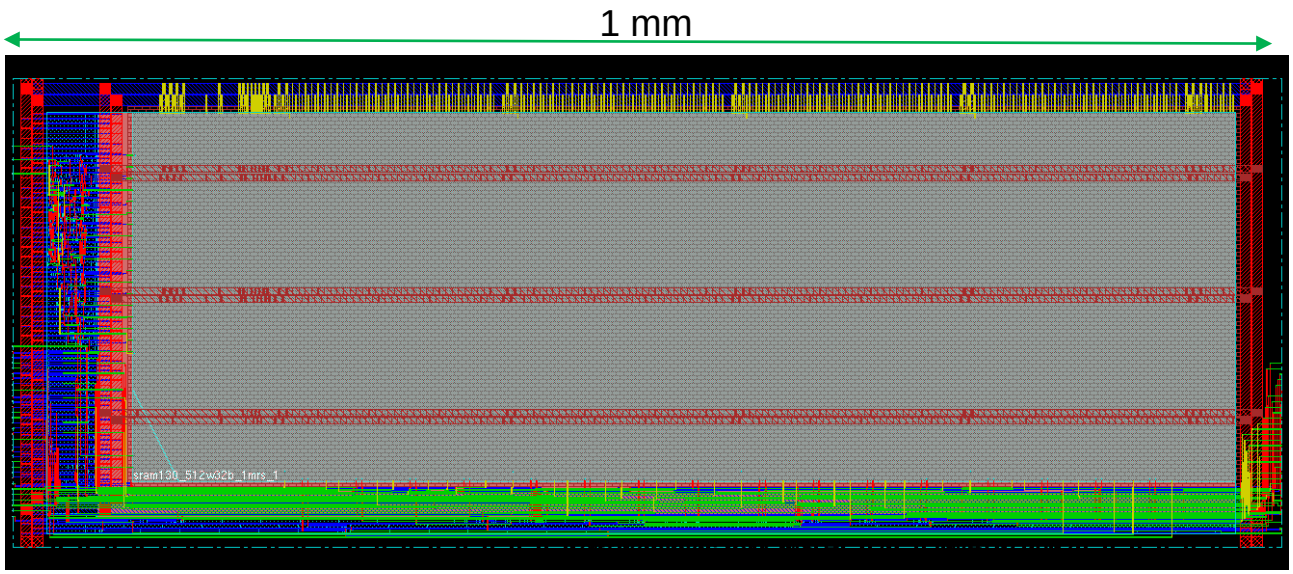
TV2: L1 Buffer SRAM

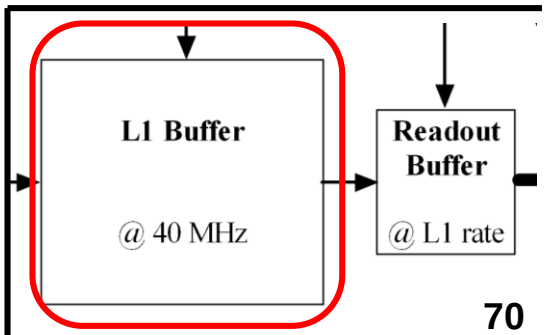
- L1 Buffer in TV2 (TSMC 130 nm):
  - 512w x 32 bits
  - Use CERN memory generator (beta version)
  - 1 buffer / channel (in TV2)

	Area mm²	Power mW / ch	Processing Time (ns)
RAM 32b x 512w	0,35	**~ 4**	R @ 1 MHz W @ 40 MHz

	energy READ*	energy WRITE*	energy R&W*	energy NOP	leakage
	uW/MHz	uW/MHz	uW/MHz	uW/MHz	uW
WC	51.2	71.3	130.0	20.2	30.55
TC	65.7	85.6	148.4	16.1	3.75
BC	86.5	108.2	179.9	24.9	5.06
TL	70.5	93.3	161.9	24.7	90.53
LT	81.5	105.5	187.4	32.6	1.82
ML	98.9	128.4	223.1	33.6	283.22

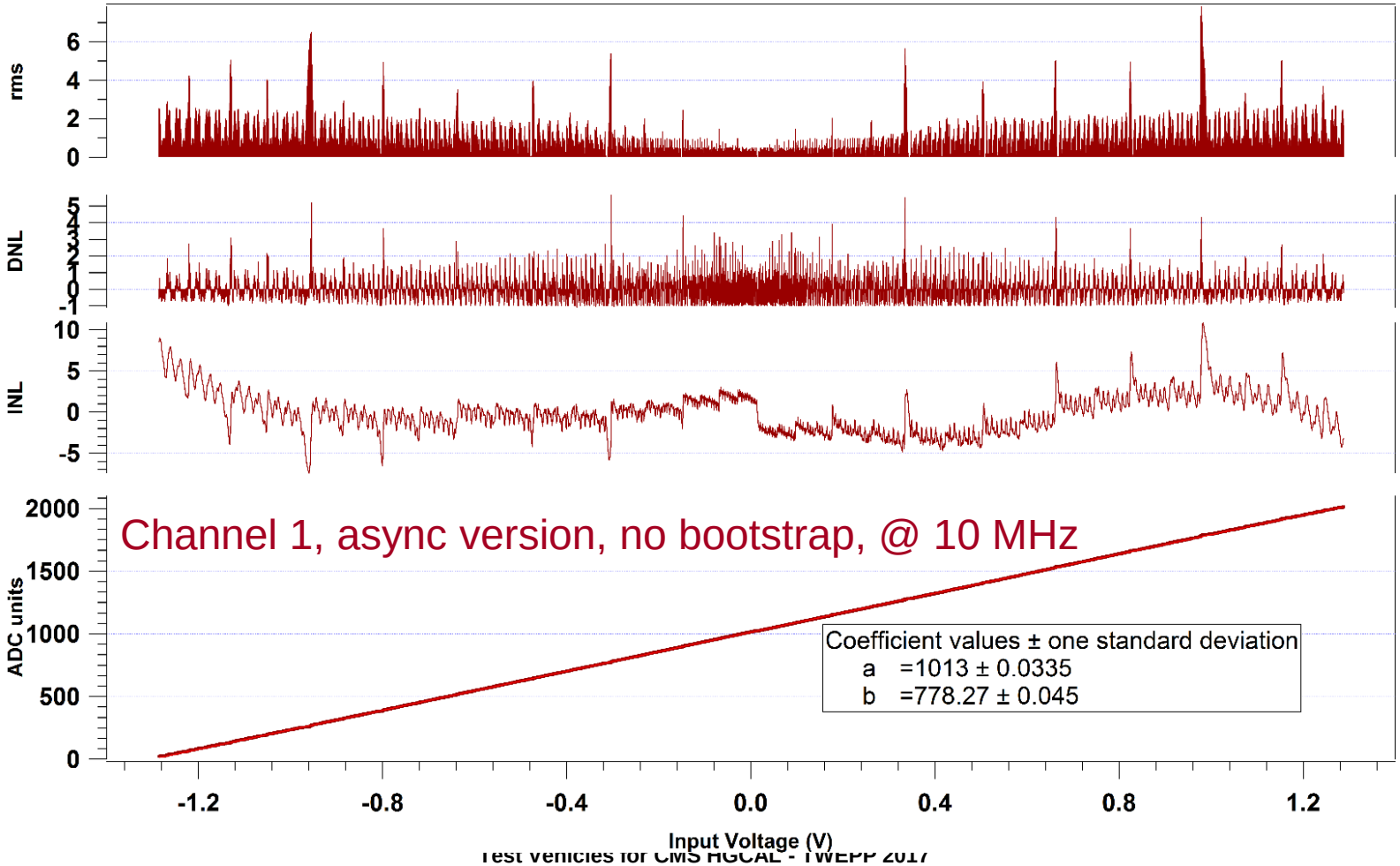
Measured 3mW/SRAM with only 12bits toggling (data toggling @10MHz, writing @40MHz, reading @1MHz) is in agreement with expectations





TV2: SAR ADC tests

- Maximum sampling frequency: 10MHz
- DC characterization: INL, DNL, capa network, noise
- Many parameters to be explored: delay, reference voltages,
- Just starting: lots of work ahead (SINAD, ENOB, SNR …)

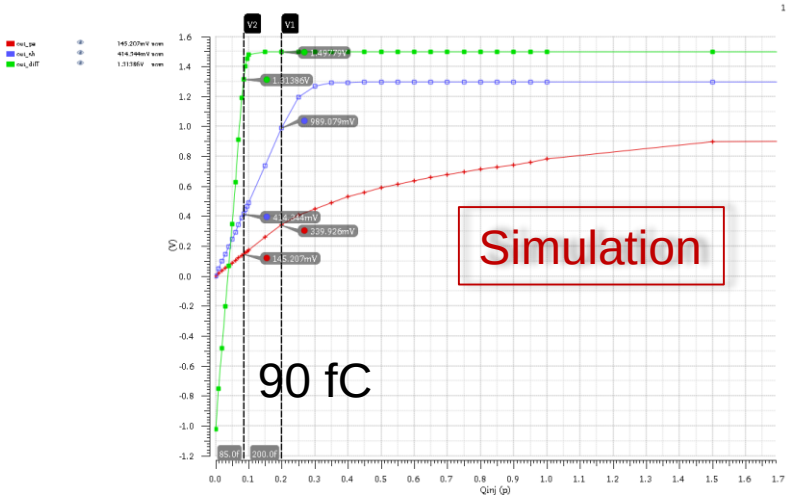


Preliminary

TV2: Charge linearity

Good agreement between simulation and measurement

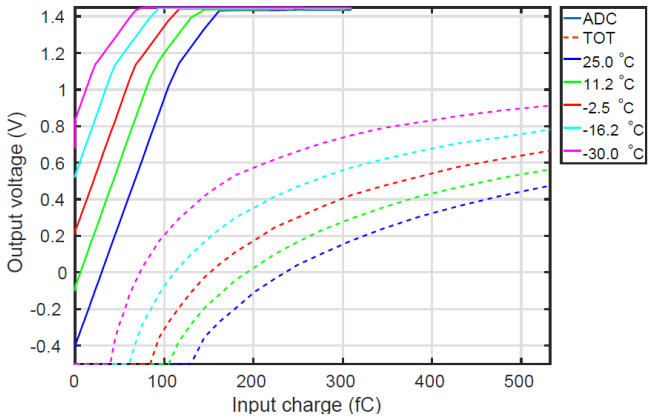
- Linear up to 90fC
- But ADC brings a non linearity, likely due to mismatches of its capa network (half range)

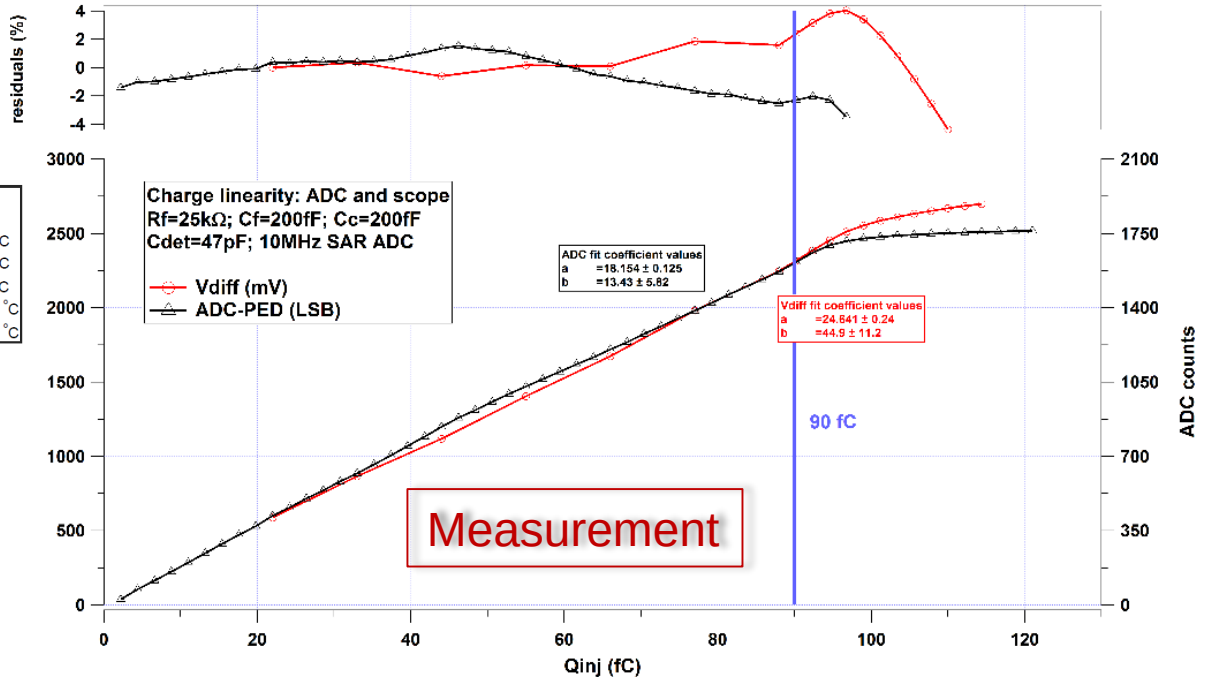


- Strong DC dependency to the Temp
  - DC coupled channel, gain 15
  - Input preamp 1mV/°C

  ⇒ 15 mV/°C at the ADC

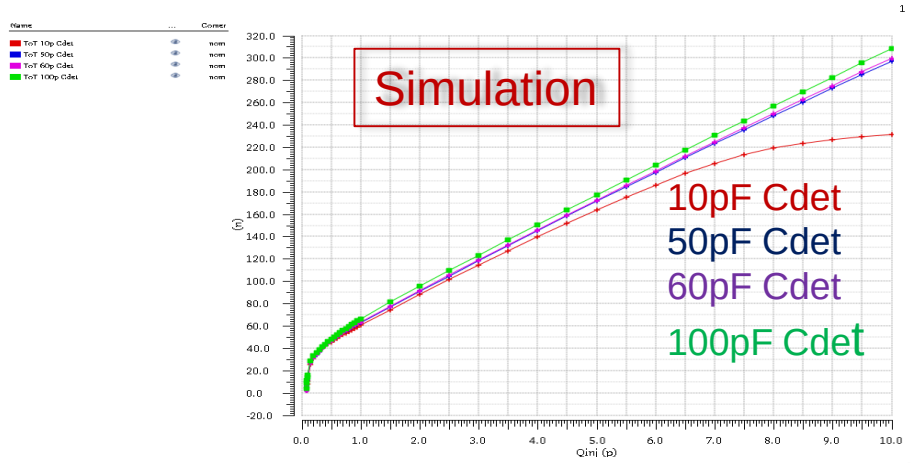
  ⇒ See in room condition

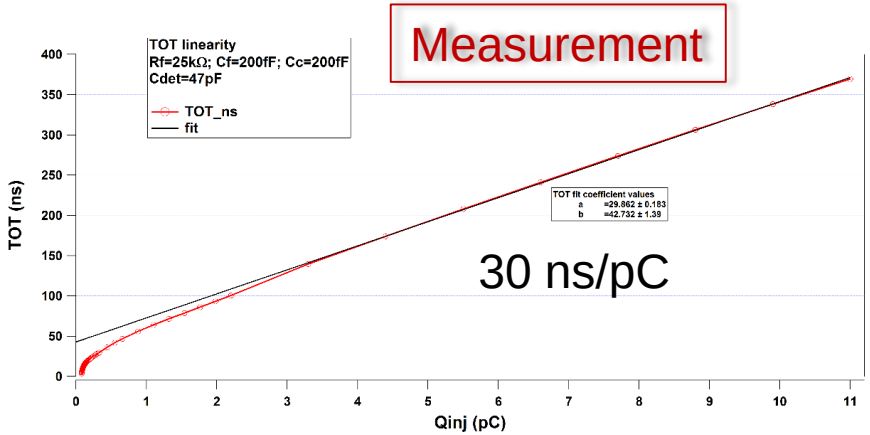


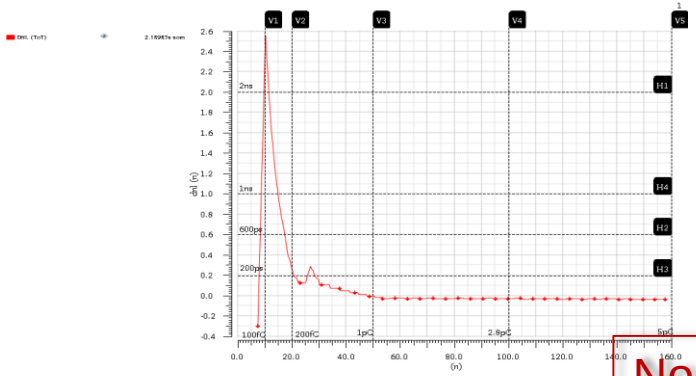


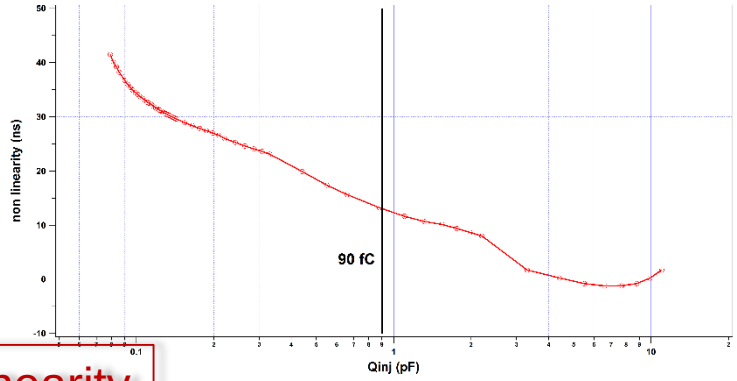
TV2: TOT linearity

Good performance of TOT but after 3pC, 1pC in simulation => have to be understand









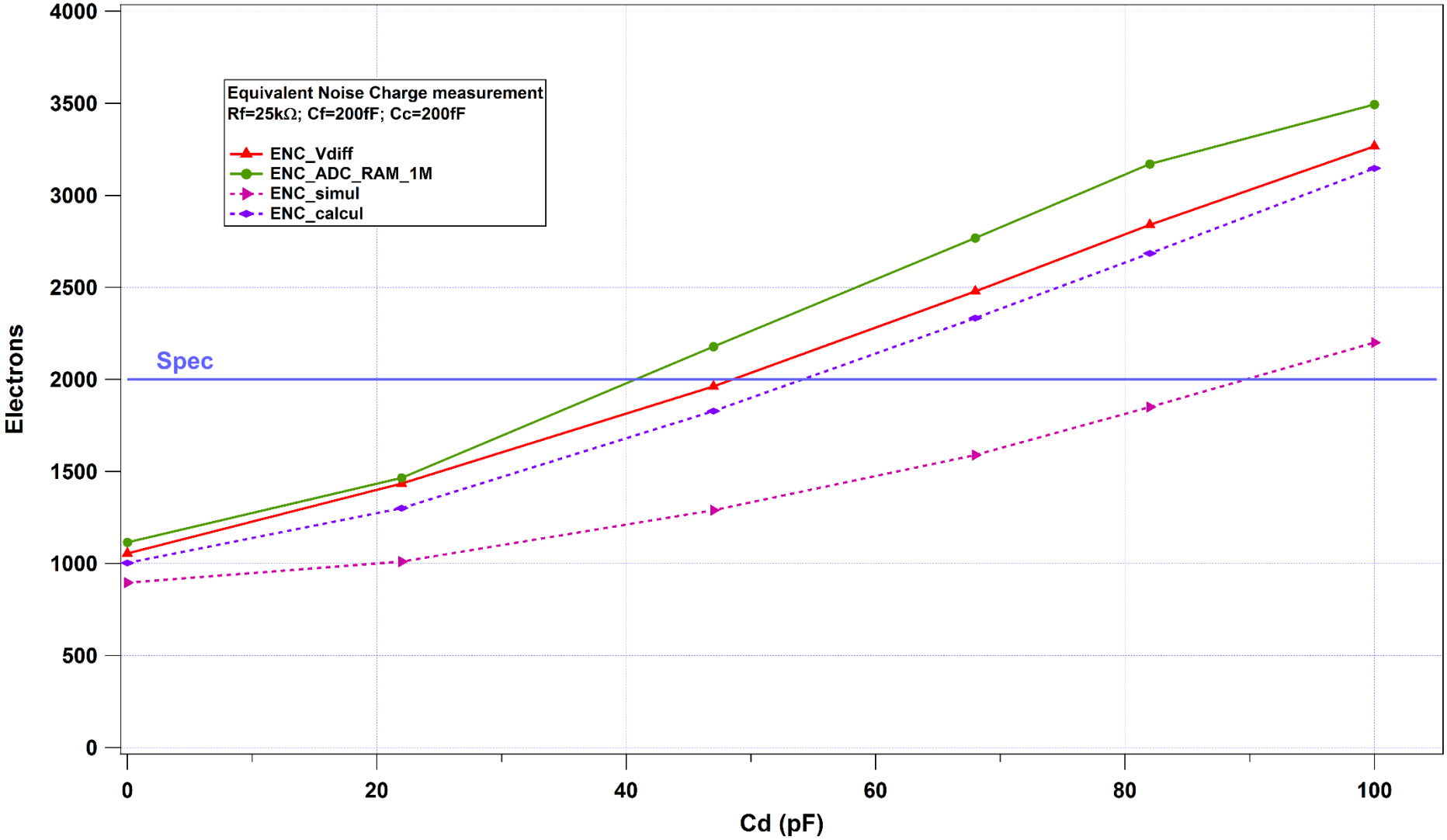
Non linearity

Jitter on TOT

- Spec < 50ps
- @ 200 fC 30ps simulated, 75ps measured

TV2: Noise measurements

- Spec 2000 electrons with 50pF detector capacitance
- OK without ADC and running RAM
- Discrepancy between simulated and theoretical/measured values



Timing optimization : common view

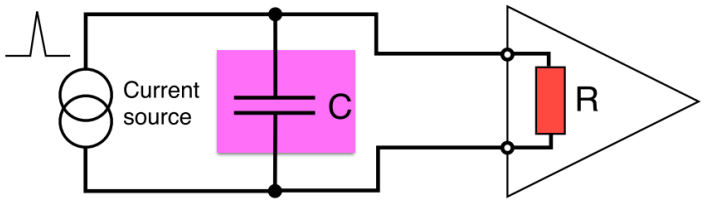
- Jitter due to electronics noise:

$$\sigma_t^J = \frac{N}{\frac{dV}{dt}}$$

- also presented as j = tr / (S/N)
- dV/dt prop to BW, N prop to √ BW => jitter prop to 1/√BW

⇒ « the faster the amplifier the better the jitter ? »

⇒ « High speed preamps need to be low impedance (50 Ω or less) »



NB : tr = $t_{10\text{-}90\%}$ = 2.2 tau.

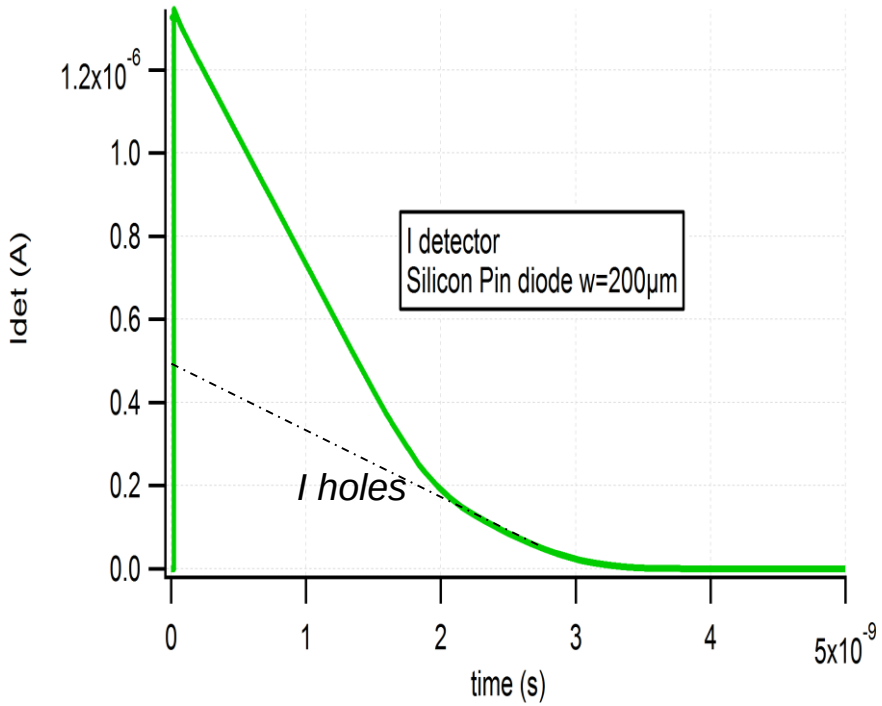
f_{-3dB} = 1/2πtau = 0. 35 / $t_{10\text{-}90}$

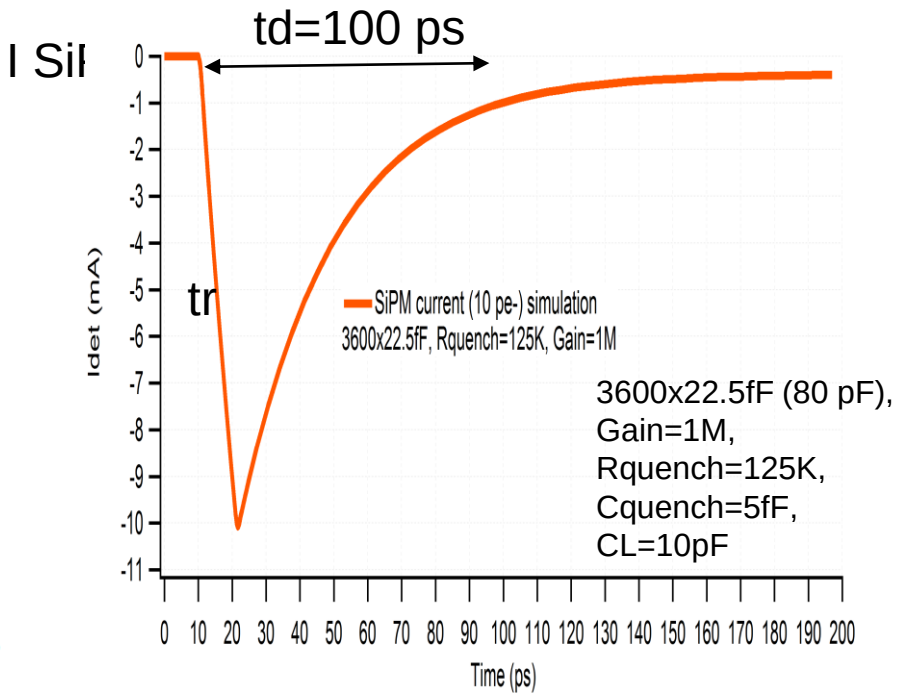
f_{-3dB} = 1 GHz <-> $t_{10\text{-}90\%}$ = 300 ps

Signal : detector current

- PN diode w =200µm
- Very short rise time : tr~10ps
- Relatively long «drift time» : td~2ns

- SiPM detector (10pe-)
- very short rise time : tr~10 ps
- Short duration : td~100ps),

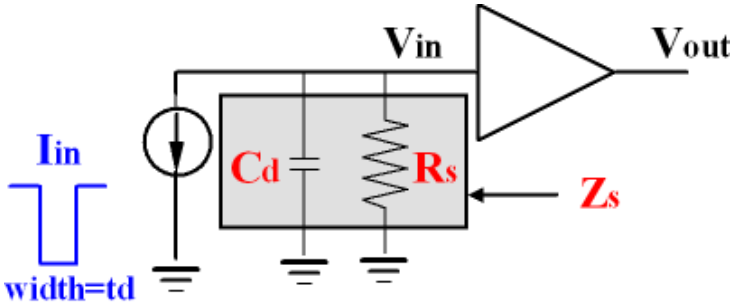


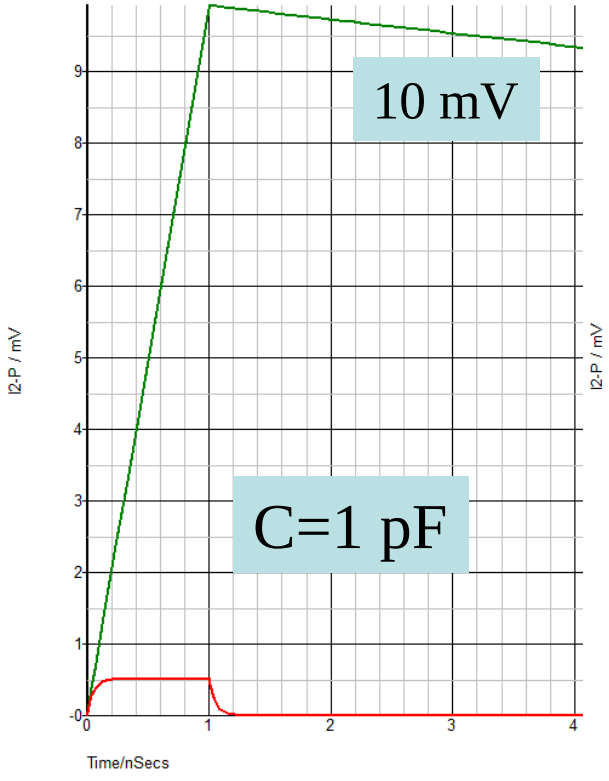


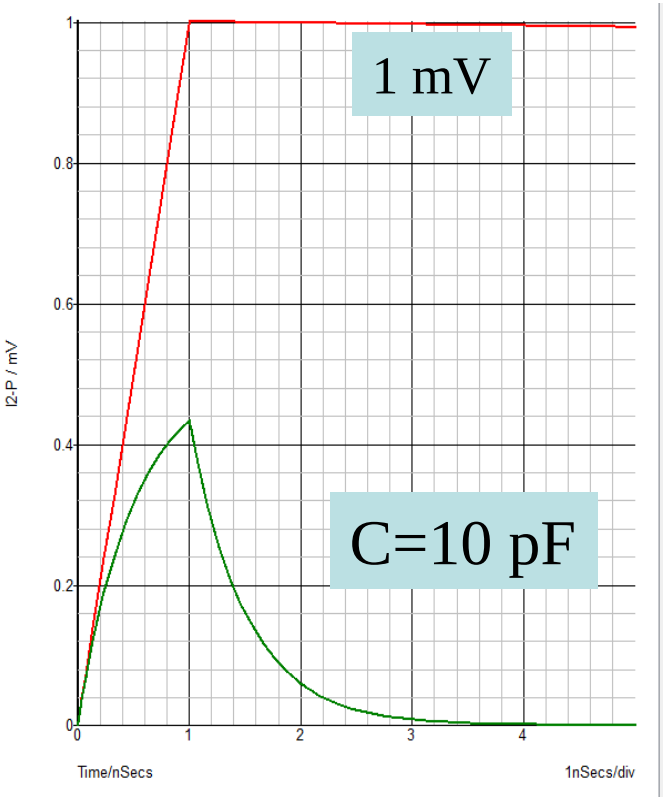
© Harmut Sadrozinski (Santa Cruz) "the beautiful risetime of the detector is spoilt by the electronics"

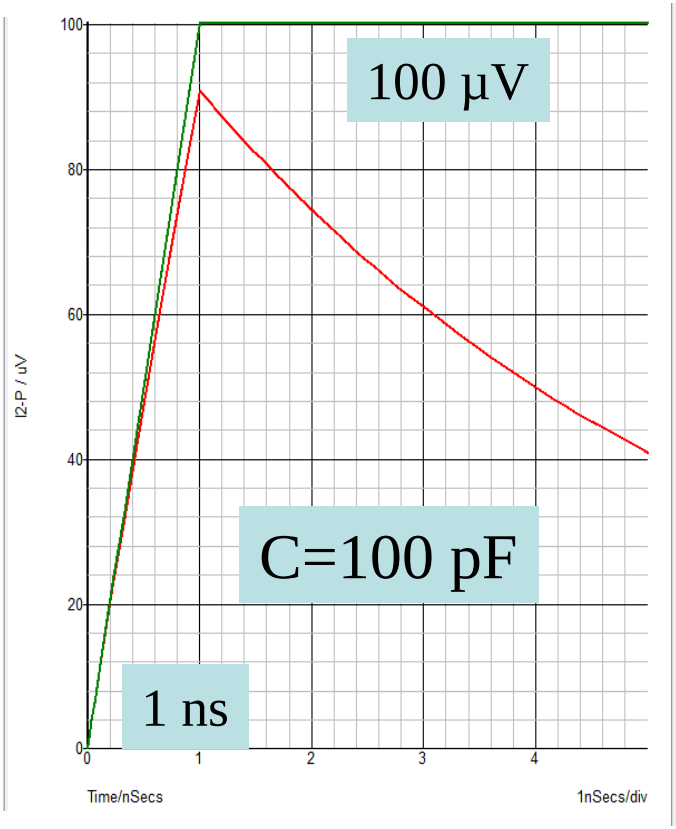
voltage vs current sensitive

- *Example* : 10 fC – 1 ns signal from 1-10-100 pF sensors into 50 Ω (current) or 50k (voltage) preamp



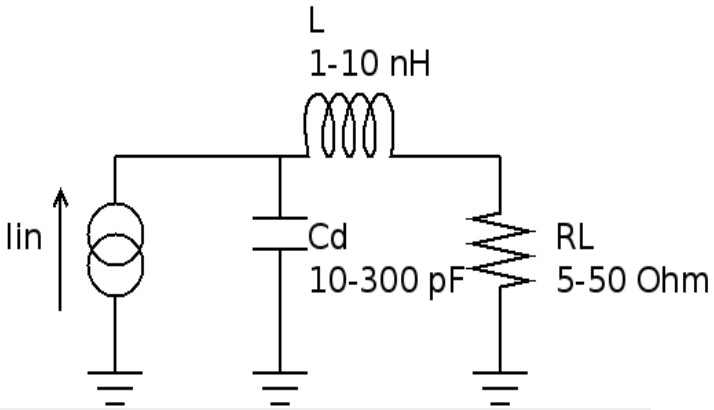


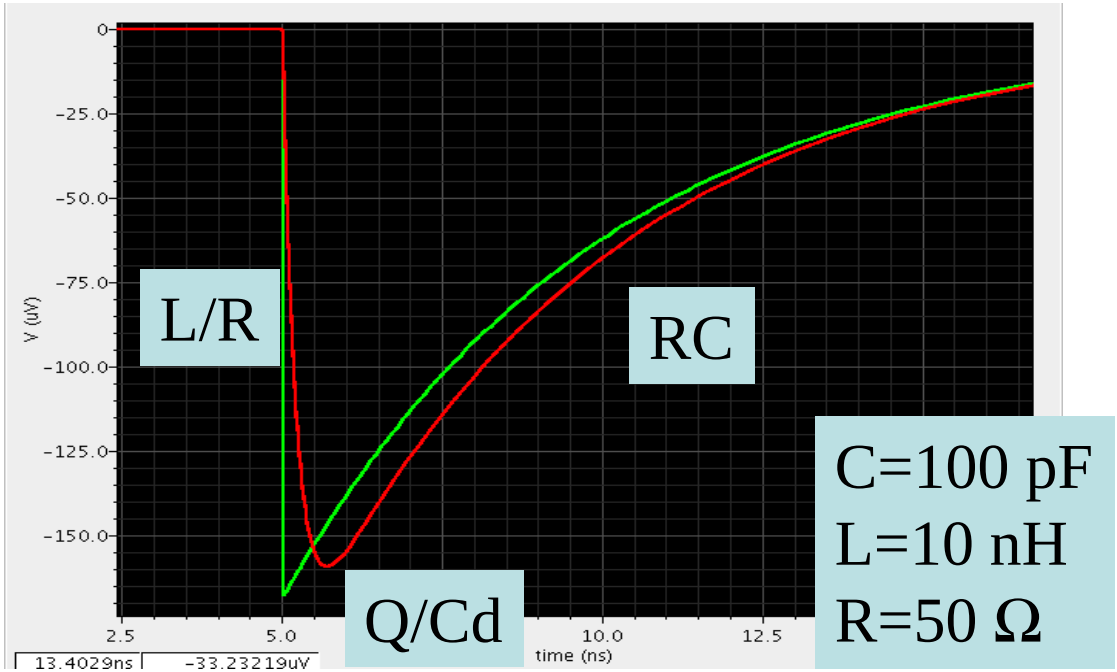


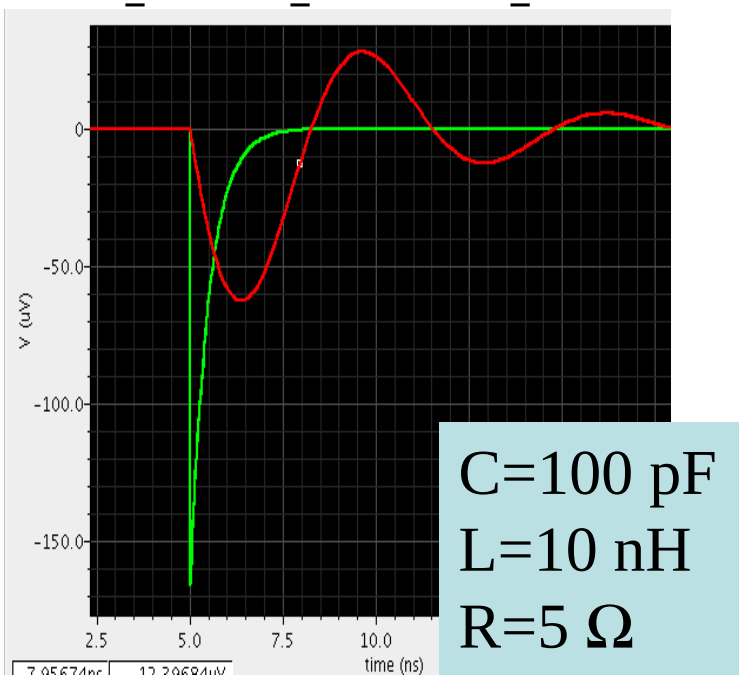


Examples of pulse shapes

- SiPM pulse : Q=160 fC, C_d=100 pF, L=0-10 nH, R_S=5-50 Ω
- Sensitivity to parasitic inductance
- Choice of R_S : decay time, stability
- Small R_S not necessarily the fastest
- Convolve with current shape… (here delta)

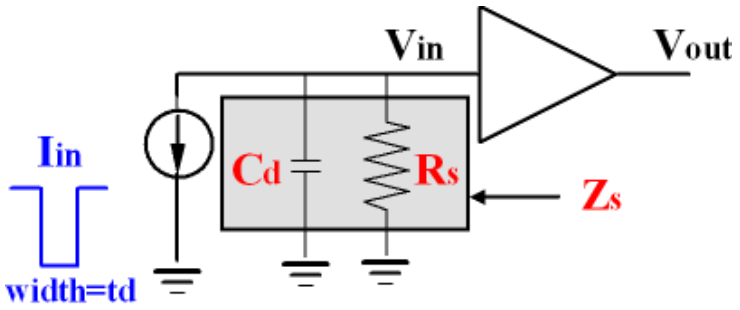




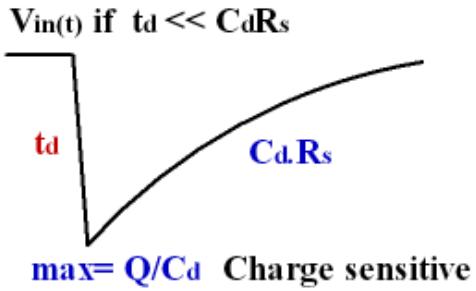


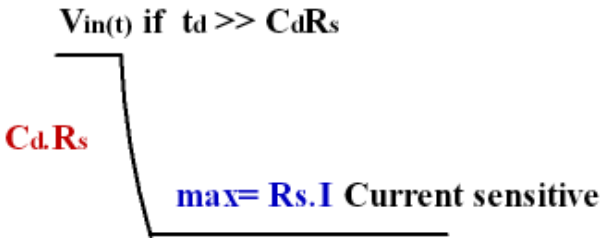
Detector impedance and input voltage

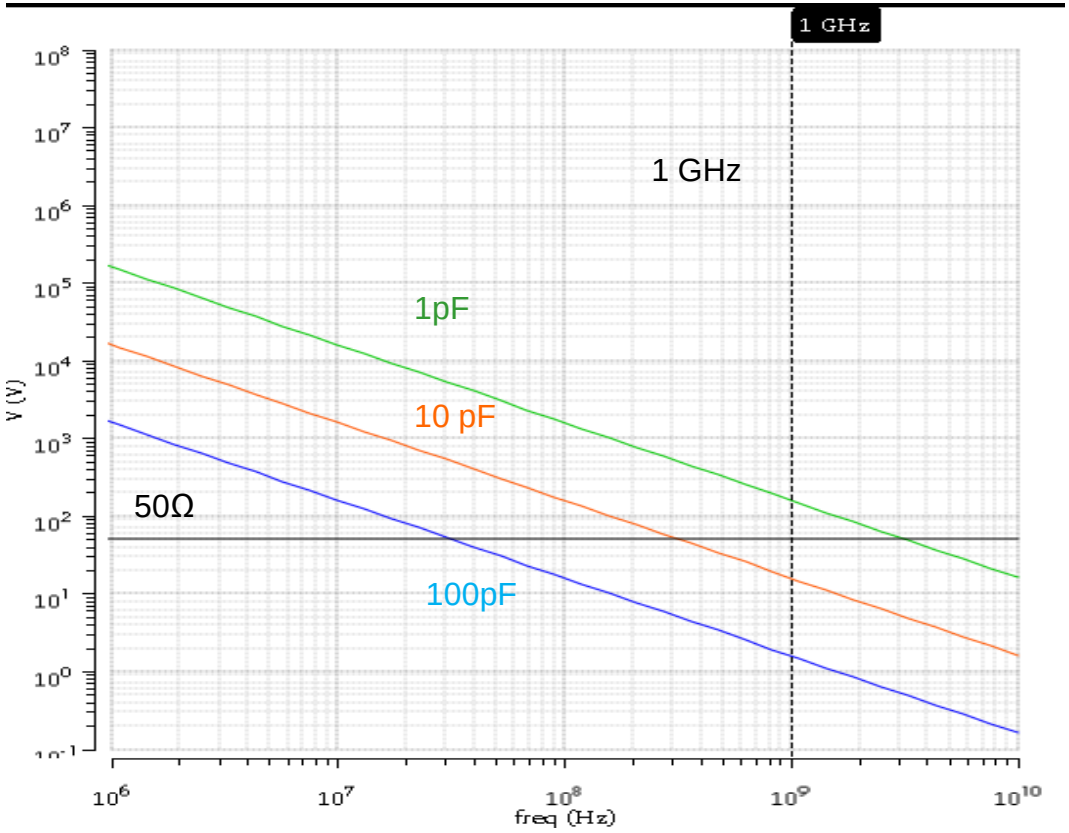
- 1 GHz, Cd=few tens of pF, input signal width <1ns
- Cd>1 pF, Zs@1GHz dominated by Cd
- Rise time: tr= td when td<< $R_S C_d$ and tr= $R_S C_d$ when td>> $R_S C_d$



At HF : difficult to beat the capacitance

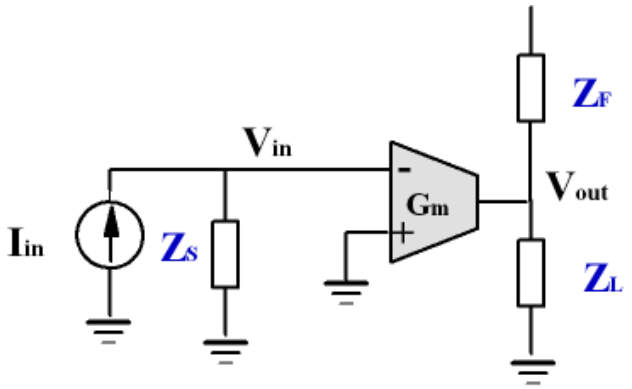




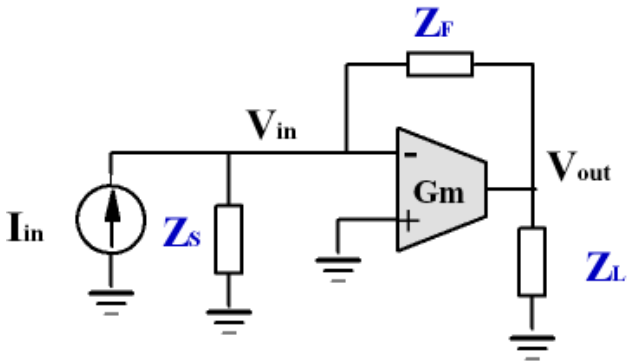


- Response to very short pulse

- Broadband
  - Zin=Rs (50 Ohm)
  - Vin = Q/Cin
  - $V_{OUT} = -G_m R_F \frac{Q_{IN}}{C_d}$



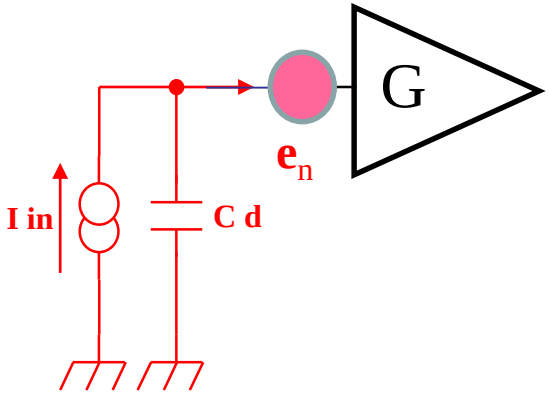
- Transimpedance
  - Zin ~ Zf/G ~ 1/gm
  - $V_{OUT} = \frac{\frac{1}{G_m} - R_F}{1 + j\omega\frac{C_d}{G_m}} I_{IN} \approx -G_m R_F \frac{Q_{IN}}{C_d}$



- Same response at High Frequency

Signal and noise in Broadband amplifiers

- Signal of duration t_d, across capacitance Cd with BB amplifier of impedance R_S



- Signal scales as 1/ C_d if $R_S C_d >> t_d$ and $C_{PA} << C_d$

$$S = V_{OUT} = G\frac{Q_{IN}}{C_d}$$

- Rise time is the convolution of signal duration t_d and amplifier risetime $t_{10\text{-}90\_PA}$

$$t_r \approx \sqrt{t_{10-90\_PA}^2 + t_d^2}$$

- Noise is given by the preamp noise density e_n and bandwidth

$$N = G.e_n\sqrt{\frac{\pi}{2}BW} = \frac{G.e_n}{\sqrt{2t_{10-90\_PA}}}$$

- Jitter is then :

$$\sigma_t^{\ J} = \frac{N}{dV/dt} = \frac{e_n C_d}{Q_{in}}\sqrt{\frac{t_{10-90\_PA}^2 + t_d^2}{2t_{10-90\_PA}}}$$

Jitter in Broadband amplifiers

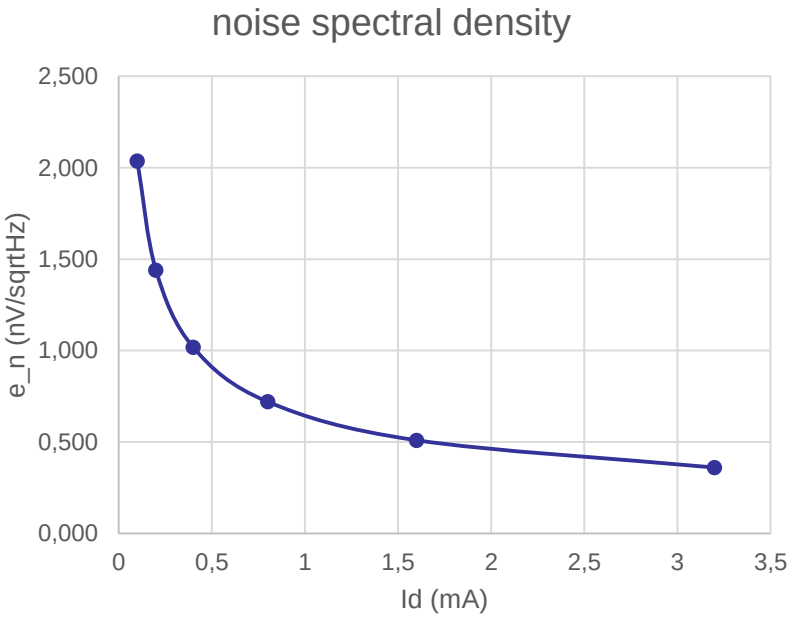
- Optimum value: $t_{10\text{-}90\_PA} = t_d$ (current duration)

$$\sigma_t^{\ J} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

Dominated by sensor
Electronics only gives e_n

- Electronics noise e_n given by input transistor transconductance g_m :
  - Typically ~1 nV/√Hz at I_D = 0.5 mA
  - Scales with the square root of current in transistor (weak inversion)

$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_D}}$$

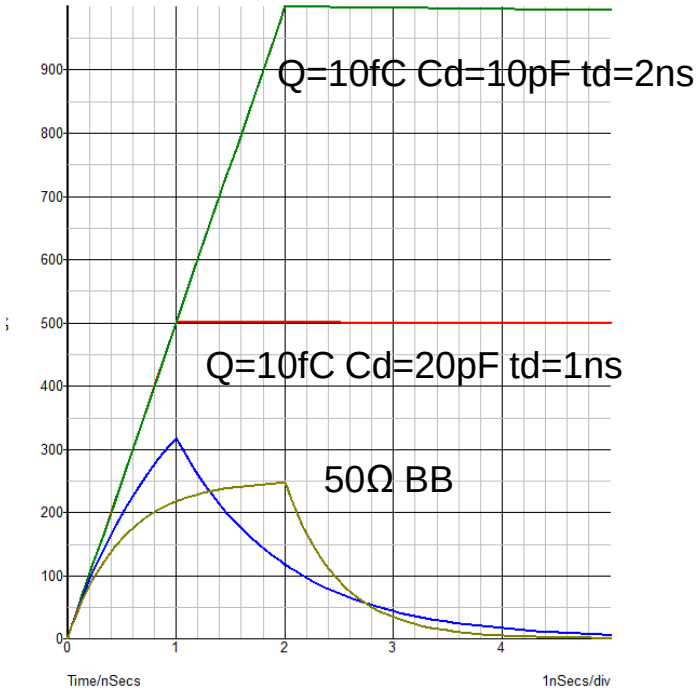


Expected jitter with thickness

- Evaluate jitter(Q) with thickness (th)
  - At given Q, C_d ~1/th, t_d ~ th, expect j ~ 1/√th
  - dV/dt = Q / C_d.t_d = Cte
  - Better jitter : longer signal, smaller BW
  - Not seen in testbeam setup because 50 Ω amplifier not optimum at low capacitance
- Jitter(MIP) even better because more charge
- But more Landau fluctuations…

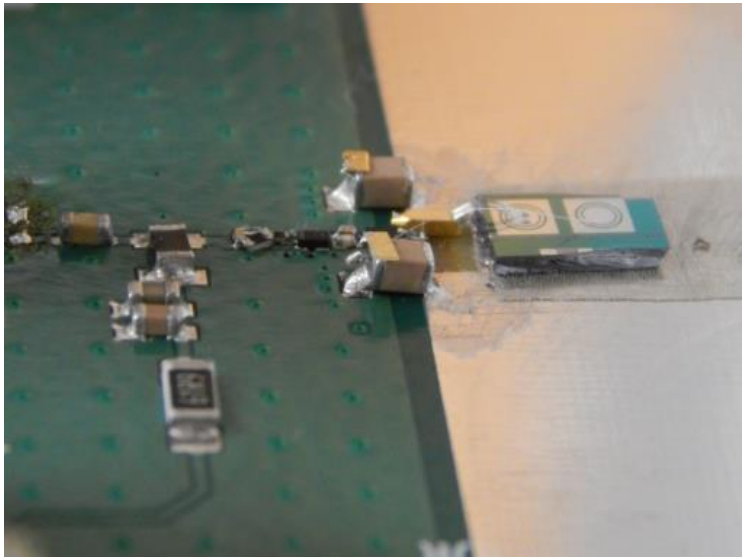
$$\sigma_t^J = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

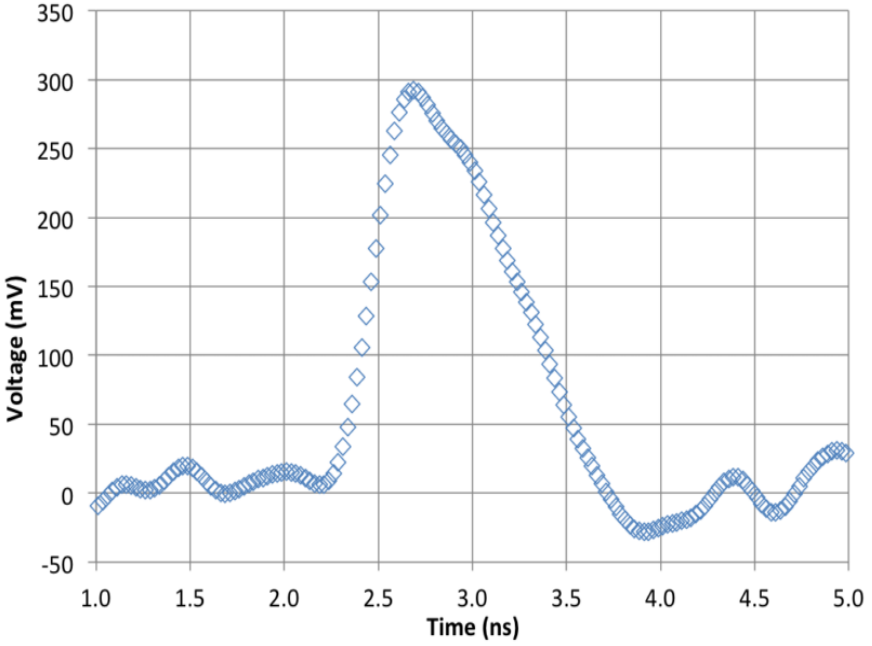
CMS	100um calc	200um calc	300um calc	200um meas
th (µm)	100	200	300	210
Cd (pF)	23	12	8	14
fC/MIP	1,3	2,6	3,8	2,7
en (nV/√Hz)	1	1	1	
td (ns)	1	2	3	
jitter/Q(fC)	727	514	420	1021
jitter/MIP	568	201	109	380

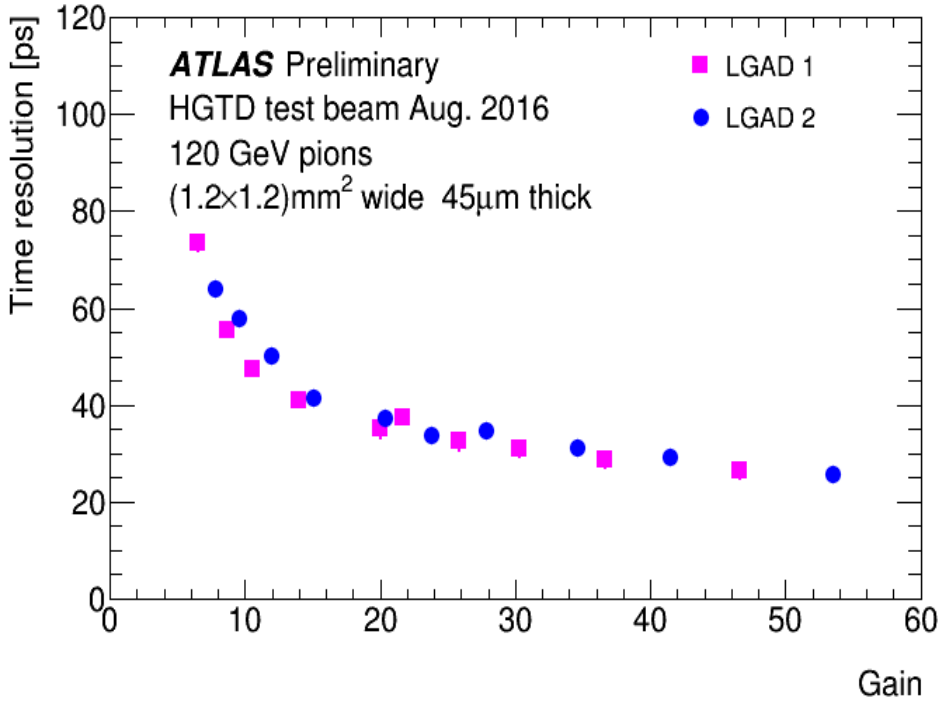


LGAD with SiGe hybrids

- 2 mm² LGAD 50 µm thick
- SiGe discrete readout BW = 2 GHz
- Jitter measured : j = 200 ps / Q(fC)
  - MIP = 4.6 fC at G = 10, t_d = 0.5 ns, C_d = 2 pF, e_n = 1 nV/√Hz
  - Theory : j = 50 ps/Q(fC)
- ATLAS HGTD will use 2 mm² LGADS for ~30 ps timing with G = 10-20







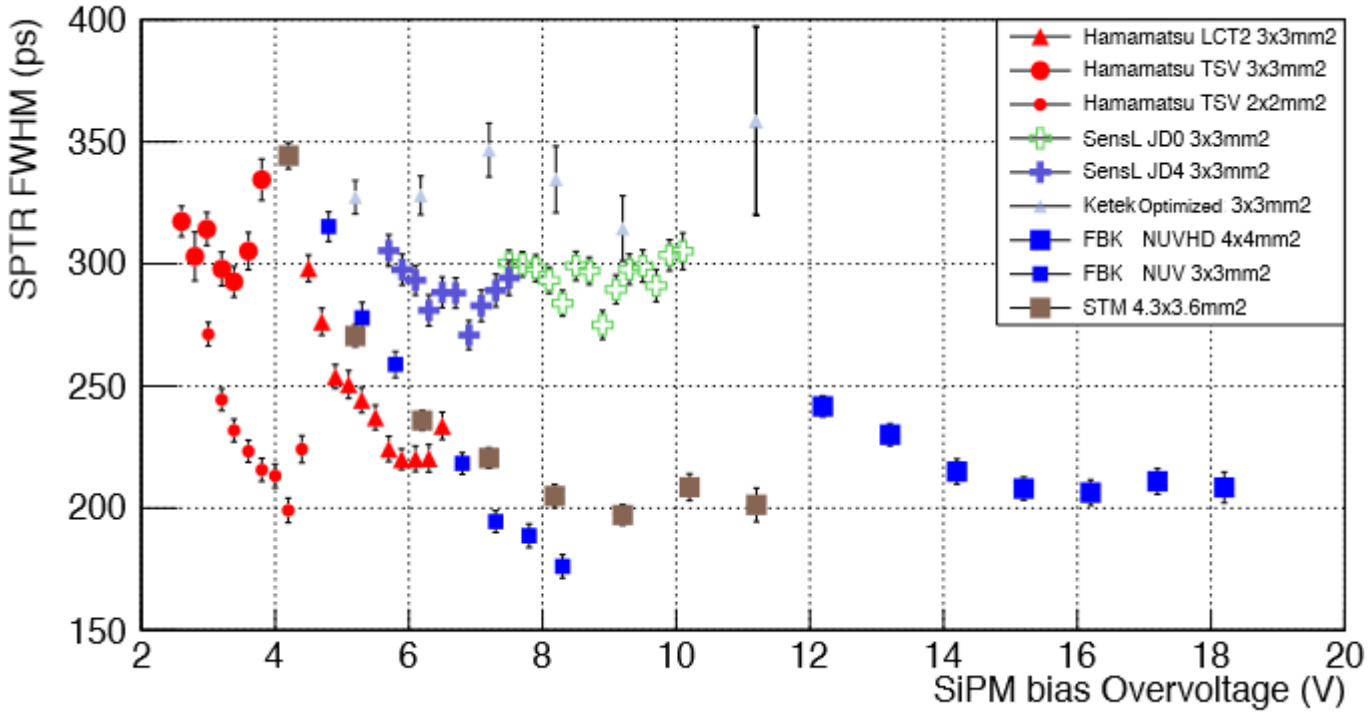
With SiPMs : SPTR [JINST 11 P10016]

- SPTR
  - FWHM ~200 ps
  - Rms ~ 80 ps

Single photon time resolution of state of the art SiPMs

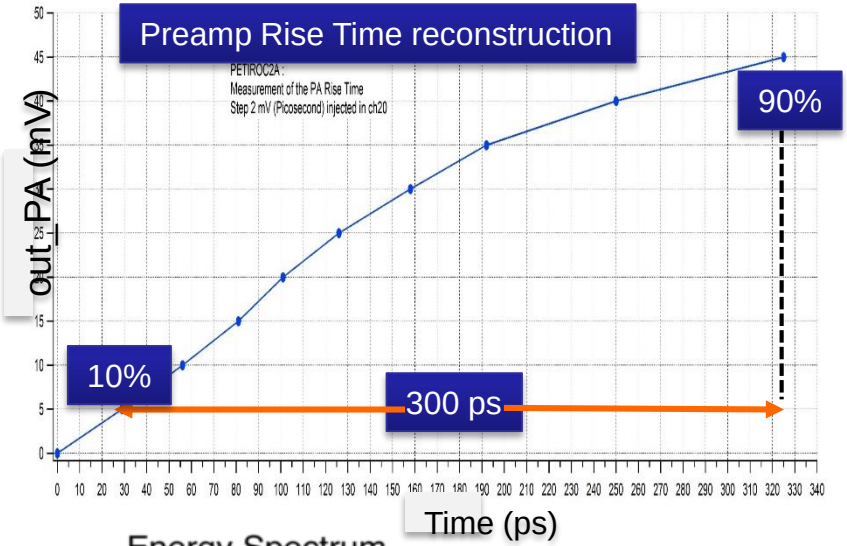
M.V. Nemallapudi,[1] S. Gundacker, P. Lecoq and E. Auffray

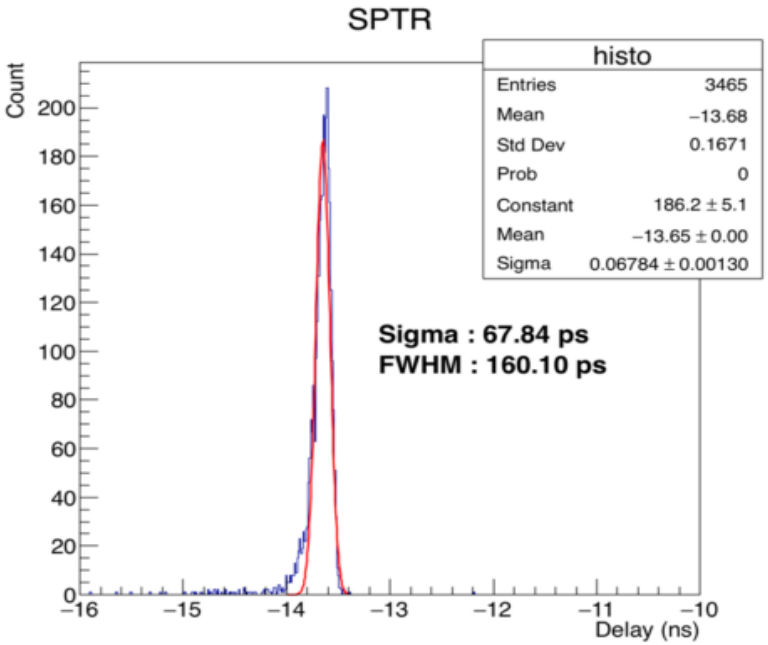
CERN,
23 Rue de Meyrin, Geneva, 1211-CH

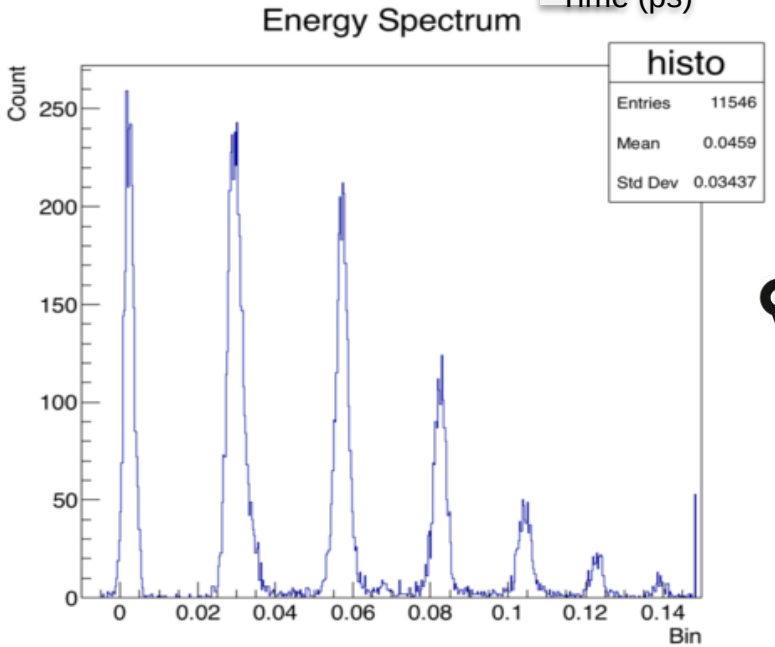


Going to lower SPTR

- Expect ~ 20 ps/pe
- NINO risetime ~1 ns
- Test with PETIROC2 (tr = 300 ps)
  - SPTR = 67 ps rms (180 ps FWHM)
- Possible effect of stray inductance
- Furhter studies in FAST framework







weeroc

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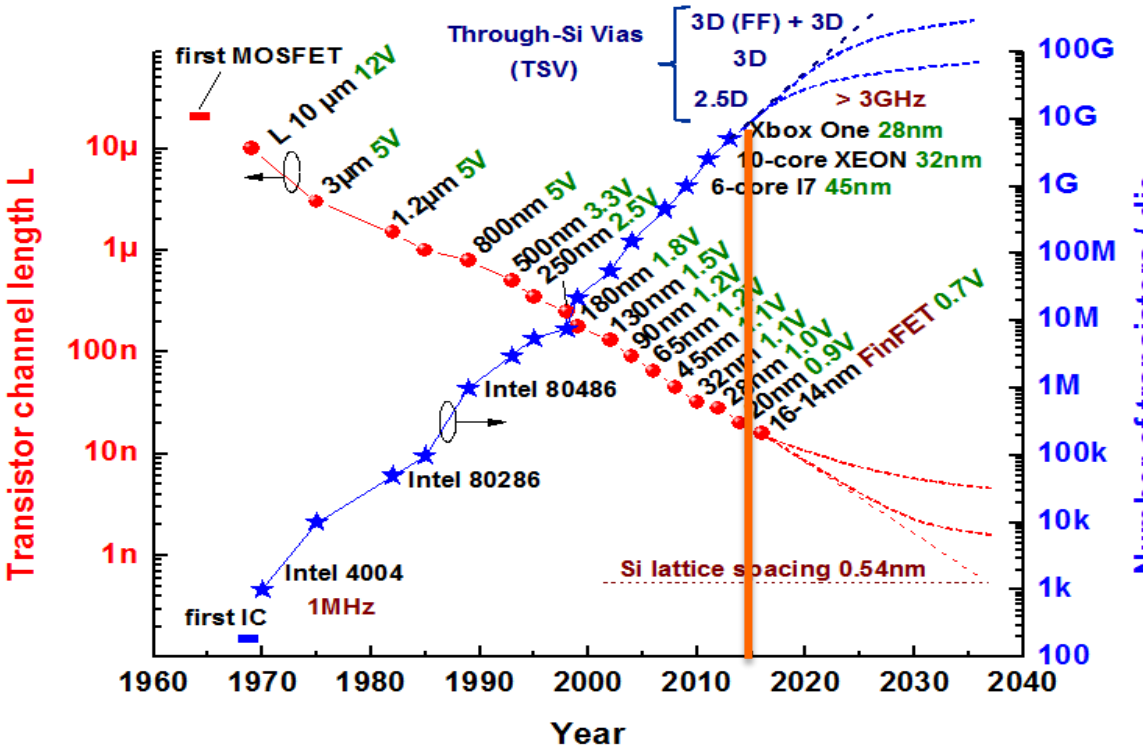
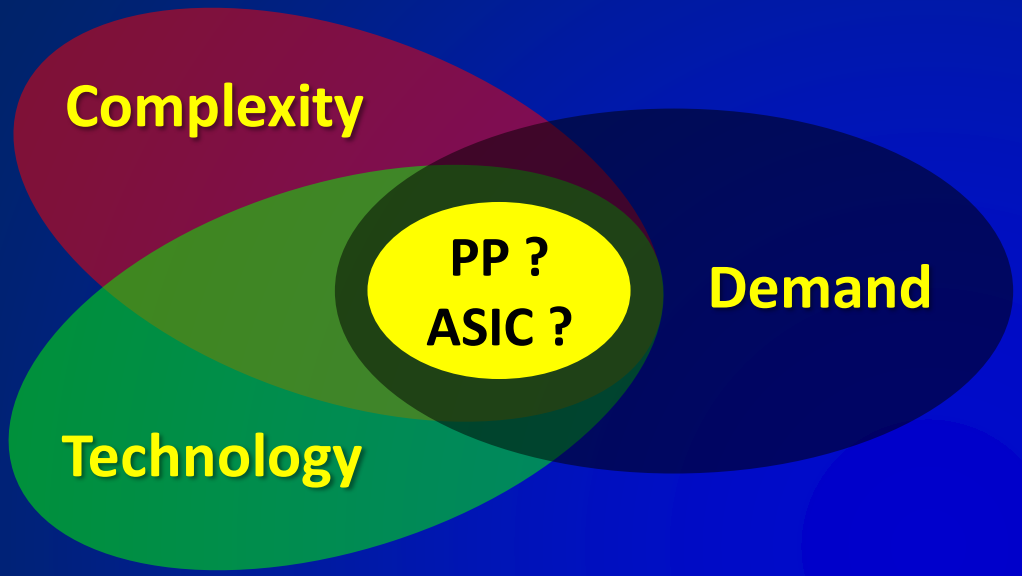
Evolution of technologies

- More and more functions are integrated inside chips (ASICs)
- Evolution of technologies make them more and more performant but more and more complex
- Cost increases …
  - MPW costs :
  - 350 nm : 1 k€/mm²
  - 130 nm : 2 k€/mm²
  - 65 nm : 6 k€/mm²
- Chip size also…
- CERN targets 65/130 nm
- SiGe in AIDA2020



10 ans d'évolution des spécifications techniques pour la réalisation

The PP-ASIC Paradigm



Collaborations ?
- only part of the solution
- communication
- overhead
- lead of large group

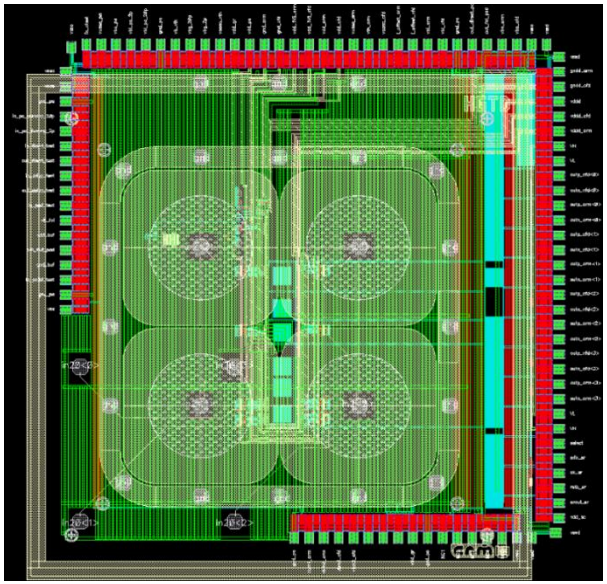
The number of ASIC designers has to increase !

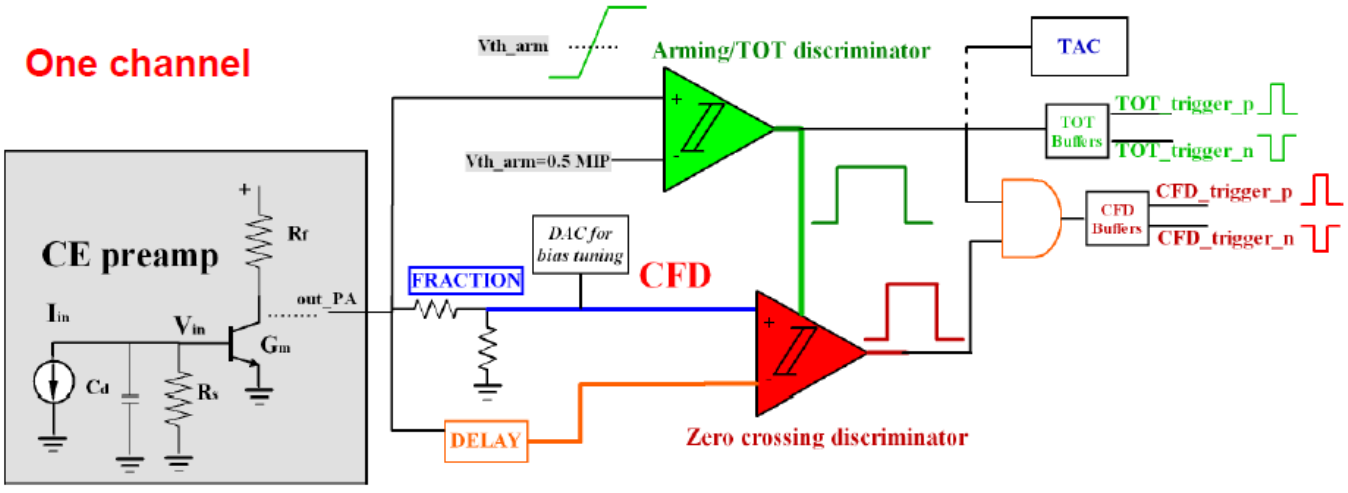
involve non-PP ASIC groups

increase size of PP ASIC groups

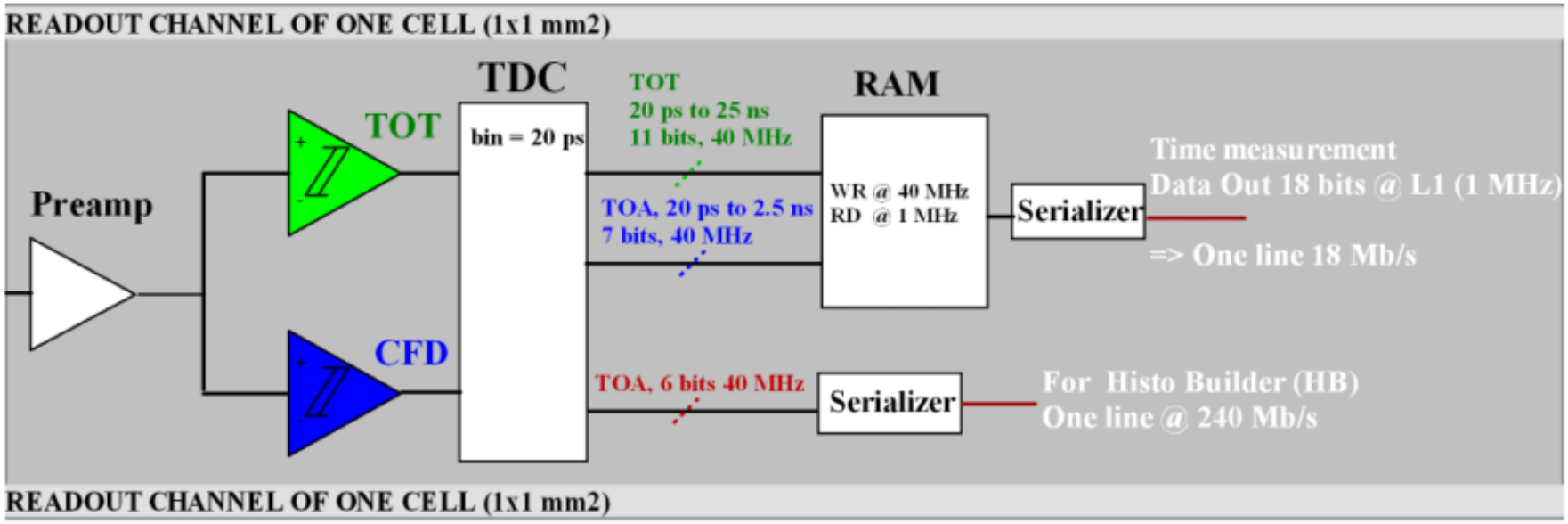
ALTIROC

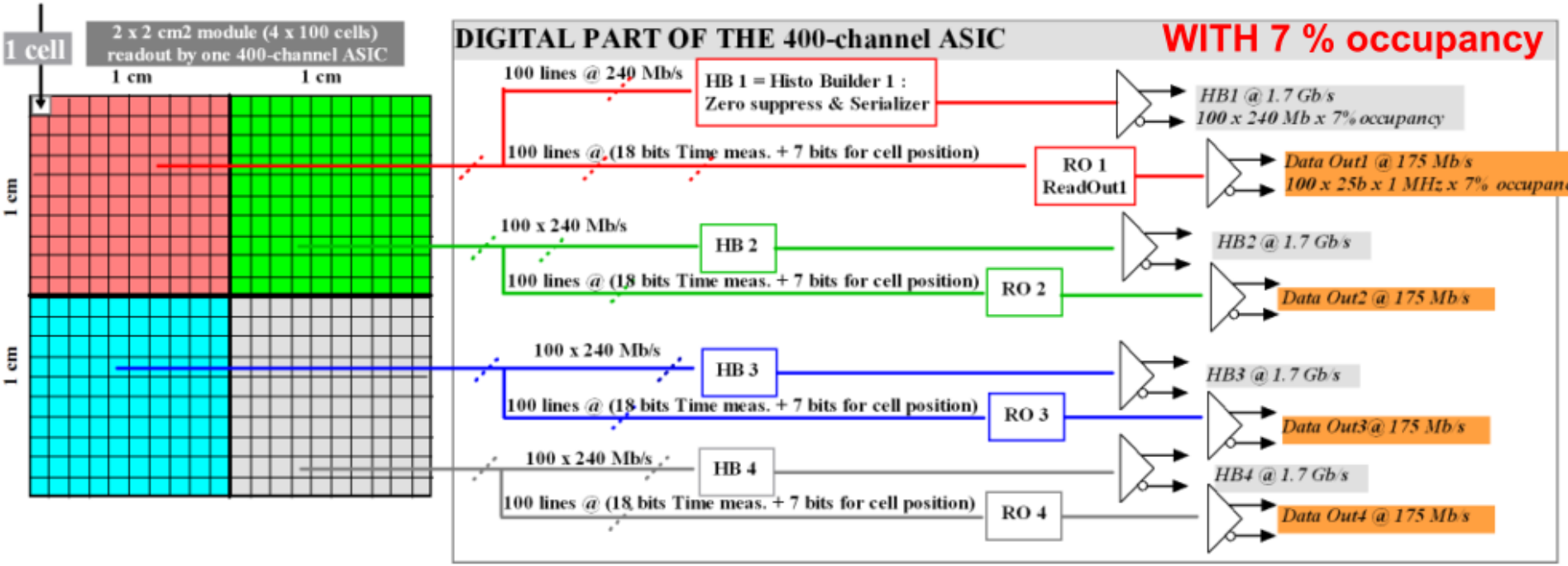
- ALTIROC = ATLAS LGAD Timing ROC
  - 20 ps timing measurement with LGAD sensors for ATLAS HGTD
  - Jitter : j = 110 ps/Q(fC) @ Cd=2 pF
  - Test chip bondable to sensors of 1x1 mm² and 2x2 mm², submitted in dec 16 in TSMC 130n
  - High speed preamp (1 GHz) + constant fraction discriminator (20 ps)
- Will evolve to 400 ch chip
  - With internal TDC, bump bonded to sensor. Collaboration with SLAC





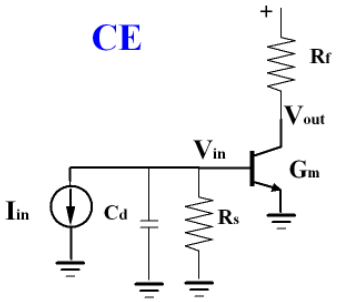
HGTD architecture

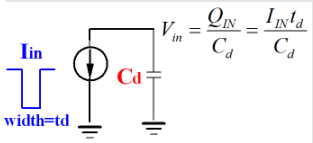




CE in SiGe 130nm and in TSMC 130 nm

- Broad Band amplifier CE configuration
- Same current (Ic=700 µA), same Rf=4K, vdd=1.2V
- Higher gain with SiGe but larger noise due to rbb'



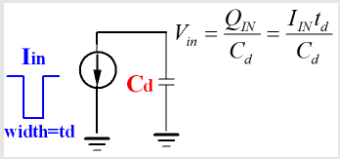
	CE 10pF TSMC 130 nm	CE 10pF SiGe 130nm Trans size= 20
td=10ps Qin=Iin.td= 100µA.10ps=**1fC** 	out=3.7mV tr=220ps BWa=1.6 GHz rms=1.3 mV S/N=2.8 σj=220ps/2.8=78 ps	out=8.95 mV tr=176 ps BWa= 2GHz rms=3.14mV S/N=2.85 σj=176ps/2.85=60 ps
td=1ns and tr_ampli=td CL=100fF Qin= 1µA.1ns=**1fC**	out=3.52mV(CL=100fF) tr=1.1ns BWa=440MHz rms=0.66mV S/N=5.3 σj=1100ps/5.3=206 ps	out=7.5mV (CL=110fF) tr=1.1 ns BWa=440MHz rms=1.4 mV S/N=5.4 σj=1.1ns/5.4=204 ps

CE in TSMC 130 nm: jitter vs tr (BW) and td

- With I source trans (0 for 2 pF or 1.8mA)
- Follower (connected to a discriminator)
- Normalization to 1 fC, square pulse.
- LGAD signa would give 6 fC/MIP

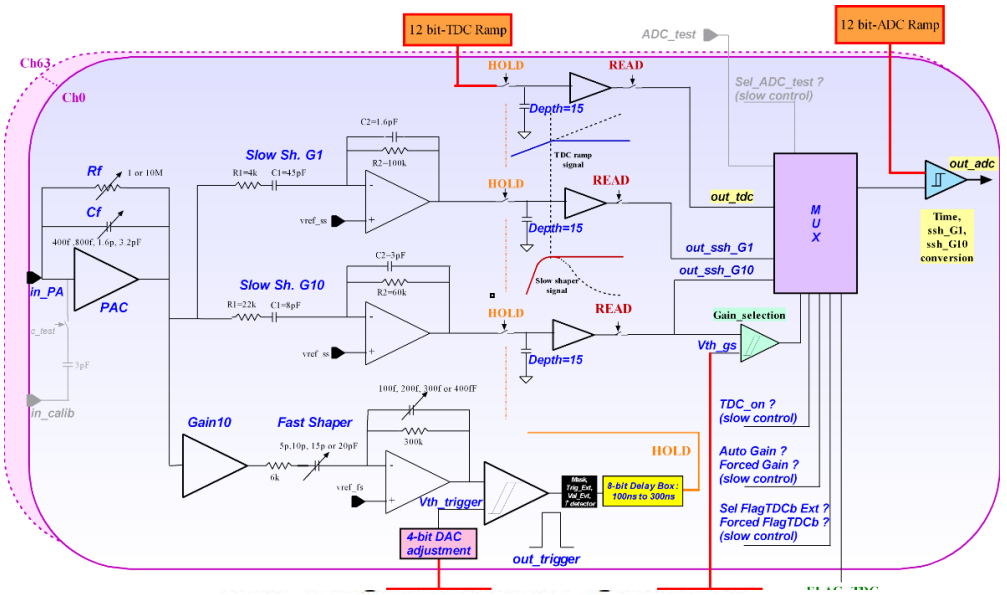
$$\sigma_t^J = \frac{\sigma_N}{\frac{dV}{dt}} = \frac{t_r}{\frac{S}{N}} = \frac{\sqrt{t_{r\_ampli}^2 + t_d^2}}{\frac{S}{N}}$$

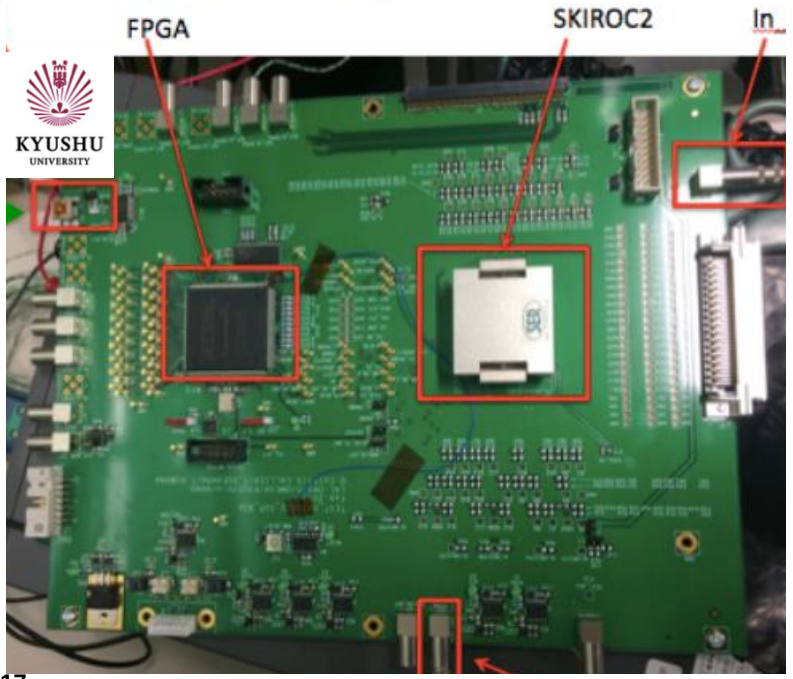
POWER: 0.5mW/ mm²

CE	Cd=2pF (Id=220 µA)	Cd=20pF (Id=2.1 mA)
td=10ps Qin=Iin.td= 100µA.10ps=**1fC** 	out = 6.9 mV out_fol=6.1 mV tr_fol=284 ps BWa=1.2 GHz rms=0.485 mV S/N=12.6 σj=284ps/12.6=23 ps	out=3.37 mV out_fol=3.1 mV tr_fol=290 ps BWa=1.2 GHz rms=1.2 mV S/N=2.6 σj=290ps/2.6=110 ps
td=1ns and tr_ampli=td CL=100fF Qin= 1µA.1ns=**1fC**	out=6.4 mV out_fol=5.9 mV tr_fol=1.1ns BWa=410 MHz rms=0.39 mV S/N=15 σj=1.1ns/15=73 ps	out=3.2 mV out_fol=3.05 mV tr_fol=1.1 ns BWa=440 MHz rms=0.8mV S/N=3.8 σj=1.1ns/3.8=288 ps

SKIROC2_CMS for HGCAL

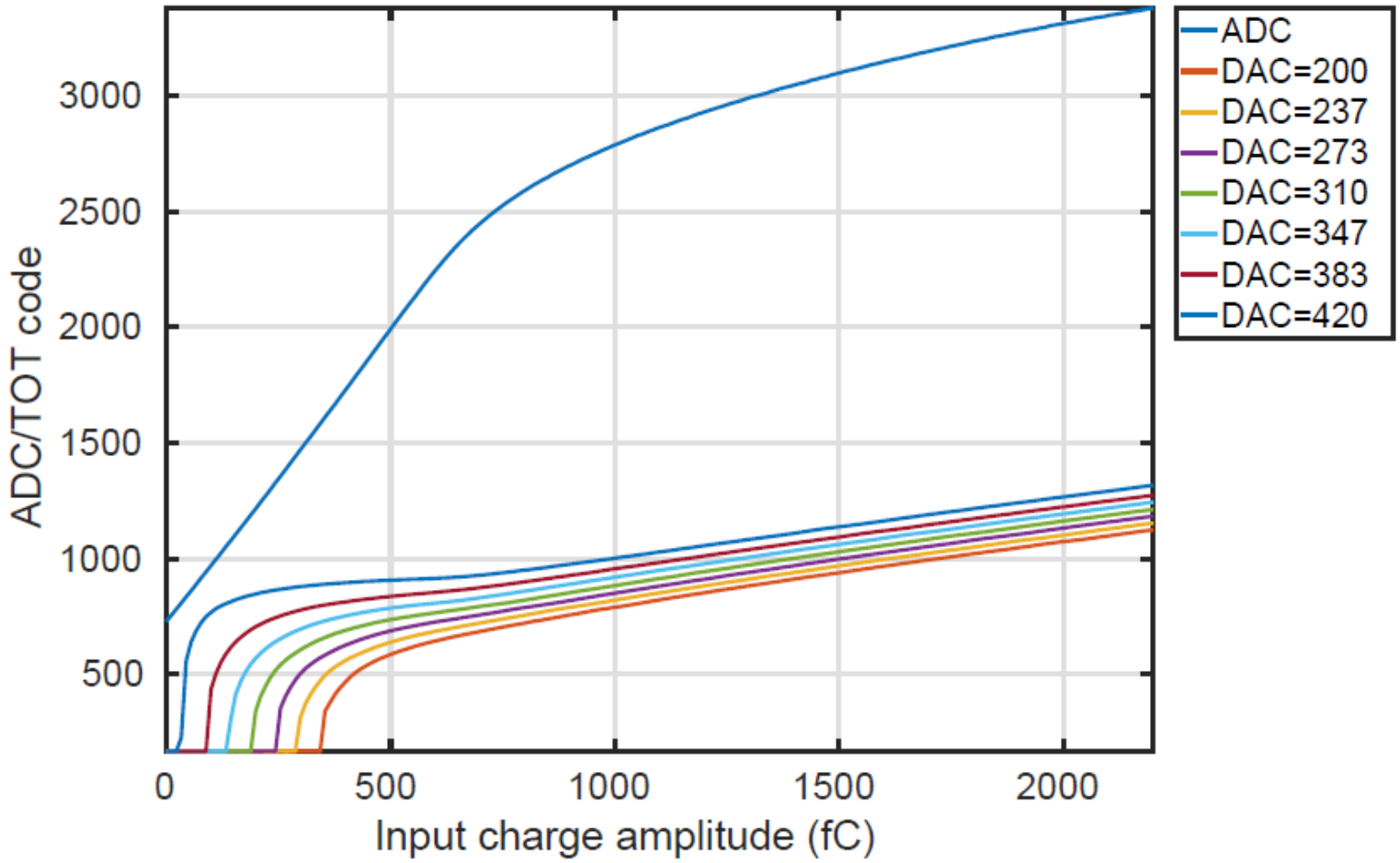
- new SKIROC2 for CMS
  - Optimized version for CMS testbeam, pin to pin compatible
  - Dual polarity charge preamplifier
  - Faster shapers (25 ns instead of 200 ns)
  - 40 MHz circular analog memory, depth= 300 ns
  - TDC (TAC) for ToA and ToT , accuracy : ~50 ps
  - Submitted jan 2016 SiGe 350nm
- Tests :
  - First tests on BGA testboards
  - 4-5 boards will be equipped





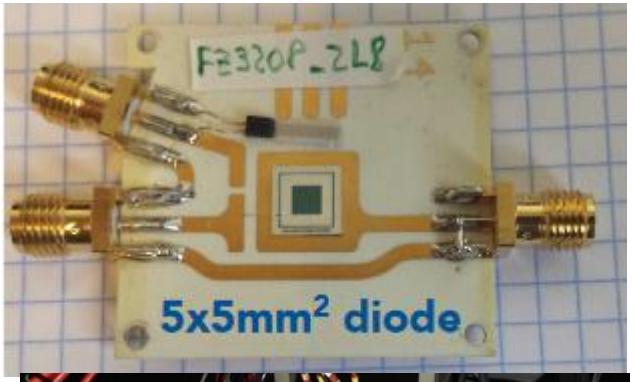
Time over Threshold (ToT)

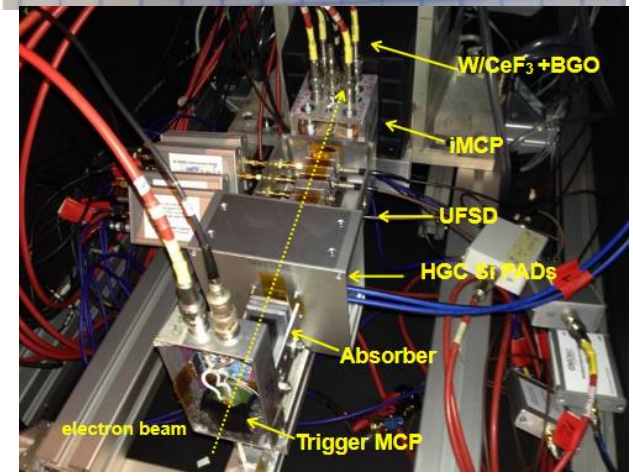
- TOT measured in current sensitive config : Rf=20k Cf=300f
- ADC range : 0-500 fC TOT above
- energy reconstruction around 500 fC, calibration, pedestal evaluation

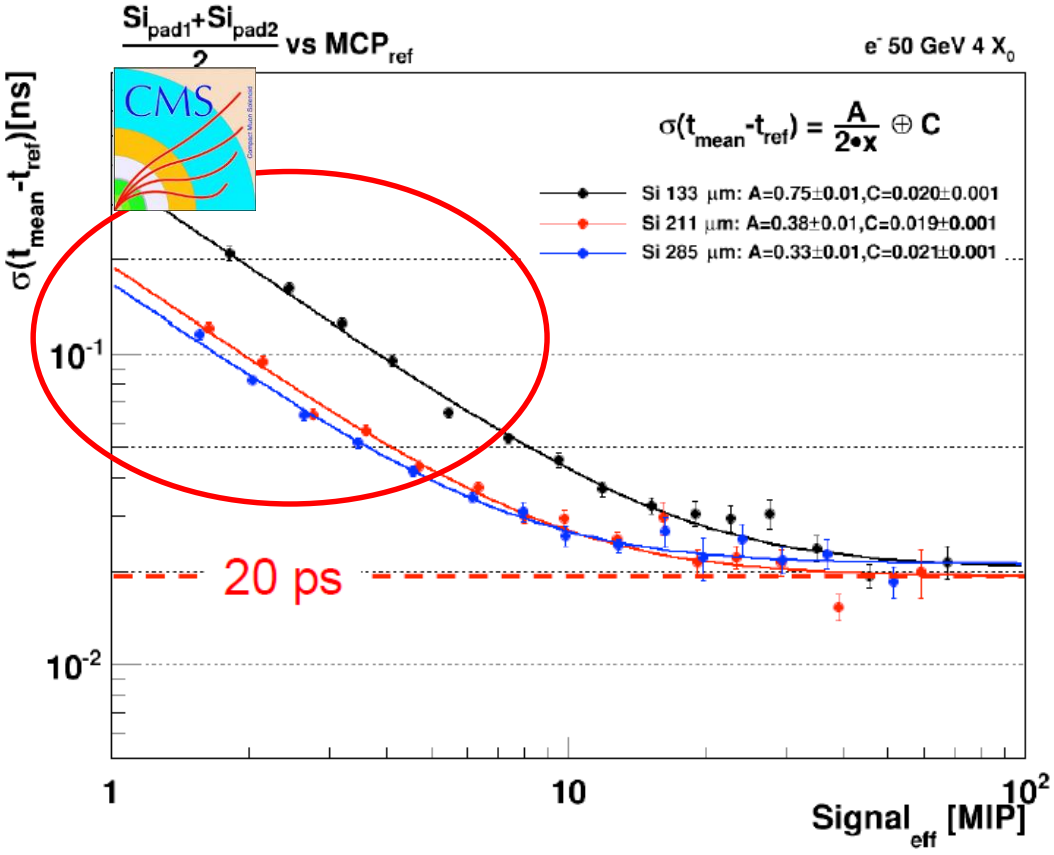


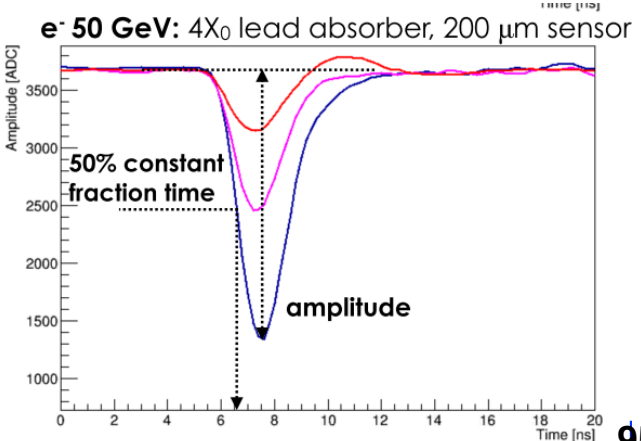
Results : CMS pin diodes caracterization

- Measured jitter In testbeam [A. Martelli et al.] :
  - jitter ~ 1 ns/Q(fC) (+) 20 ps





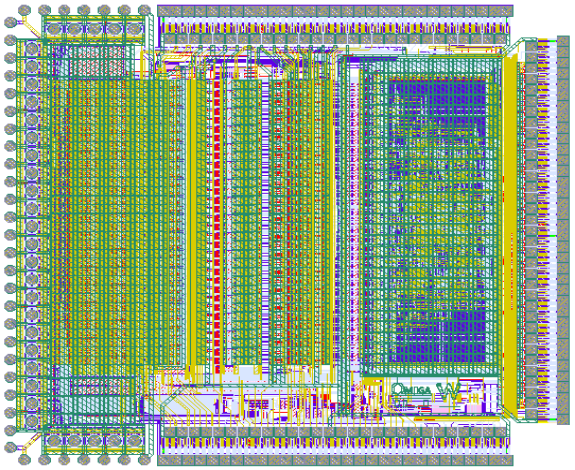




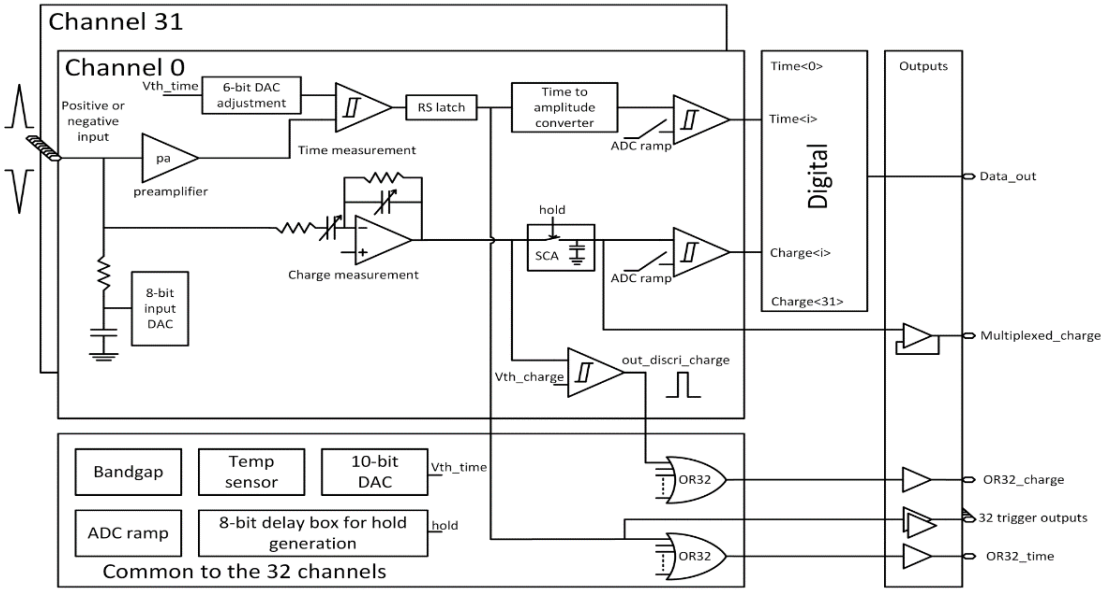
PETIROC2 DESCRIPTION

- Time of Flight read-out chip with embedded TDC (25 ps bin) and ADC
- Dynamic range: 160 fC up to 400 pC
- 32 channels (negative input)
  - 32 trigger outputs
  - NOR32_chrage
  - NOR32 time
  - Charge measurement over 10 bits
  - Time measurement over 10 bits
  - One multiplexed charge output
- Common trigger threshold adjustment and 6bit-dac/channel for individual adjustment
- Variable shaping time of the charge shaper
- 32 8bit-input dac for SiPM HV adjustment
- Power consumption 6 mW/ch
- Front-end
  - Broad Band SiGe fast amplifier
  - Fast SiGe discriminator
  - 1 GHz overall bandwidth, gain = 25

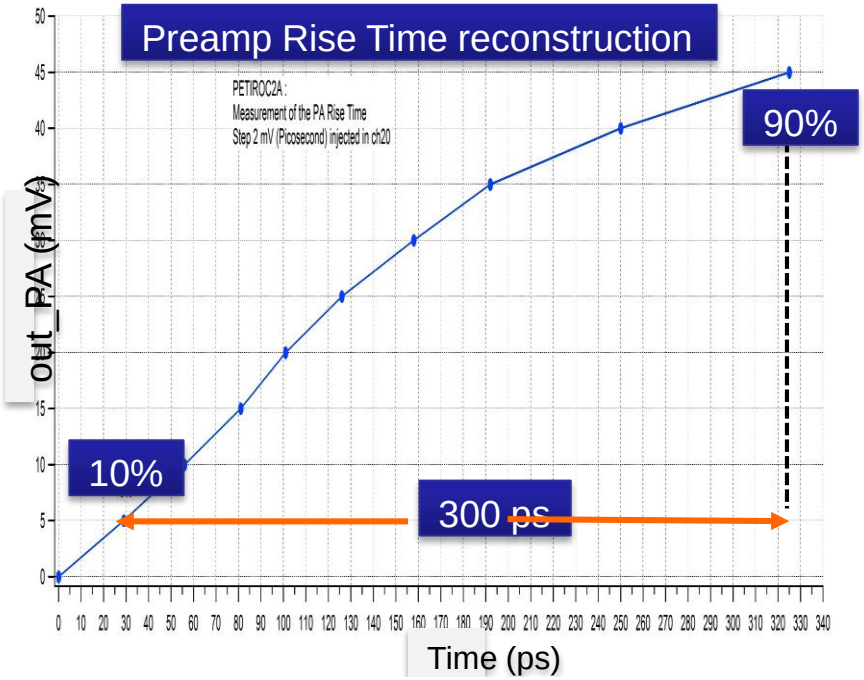
AMS 0,35µm SiGe

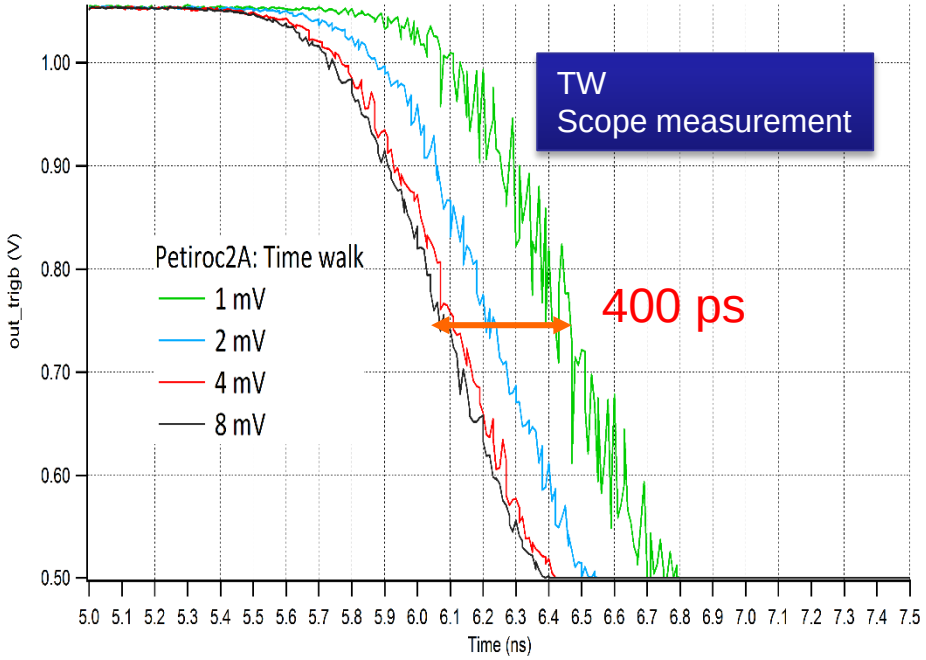


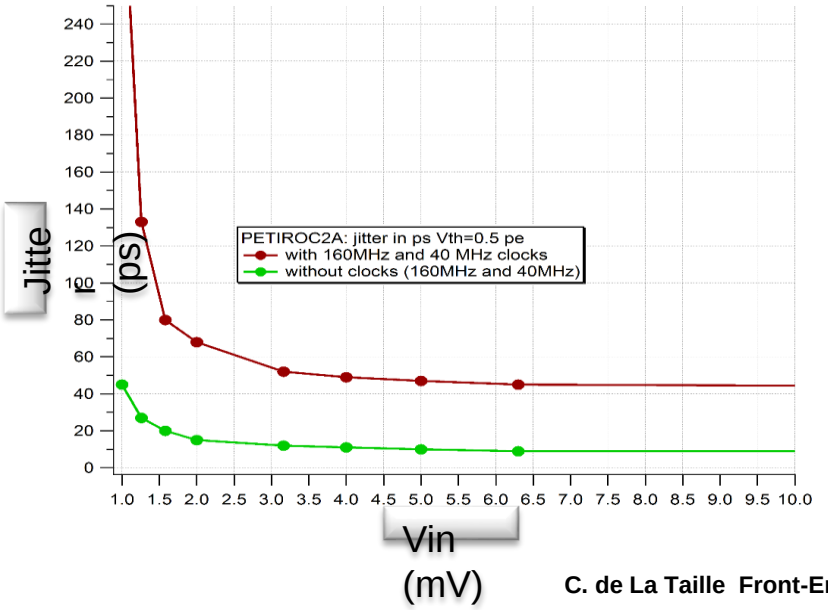
weeroc

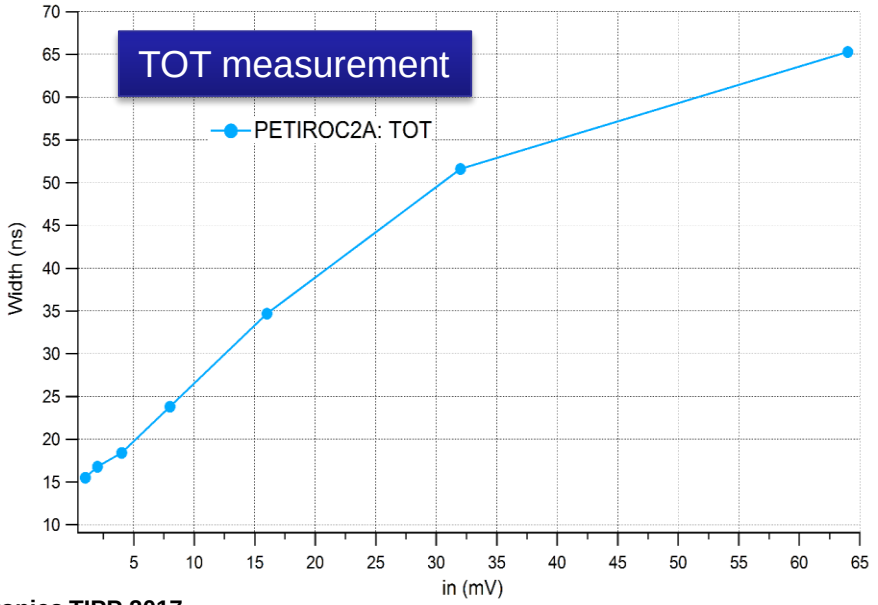


PETIROC2A: performance



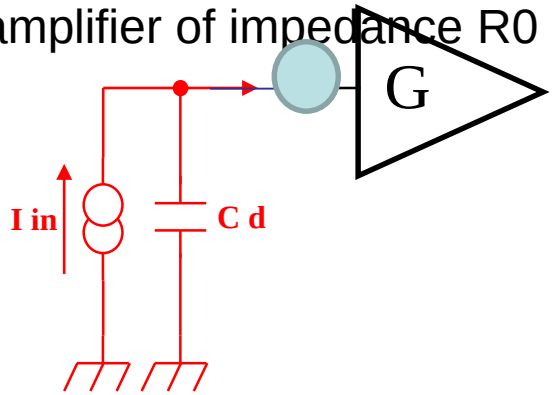






Signal and noise in Broadband amplifiers

- Signal of duration td, across capacitance Cd with BB amplifier of impedance R0



- Signal scales with 1/ Cd if R0Cd>>td and C_{PA}<<Cd

$$S = V_{OUT} = G\frac{Q_{IN}}{\mathbf{C_d}}$$

- Signal rise time is the convolution of signal duration td and amplifier risetime $t_{10\text{-}90\_PA}$

$$\frac{dV}{dt} == \frac{G.Q_{in}}{C_d\sqrt{t_{10-90\_PA}^2 + t_d^2}}$$

- Noise is independent of Cd

$$N = G.e_n\sqrt{\frac{\pi}{2}BW} = G.e_n\sqrt{\frac{\pi}{2}\frac{0.35}{t_{10-90\_PA}}} = \frac{G.e_n}{\sqrt{2t_{10-90\_PA}}}$$

Signal and noise on Broadband amplifiers

- Jitter is given by

$$\sigma_t^{\ J} = \frac{N}{dV/dt} = \frac{e_n}{\sqrt{2t_{10-90\_PA}}} \frac{C_d\sqrt{t_{10-90\_PA}^2 + t_d^2}}{Q_{in}} = \frac{e_n C_d}{Q_{in}} \sqrt{\frac{t_{10-90\_PA}^2 + t_d^2}{2t_{10-90\_PA}}}$$

- Optimum value: $t_{10\text{-}90\_PA} = t_d$ (current duration)

$$\sigma_t^{\ J} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

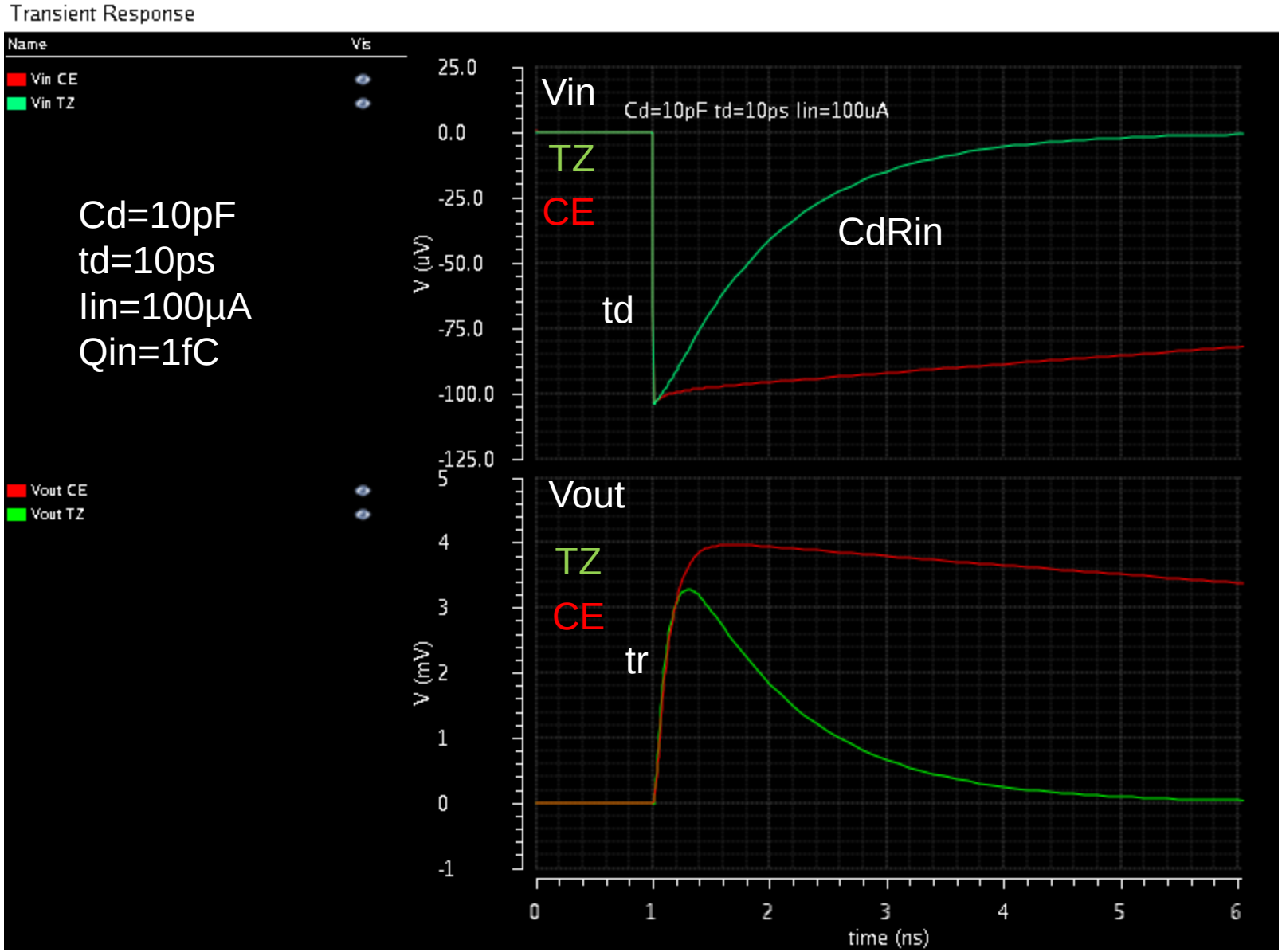
Dominated by sensor
Electronics only gives en

- Electronics noise en given by input transistor transconductance :

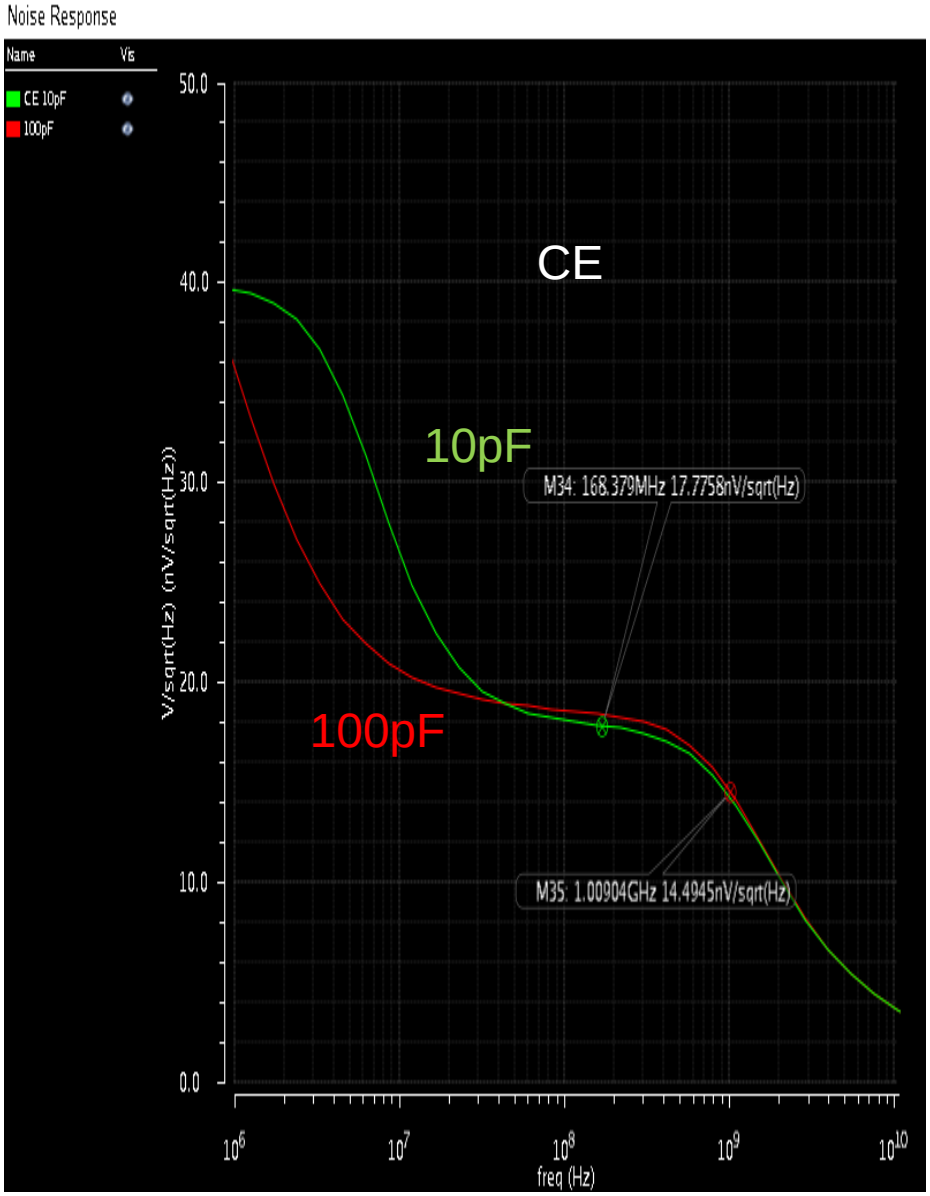
$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_D}}$$

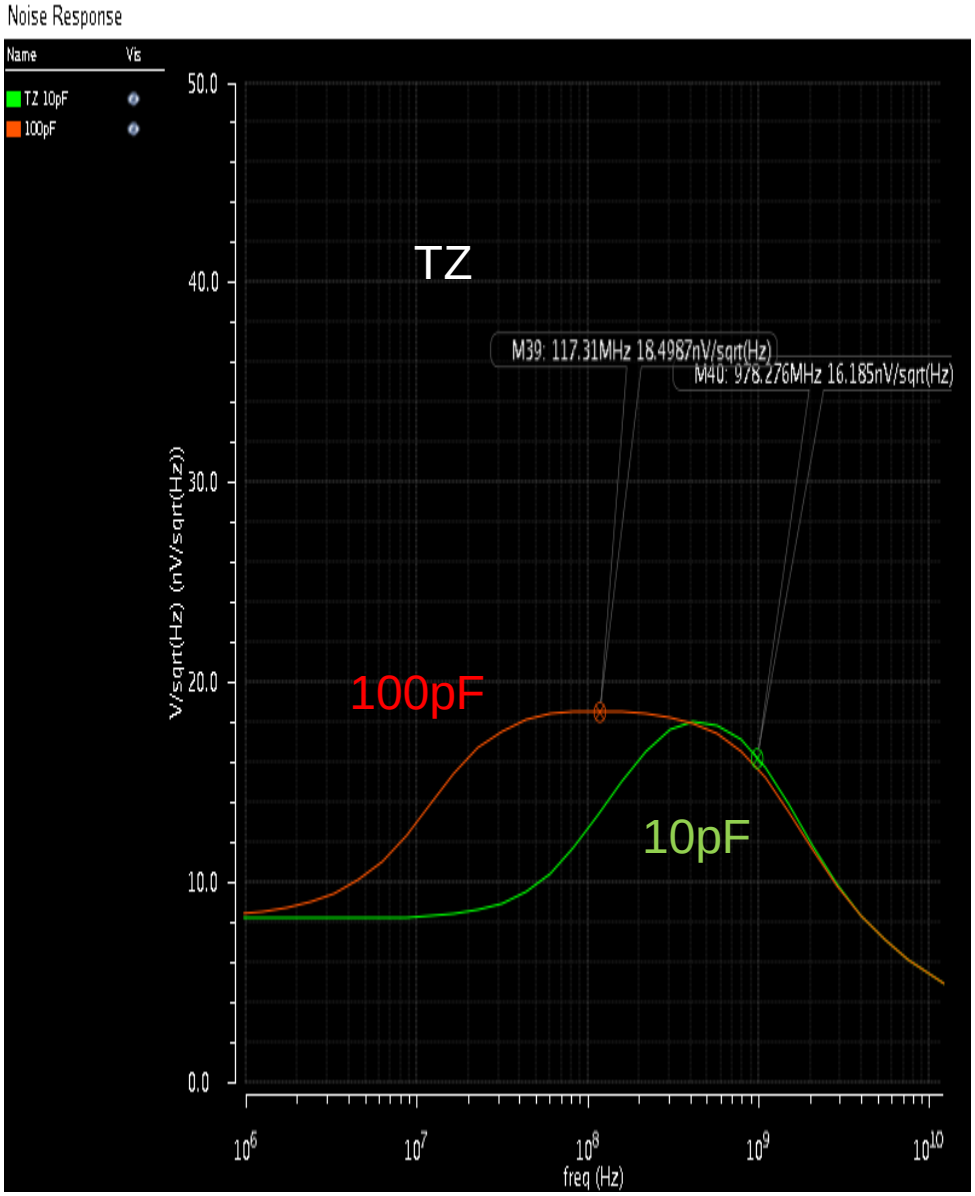
$$\sigma_t^{\ J} = \frac{C_d}{Q_{in}} \sqrt{\frac{2kT}{g_m} t_d}$$

Vin and Vout CE, TZ Cd=10pF td=10ps 1fC

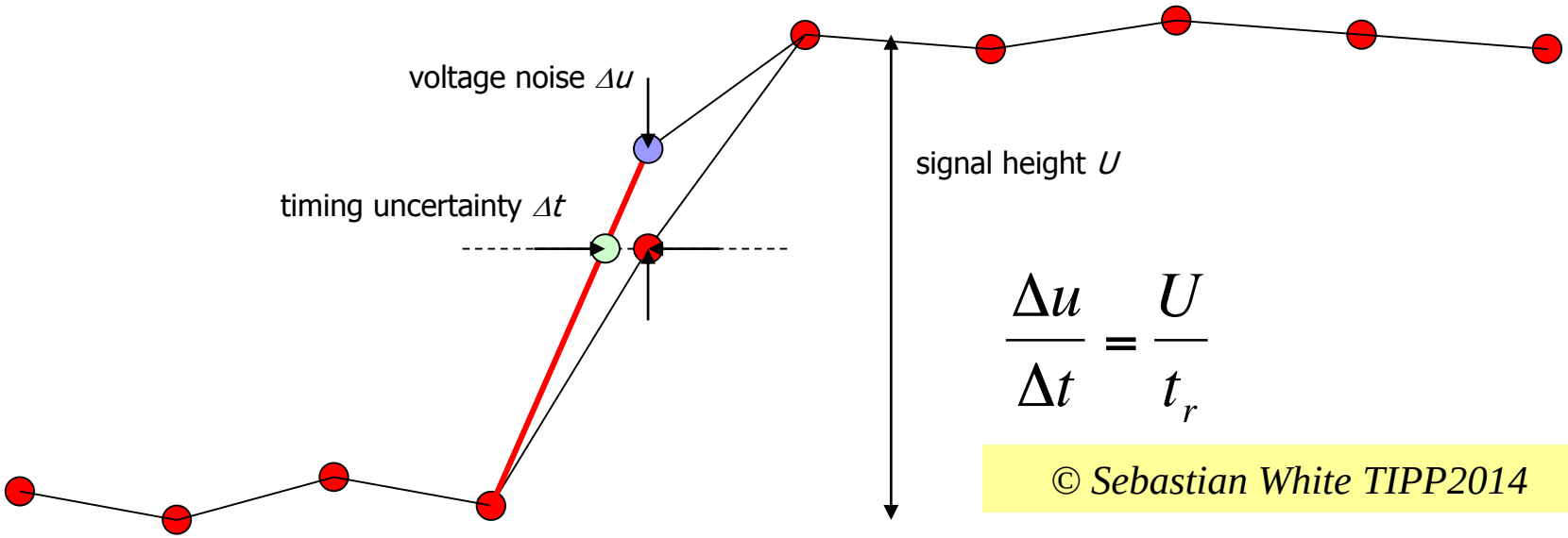


Output noise CE and TZ for Cd= 10pF 100pF





Timing with waveform samplers



$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}$$

$$\Delta t = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

Assumes zero aperture jitter

Optimistic for S/N and neglects noise autocorrelation

	U	Δu	f_s	f_{3db}	Δt
today:	100 mV	1 mV	2 GSPS	300 MHz	~10 ps
optimized SNR:	1 V	1 mV	2 GSPS	300 MHz	1 ps
next generation:	1V	1 mV	10 GSPS	3 GHz	0.1 ps