ILD & CALICE ECALs

Vincent Boudry

École polytechnique, Palaiseau

CepC WS
Roma, 25/05/2018

Silicon

Scintillators

Sponsors

The ILD model(s)

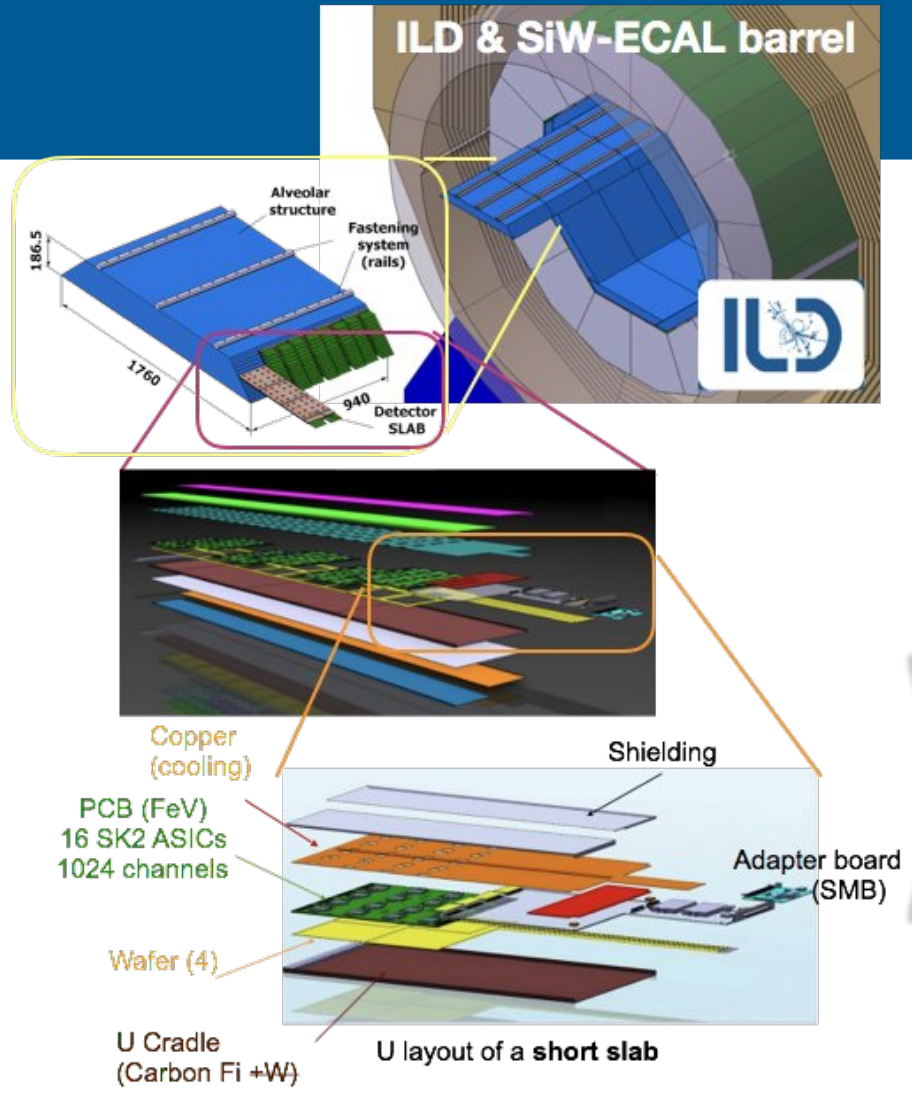
ILD “baseline” model described in DBD (2013)

- R_{TPC} = ~1843 mm
- Z_{Barrel} ~ 4700 mm
- 24 X_0 of W (thickness ~ 220 mm), R_M ~ 9mm, X_0 ~ 9 mm
- 30 layers of detection (20 single W + 10 double W thicknesses)
- Lateral cell dimension d_{cell} = 5mm

Re-optimisation of performances / cost ratio on-going

- for lower energies ⟶ 250 GeV
  - ILC @ 250–500 GeV
  - CepC @ 250, 90 GeV

  ⇒ Smaller R_{TPC}, N_{Layers}, B field



Dimension constructions (reminder)

Barrel length fixed at 4700 mm in all models, *same as HCal or TPC*

- 8 staves ⊃ 5 CF/W modules ⊃ 5 alveoli columns
- 1 alvoli width = ~ 2 × wafers width + walls + clearance

Endcaps

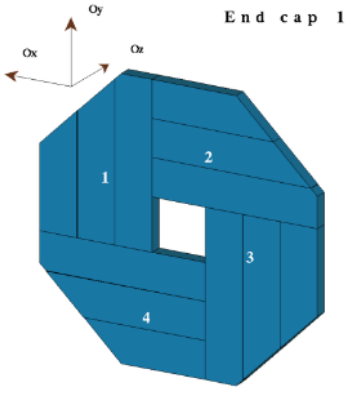
- $R_{INNER}^{EndCaps}$ fixed at 400 mm ⇒ ECal ring & Forward detectors
- $R_{outer}^{EndCaps} = R_{outer}^{Barrel}$ + overshoot
- $Z_{front}^{EndCcaps} = Z_{outer}^{BarrelL}$ + overlap

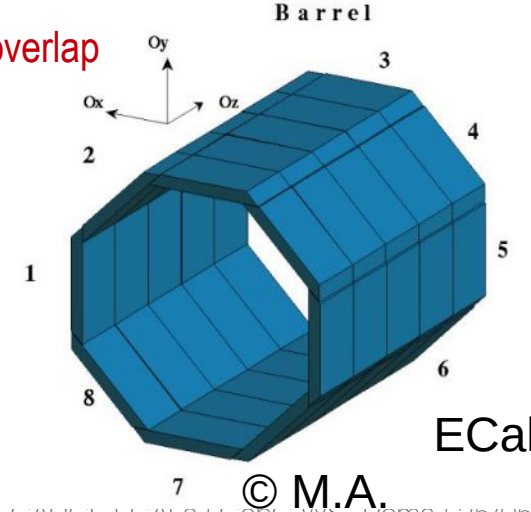
Baseline

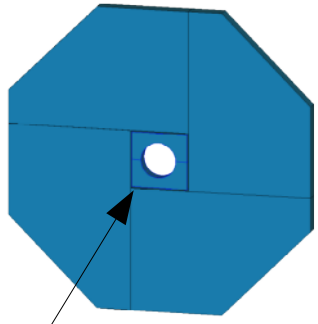
- Endcap quadrant with 3 modules of 3 alveoli

Reduced

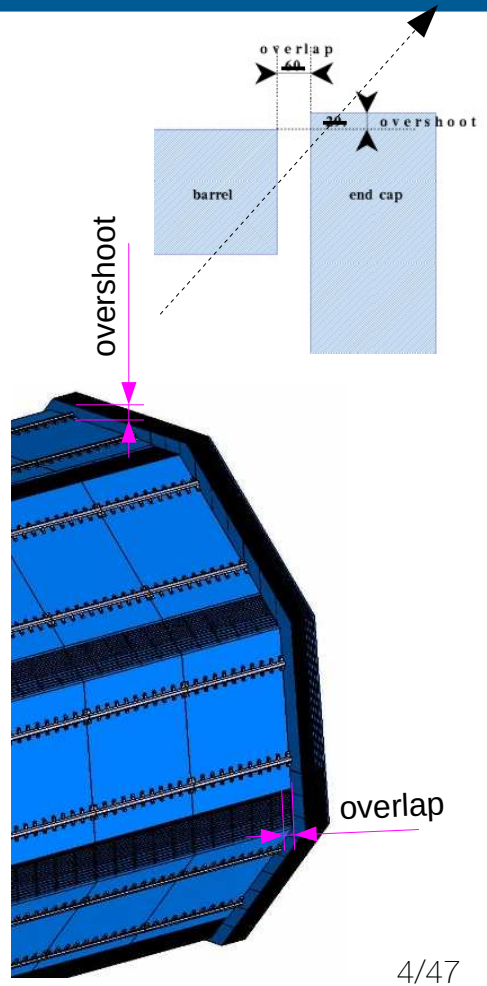
- Endcap quadrant with 2 modules of 4 and 3 alveoli







ECal ring

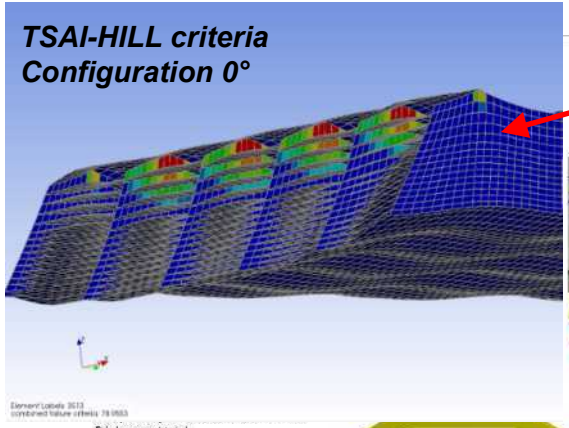


Mechanical simulations

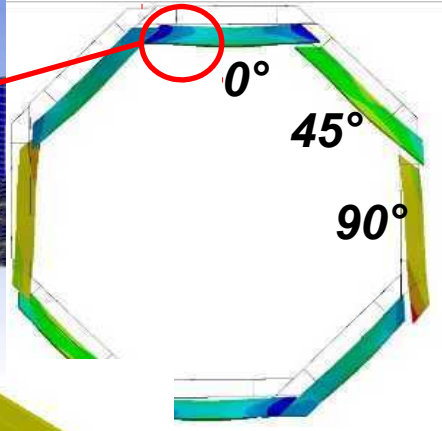
M. Anduze, T. Pierre-Emile (LLR)

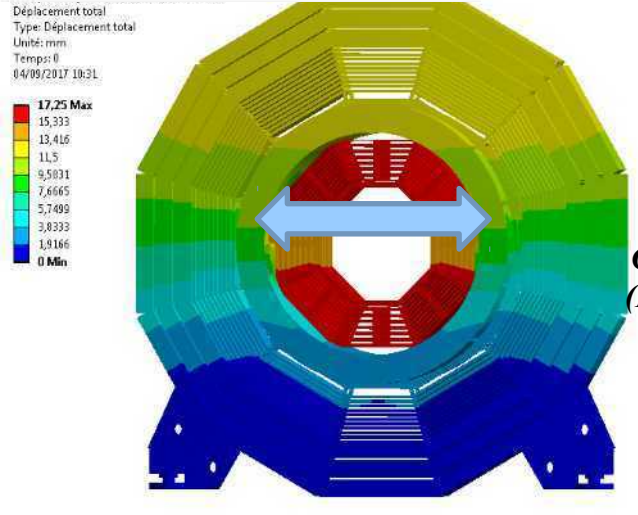
- All dimensions of the ILD prototype are defined according to FEA results in static and dynamic (earthquake) conditions and for all positions of final modules in the barrel (8 cases)
- Study of deformations and limit stresses analysis using composite criteria (TSAI-HILL) Max stresses are located on the top ribs, a strong effort is needed to define correctly its thickness
- Proposal: Study internal stresses by using new sensors : optical fiber Bragg grating sensors embedded directly within ribs (strain gauge behaviour)

Optical fiber equipped with BG sensors



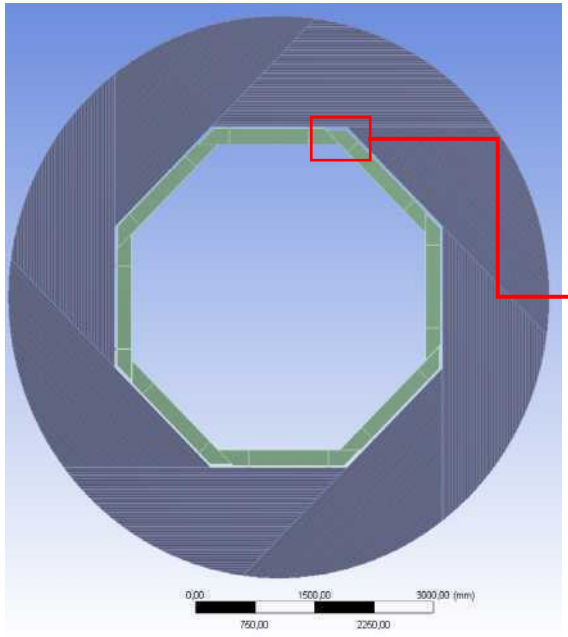
Global deformation of ECAL module (static case)

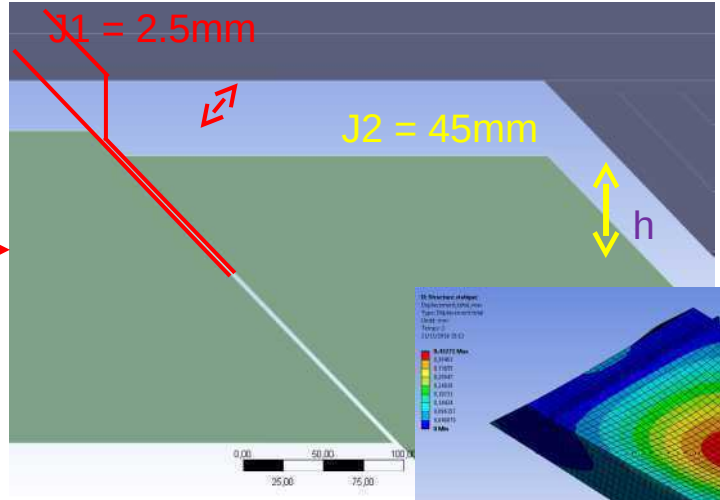




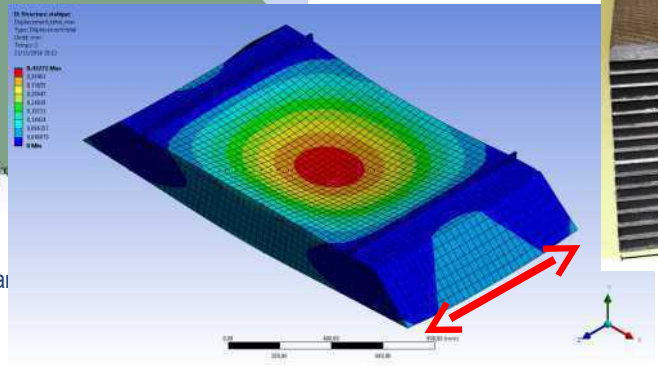
Global déformation (Response spectrum in lateral only)

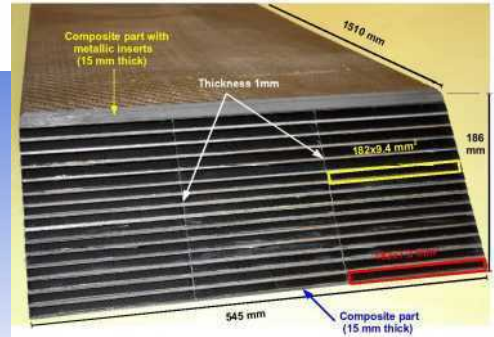
Thermo-mechanical simulations

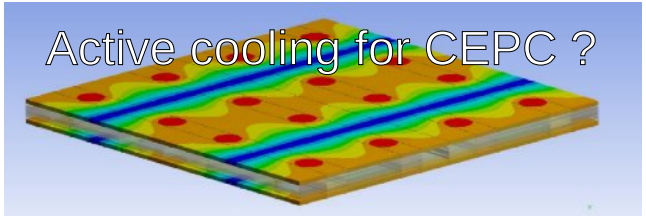


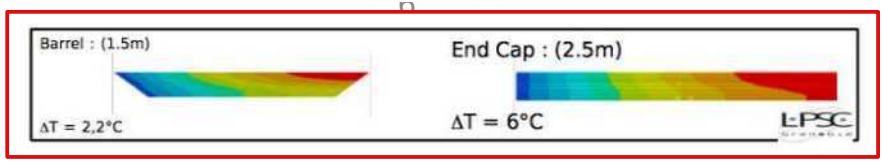


J1 = clearance between modules for the ECAL
J2 = Clearance at ECAL edges between ECAL a
h = height of the rails 30mm





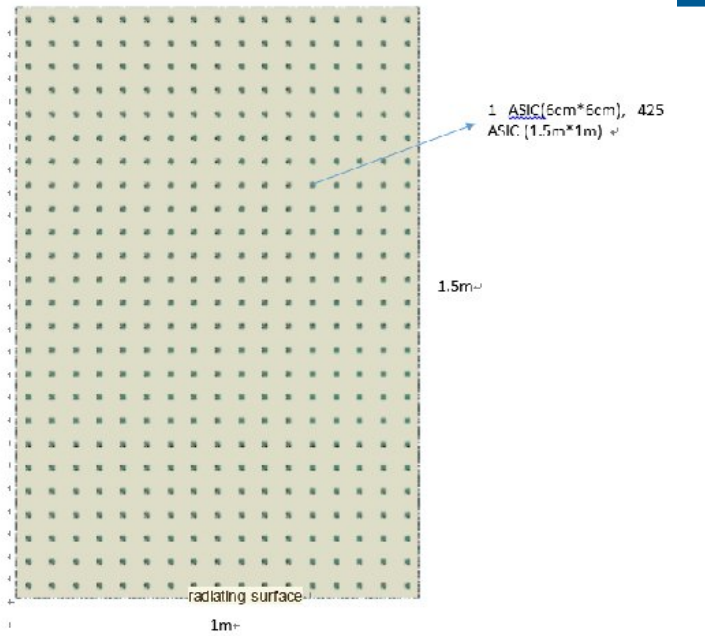




H. Videau, M. Anduze, T. Pierre-Émile
+ LPSC (D. Grondin, J. Giraud)

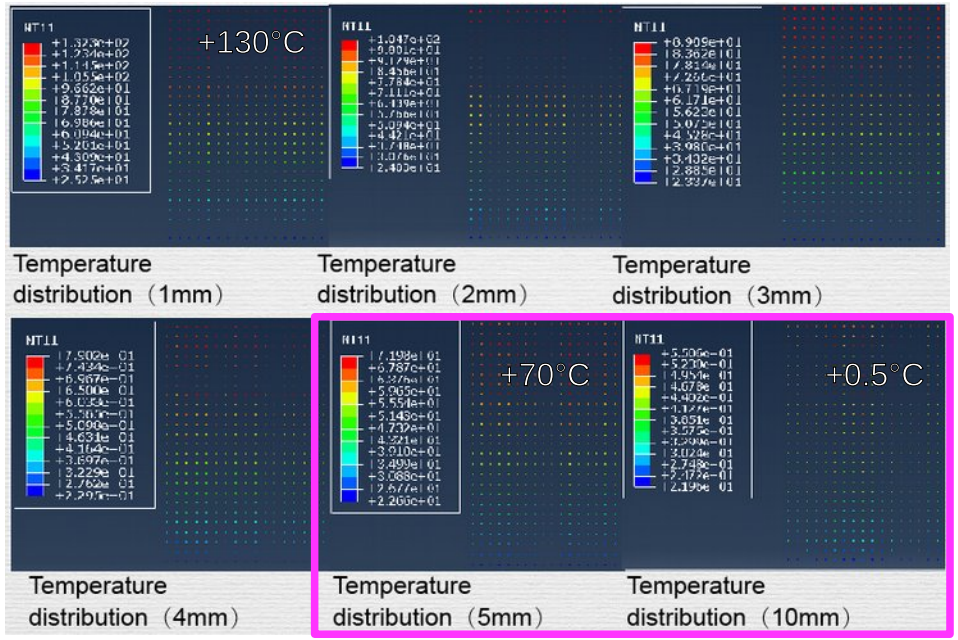
Passive cooling for CepC ECAL ? A first look...

Huaqiao Zhang (SJTU)



Thermal contact resistance :1000W/m²*K
The temperature of radiating surface: 20°C
The heat rate of 1 ASIC: 0.36W

ABAQUS FEM Simulation VERY PRELIMINARY!



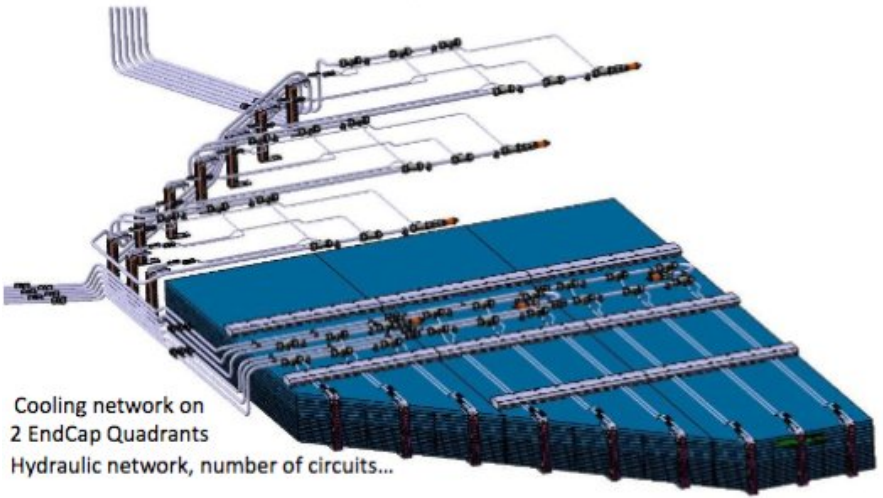
5–10 mm Acceptable ?

→ Physics Simulations

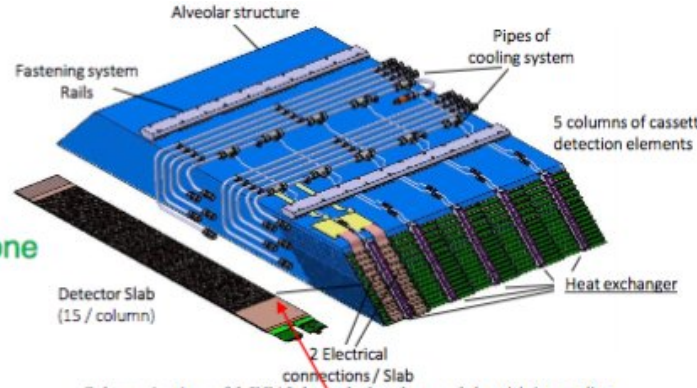
Cooling

ECAL: (CFRP+W structures + Silicon detectors)
The cooling technology is active, using fluid circulation

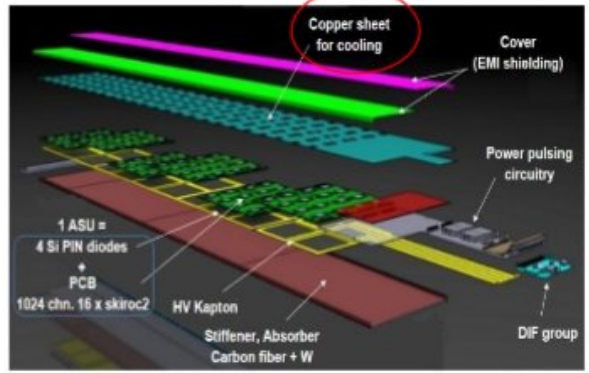
- **Tests and simulation on detector** (EUDET module)
  - Demonstration and performance of Thermal model ⟹ done
- **Integration**
  - Detailed design of cooling pipes scalable to ECAL detector ⟹ done
- **Thermal model**
  - Full Leakless System Design and Analysis: update in for estimation of global pressure drops ⟹ done



Cooling network on
2 EndCap Quadrants
Hydraulic network, number of circuits...



Schematic view of 1 ECAL barrel alveolar module with its cooling system - 10 to 15 layers of double sided integrated detector elements (SLABs) in a Tunsgten-Carbon Fiber (W-CF) support



Exploded view of half a long slab with 6 ASU – (An assembly line for long slabs with 8 connected ASU is AIDA-2020 deliverable D14.3) final goal with power pulsing 1/100 s: ECAL 4.6 Kw

ECAL Services & Cables (Baseline)

Realistic detector proposal

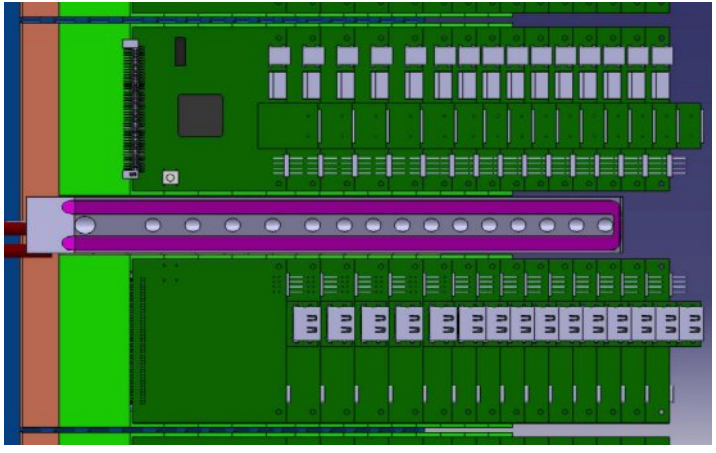
Power, cables and cooling would run between HCAL and ECAL on the back of ECAL (the way it is shown in the picture which exhibits the principle rather than any real design)

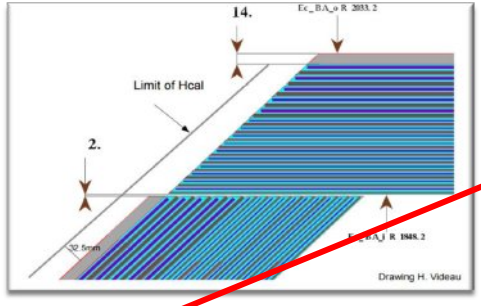
The paths of cables and cooling interfere strongly (cross).
As a working assumption the cables would run to one end of the staves and the cooling to the other end.

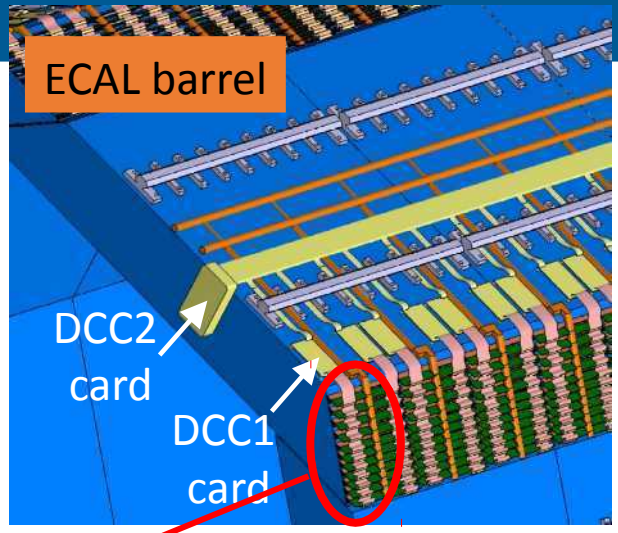
- DCC1 figures a concentration/distribution at the alveoli level
- DCC2 (or Hub2) a concentration/distribution at the stave level.

From then cables or fibres run along each sub-detectors to the outside

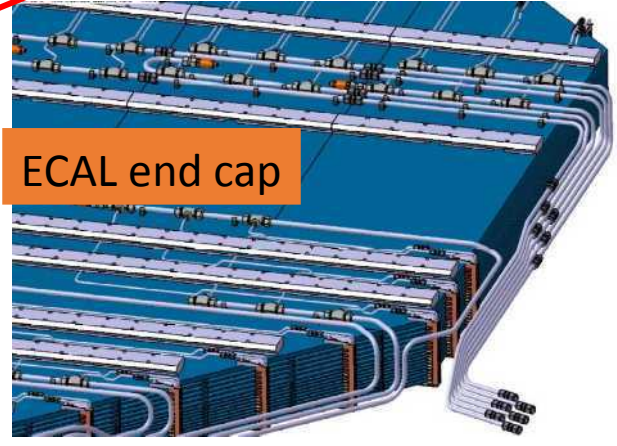
Same principle will apply for End cap cooling and cables







Pipes of cooling

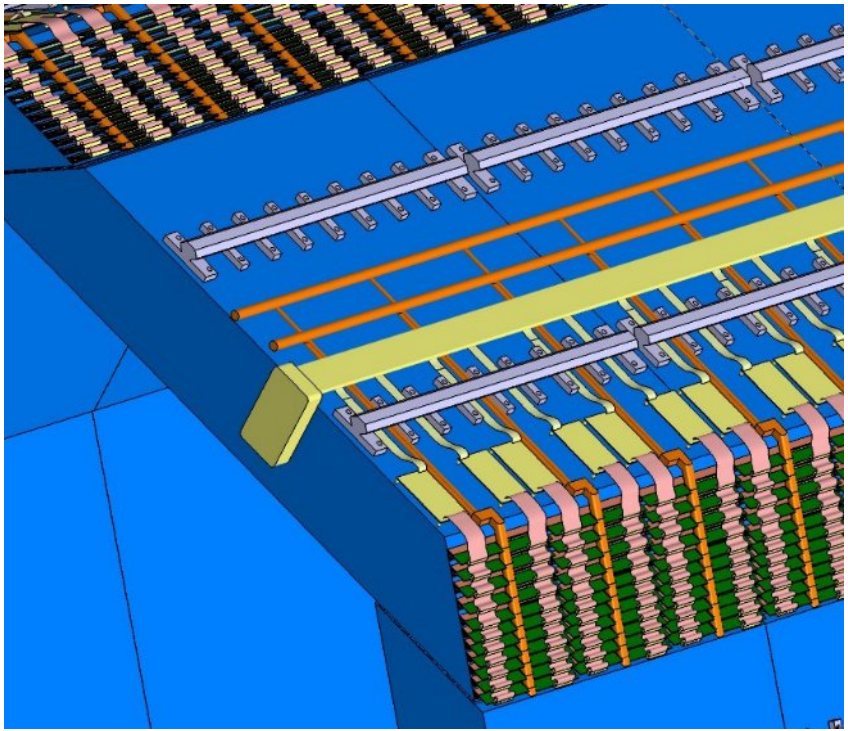


Readout for ILD

Adaptation of the prototype DAQ to ILD constraint

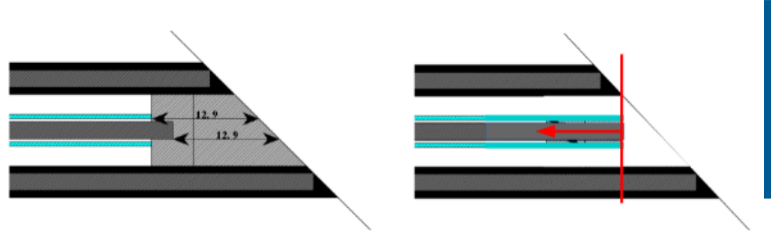
- End of SLAB
- DIF suppression / Compactification
- Redesign of the DCC's
- Reducing wires by buses or combined protocols
- HV generation inside DCC's

Redesign work started (LAL, LLR)



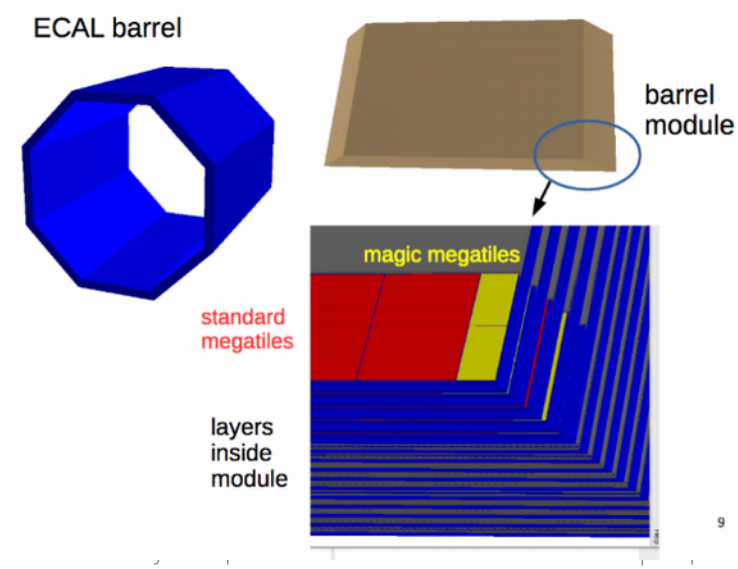
Simulation

D. Jeans (KEK)



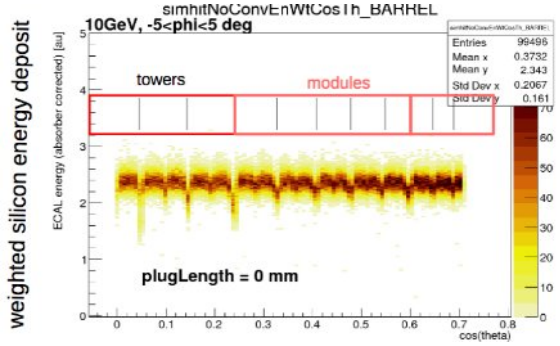
ECAL driver used in ILD models has been largely re-written (Mokka → DD4HEP)

- more modular code (less duplication Barrel & Endcap)
- more configurable…
- **Combined Sc + Si version : the other is the PCB**

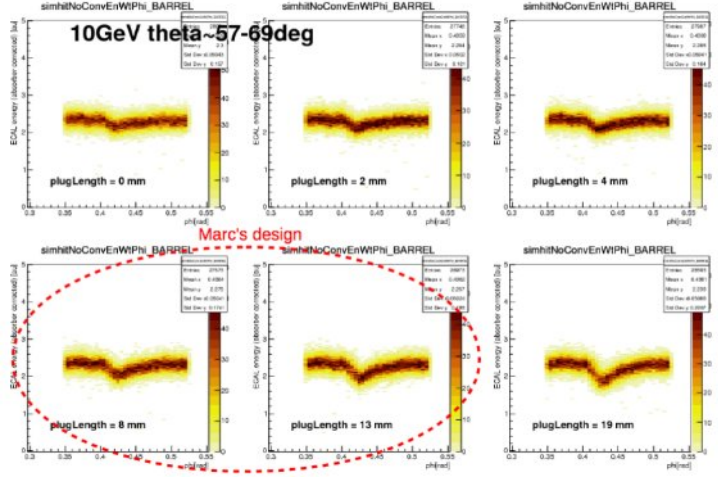


Effect of cracks [RAW= no correction at all!!]

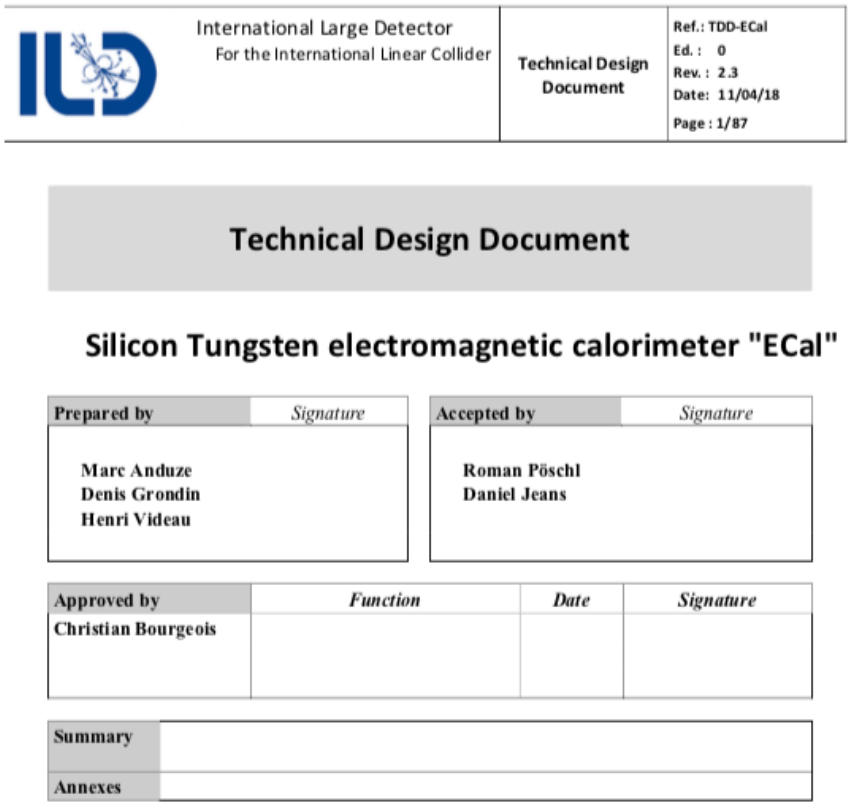
- Drop ~ 15%



Effect of plug (missing in previous simulations)



ILD SiW-ECAL Technical Design Document



International Large Detector For the International Linear Collider	Technical Design Document	Ref.: TDD-ECal Ed. : 0 Rev. : 2.3 Date: 11/04/18 Page : 1/87

Technical Design Document

Silicon Tungsten electromagnetic calorimeter "ECal"

Prepared by	*Signature*
Marc Anduze Denis Grondin Henri Videau	

Accepted by	*Signature*
Roman Pöschl Daniel Jeans	

Approved by	*Function*	*Date*	*Signature*
Christian Bourgeois			

Summary	
Annexes	

87 page document (counting)

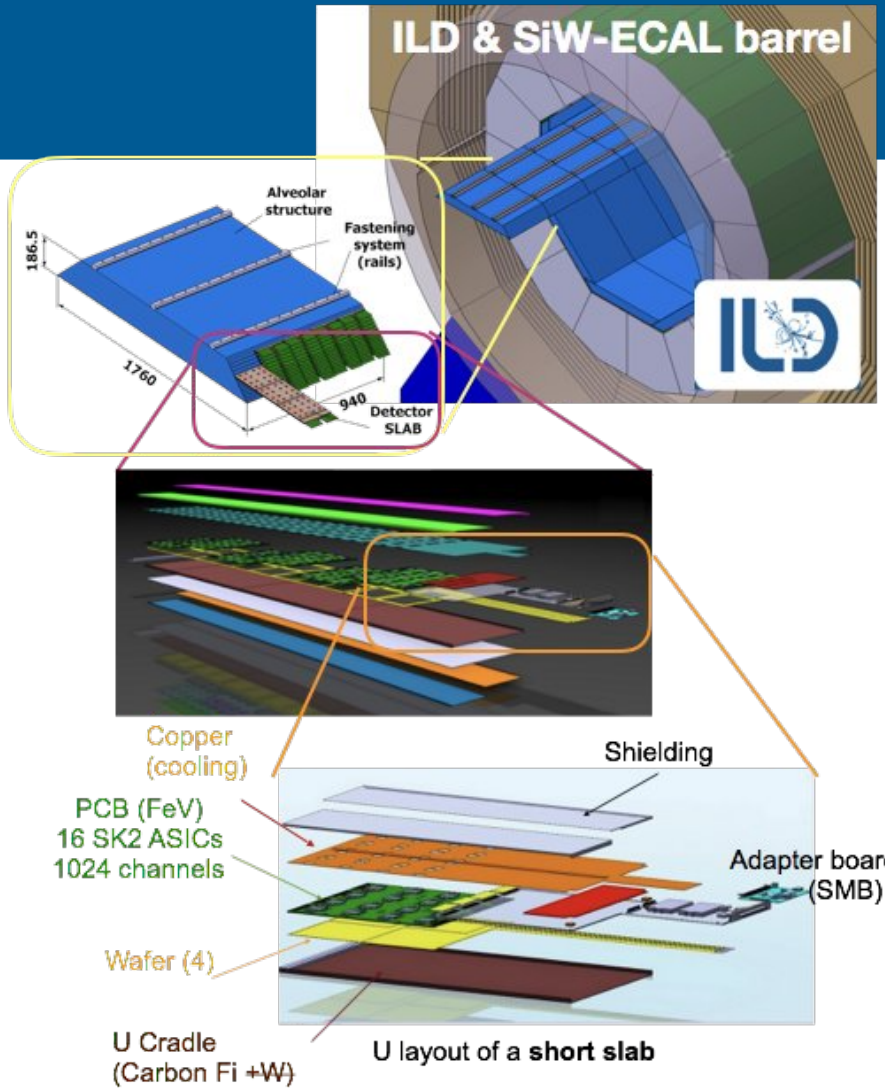
being written (near completion)
by H. Videau*, D. Grondin, M. Anduze

- 2 models: Large (R~1800) and Small (R~1600)
  N_{Layer} = 30 26
- Consolidated definitions, mechanical constrains
- Optimal use of 6" (150mm) and 8" (200mm) wafers (8")
  500 and 750µm thicknesses
- Costs
- Power & Cooling

Not (yet) in this document:

- Interfaces: DAQ, Grounding, ...

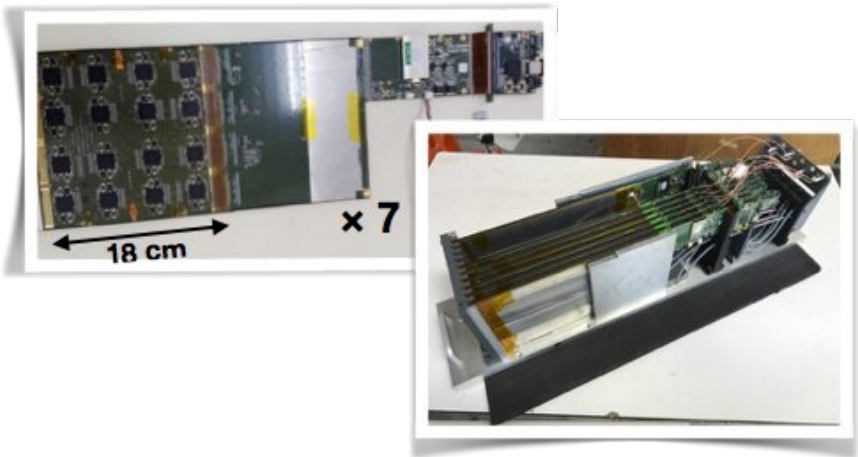
Toward SiW-ECAL for ILD



ILD SiW-ECAL	Prototyped*
~10,000 SLAB's	~0.3
100,000 ASU's	~20
400,000 Wafers	~350
1,600,000 ASIC's	~1000
100,000,000 channels	~2000/20000*

* incl. Physical Prototype

+ Mechanics , Cooling, Integration, ...

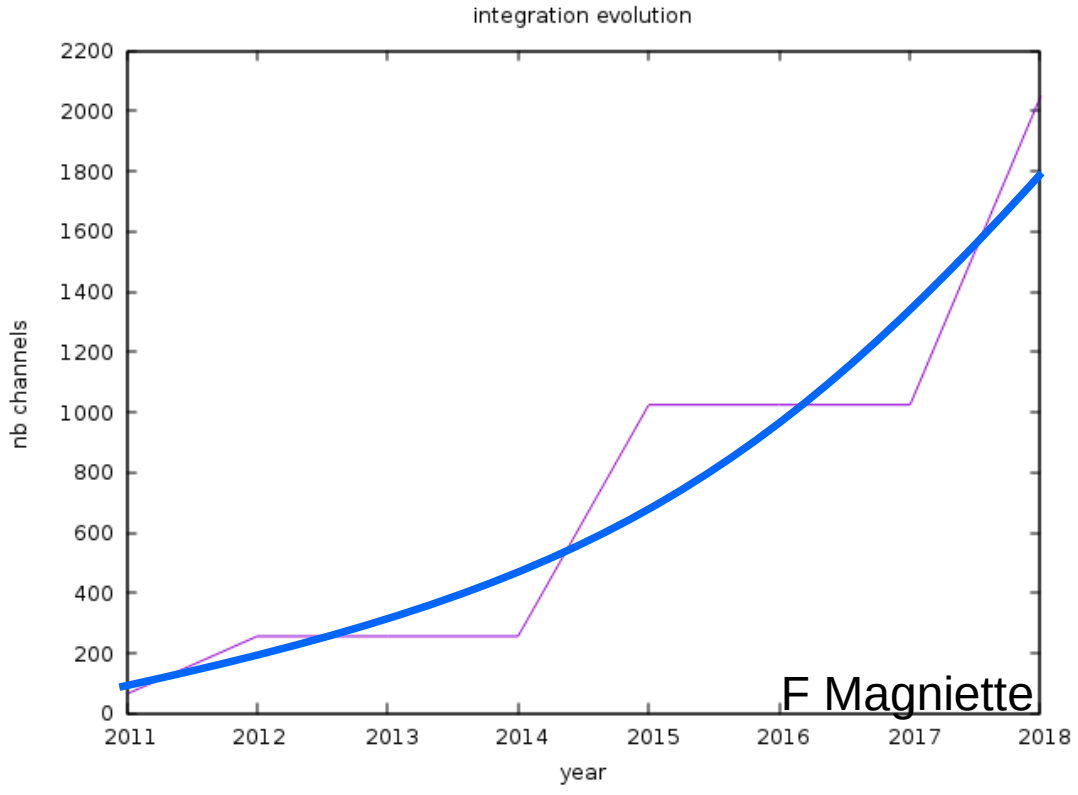


Sketch for a Historical Picture of the Progress of the ILD Silicon ECAL

Milestone	Date	Object	Details	REM
1st ASIC proto	2007	SK1 on FEV4	36 ch, 5 SCA	proto, lim @ 2000 mips
1st ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1st prototype of a PCB	2010	FEV7	8 SK2	COB
1st working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1st working ASU in BT	2012	FEV8	4 SK2 readout (256ch)	best S/N ~ 14 (HG), no PP retriggers 50–75%
1st run in PP	2013	FEV8-CIP		BGA, PP
1st full ASU	2015	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (High Gain) retrigger ~ 50%
1st SLABs	2016	FEV10 & 11	7 units	
pre-calo	2017	FEV10 & 11	7 units	S/N ~ 20, 6–8 % masked
1st technological ECAL ?	2018	SLABvFEV10 & 11 & 13 SK2a+ COB + Compact stack	SK2 & SK2a (⊃timing)	Improved S/N Timing...

Graphical progress

Number of channels

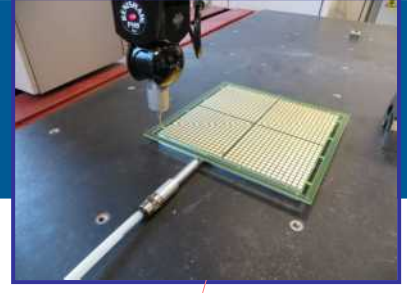


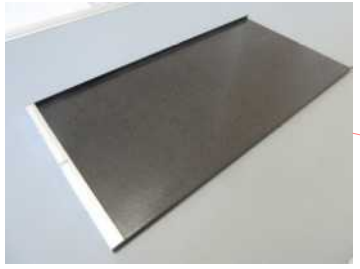
Short Slabs

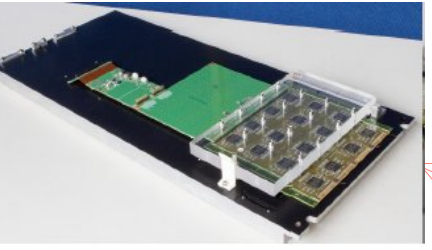
Assembly chain IdF

resp: R. Cornat

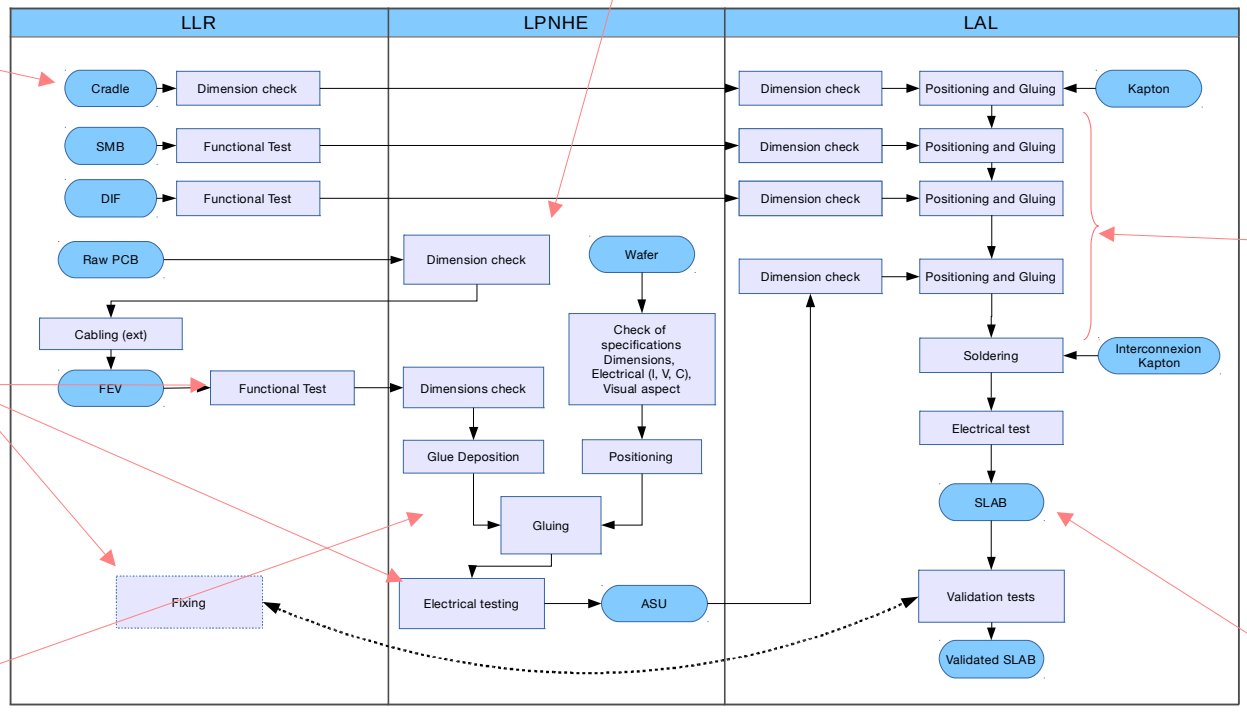
J. Nanni, M. Louzir, M. Frotin, J. Bonis, P. Cornebise, J. David, D. Lacour, S Pavy, P. Ghislain

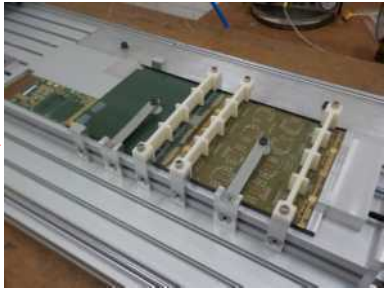






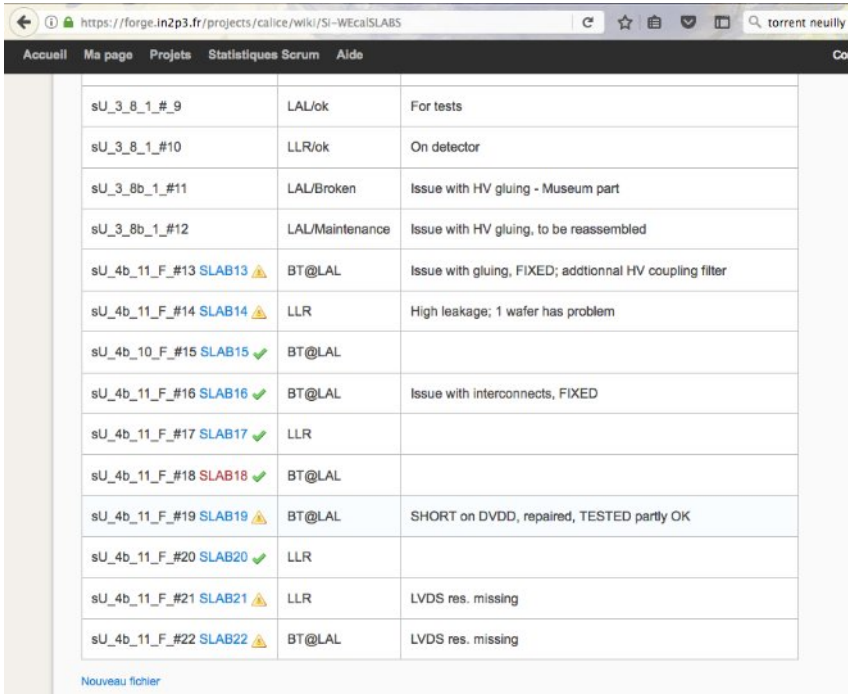
‘Simplified view’





Data-Quality: 10 SLABs produced in 2016

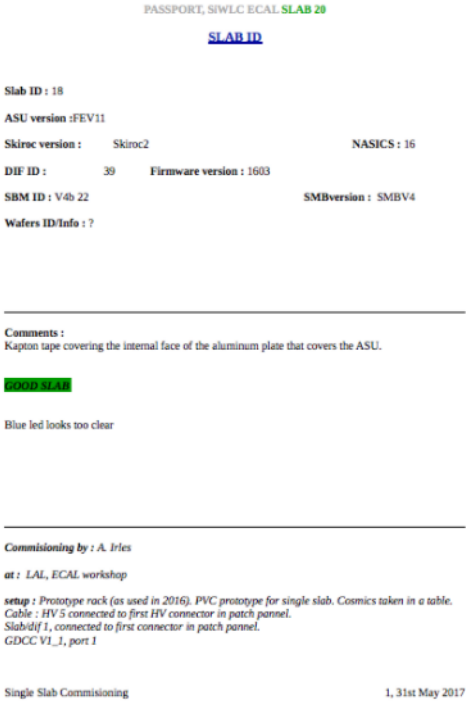
Forge Page (redmine in2p3, LLR) Boards



sU_3_8_1_#_9	LAL/ok	For tests
sU_3_8_1_#10	LLR/ok	On detector
sU_3_8b_1_#11	LAL/Broken	Issue with HV gluing - Museum part
sU_3_8b_1_#12	LAL/Maintenance	Issue with HV gluing, to be reassembled
sU_4b_11_F_#13 SLAB13	BT@LAL	Issue with gluing, FIXED; addtionnal HV coupling filter
sU_4b_11_F_#14 SLAB14	LLR	High leakage; 1 wafer has problem
sU_4b_10_F_#15 SLAB15	BT@LAL	
sU_4b_11_F_#16 SLAB16	BT@LAL	Issue with interconnects, FIXED
sU_4b_11_F_#17 SLAB17	LLR	
sU_4b_11_F_#18 SLAB18	BT@LAL	
sU_4b_11_F_#19 SLAB19	BT@LAL	SHORT on DVDD, repaired, TESTED partly OK
sU_4b_11_F_#20 SLAB20	LLR	
sU_4b_11_F_#21 SLAB21	LLR	LVDS res. missing
sU_4b_11_F_#22 SLAB22	BT@LAL	LVDS res. missing

Nouveau fichier

Files: Wafer test (LPNHE),



PASSPORT, SiWLC ECAL **SLAB 20**

SLAB ID

Slab ID : 18

ASU version :FEV11

Skiroc version : Skiroc2 **NASICS :** 16

DIF ID : 39 **Firmware version :** 1603

SBM ID : V4b 22 **SMBversion :** SMBV4

Wafers ID/Info : ?

Comments :
Kapton tape covering the internal face of the aluminum plate that covers the ASU.

GOOD SLAB

Blue led looks too clear

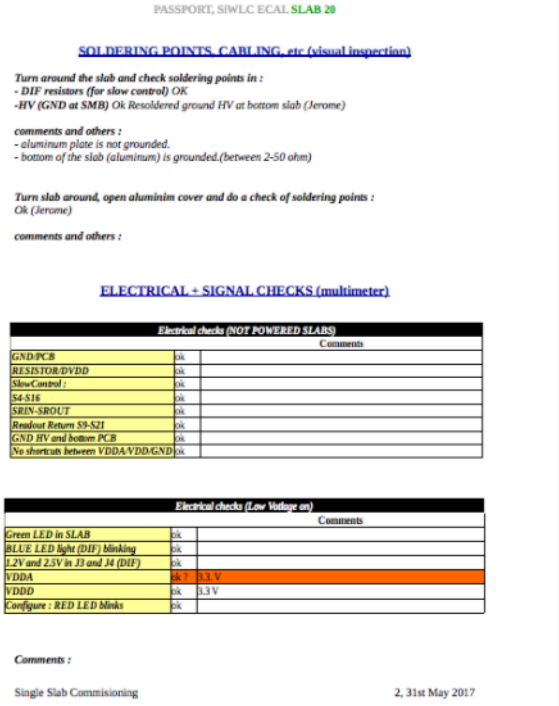
Commisioning by : *A. Irles*

at : *LAL, ECAL workshop*

setup : *Prototype rack (as used in 2016). PVC prototype for single slab. Cosmics taken in a table.*
Cable : HV 5 connected to first HV connector in patch pannel.
Slabidif 1, connected to first connector in patch pannel.
GDCC V1_1, port 1

Single Slab Commisioning 1, 31st May 2017

Passport (A. Irles @LAL) Commissioning



PASSPORT, SiWLC ECAL **SLAB 20**

SOLDERING POINTS, CABLING, etc (visual inspection)

Turn around the slab and check soldering points in :
- DIF resistors (for slow control) OK
-HV (GND at SMB) Ok Resoldered ground HV at bottom slab (Jerome)

comments and others :
- aluminum plate is not grounded.
- bottom of the slab (aluminum) is grounded.(between 2-50 ohm)

Turn slab around, open aluminim cover and do a check of soldering points :
Ok (Jerome)

comments and others :

ELECTRICAL + SIGNAL CHECKS (multimeter)

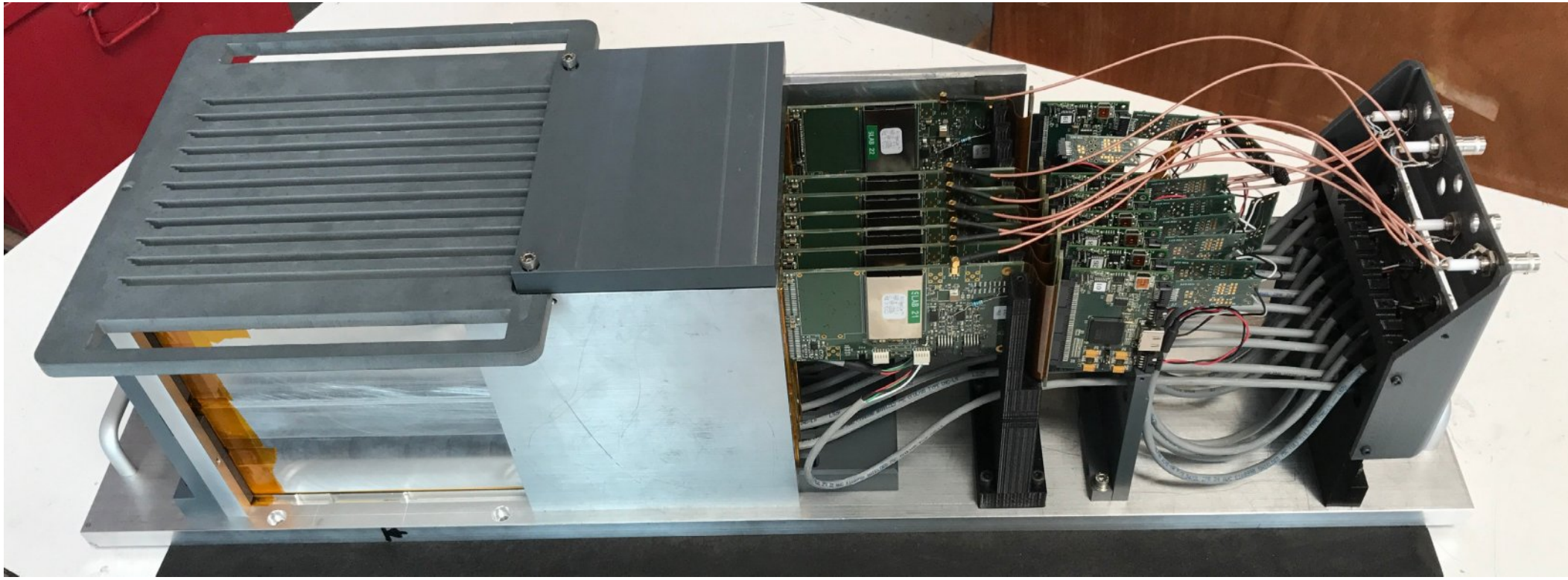
Electrical checks (NOT POWERED SLABS)		Comments
GND/PCB	ok	
RESISTOR/DVDD	ok	
SlowControl :	ok	
S4-S16	ok	
SRIN-SROUT	ok	
Readout Return S9-S2I	ok	
GND HV and bottom PCB	ok	
No shortcuts between VDDA/VDD/GND	ok	

Electrical checks (Low Voltage on)		Comments
Green LED in SLAB	ok	
BLUE LED light (DIF) blinking	ok	
1.2V and 2.5V in J3 and J4 (DIF)	ok	
VDDA	ok ?	3.3 V
VDDD	ok	3.3 V
Configure : RED LED blinks	ok	

Comments :

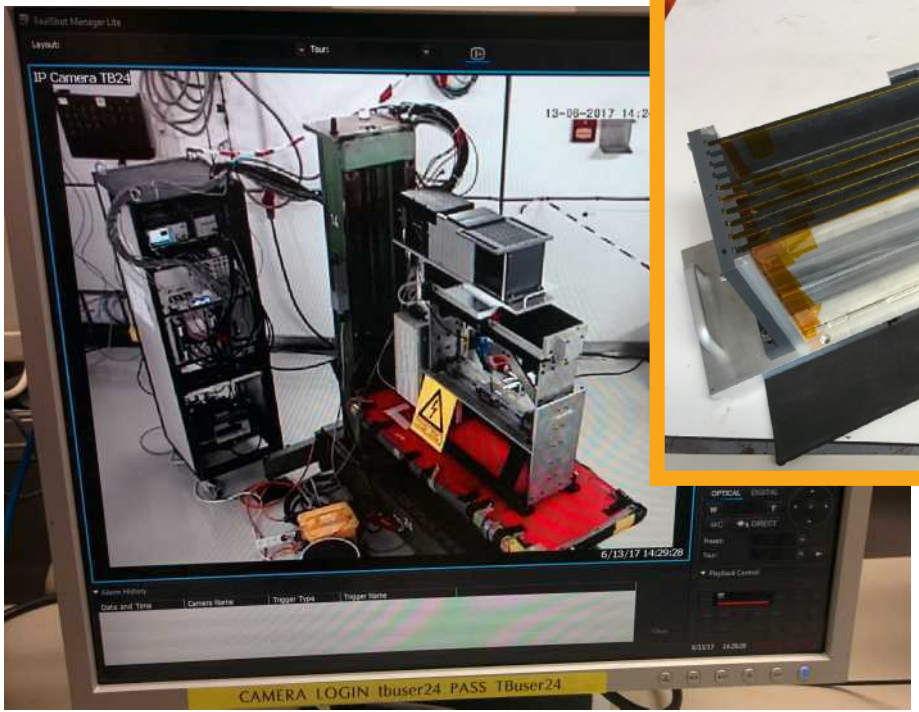
Single Slab Commisioning 2, 31st May 2017

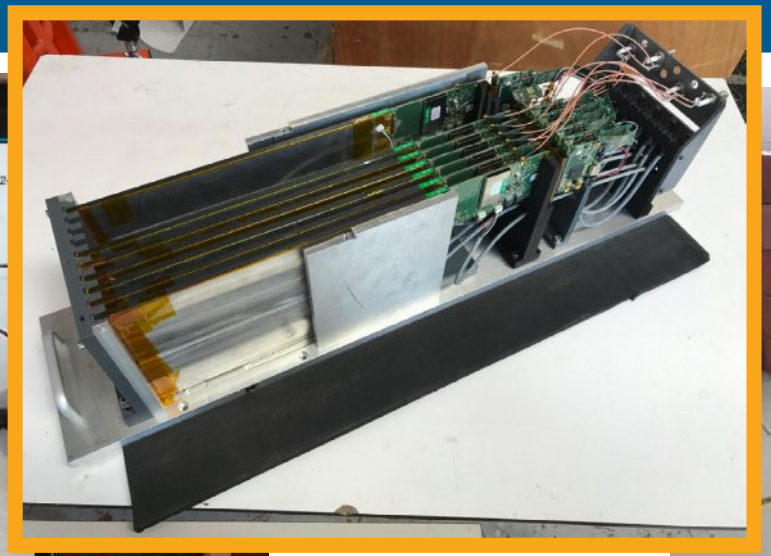
Pre-calo



Beam Test at DESY

CNRS-LLR, CNRS-LPNHE,
CNRS-LAL, Kyushu, SKKU





Beamtime 12/6/17 – 23/6/17 at DESY, AIDA-2020 TA

Detector and energy scans, plus tests in magnetic field (PCMAG)

Thanks to DESY for support

Long calibration run

A. Irles

MIP scan

- Positrons of 3 GeV (~2 kHz rate, beam spot with slightly irregular shape and size <2cm diameter)
- Grid of 9x9 points separated by 2 cm → automatized runs (movable stage commanded by pyrame)

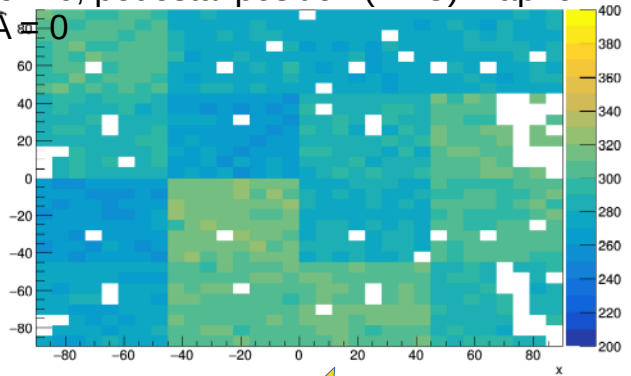
Data used for pedestal subtraction and energy calibration:

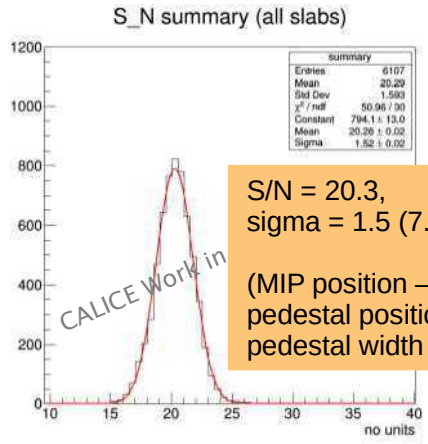
- Pedestal correction done chip/channel/sca wise (~10% var).
- Energy calibration done chip/channel wise

Fit the 98% of available channels. Channel dispersion of 5%.

Also 45 degrees inclination run: MIP value scaling as expected → good thresholds choices.

Layer #6, pedestal position (ADC) map for SCA = 0

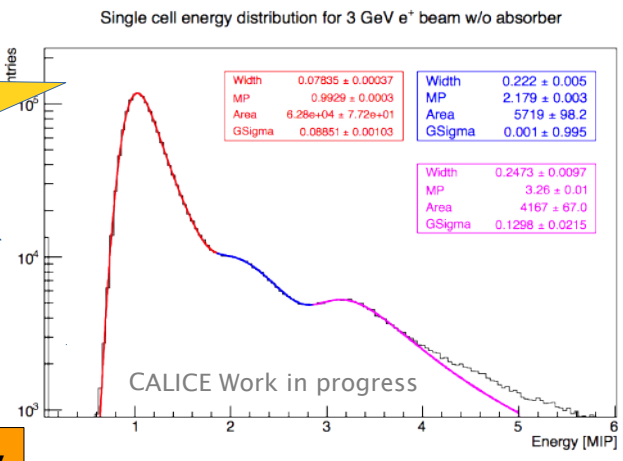




S/N = 20.3, sigma = 1.5 (7.4 %)

(MIP position – pedestal position) / pedestal width

See presentation @ CHEF 2017

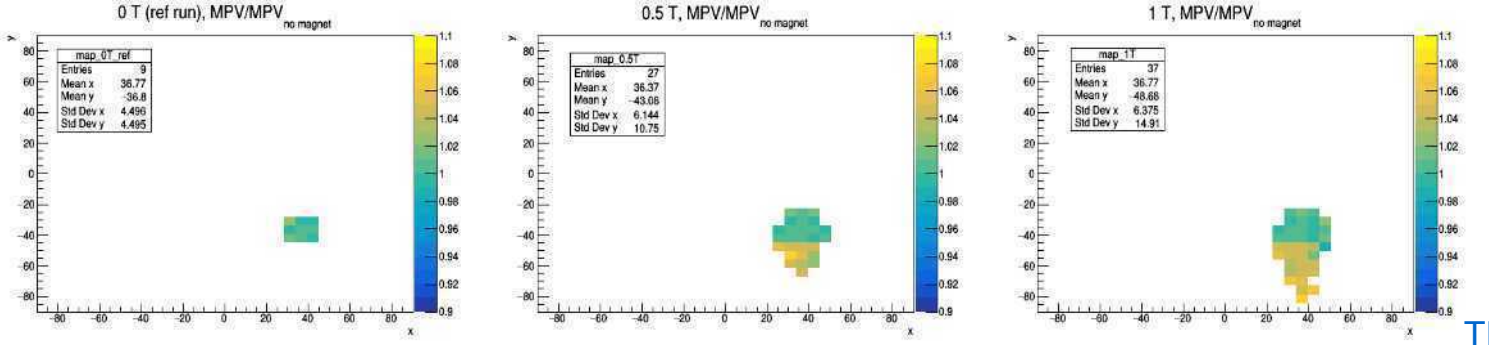


⇒ auto-trigger at 1/3 of mip with ~100% efficiency

Test in B field

Magnetic field tests

- Single Slab (21, first layer in the full stack)
- (Magnetic field from 0, 0.5, 1 T) ⊗ (With and without beam)
  - Same configuration than in the other beam area.
- Not evident failure/loss of performance during visual inspection on the web cam & online monitor.
- ~20 hours of data in total



What is still to be measured ?

Technological prototype (τ)
vs **Physical** prototype (φ)

- 4× surface density,
- ~ /2 longitudinal density
- Wafers thickness ~ /2 (320 µm vs 500 µm)
- ≠ Wafer configuration (Smaller GR, less coupl.)

Expected effects :

- Decreased capacity ⇒ lower noise
- /4 (surface) × 2 for thickness
  - S/N ~ ....
- Decreased sampling fraction ⇒ worse resolution
- Small dead zones

Energy resolution

- various W configurations
- low energy response
- High Energy response vs rate

Angular resolution

- not finalised on φ-proto

Timing

- σ(mip) ~ 1.4 ns with SK2a (on test board)
- Noise pattern for PFA studies

Uniformity: space, time

Update of PFA studies

- Separation power γ–e

Hadronic interactions (×4 in lat gran.)

New FEV13

F. Magniette, J. Nanny, R. Guillaumat, M. Louzir, V. Boudry (LLR_), R. Cornat (LPNHE), S. Callier (Omega), T. Suehara (Kyushu),

Expert review of FEV11 after BT

⇒ 15 points of improvements being implemented:

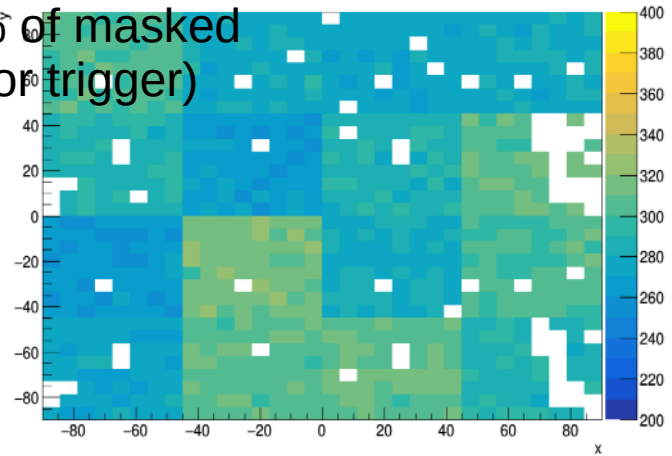
- Low noise design: differentiated analog supplies, data routing, phasing of clock, new decouplings...
- Unique Tag, PT100, …
- FW: Clock Freq, UDP, sync of EventID, …
- Optimized routing to avoid long paths

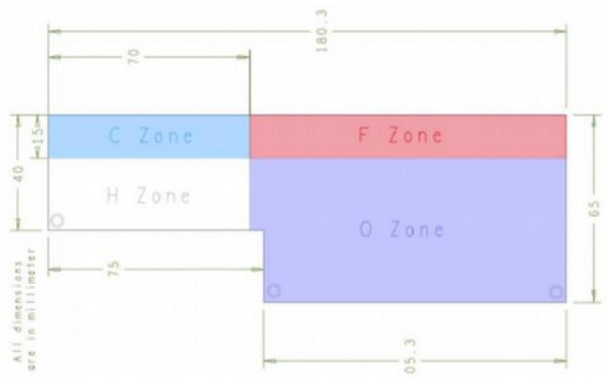
thin connectors (compatible with ILD-like design)

Adaptor board: new design (SMBv5)

- to be produced by Kyushu

8 – 4 % of masked chan (for trigger)





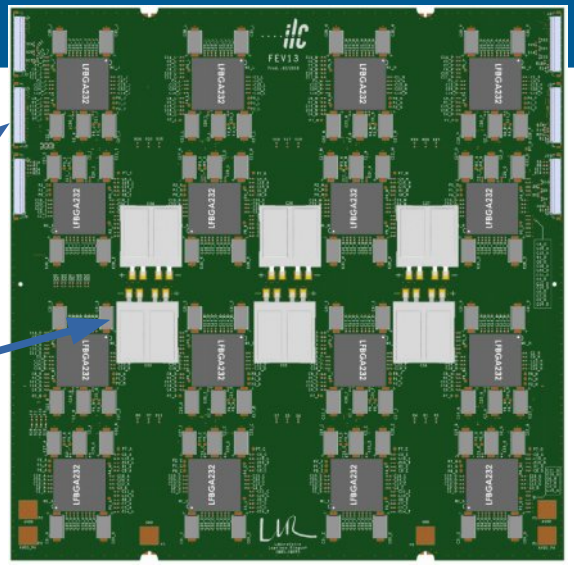
new PCB's

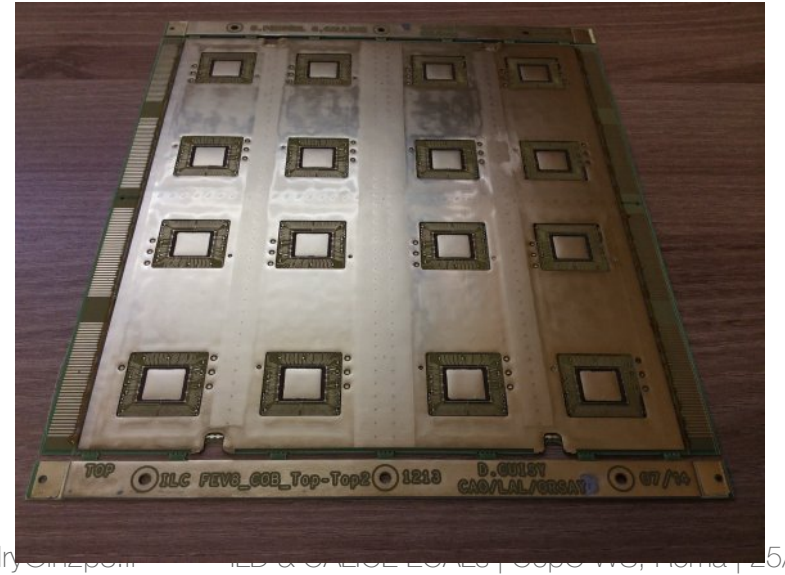
FEV13: 1st batch scheduled for end of March (delayed)

+ 2–3 weeks of cabling.

Connectors on one side

Ultra-Thin capacitors





FEV-COB (Chip-On-Board): produced by SKKU

Bounding by CERN

being commissioned (LAL)

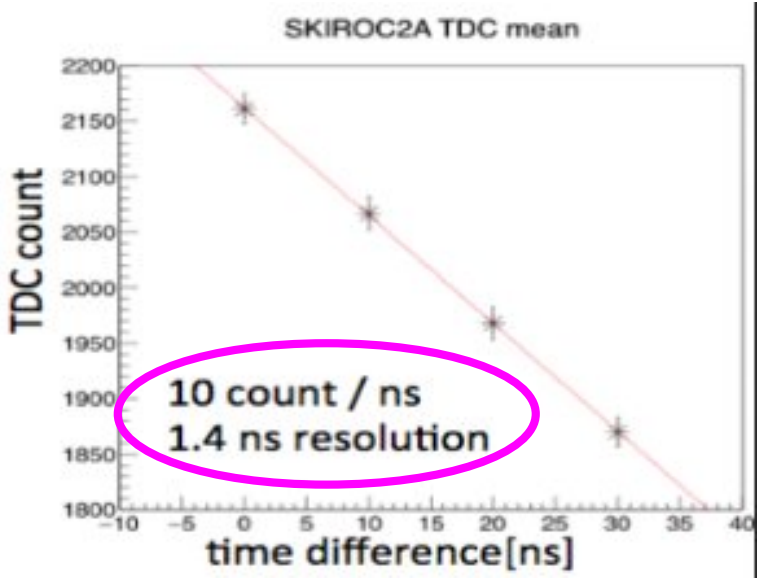
Additional production of shorts SLABs in 2018

2016-17: **10 ASU's produced**: 325 µm Wafers + FEV11 + SK2: *7 OK for physics*

- 3 SLABs are broken (bef. Beam test) : 1 broken, 2 too noisy (1 after manipulation) ⇒ **To be repaired** (if possible)

Material is available for **additional production**

- **Wafers:** 10 ordered by LPNHE from HPK (**525 µm**) + 25 @ LLR + new production in Kyushu (**650 µm**) (~20)
- **ASICs:** ~230 SK2a packaged and tested.
  - include ~1.5ns time resolution; pin-to-pin compatible SK2
- **PBC's**
  - FEV13 ~ 5 units ?
  - **FEV11_COB** ~ 2 units ?



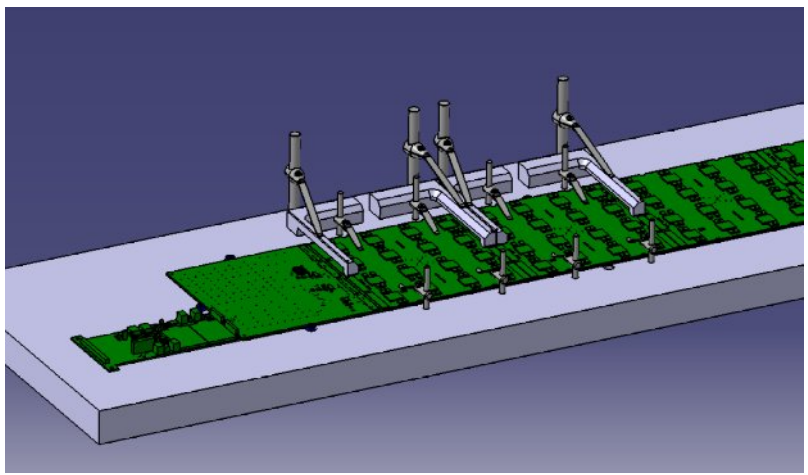
Long Slabs

Test benches for Long Slab

Mechanical @ LAL

– Precision needed

Cumulative errors ⇒ need for positioning



Electronics @ LLR

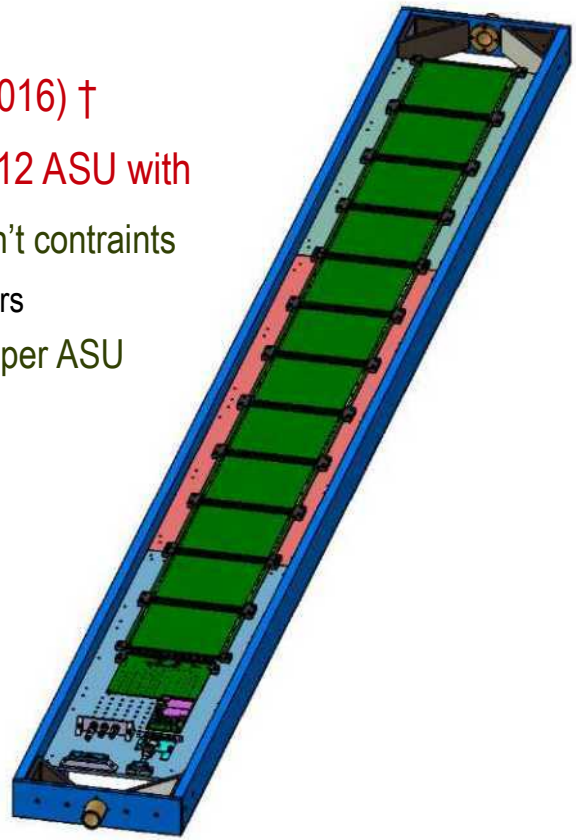
– 4 ASU set-up (2016) †

– New one ⇒ 10-12 ASU with

- no space /align't contraints

  ⇒ Connectors

- 1 baby wafers per ASU



Mechanical assembly chain for long SLAB

J. Bonis, A. Thiebault

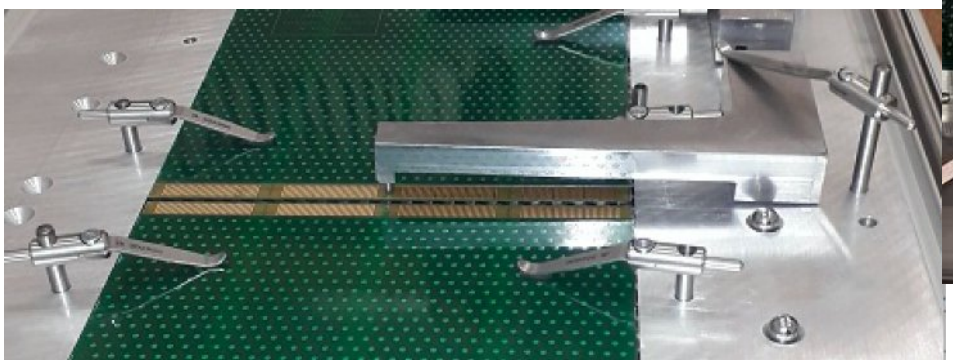
Gluing on HV Kapton & Soldering of

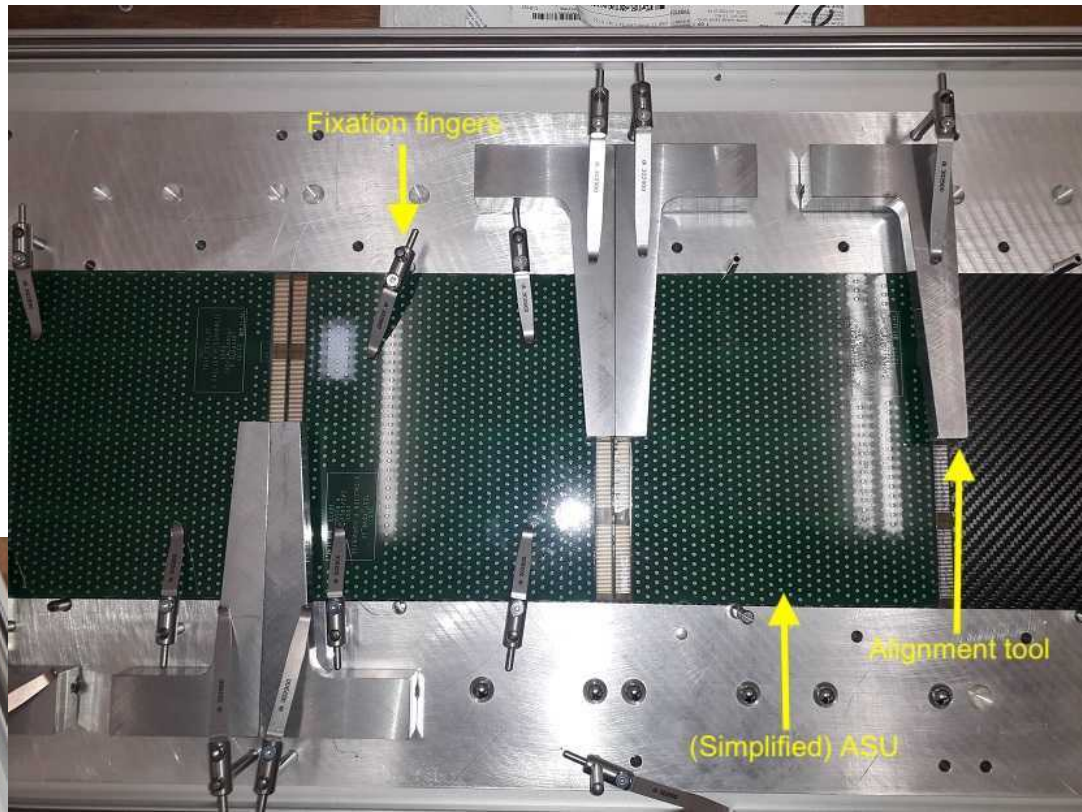
- 8 ASU's of 180.3 or 180.5 mm.
- in U-shape carbon-fibre cradle *or* on simple carbon plate. (181.4 ± 0.3 mm)

Alignment of two ASU wrt each other :±0.1 mm, Straightness deviation of 0.1 mm.

In test phase with simplified ASU's

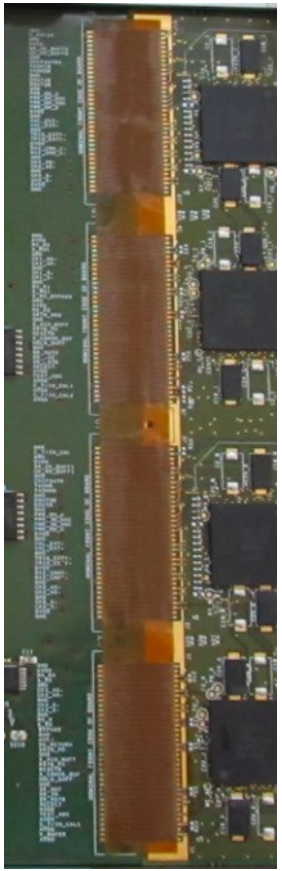
using pick-and-place manipulator





On interconnection

J. Bonis, A. Thiebault,
J. Jeglot



Interconnection is maybe the most involved piece of the assembly

Current solution with Flat Kapton + Iron Soldering works → Short Slabs

- But… Interconnection so far made by hand & Delicate work

Application for long slab requires automatised (robust) procedure

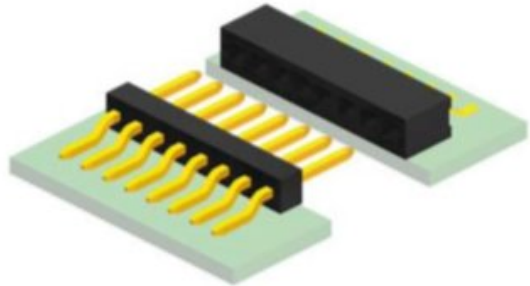
- difficulties to find supplier for developing such a procedure…

Test of GradConn (Taiwan) connectors

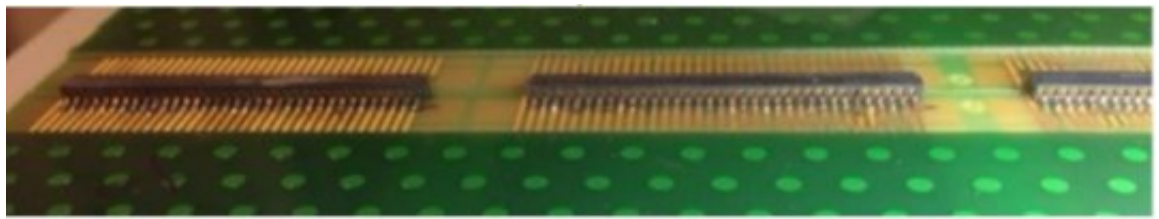
- BB02-YN series: 35 pins, a pitch of 0.1 mm
- height 1.5 mm (1.27 mm are also available).
- 1 A at 300 V AC.

Under tests…

- No defect found (yet)
- mechanically sound



GradConn connectors
(from Taiwan)



New design for "electronic long slab support"

M. Anduze, F. Magniette, J. Nanni,
Realisation: G. Fayolle

Scale to support electronics

- 2+6+4 ASUs = ~3.2 m
- Support of SMB
- Total access to upper and lower parts
  - Baby wafers (4×4 pixels) on the bottom

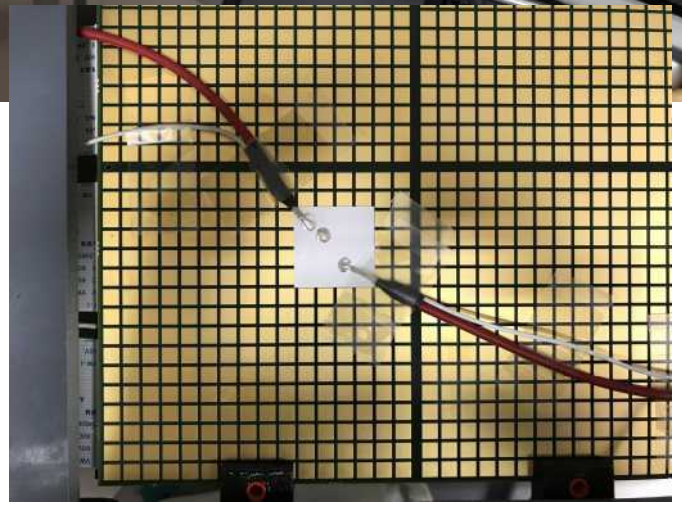
Mechanical characteristics

- Movable: table and to beam test
- Rotatably along long axis (for beam test)

  Rigidity : ≤ ~1 mm per ASU
- No electrical contacts scale / cards

Shielding

- vs Light and CEM



‘Electrical’ Long Slab

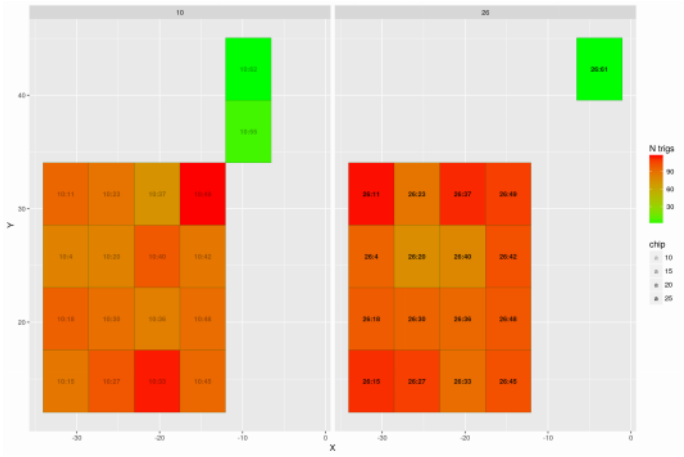
G. Fayolle (LLR)

2 ASUs mounted – up to 12 expected

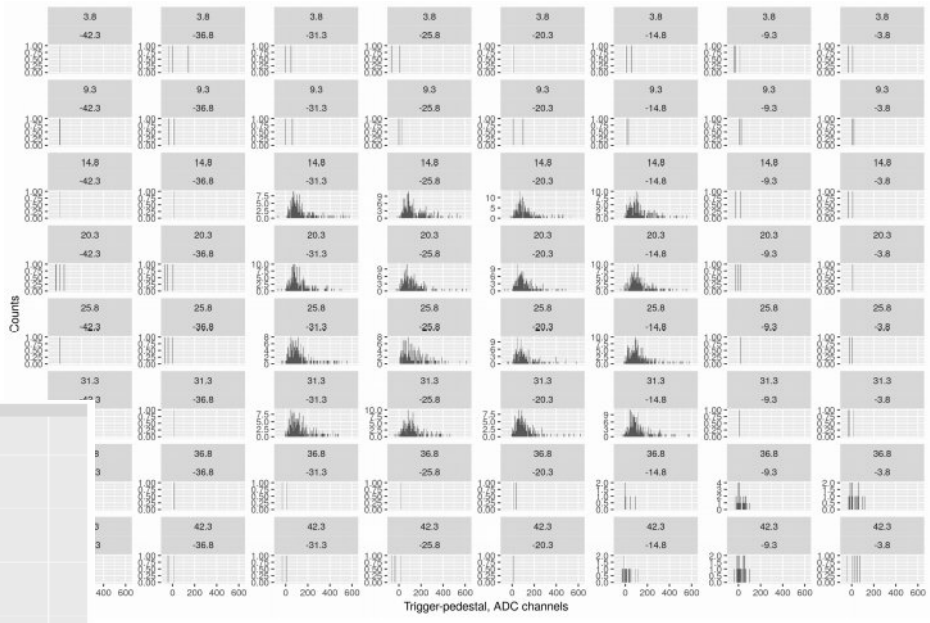
- Added one-by-one
- Equipped with baby-wafer (4x4)
- Hood for light protection
- Handling structure for beam-tests

Cosmic run

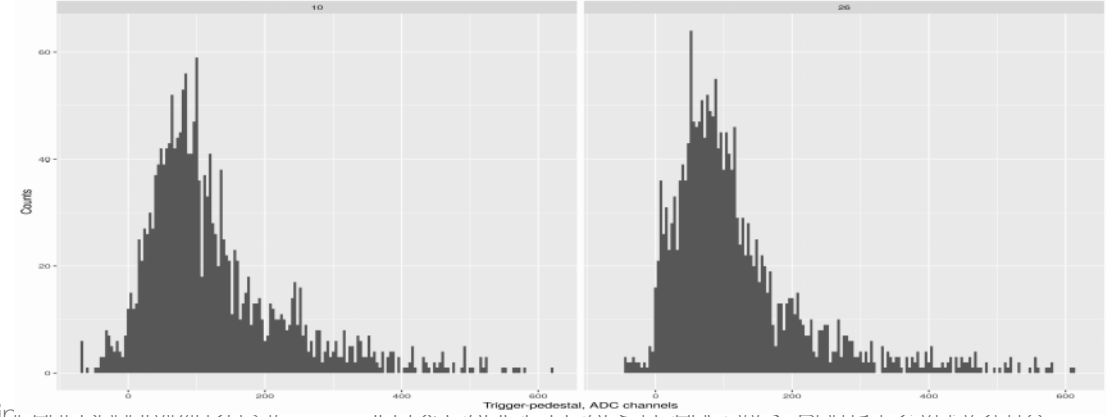
Trigger map



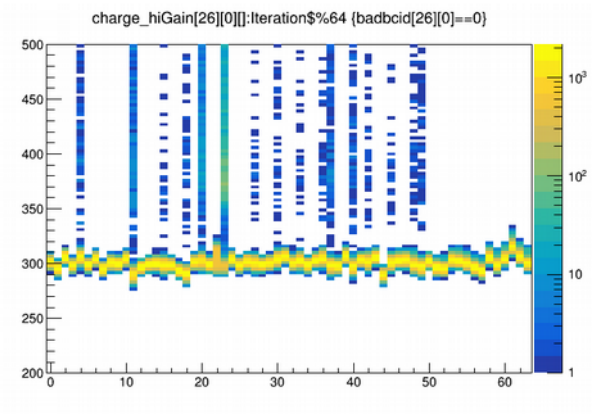
ADC map single CHIP

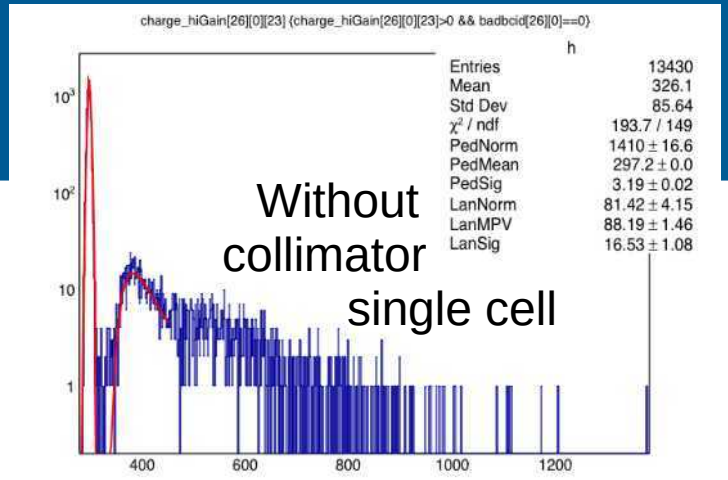


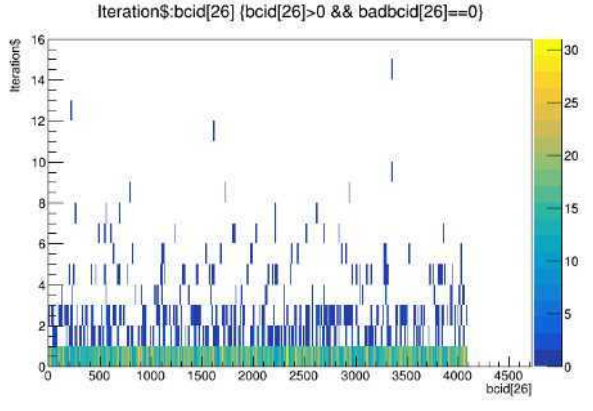
All cells per chip

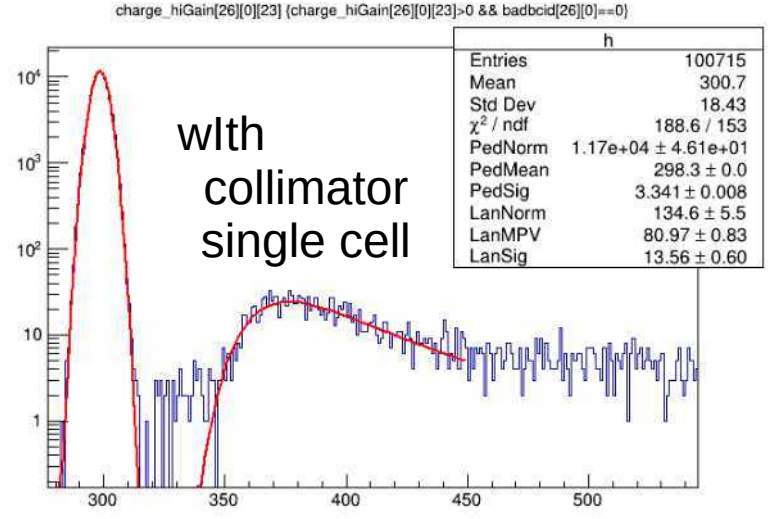


Test with ^{90}Sr source









Some prelim conclusions:

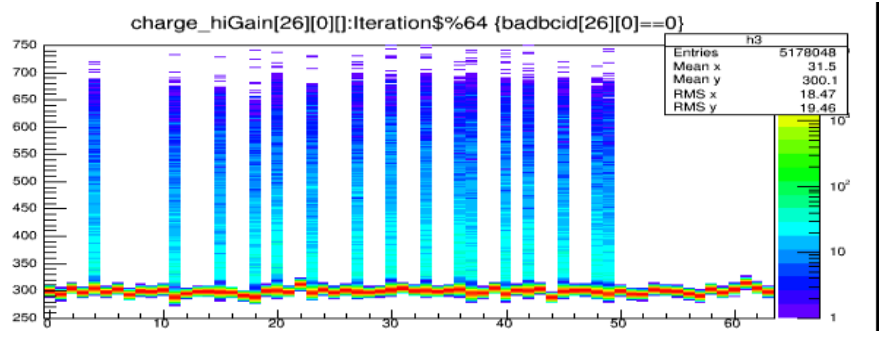
- Perfect noise cellwise
- punch through electron ~ mip like
- Signal is ~30% higher than in BT (scattering)

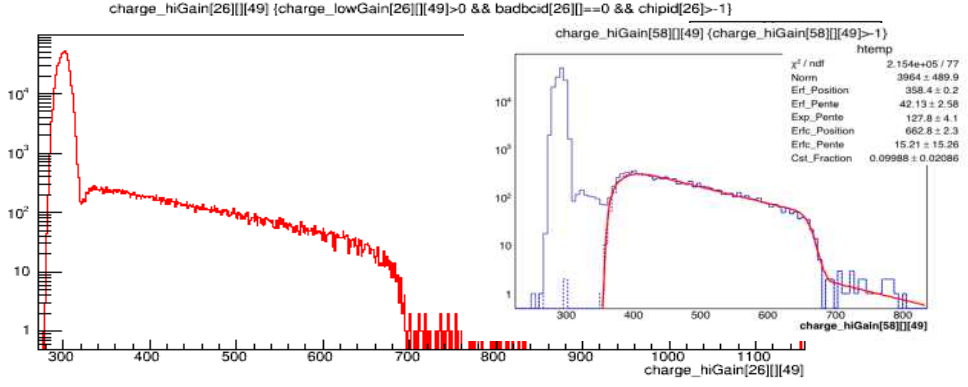
OK for additional ASU's

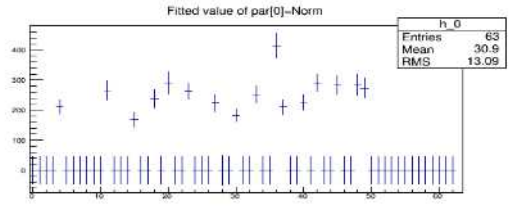
Test with 137Cs source

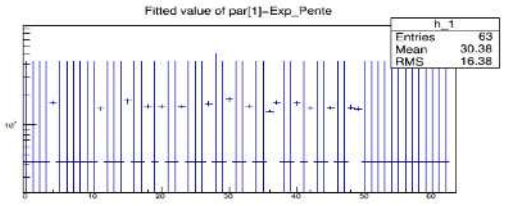
$^{137}Cs \rightarrow {}^{137}Ba^{*} + ß$;

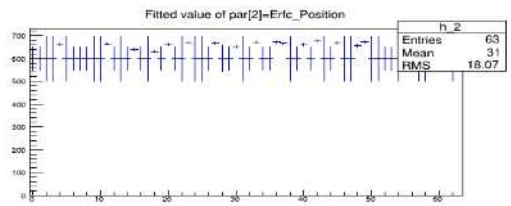
$^{137}Ba^{*} \rightarrow {}^{137}Ba + \gamma$ (662 keV) or X (32keV)

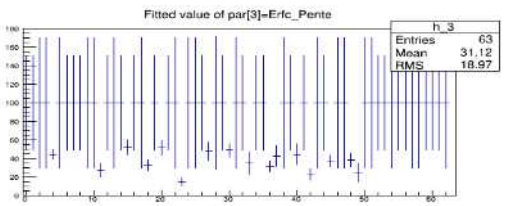


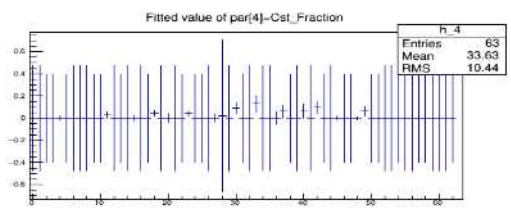


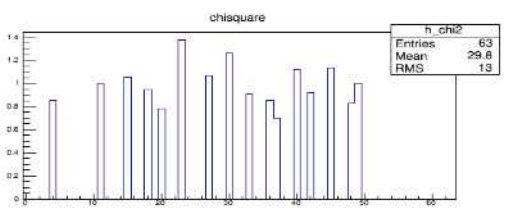












Spectrum in hours with 250kBq source

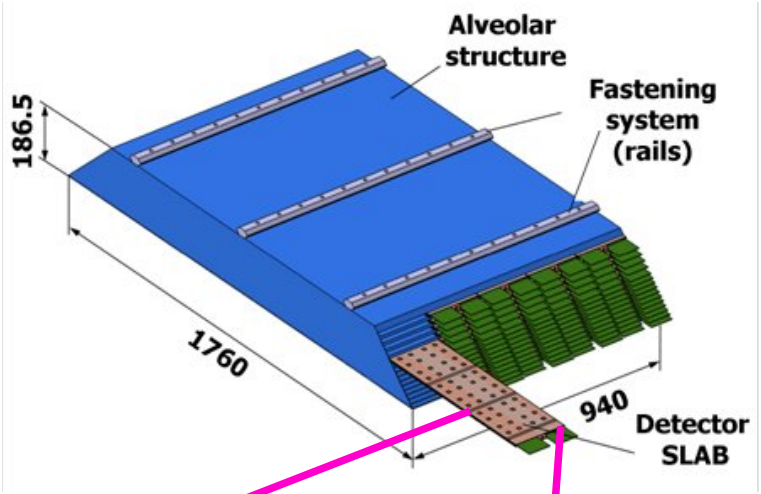
– calibration at 6 mips in all chans + pedestal

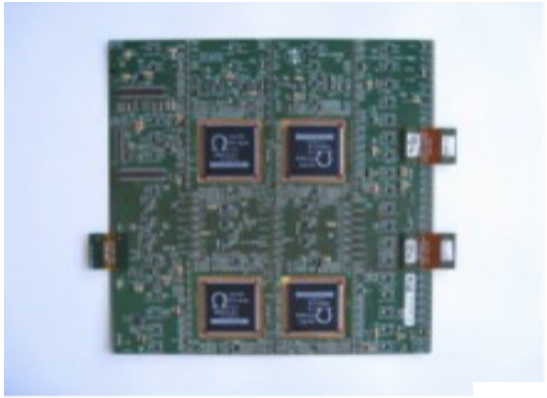
To be tested with 37 MBq source

Scintillator ECAL

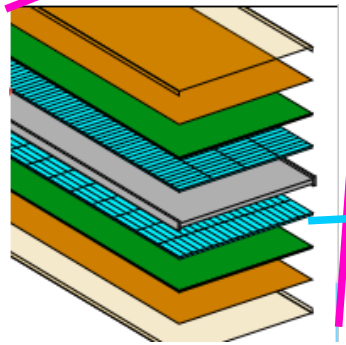
Scintillator option

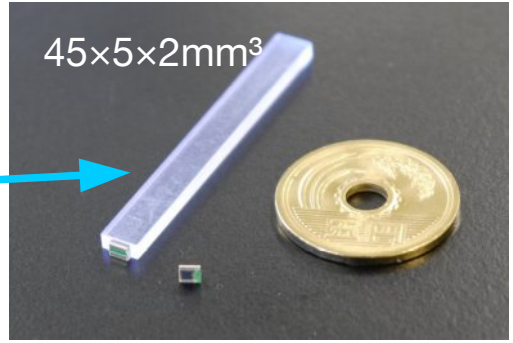
T. Takeshita

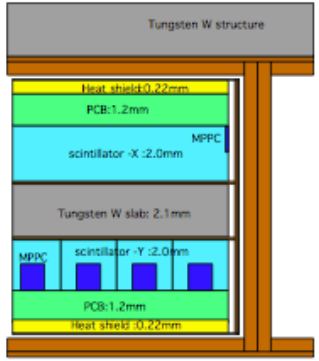




based on CALICE AHCAL board with SPIROC





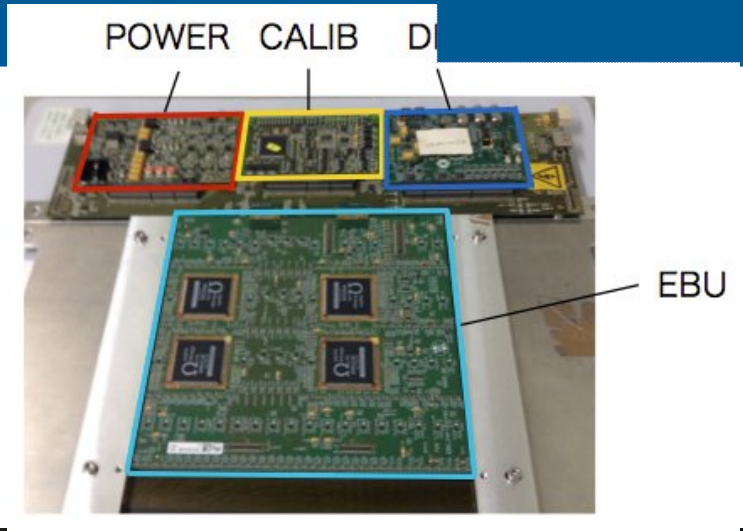


EBU: ECAL base unit

T. Takeshita

1 EBU =

- 144 strips in 18x18 cm2 unit (EBU)
- four ASICs (SPIROC2b 36ch)
  - Amp/shaper/ADC/memory
  - auto-trigger mode with threshold setting!
- bias voltage control
- LEDs for calibration purpose



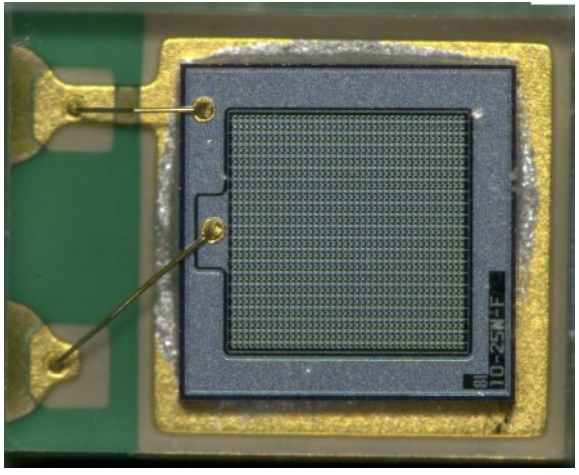
MPPC : Dynamic range & Noise

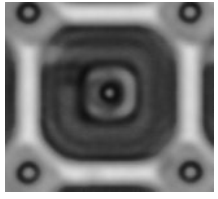
T. Takeshita

max energy/strip ~<1500 MIPs at 500GeV for Bhabha events

~ needs 10000 pixels (7p.e./MIP)

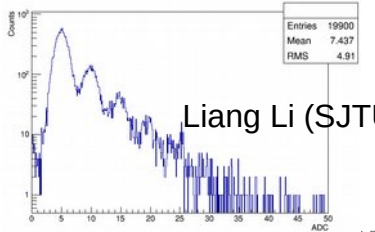
- 10μm pitch in 1x1mm² =10kpix
- 15μm pitch in 1x1mm² ~ 5kpix

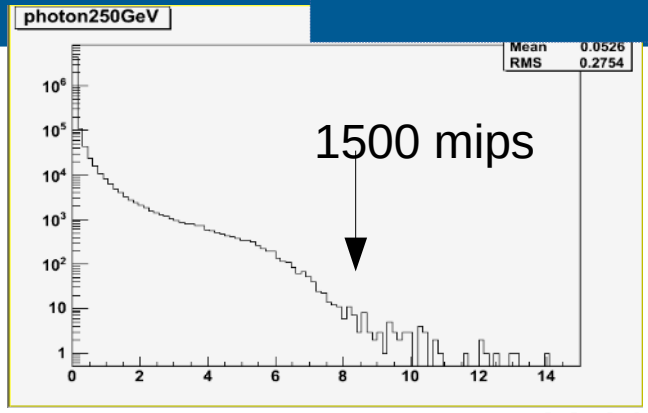




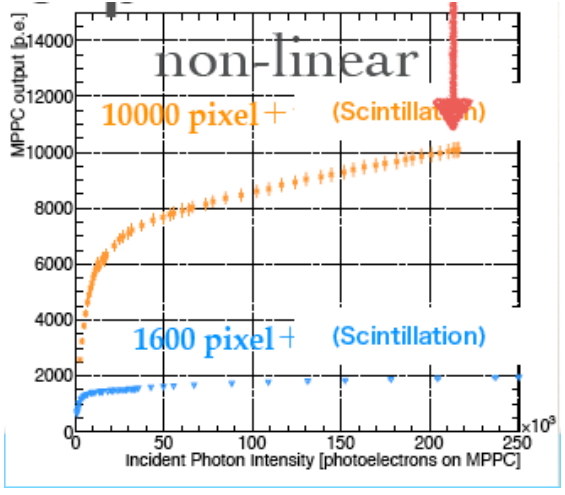
10 μm

10-15um Noise rate~100kHz
25um Noise rate=50kHz





MeV/strip



Noise handling: first results

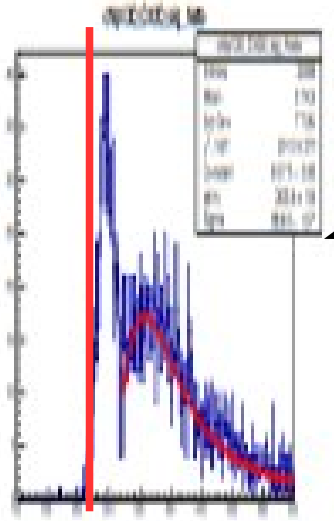
T. Takeshita

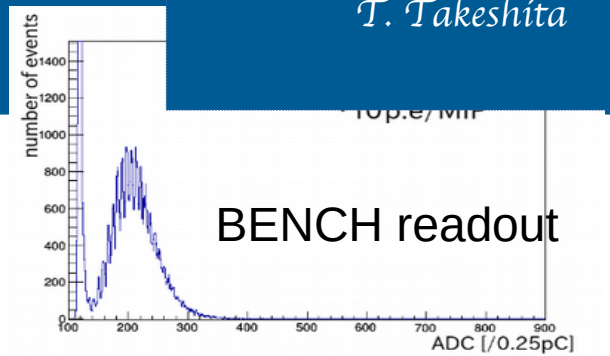
Much improved with latest version of MPPC
+ more efficient scintillators:

– SCSN38 → EJ204
10 → 14 p.e. / mip

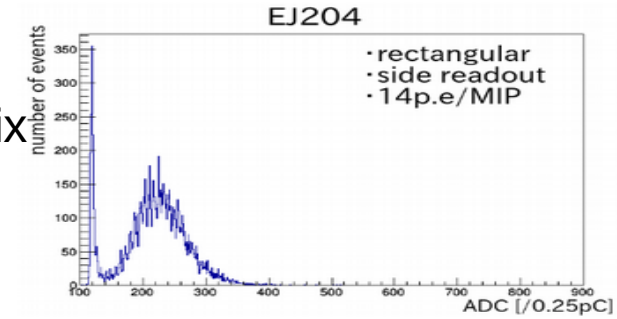
with EBU EJ204-3m

in EM Showers
(one of best result)

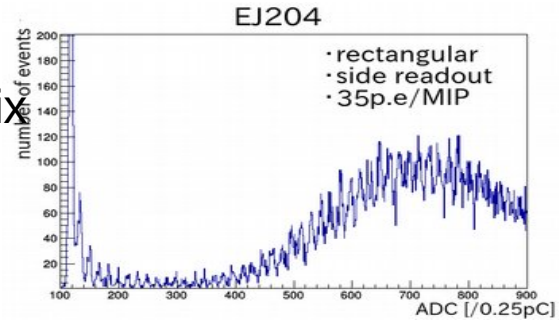




10μm pix



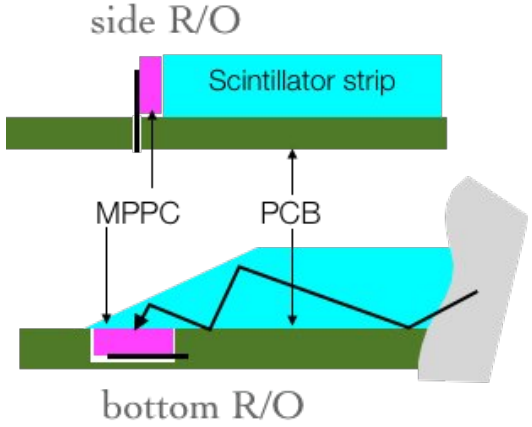
15μm pix

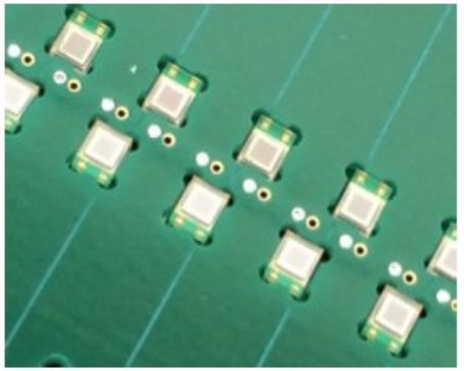


Wedge geometry

T. Takeshita

図 4.9: Single tapered wedge



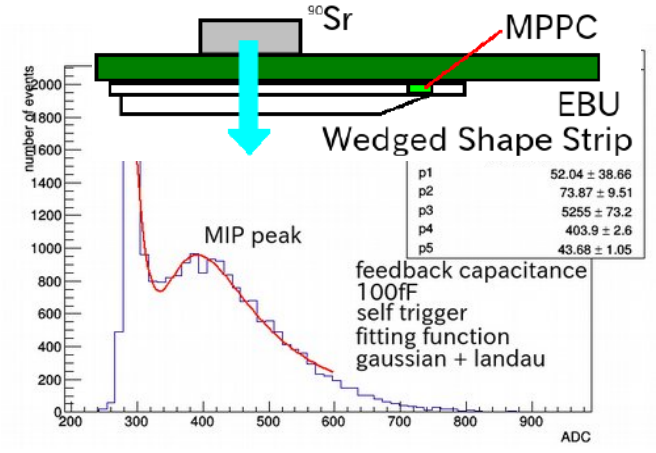


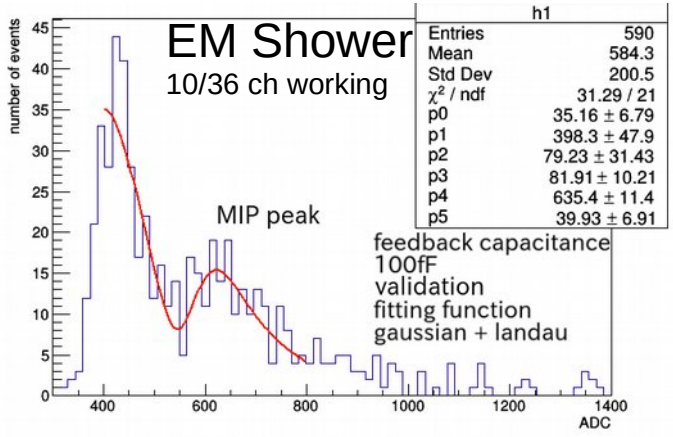
Better uniformity

- No dead space

Better integration of MPPCs

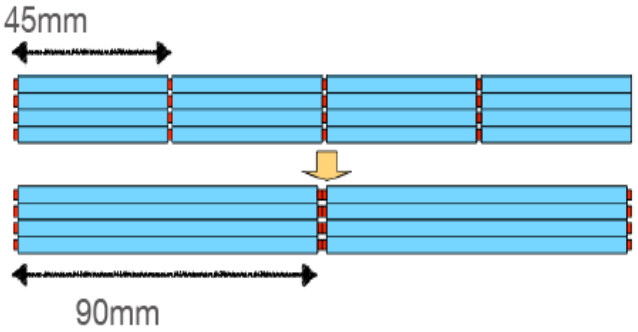
- soldering on board
- loss of signal (p.e.) by ~30%





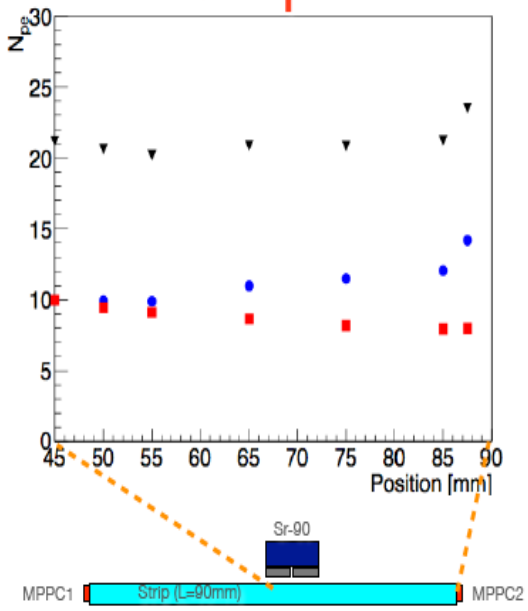
Uniformity studies

- double sided read out
  coincidence reduce Nnoise
- with 10um pitch MPPC
- keeping the same numb. =Nch
- with longer strips



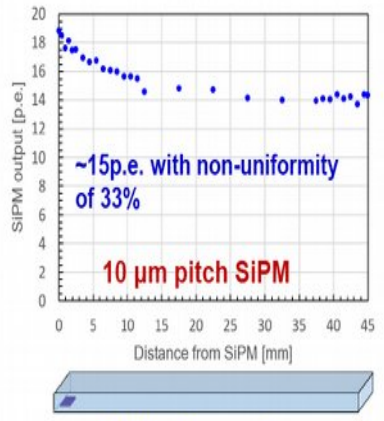
EJ212~BC400

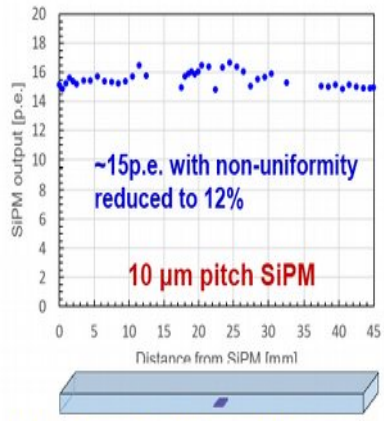
LY>20p.e.



Standalone Geant4 simulation is used to optimize scintillator module

- PhysicsList: QGSP_INCLXX + Standard Geant4 Optical Physics (Version: Geant 4.10.3)
- Scintillator Strip: BC408, dimension: 45×5×2mm³
- SiPM: 1×1×0.1mm3 , Pitch size 25μm, 1600pixel
- Cladding: ESR, Tyvek
- Particle source: Sr-90, Center of the Strip, Vertical incidence





The bottom-center coupled mode is chosen for the prototype

Much done !

…

Much to do !

Silicon ECAL for ILD

- base unit and technology validated integrated device
  - S/N, auto-triggering, uniformity…
- Optimisation work on-going
  - round 13 of FEV, COB
  - 8'', 725µm Wafers
- Timing still to be studied
- "Last" big piece: building of a long slab

Silicon ECAL for CEPC:

- Cooling → Thermal & Physics simulation
- Chip and Acquisition
  - S/N ≠ for central trigger as for auto-trigger

Scintillator ECAL (personal view)

- Much progress on SiPM (MPPC)
- Nice performance of device on test stand
- performance in integrated device to be assessed

Lot to Learn
from HGCAL

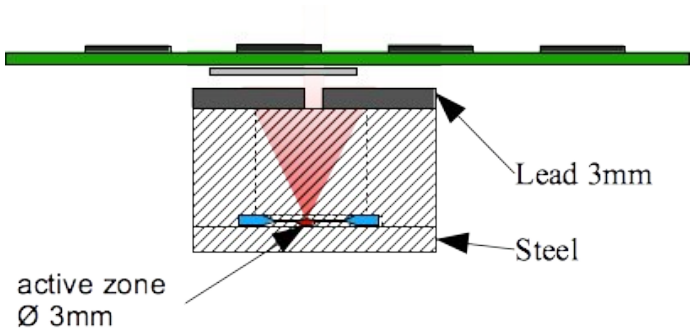
Back-up

Analysis & Papers

On-going

- Construction & Commissioning paper(s?) – technical mid 2018 ?
  - By layer analysis: mips+noise → noise, S/N, uniformity, …
    - Presented at CHEF'2017 (A. Irles), LCWS'2017 (A. Lobanov), Poster @ IEEE (A. Irles).
  - DAQ presented CHEF'2017 (F. Magniette)
    - Proceeding submitted
  - Test of SK2a Paper presented at CHEF'2017 (T. Suehara)
- Shower paper – end 2018 ?
  - "Collective behaviour" / High energy: Shower profile, response to high energies
  - Might be completed with DESY BT results July 2018.

Test with ^{90}Sr source



2.2 + 0.546 MeV electrons

- no straightforward mip but fine...