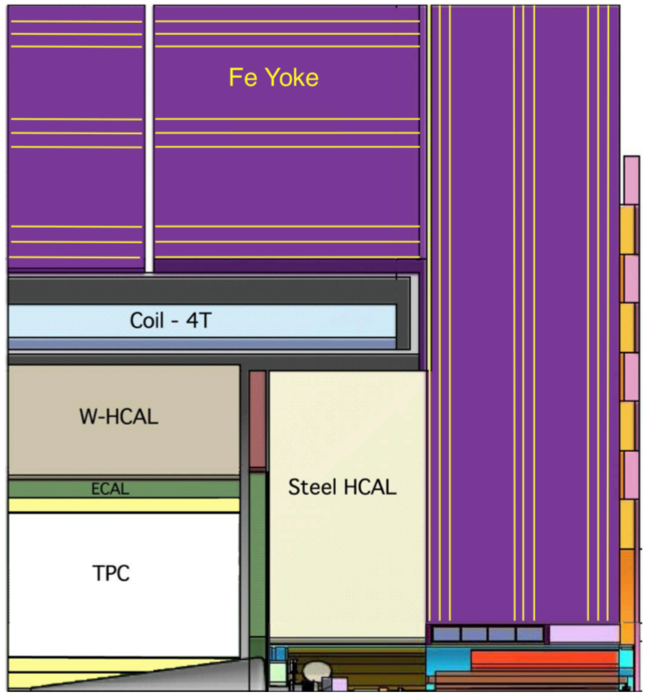
A silicon vertex and tracking system for CLIC and FCC-ee

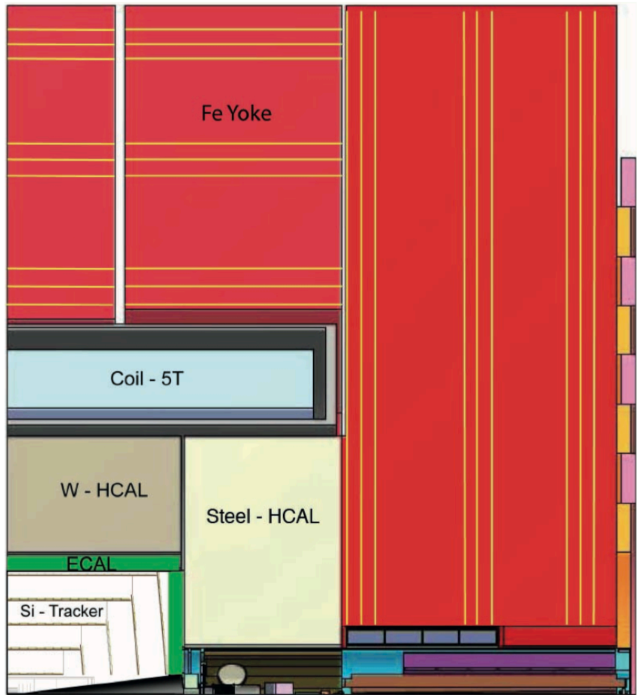
Emilia Leogrande (CERN),
on behalf of the CLICdp and FCC Collaborations

Workshop on the Circular Electron-Positron Collider
24-26 May 2018, Rome

A bit of history

- CLIC CDR [1]: two detector concepts, both based on ILC concepts
  - CLIC_ILD = silicon vertex + TPC + silicon layers
  - CLIC_SiD = all silicon





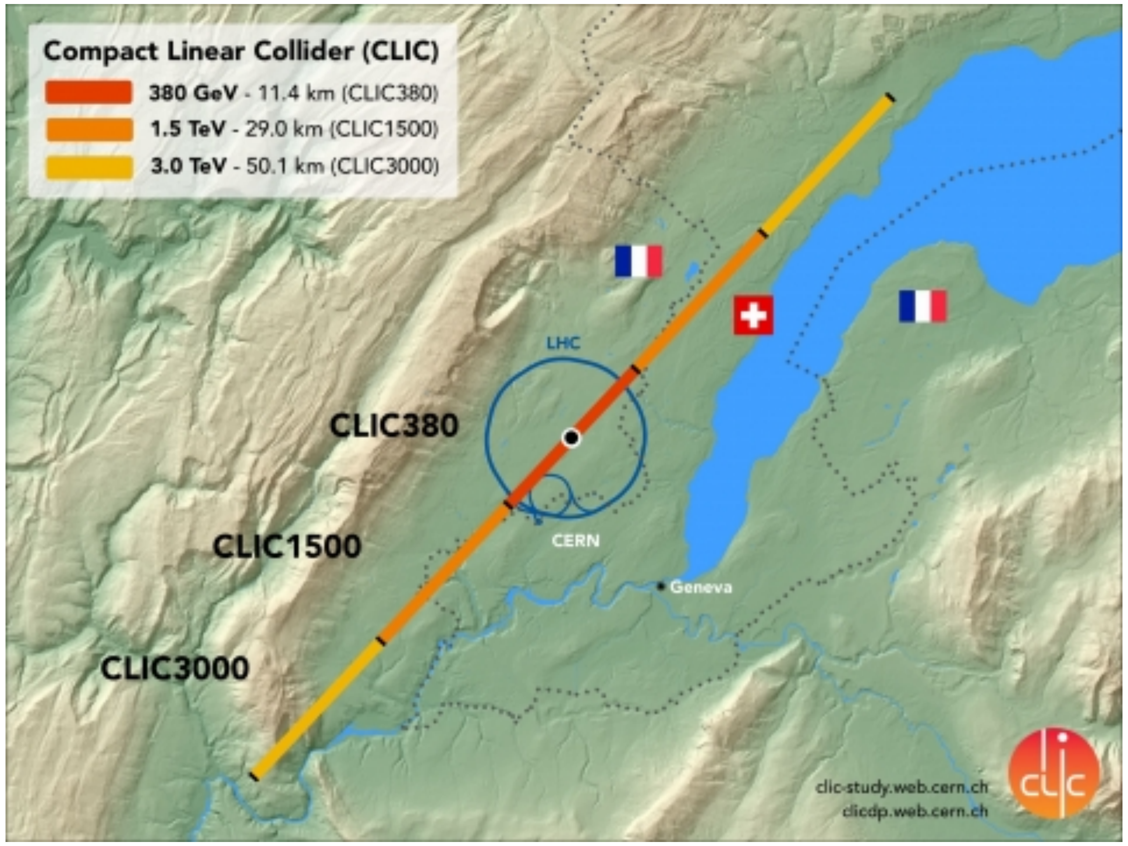
- Post-CDR [2]: *one* all-silicon detector concept **CLICdet**
- Adaptation of the CLICdet to **FCC-ee** experimental conditions and physics requirements: **CLD**

[1] https://arxiv.org/abs/1202.5940
[2] https://cds.cern.ch/record/2254048?ln=it

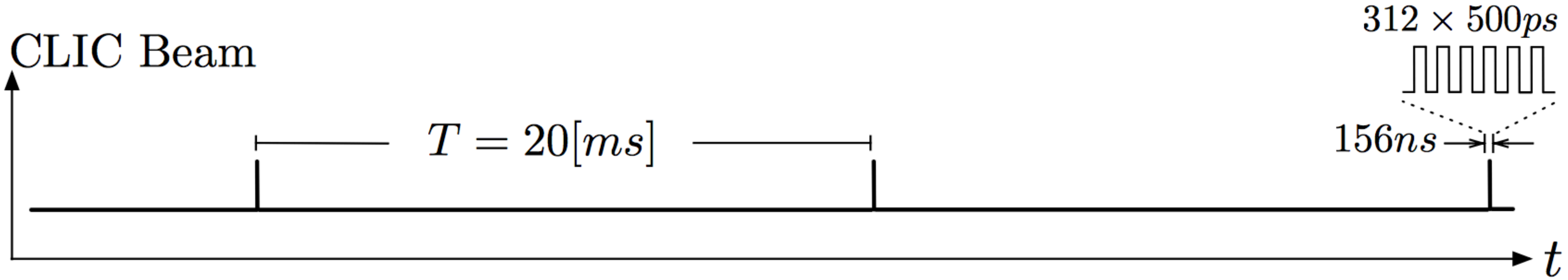
Content of this talk

- The CLICdet
  - CLIC experimental conditions and beam-beam effects
  - detector design overview
  - vertex and tracker design and performances
- The CLD
  - FCC-ee experimental conditions
  - detector design overview
  - vertex and tracker design and performances
- Technology R&D - work carried out in the CLICdp Collaboration, targeted for CLIC specifications
  - *personal selection* of (sensors + readout) technology considered for the vertex and tracker

CLIC beam

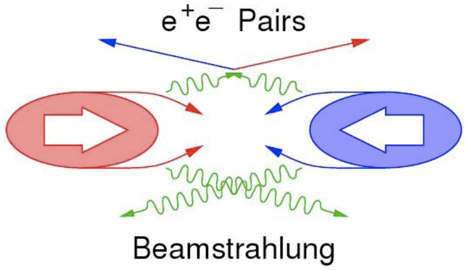


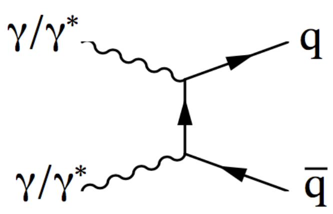
- built in stages: 380 GeV, 1.5 TeV, 3 TeV
- beam structure
  - record data during collision time, *triggerless* readout between bunch trains
  - power pulsing: detector "switched off" between bunch trains
  - crossing angle (20mrad @3TeV) in crab crossing scheme

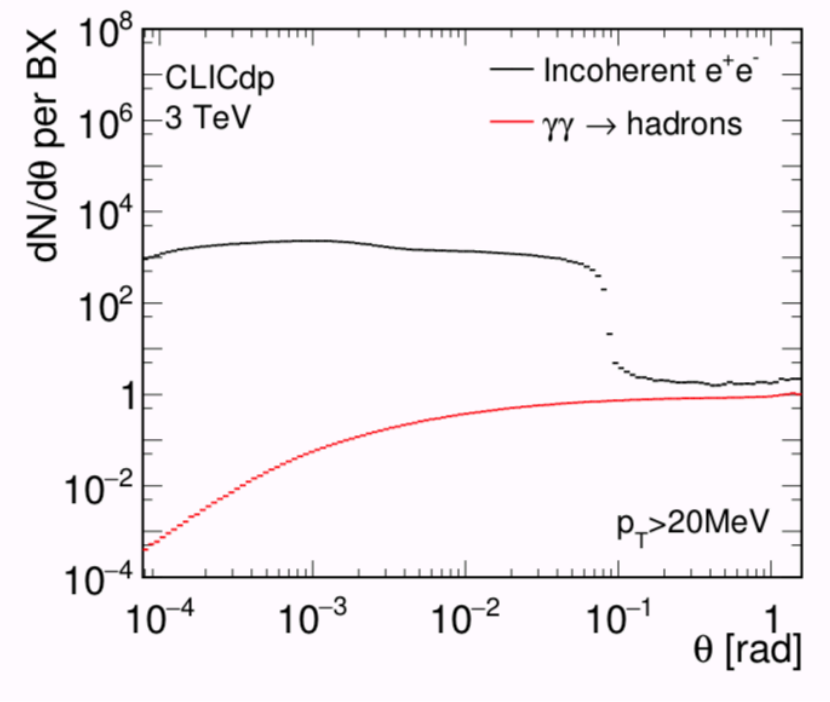


CLIC beam backgrounds

- main source of background from beamsstrahlung photons
  - incoherent pairs
  - γγ->hadrons







https://indico.cern.ch/event/718097/contributions/2951104/attachments/1629061/2625273/clicdpAB_3_expcond_sailer_v2_180410.pdf

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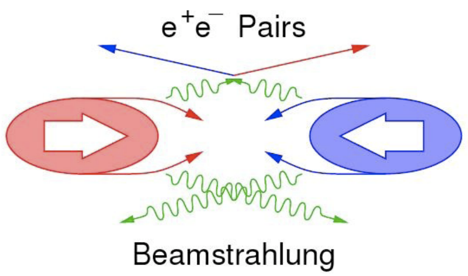
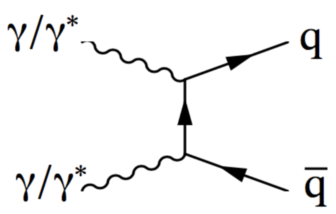
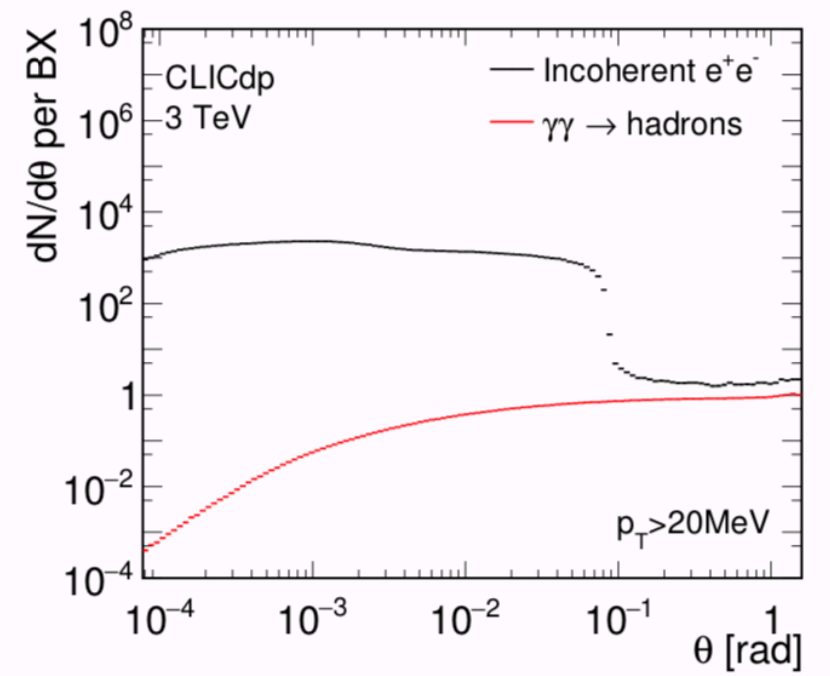
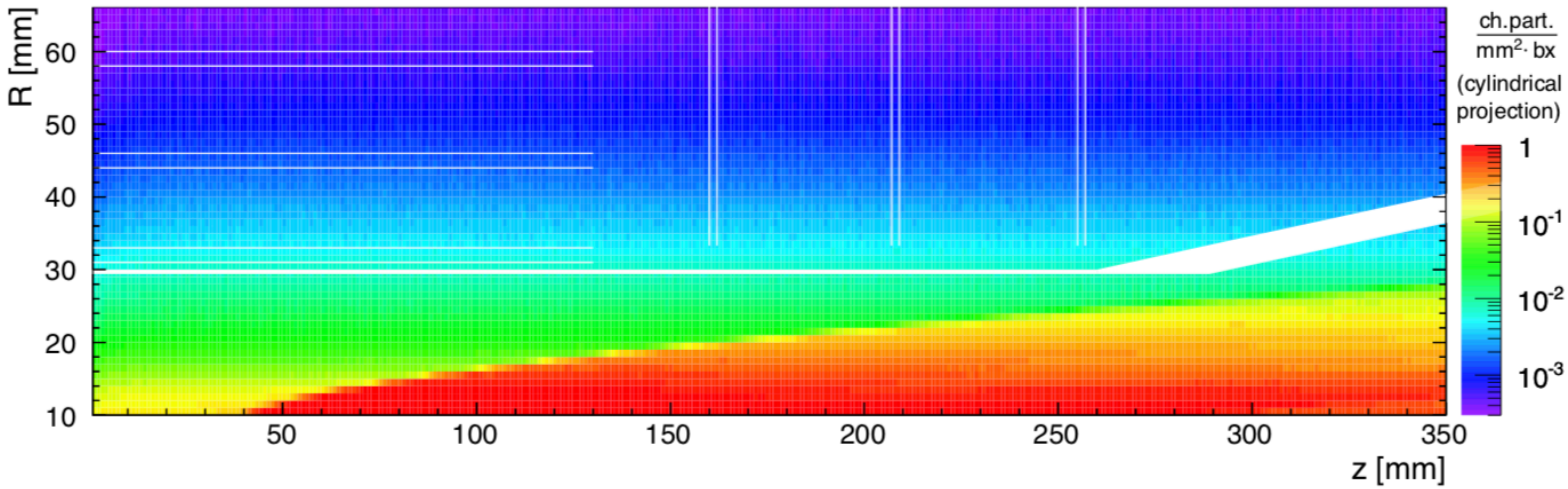






- Large flux of low-momentum particles from incoherent pairs limits the inner radius of the vertex detector



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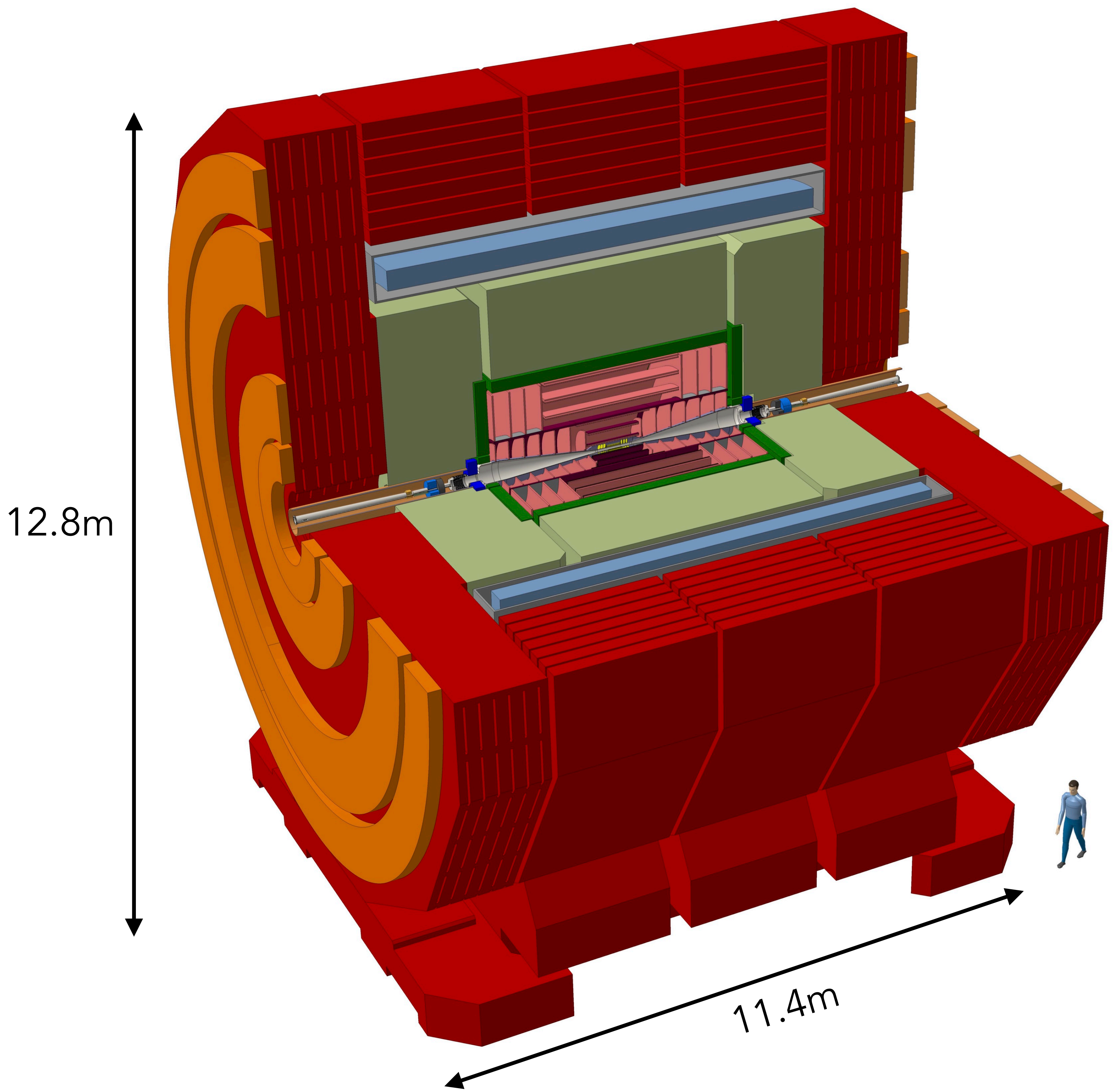
The CLICdet

optimized for the 3 TeV



- Tracking system
  - Vertex
  - Tracker

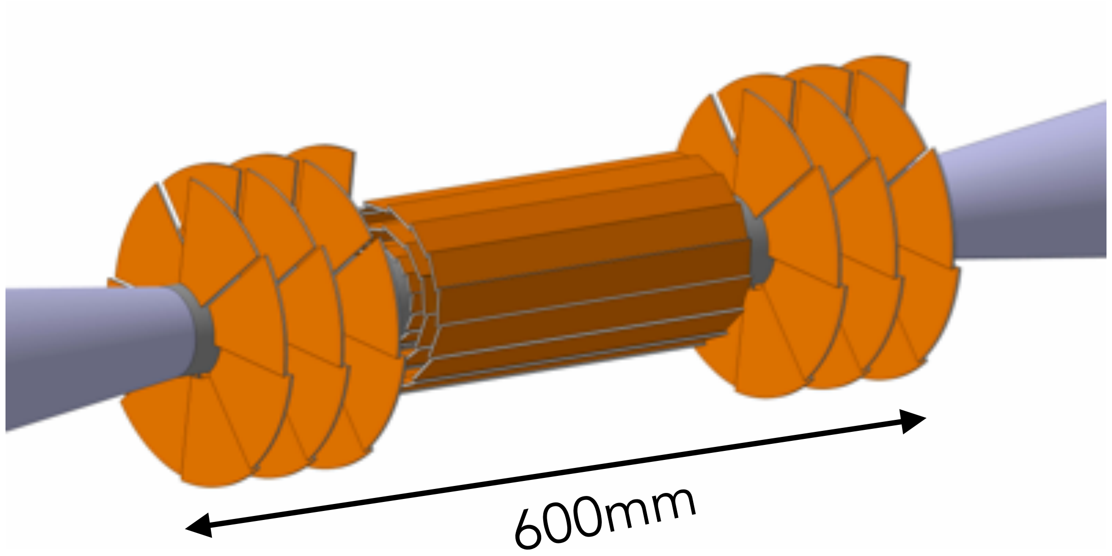
- Calorimeters
  - ECal
  - HCal

- Superconducting solenoid 4T

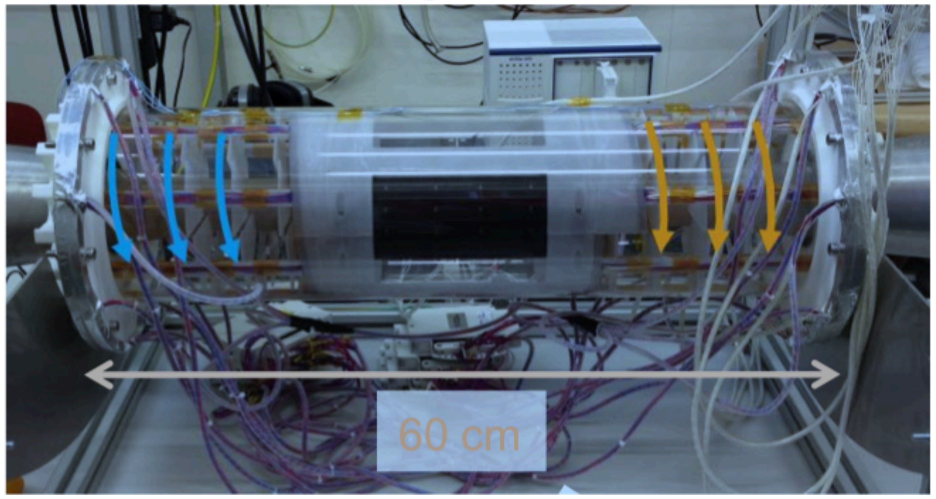
- Return yoke + muon ID system

The vertex detector (I)

- 3 double layers in the barrel
  - radius from 31** to 58 mm
    **limited by occupancy from pairs
- 3 double-layered forward disks
  - shaped in spirals to allow for air cooling (power-pulsed detector)
  - 50 mW/cm^2 achievable with power pulsing



1:1 scale air cooling thermal test setup



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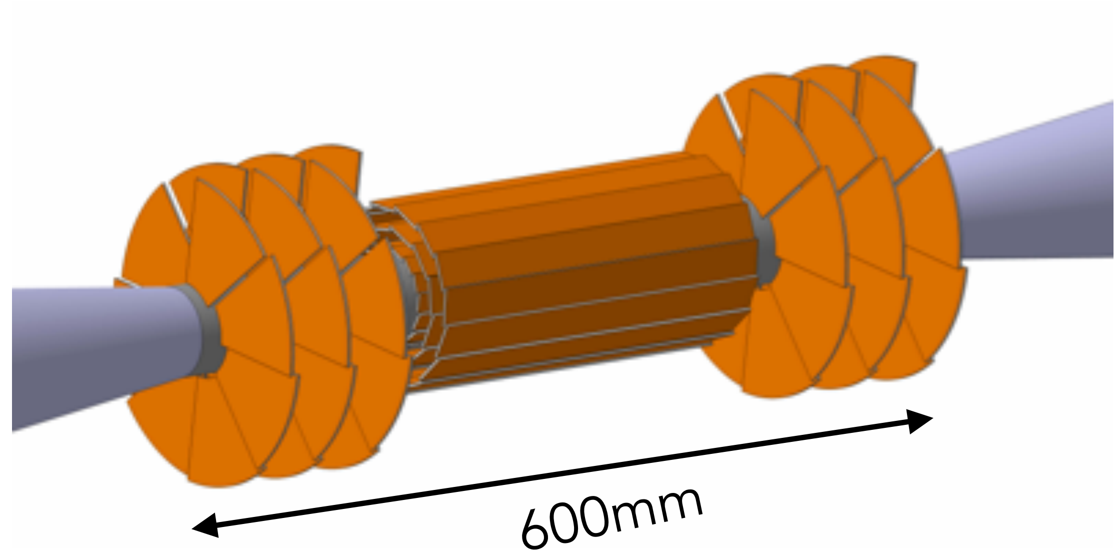

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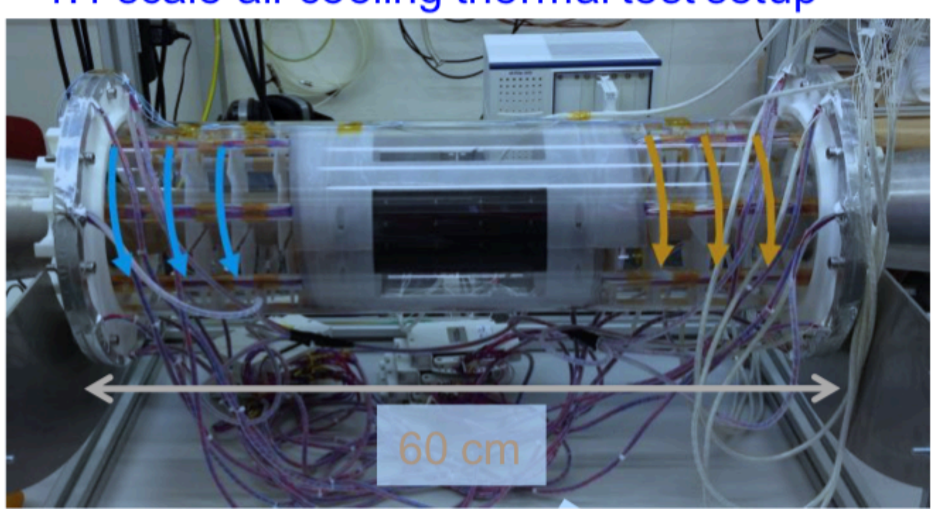

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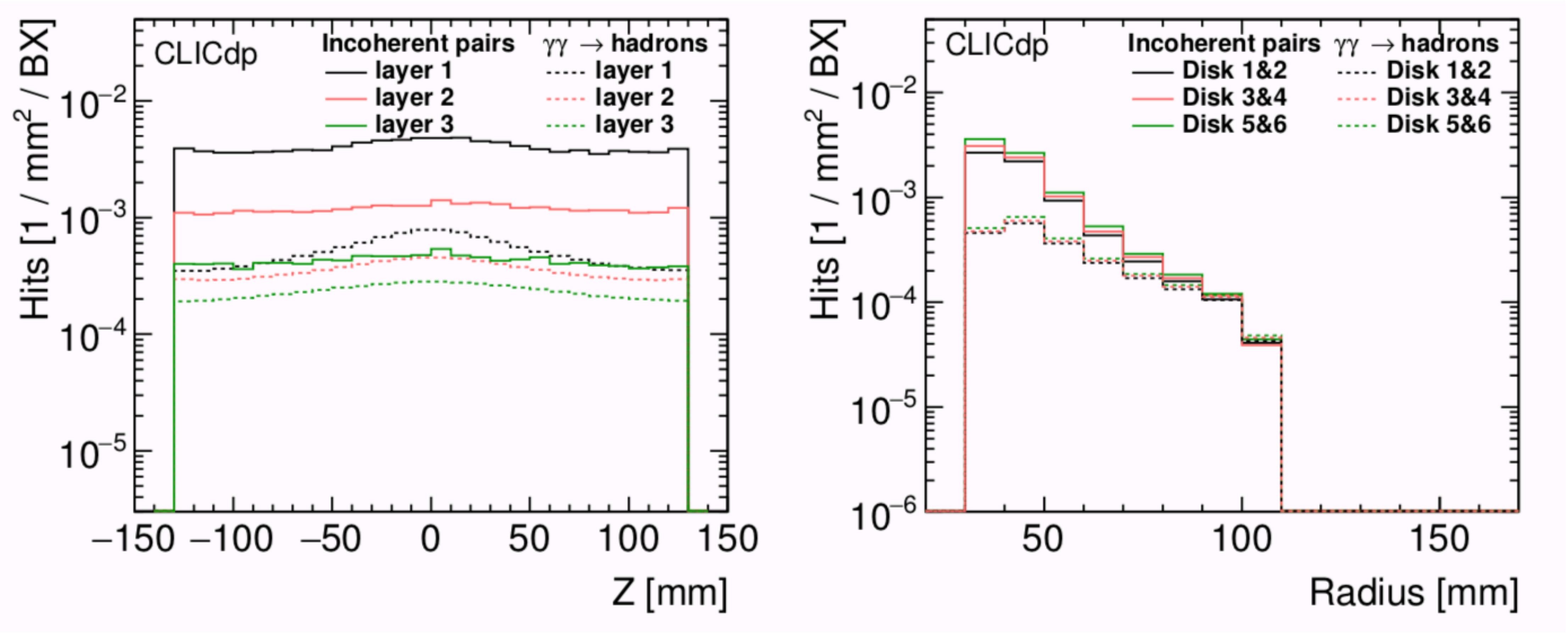
- low material budget
  - 50 μm-thick sensors
  - 0.4% X_0 per double layer (0.2% X_0 per layer)
- total sensitive area = 0.84 m^2

The vertex detector (II)

- pixel sizes 25x25 μm²
  - with analog readout => required single point resolution of 3 μm
  - time resolution of ~5 ns
  - max desired occupancy of 3%

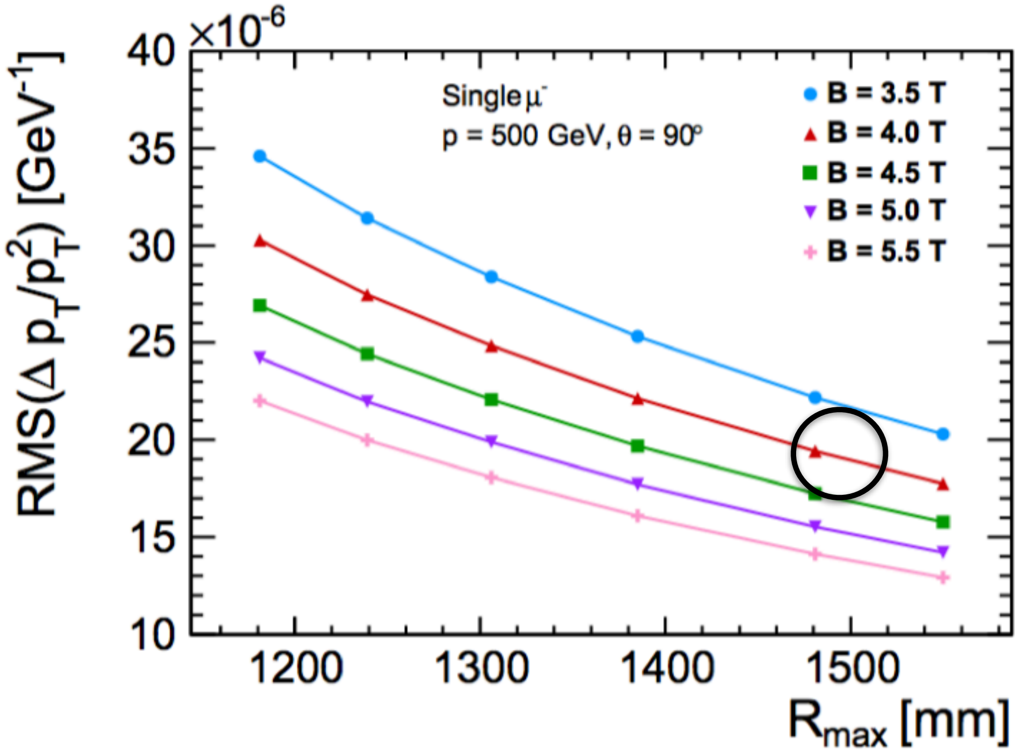


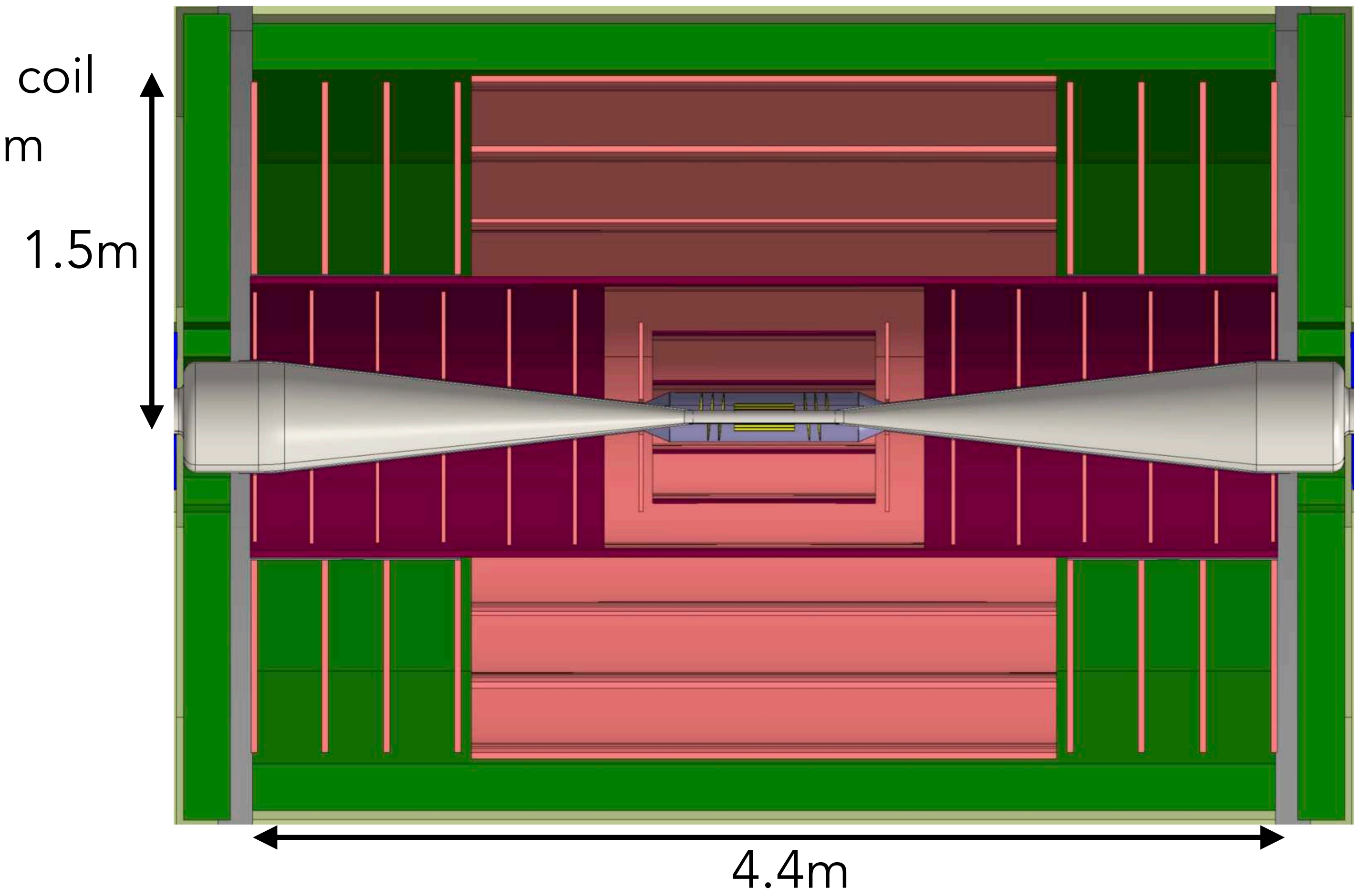
(a) Vertex barrel hit density

(b) Vertex disks hit density

The tracker (I)

- p_T-resolution goal 2×10^{-5} GeV^{-1}
- Trade-off between achievable B field at given coil radius and outer tracker radius => R_{max} = 1.5 m





- inner tracker
  - 3 barrel layers + 7 forward disks per side
- outer tracker
  - 3 barrel layers + 4 forward disks per side
- carbon fibre support structure
  - mechanical stability, integration

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- p_T-resolution goal $2x10^{-5}$ GeV^{-1}
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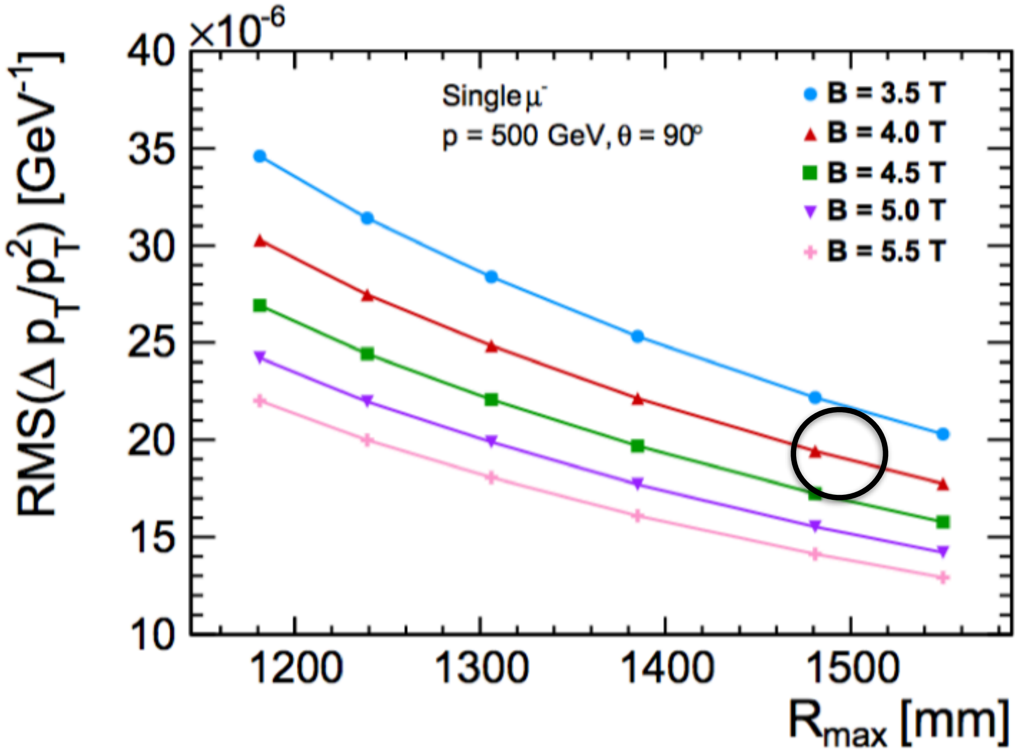
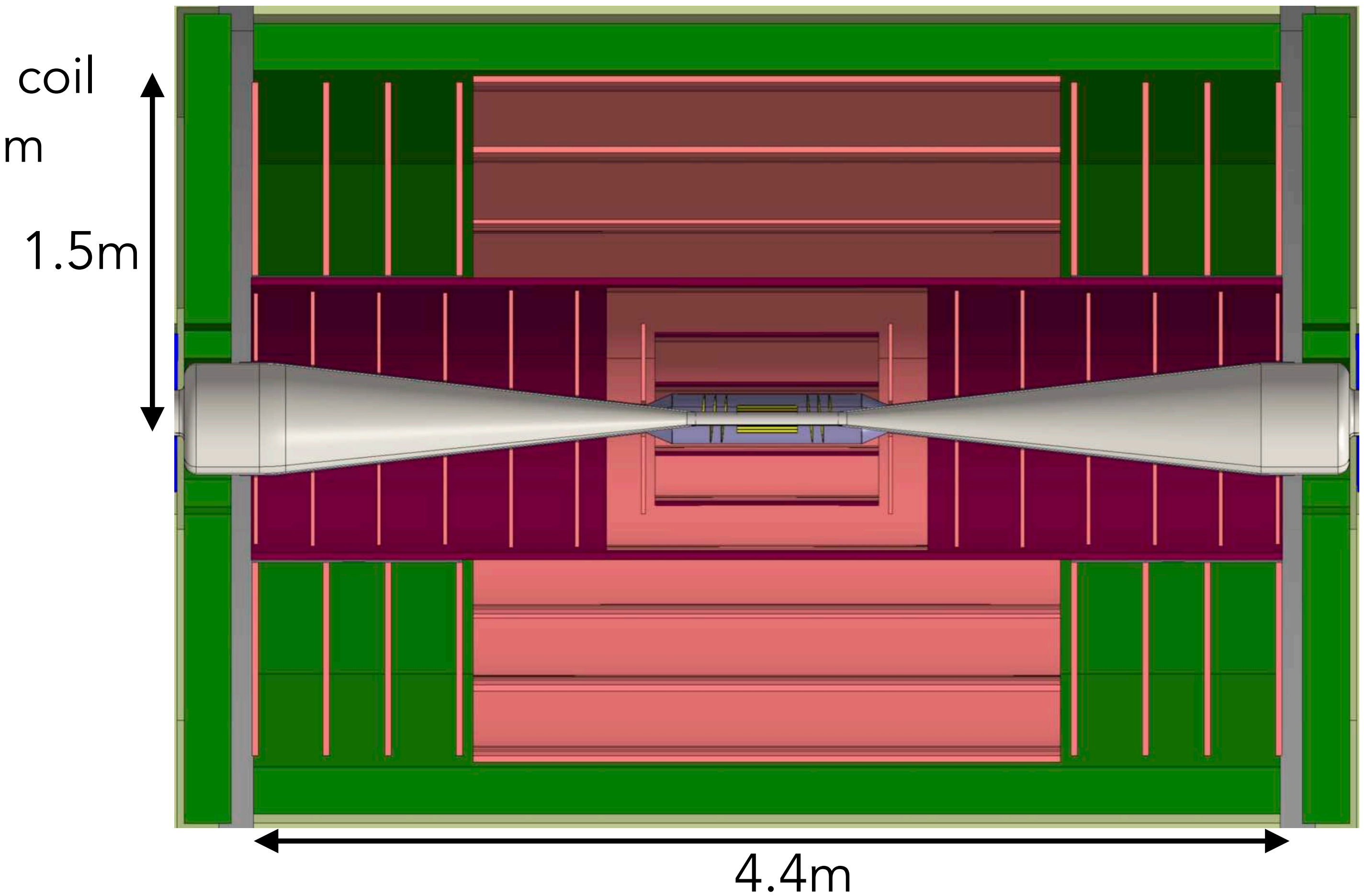


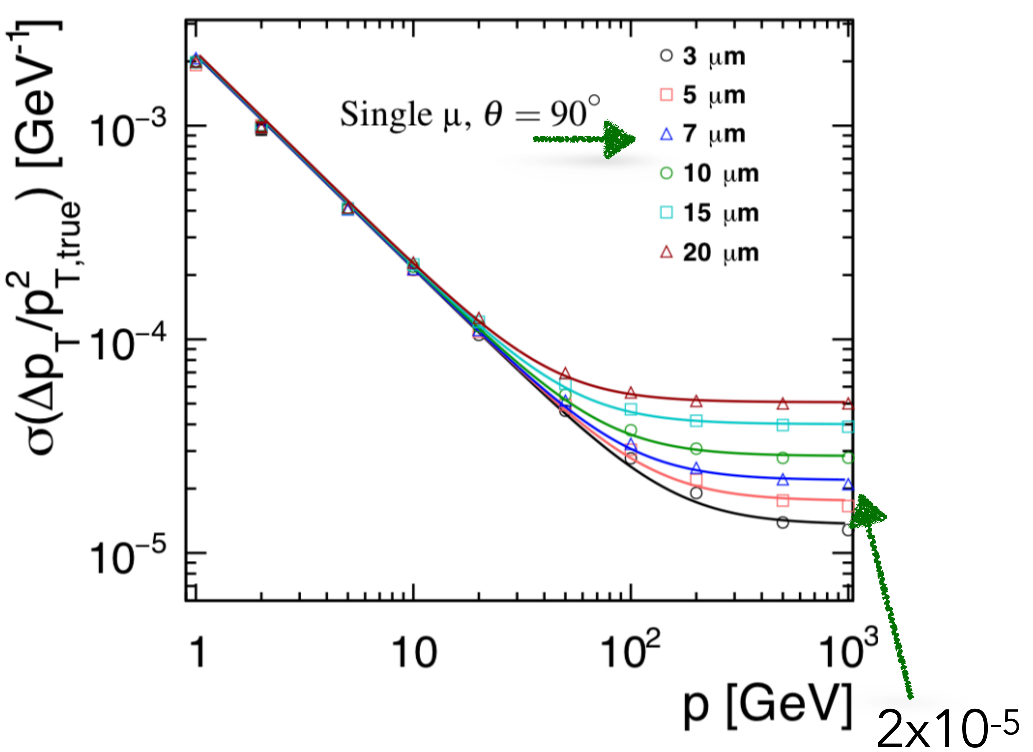


- inner tracker
  - 3 barrel layers + 7 forward disks per side
- outer tracker
  - 3 barrel layers + 4 forward disks per side
- carbon fibre support structure
  - mechanical stability, integration

- material budget
  - 200 μm-thick sensors
  - 1% X_0 per tracker layer
  - 2.5% X_0 main support tube + cables
- total sensitive area = 137 m^2

The tracker (II)

- only first inner tracker disk pixelated for pattern recognition needs
- strixel (short strips/ long pixels) sizes 30x300 µm²
  - with analog readout => required single point resolution in (R,φ) of 7 µm
  - time resolution of ~5 ns



https://cdsweb.cern.ch/record/2261066/files/CLICdp-Note-2017-002.pdf

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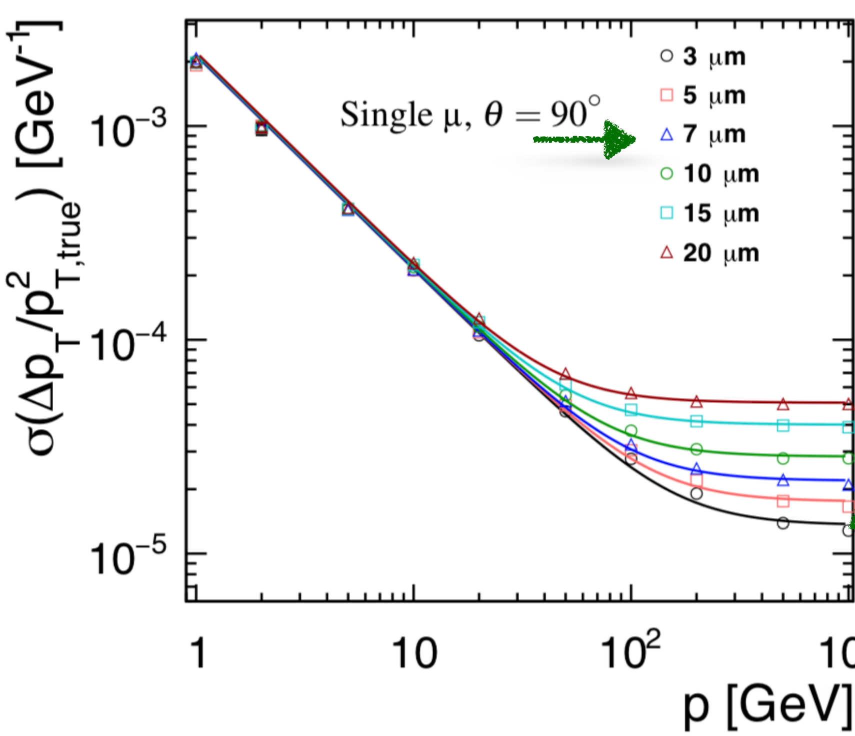
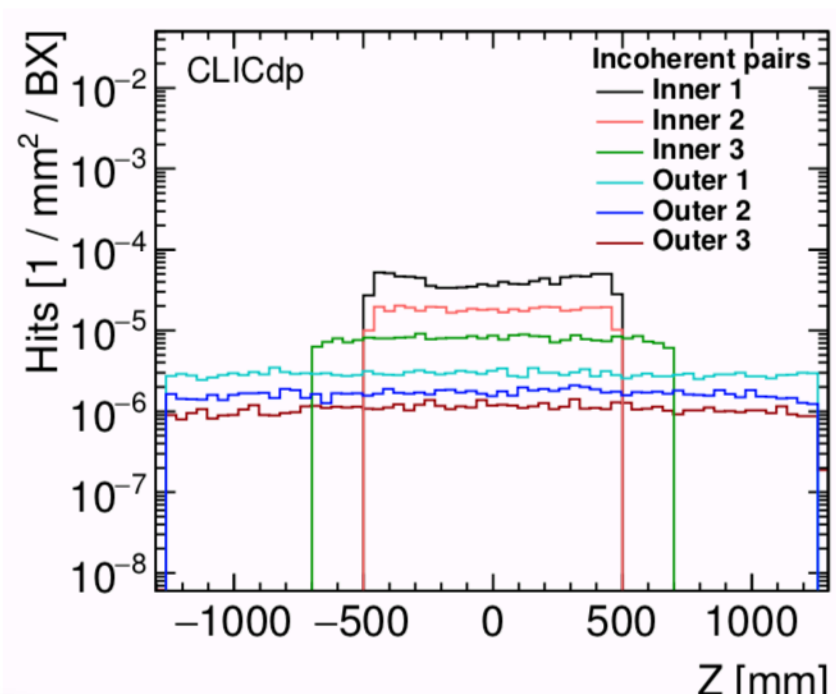
  - time resolution of ~5 ns
  - occupancy lower than vertex detector [see below for barrel]

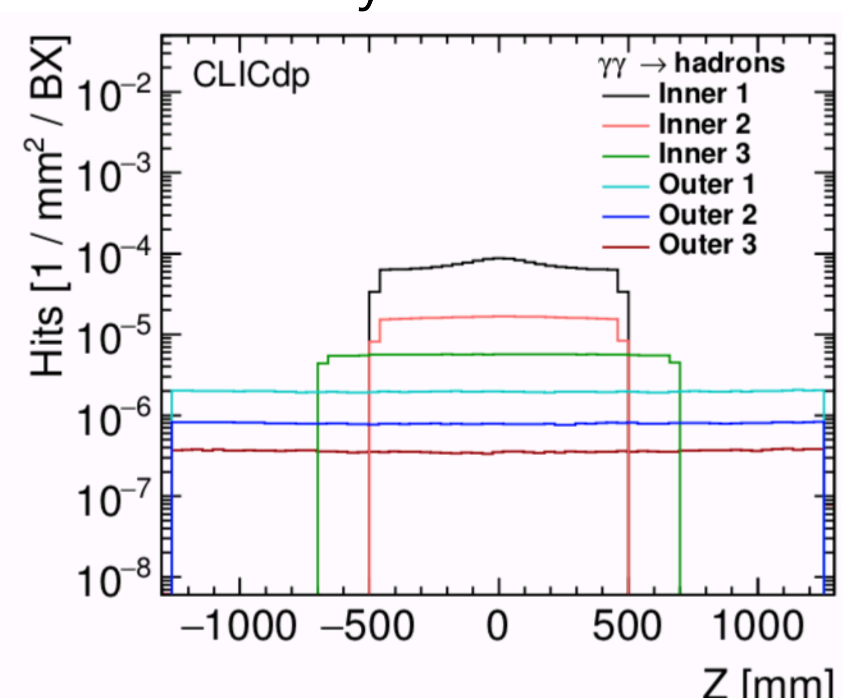
tracker barrel hit density



2x10^{-5}



a) incoherent pairs



b) γγ—>hadrons

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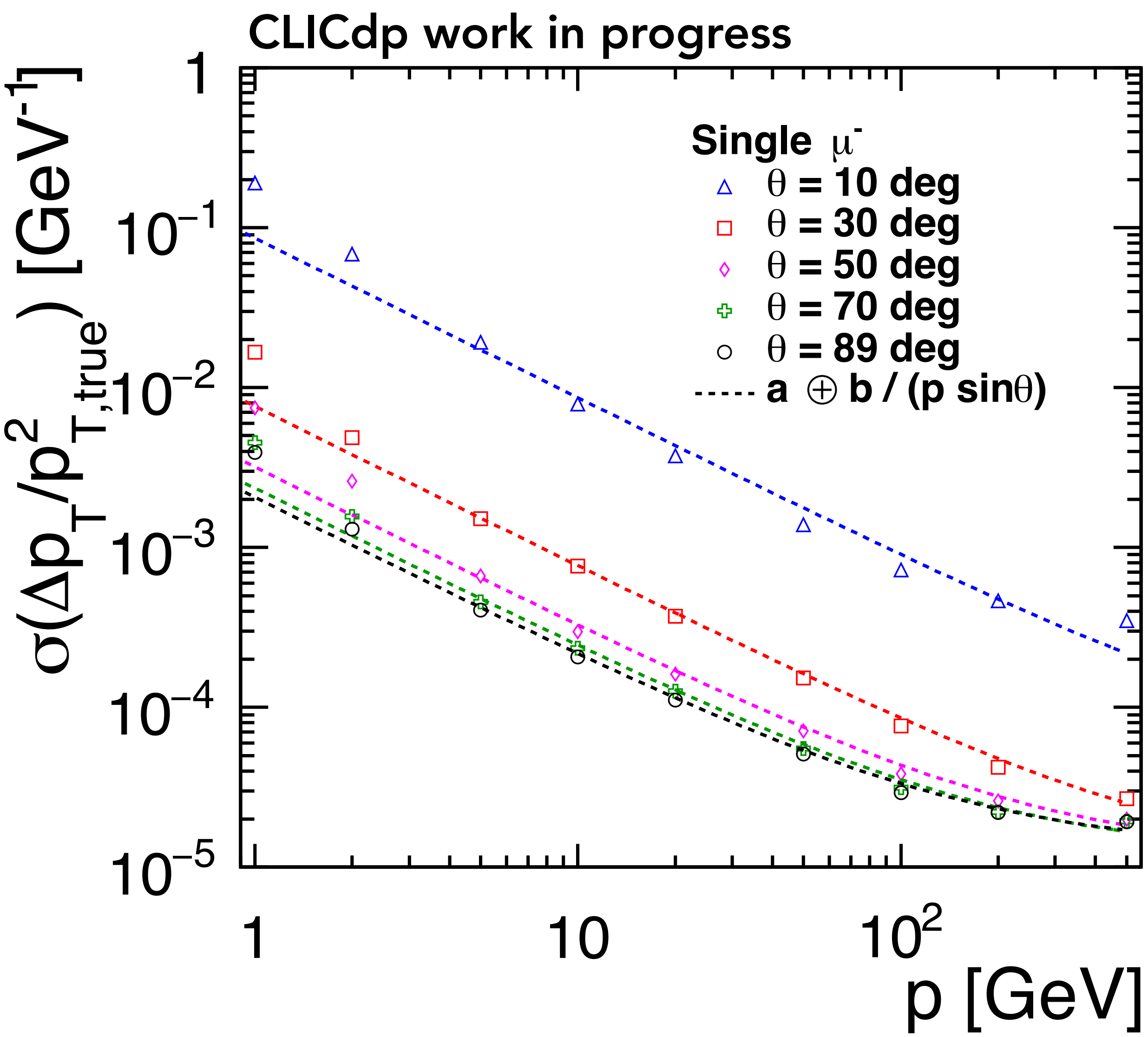
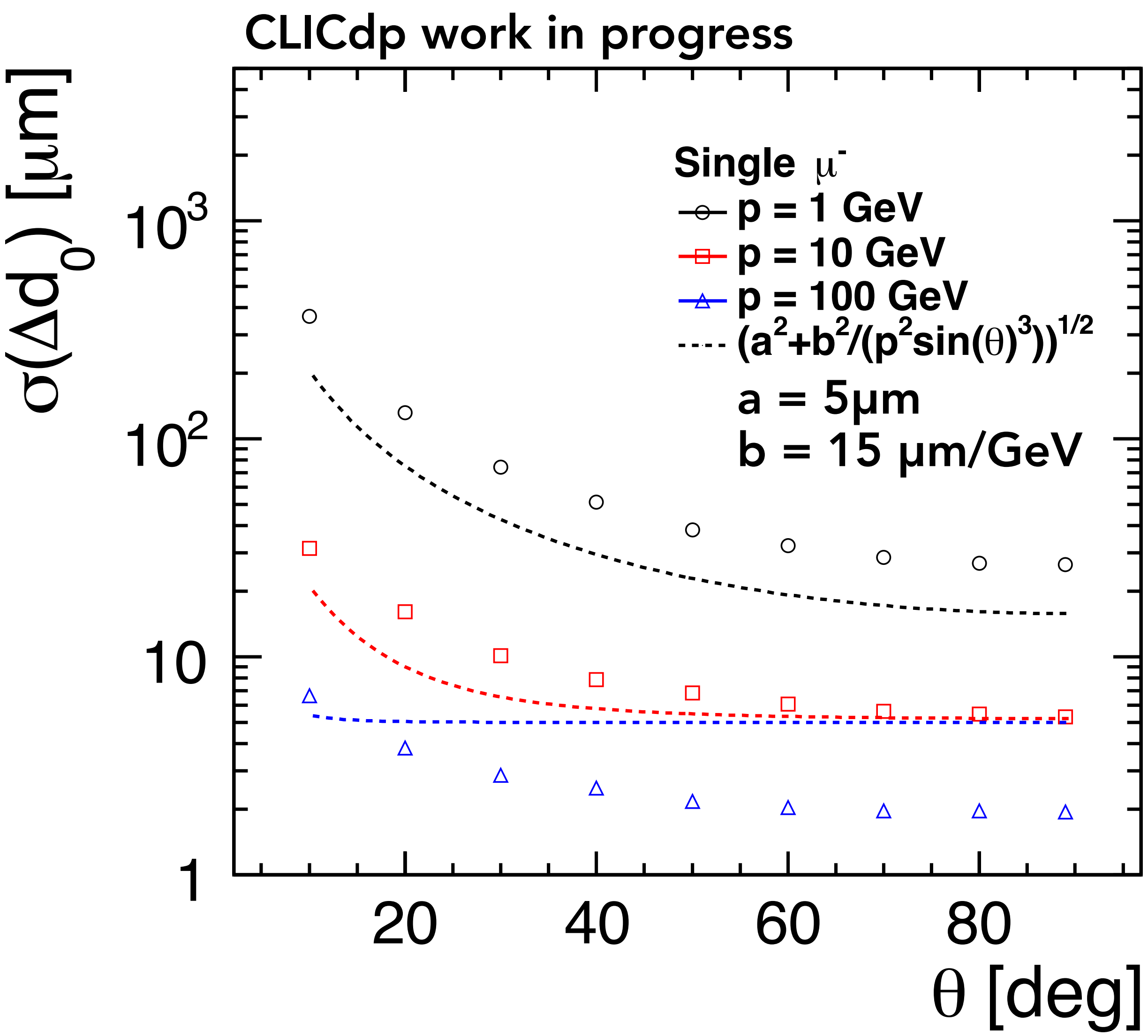
CLICdet tracking performances

all studies done in full simulation with iLCSoft

- Resolution = σ of the Gaussian fit of the (reco-true) distributions





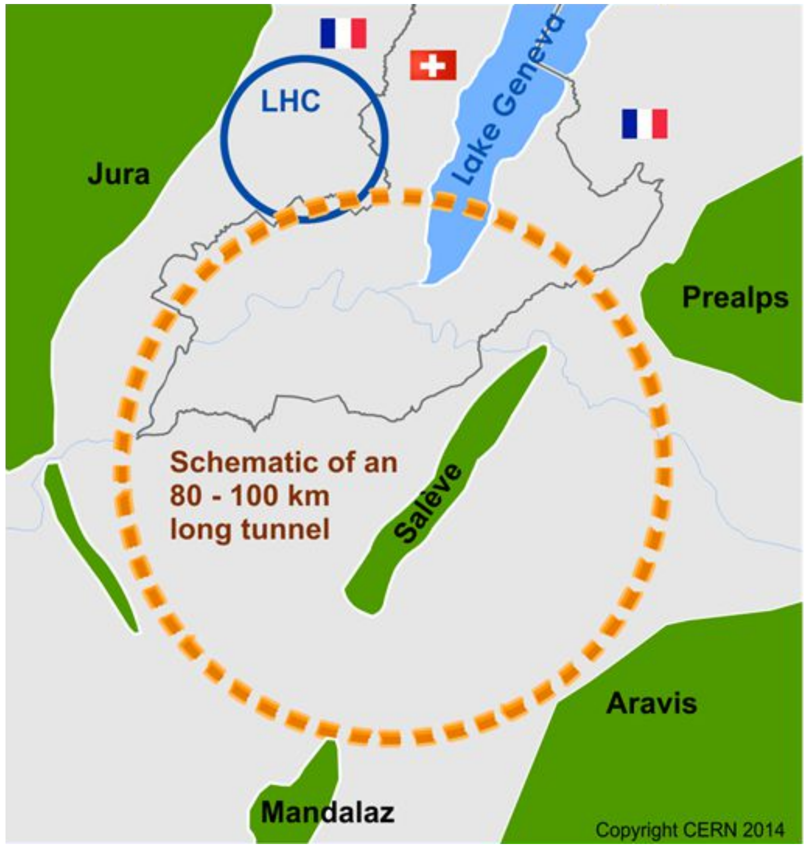
Achieved **transverse momentum resolution** goal of 2×10^{-5} GeV^{-1} for high-energy muons in the barrel

Achieved desired **impact parameter resolution**:

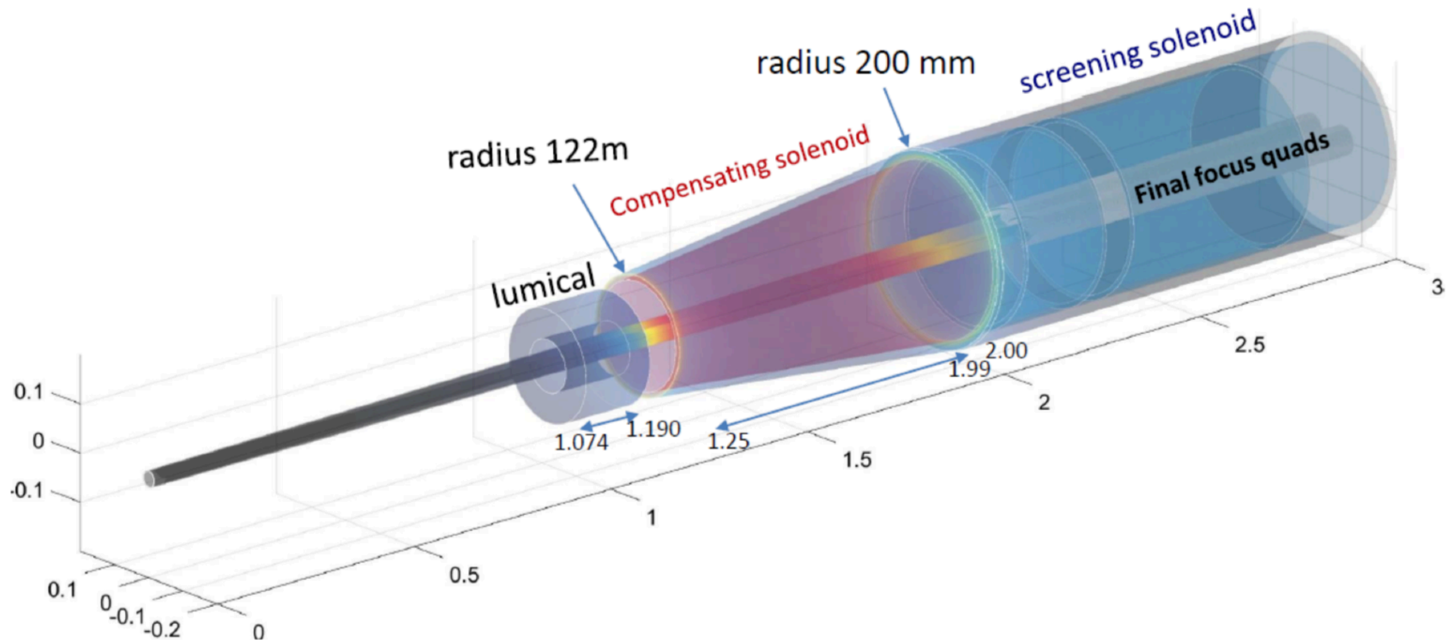
- d_0 for high-energy muons well below the high-momentum limit of 5 μm

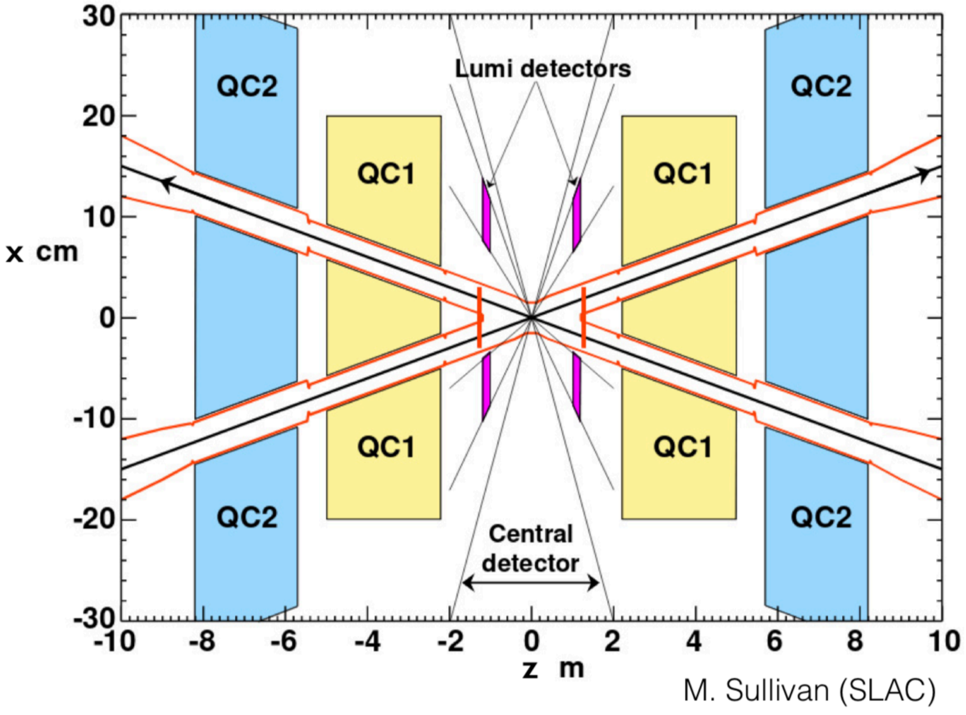
https://indico.cern.ch/event/718097/contributions/2951105/attachments/1628255/2625270/clicdpAB_4_clicdet_leogrande_v1_180410a.pdf

FCC-ee conditions



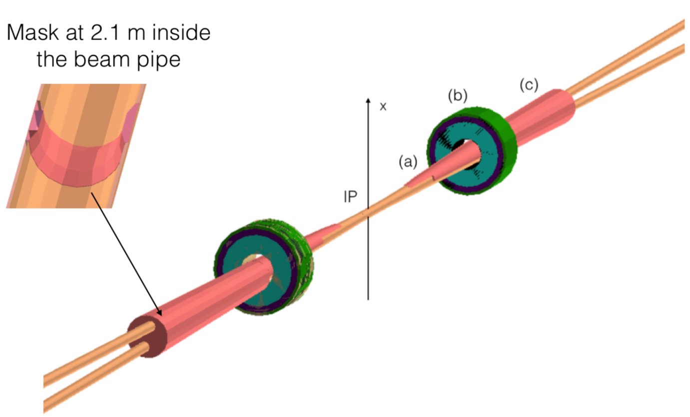
- energy-staged scenario (91.2 - 365 GeV)
- interaction region
  - crossing angle of 30 mrad in crab-waist scheme
  - beampipe radius of 15 mm
  - Machine Detector Interface elements and LumiCal assumed inside a cone of 150 mrad
  - maximum detector solenoid field of 2 T due to beam/luminosity constraints

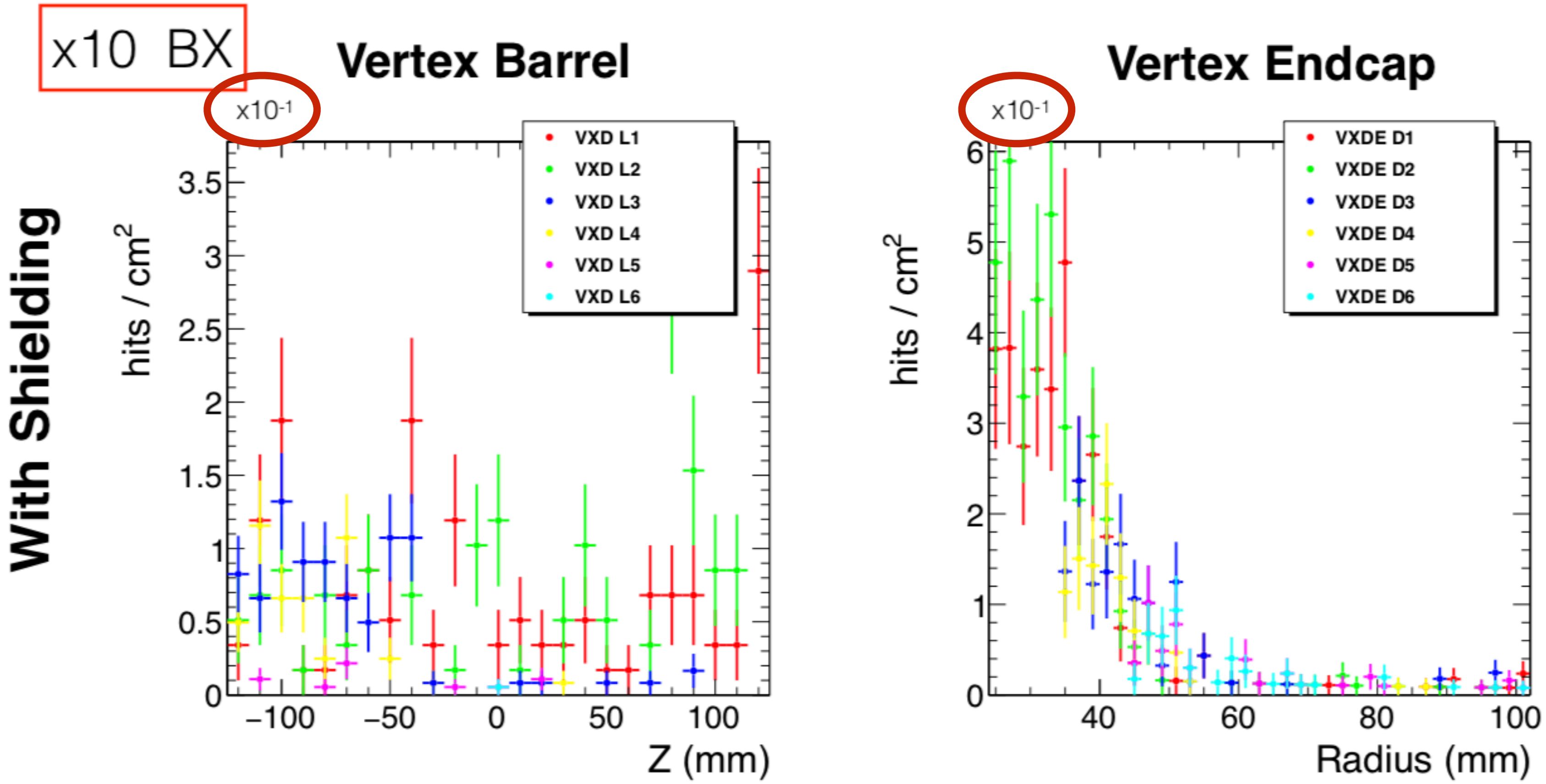




FCC-ee backgrounds

- main sources:
  - incoherent pairs
    - effects on the detector discussed later in this talk
  - synchrotron radiation
    - tungsten masks on beampipe limit the SR photons reaching the detector
    - not discussed further





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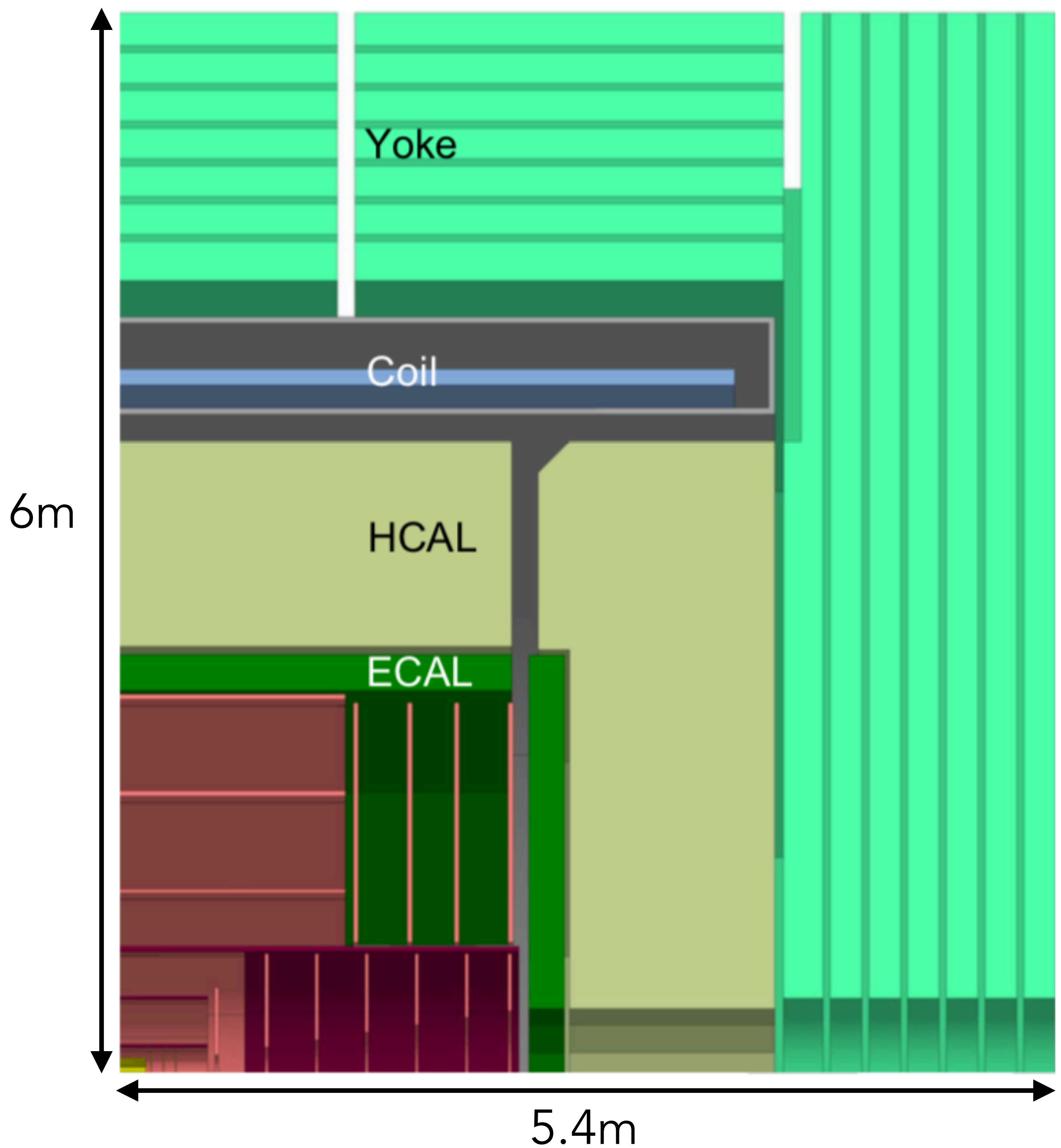
The CLD

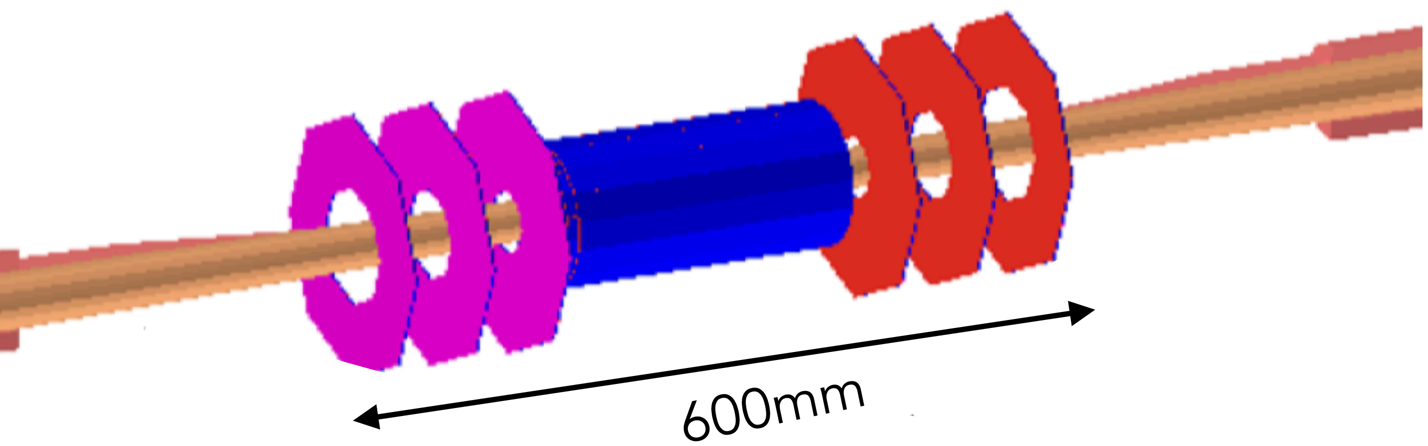
CLICdet adapted to the FCC-ee conditions



Concept	CLICdet	CLD
Vertex inner radius [mm]	31	17
Tracker technology	Silicon	Silicon
Tracker half length [m]	2.2	2.2
Tracker outer radius [m]	1.5	2.1
Inner tracker support cylinder radius [m]	0.575	0.675
ECAL absorber	W	W
ECAL X_0	22	22
ECAL barrel $r_{\min}$ [m]	1.5	2.15
ECAL barrel Δr [mm]	202	202
ECAL endcap $z_{\min}$ [m]	2.31	2.31
ECAL endcap Δz [mm]	202	202
HCAL absorber	Fe	Fe
HCAL λ_I	7.5	5.5
HCAL barrel $r_{\min}$ [m]	1.74	2.40
HCAL barrel Δr [mm]	1590	1166
HCAL endcap $z_{\min}$ [m]	2.4	2.4
HCAL endcap Δz [mm]	1590	1166
Solenoid field [T]	4	2
Solenoid bore radius [m]	3.5	3.7
Solenoid length [m]	8.3	7.4
Overall height [m]	12.9	12.0
Overall length [m]	11.4	7.5
Overall weight [t]	8100	TBC

The vertex detector

- 3 double layers in the barrel
  - radius from 17 to 57 mm
- 3 double-layered disks in the forward



- low material budget
  - 50 µm -thick sensors
  - 0.6% X_0 per double layer
    [0.2% X_0 per layer like CLICdet + 0.1% X_0 per layer (for ALICE-like cooling)]
- total sensitive area = 0.35 m^2

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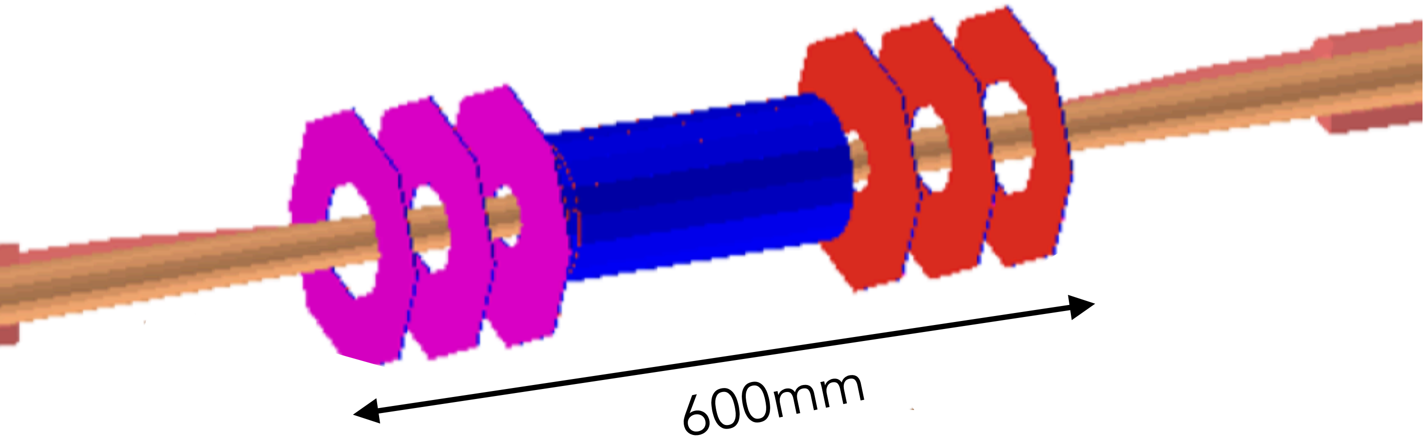

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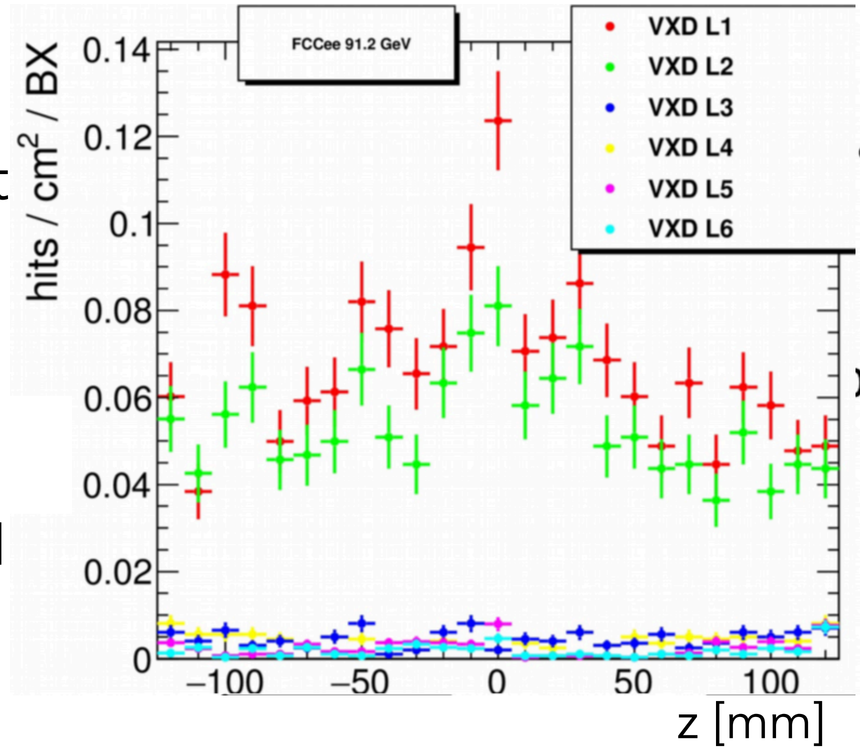
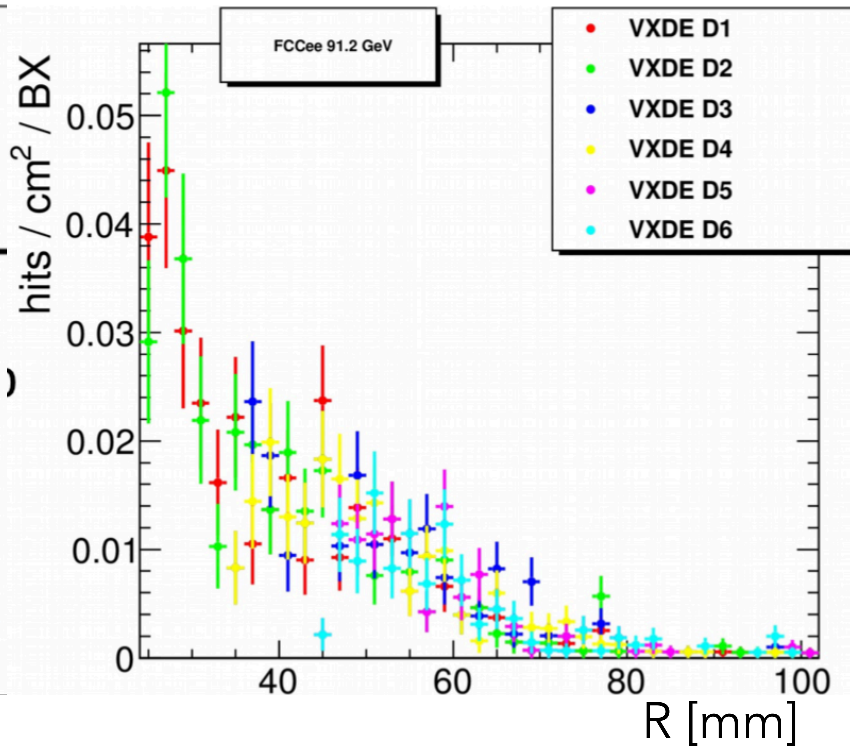
- total sensitive area = 0.35 m^2

- pixel sizes 25x25 μm^2 from CLICdet
  - with analog readout => required single point resolution of 3 µm (CLICdet)
  - occupancy results confirm the need for water cooling





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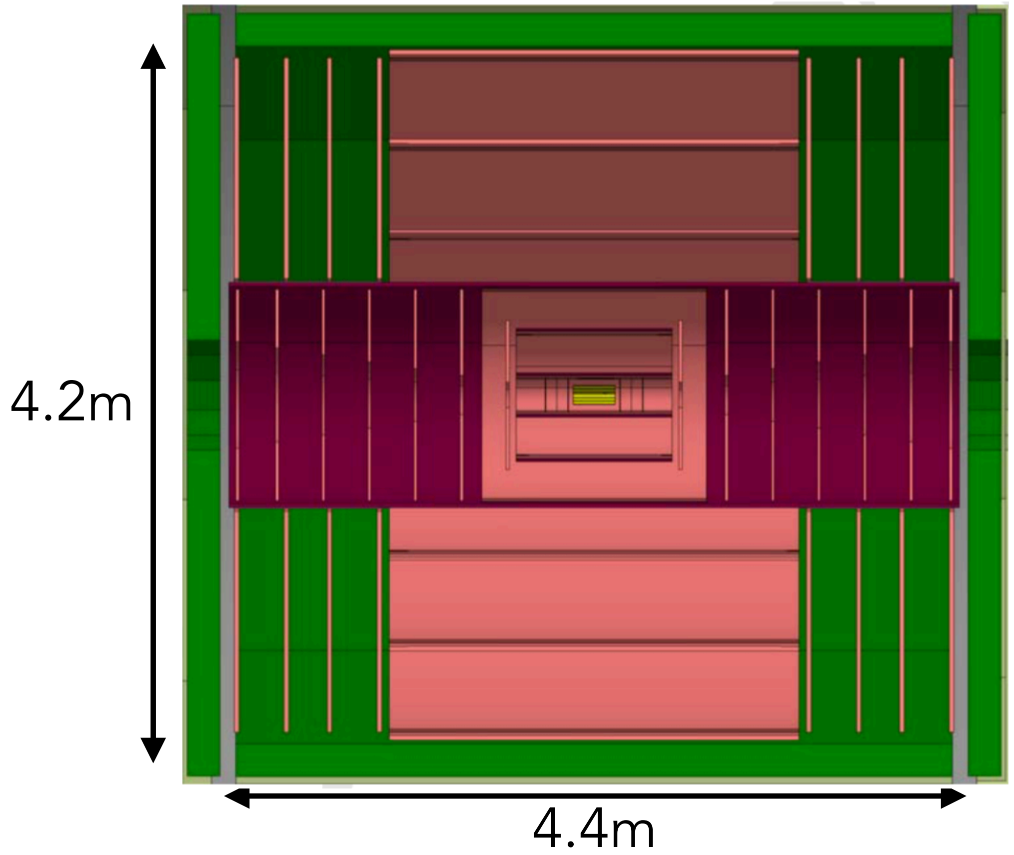
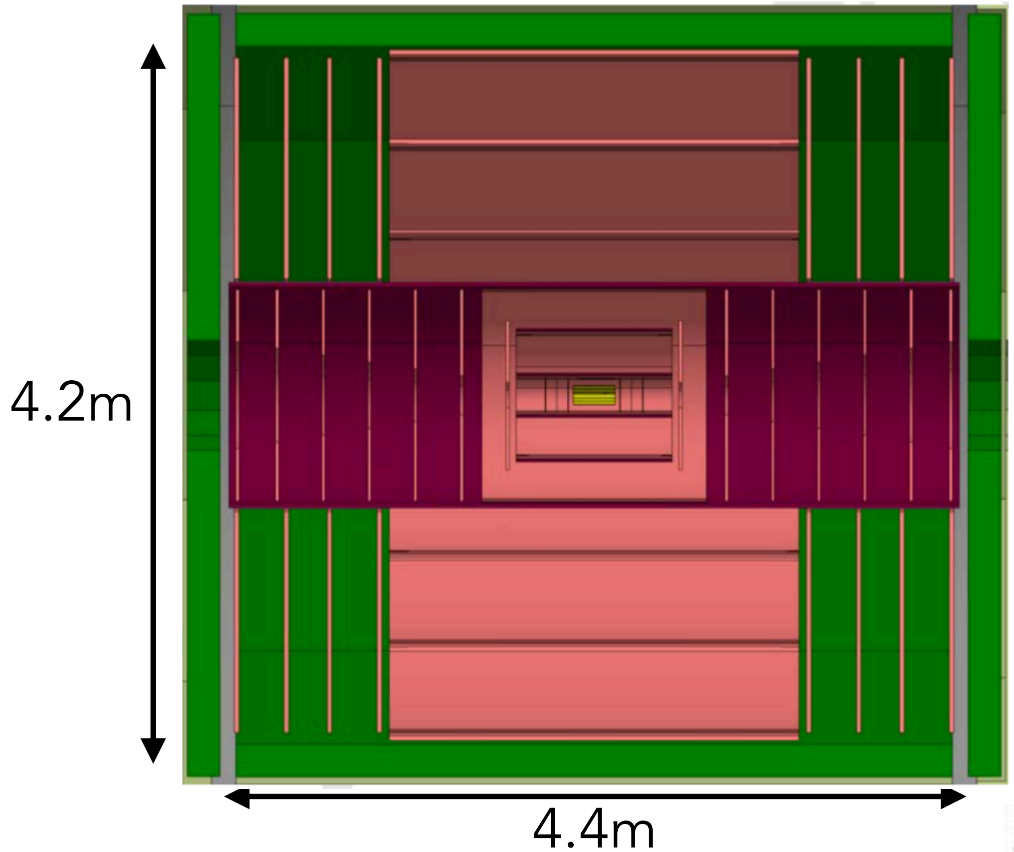
The tracker



- inner tracker
  - 3 barrel layers + 7 forward disks per side
- outer tracker
  - 3 barrel layers + 4 forward disks per side
- material budget (200 μm -thick sensors)
  - 1% X_0 per tracker layer
  - 2.5% X_0 main support + cables
- total sensitive area = 195.6 m^2

The tracker



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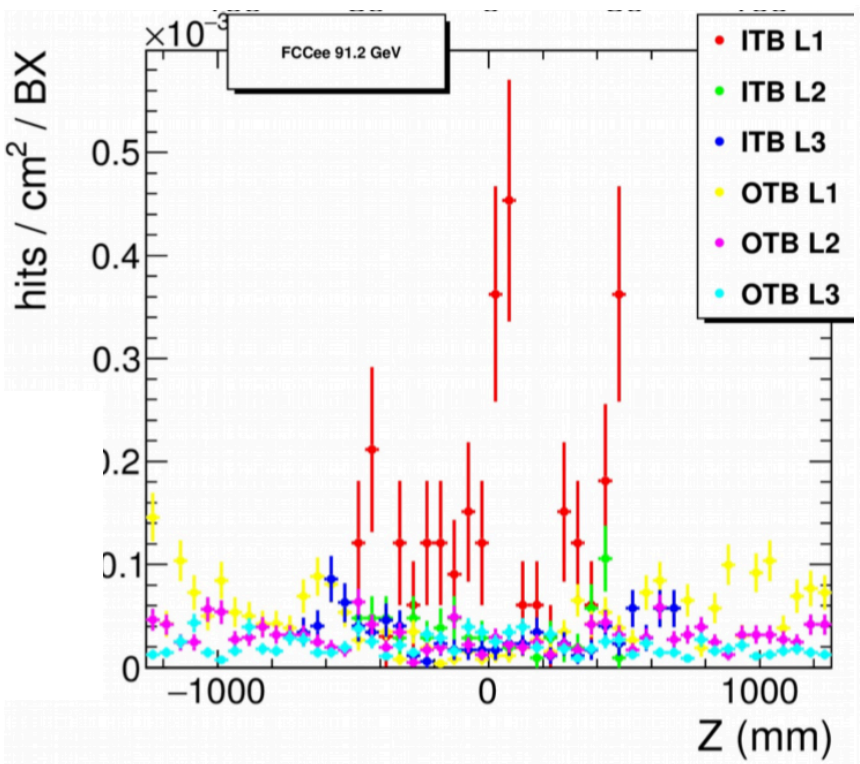
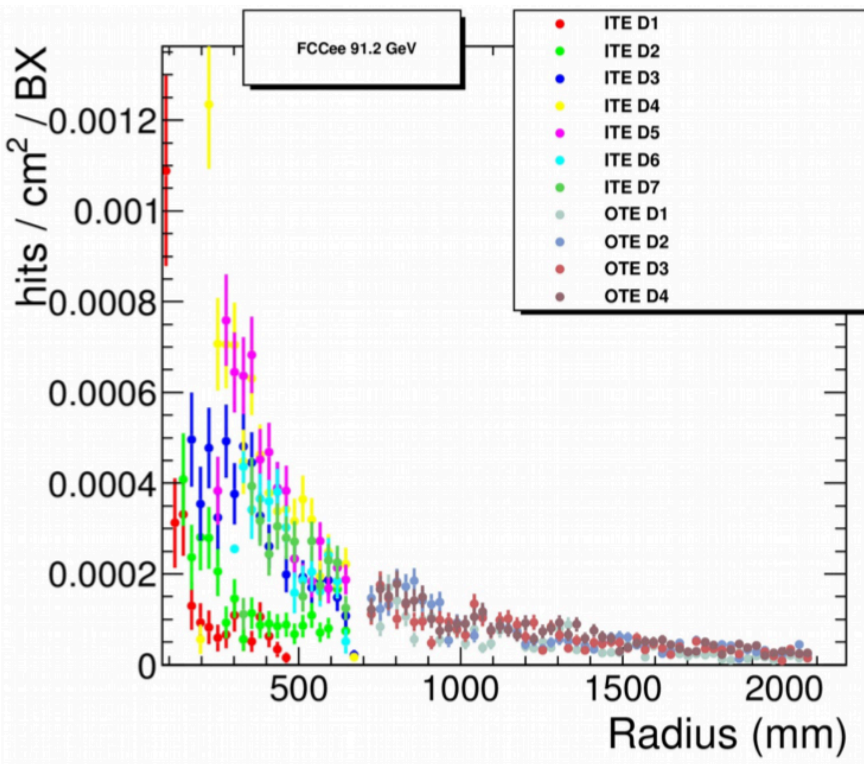
- only first inner tracker disk pixelated (from CLICdet)
- strixel sizes 30x300 μm^2
  - with analog readout => required single point resolution in (R,φ) of 7 μm
  - occupancy results confirm the need for water cooling





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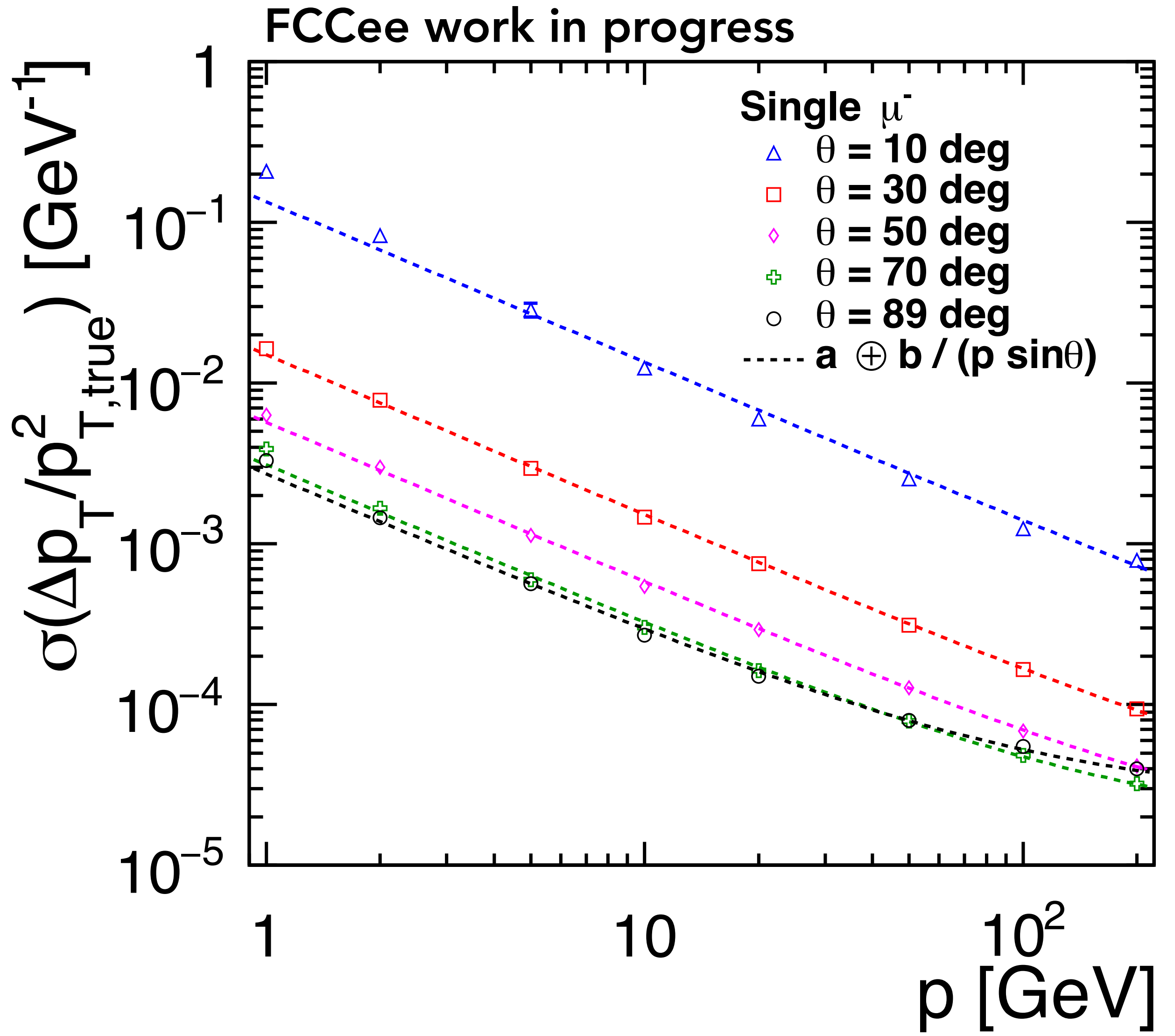
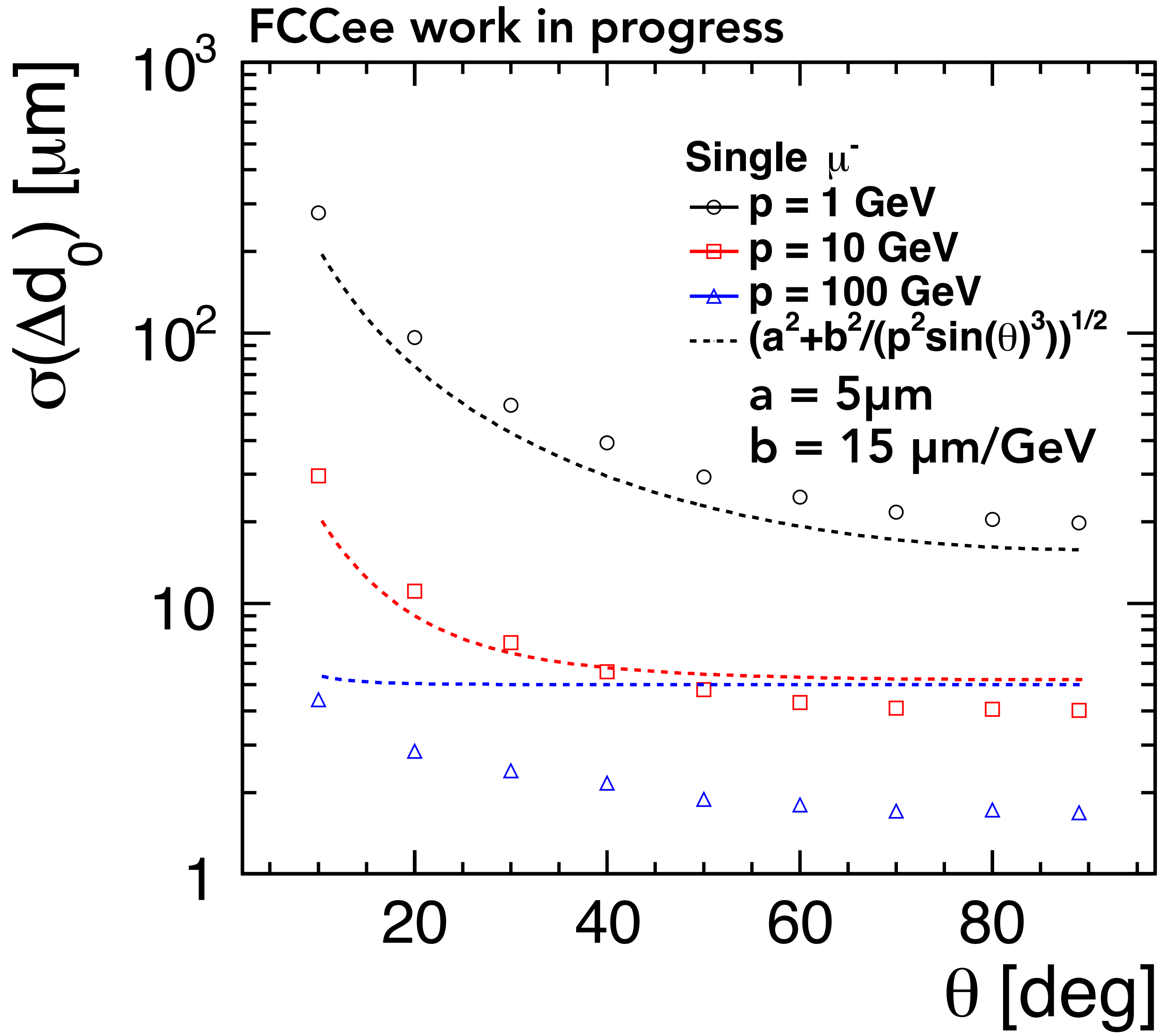
CLD tracking performances

all studies done in full simulation with iLCSoft

- Resolution = σ of the Gaussian fit of the (reco-true) distributions





Achieved **transverse momentum resolution** of 3-4x10^{-5} GeV^{-1} for high-energy muons in the barrel (highest data point under investigation)

Achieved **impact parameter resolution** below 1 μm for high-energy muons in the barrel (well below the high momentum limit of 5 μm)

Technology R&D

- Broad R&D program carried out within the CLICdp Collaboration with CLIC as a target
- motivated by stringent requirements for the CLIC vertex and tracker
- profits from some CLIC-related features, such as low-duty cicle
  - this affects mostly the powering and the readout data rates
- In this talk: a personal selection (more in the backup)

Technology R&D

https://indico.cern.ch/event/666427/contributions/2880139/attachments/1602394/2540978/CLIC-SiPixelRD_Trento-Munich_19Feb2018.pdf

Technology R&D

Sensor + readout technology	Currently considered for
Bump-bonded Hybrid planar sensors	Vertex
Capacitively coupled HV-CMOS sensors	Vertex
Monolithic HV-CMOS sensors	Tracker
Monolithic HR-CMOS sensor	Tracker
Monolithic SOI sensors	Vertex, Tracker

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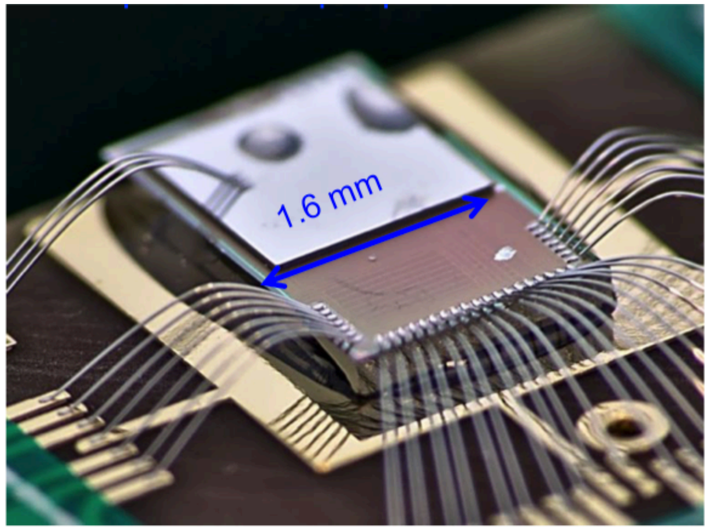
Monolithic SOI sensors	Vertex, Tracker



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Sensor + readout technology	Currently considered for
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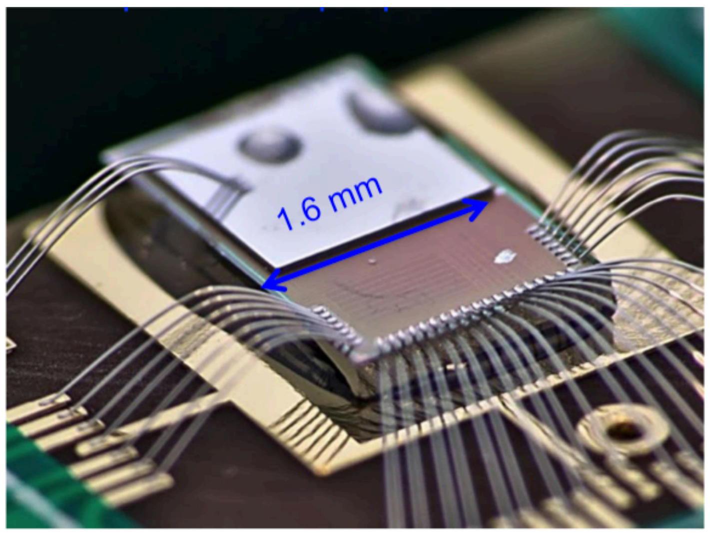
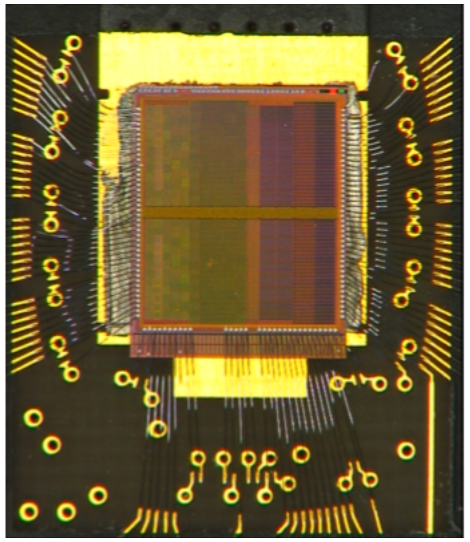
Monolithic HV-CMOS sensors	Tracker
Monolithic HR-CMOS sensor	Tracker
Monolithic SOI sensors	Vertex, Tracker

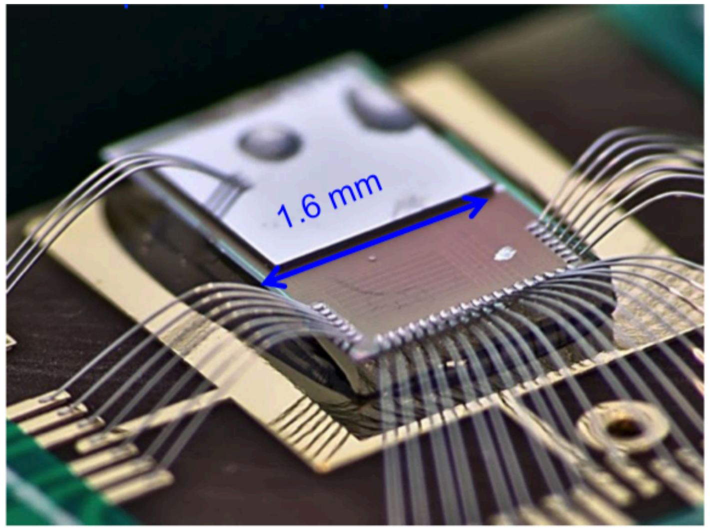


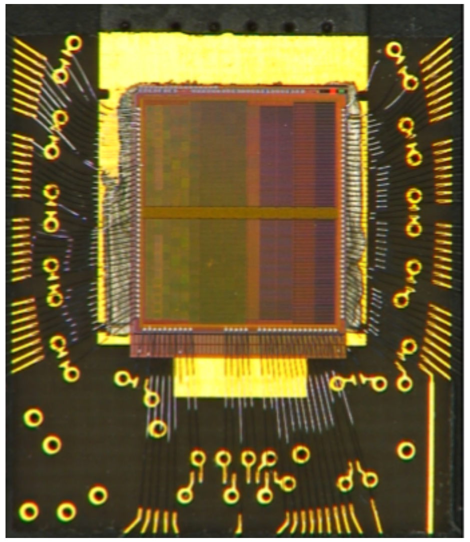


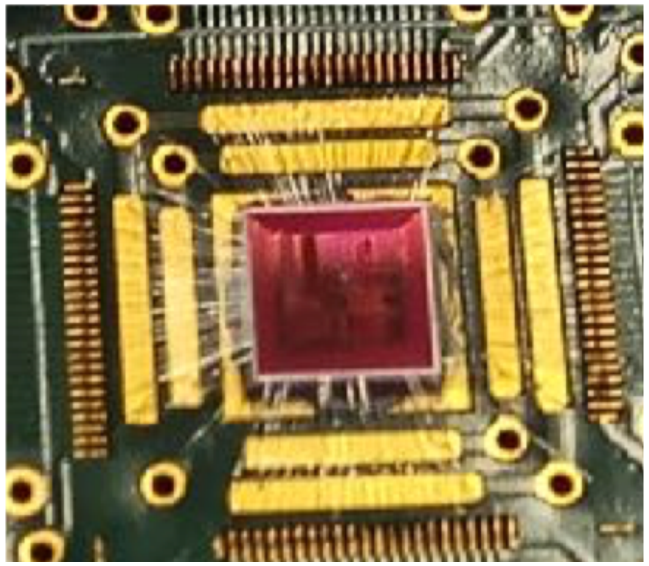
https://indico.cern.ch/event/666427/contributions/2880139/attachments/1602394/2540978/CLIC-SiPixelRD_Trento-Munich_19Feb2018.pdf

Technology R&D

Sensor + readout technology	Currently considered for
Bump-bonded Hybrid planar sensors	Vertex
Capacitively coupled HV-CMOS sensors	Vertex
Monolithic HV-CMOS sensors	Tracker
Monolithic HR-CMOS sensor	Tracker
Monolithic SOI sensors	Vertex, Tracker







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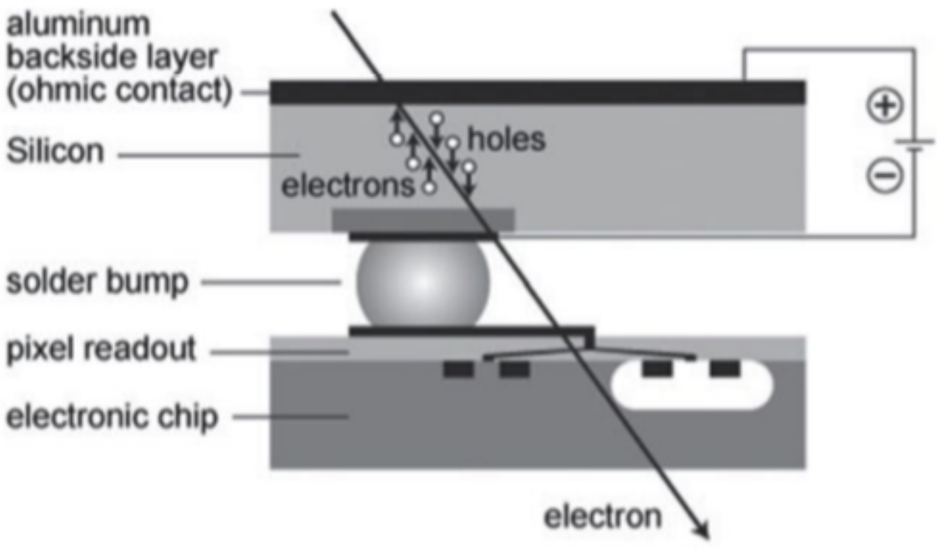
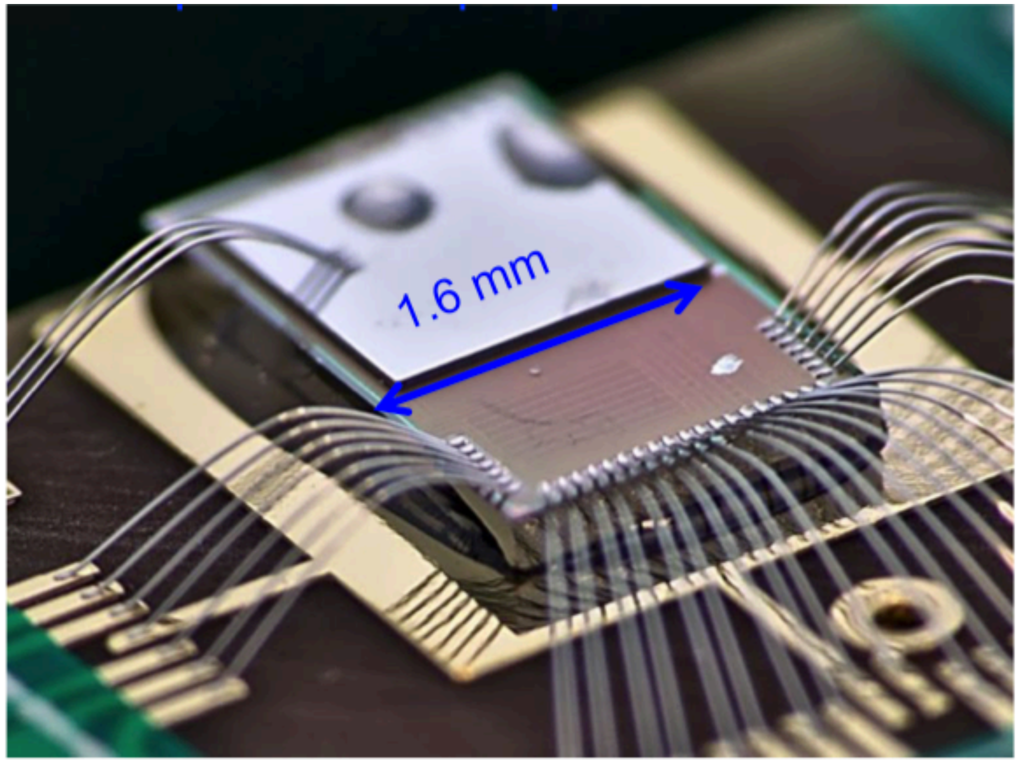
Technology R&D for vertex

Bump-bonded hybrid planar sensor

- planar pixel sensors bump-bonded to readout ASICs
- CLICpix/CLICpix2 prototype readout ASICs with in-pixel time and charge measurement, 25x25 μm^2 pitch, implemented in 65 nm process
- **~100%** efficiency, **few ns** timing, **σ_{SP} ~ 7 μm**
- ongoing work to reduce σ_{SP}: ELAD sensors with enhanced charge sharing





https://cds.cern.ch/record/2264891/files/CLICdp-Conf-2017-010.pdf

Technology R&D for vertex

Bump-bonded hybrid planar sensor

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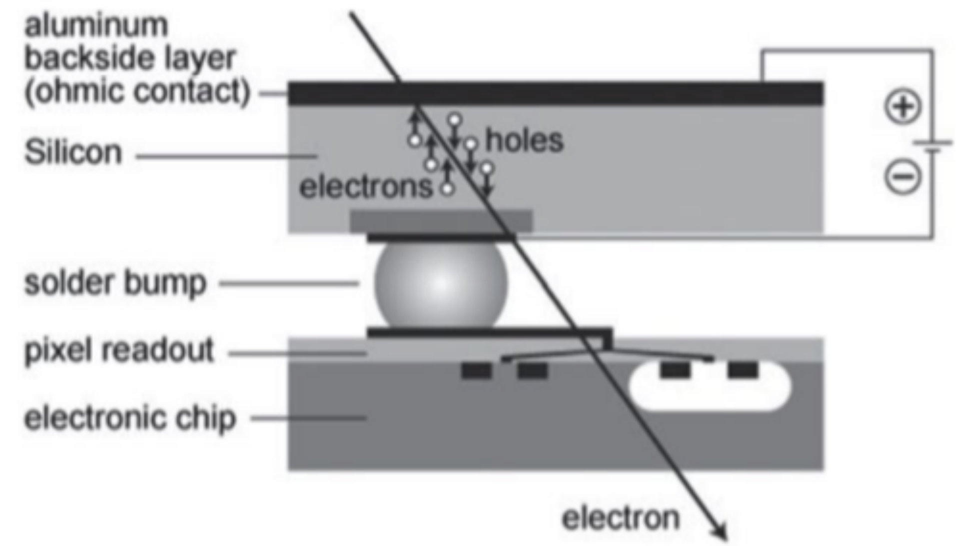
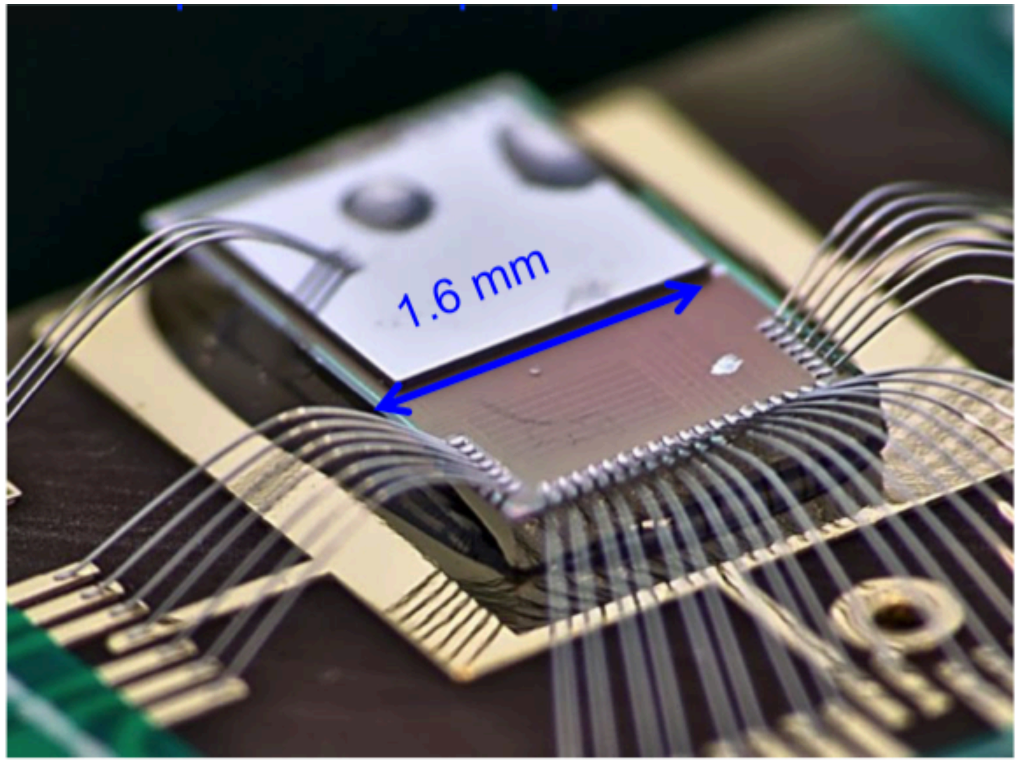
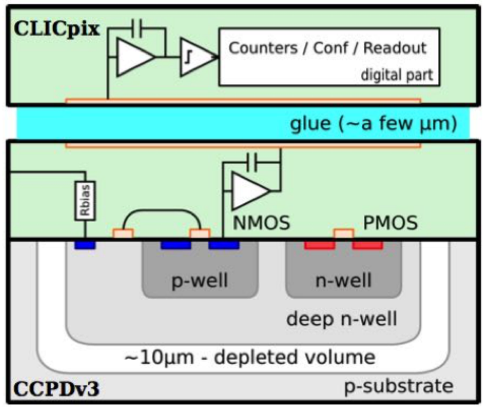




- alternative to bump-bonded sensors: **capacitively coupled HV-CMOS sensors**
  - thin glue layer replaces costly small-pitch bump bonds
  - **~90-100%** efficiency, **few ns** timing, **σ_{SP} ~ 6 μm**



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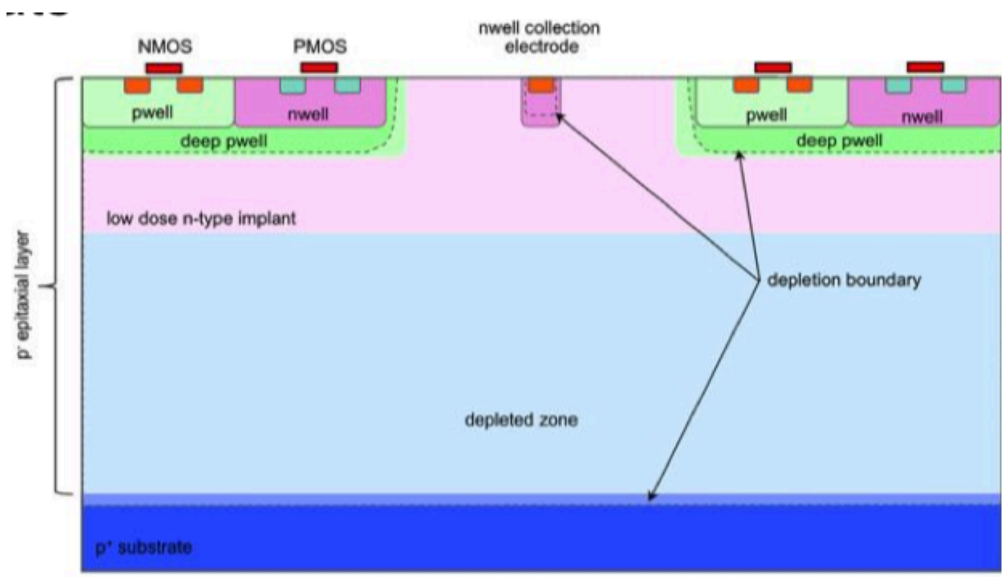
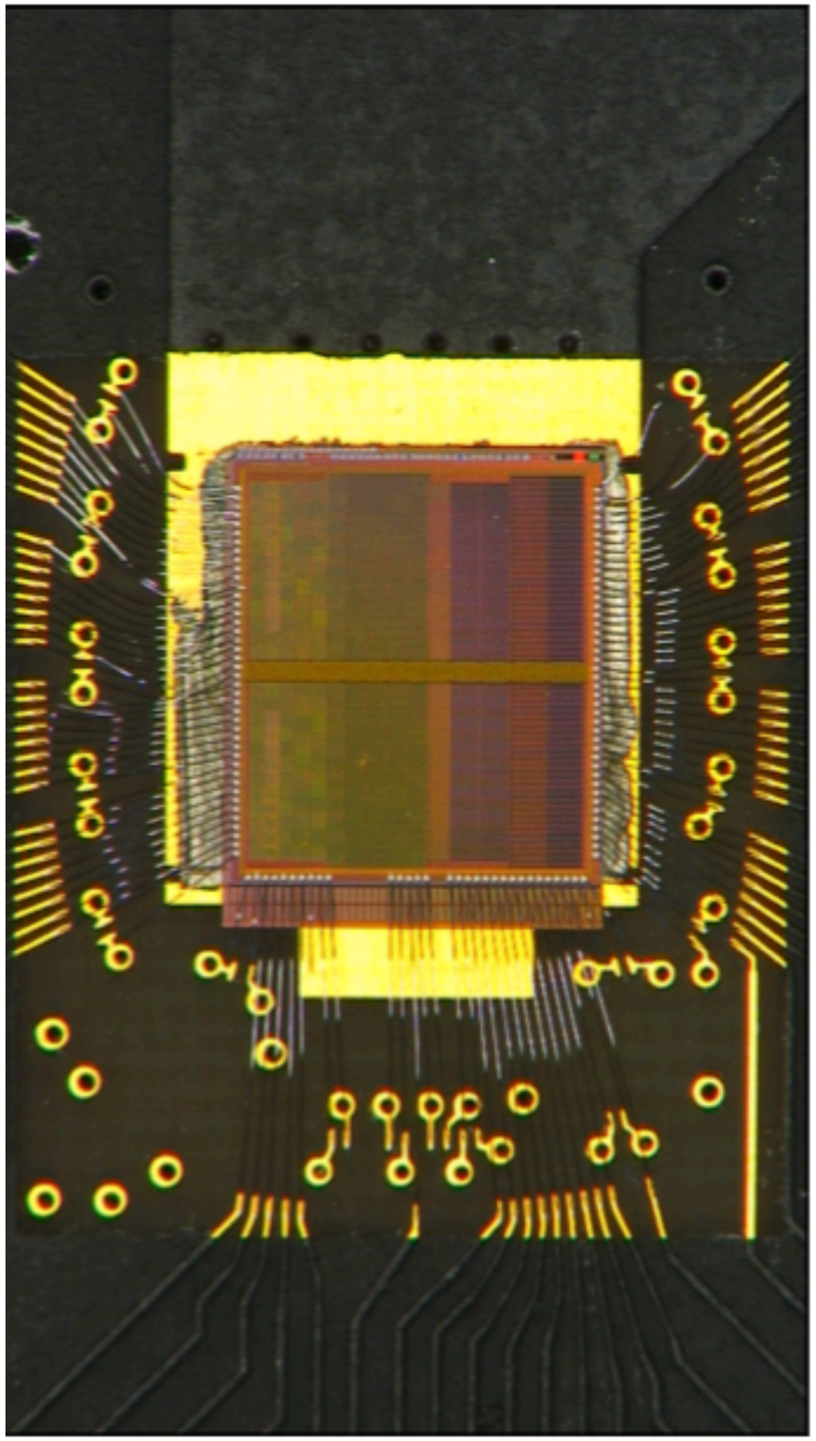
Technology R&D for tracker

Integrated HR-CMOS sensors



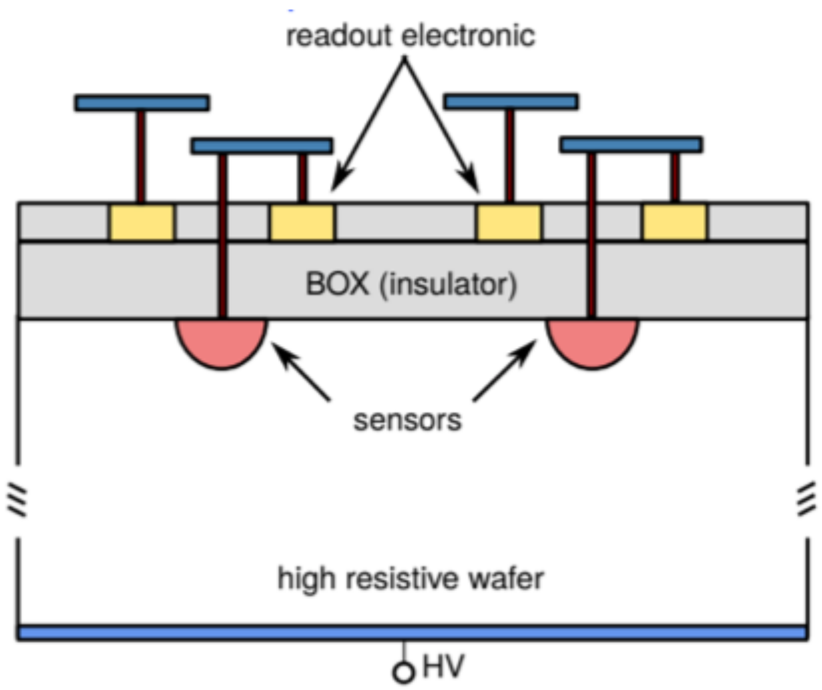


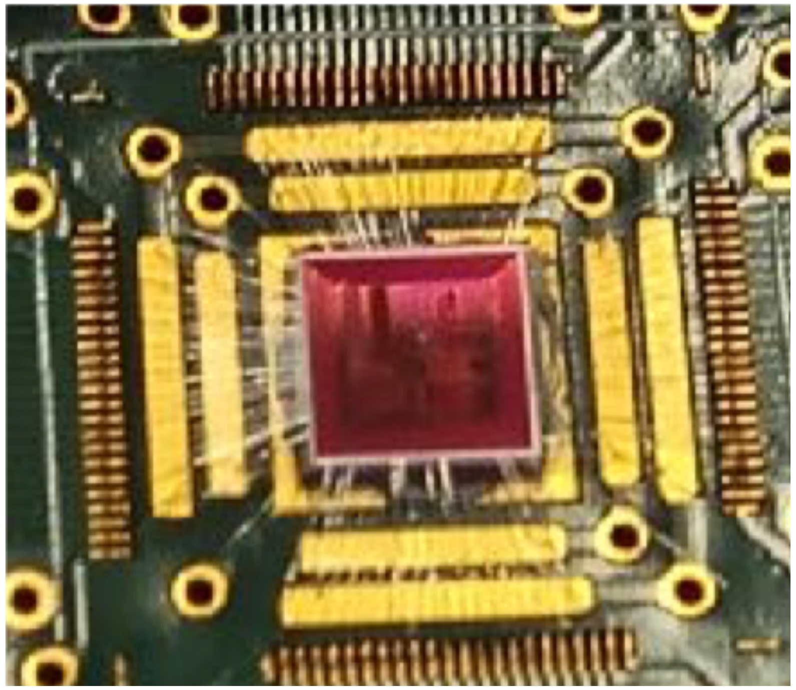
- integrated CMOS sensor on High-Resistivity substrate
- tests with INVESTIGATOR analog prototype chip in TowerJazz 180 nm HR-CMOS process (ALICE development): 20x20 - 50x50 μm^2 pitch
  - for 28x28 μm^2, with *external readout:* **~99.3%** efficiency, **<5 ns** timing, **σ_{SP} ~ 4 μm**
- ongoing work to design *fully integrated* CLICTD chip: 30x300 μm^2 pitch, be thinned to 50-100 μm
- plan to use smaller feature size processes in the future => to become an option for the vertex detector as well

http://cds.cern.ch/record/2284145/files/

Technology R&D for vtx & trk

Monolithic SOI sensors





- Silicon-On-Insulator (SOI): sensor and electronics integrated on single wafer with high-resistivity substrate
- Cracow SOI test chip in 200 nm LAPIS SOI process
  - for 500 μm thick sensors and 30x30 μm² pitch
    => **>99%** efficiency, **σ_{SP} ~ 4.5 μm**
- ongoing work is the production of CLICPS vertex test chip, *targeted to Linear Collider* vertex requirements: 20x20 μm² pitch, snapshot readout of analog time and charge measurement, >= 100 μm thickness
- promising option for tracker and also for stringent vertex requirements

http://cds.cern.ch/record/2310056

Summary

- The **CLICdet** design features an all silicon vertex + tracker system that meets the CLIC physics goals and experimental constraints
- The **CLD** detector has been adapted from the CLICdet to the FCC-ee experimental conditions
- Both detectors are implemented and validated in **full simulation** in iLCSoft
  - LCIO, DD4hep, Marlin, iLCDirac
- A broad **R&D program** is ongoing in the CLICdp Collaboration to push the available technologies to meet the stringent requirements of CLICdet
  - to be followed-up for the case of FCC-ee continuous collisions and different backgrounds

Thanks to everyone who provided material for this talk

CLIC CDR ⇒ detector requirements

★ **momentum resolution:**

e.g, HZ, $g_{H\mu\mu}$, Smuon endpoint

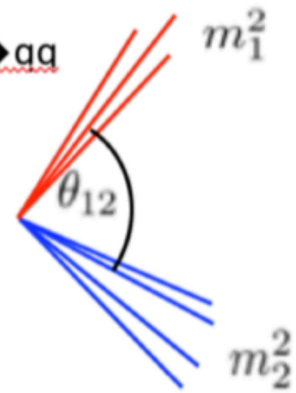
$$\boxed{\sigma_{p_T}/p_T^2 \sim 2 \times 10^{-5}\ \mathrm{GeV}^{-1}}$$

★ **jet energy resolution:**

e.g. W/Z/H di-jet mass separation, ZH with Z→qq

$$\boxed{\frac{\sigma_E}{E} \sim 3.5 - 5\ \%}$$

(for high-E jets, light quarks)

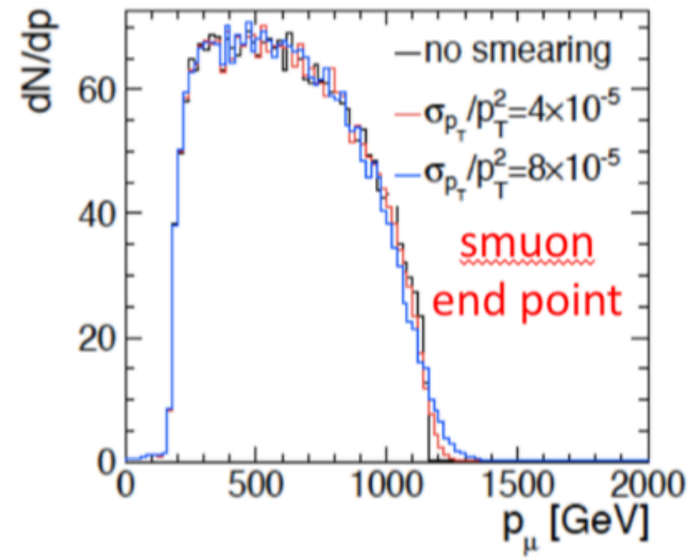


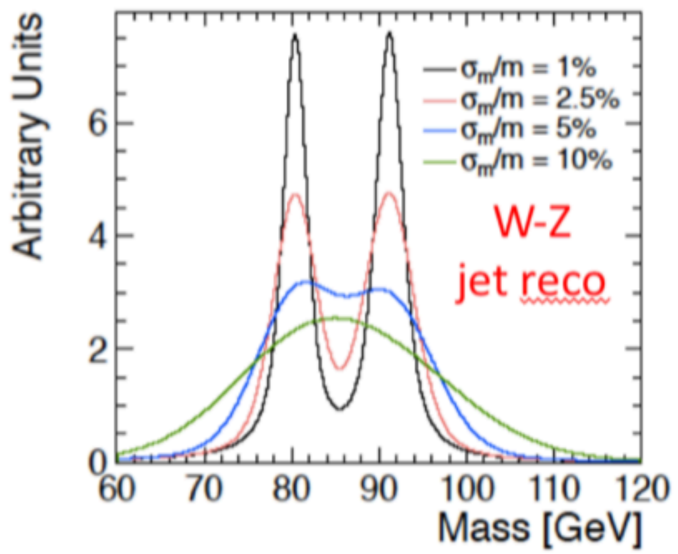
★ **impact parameter resolution:**

e.g. c/b-tagging, Higgs BR

$$\boxed{\sigma_{r\phi} = 5 \oplus 15/(p[\mathrm{GeV}]\sin^{\frac{3}{2}}\theta)\ \mu\mathrm{m}}$$

★ **angular coverage, very forward electron tagging**



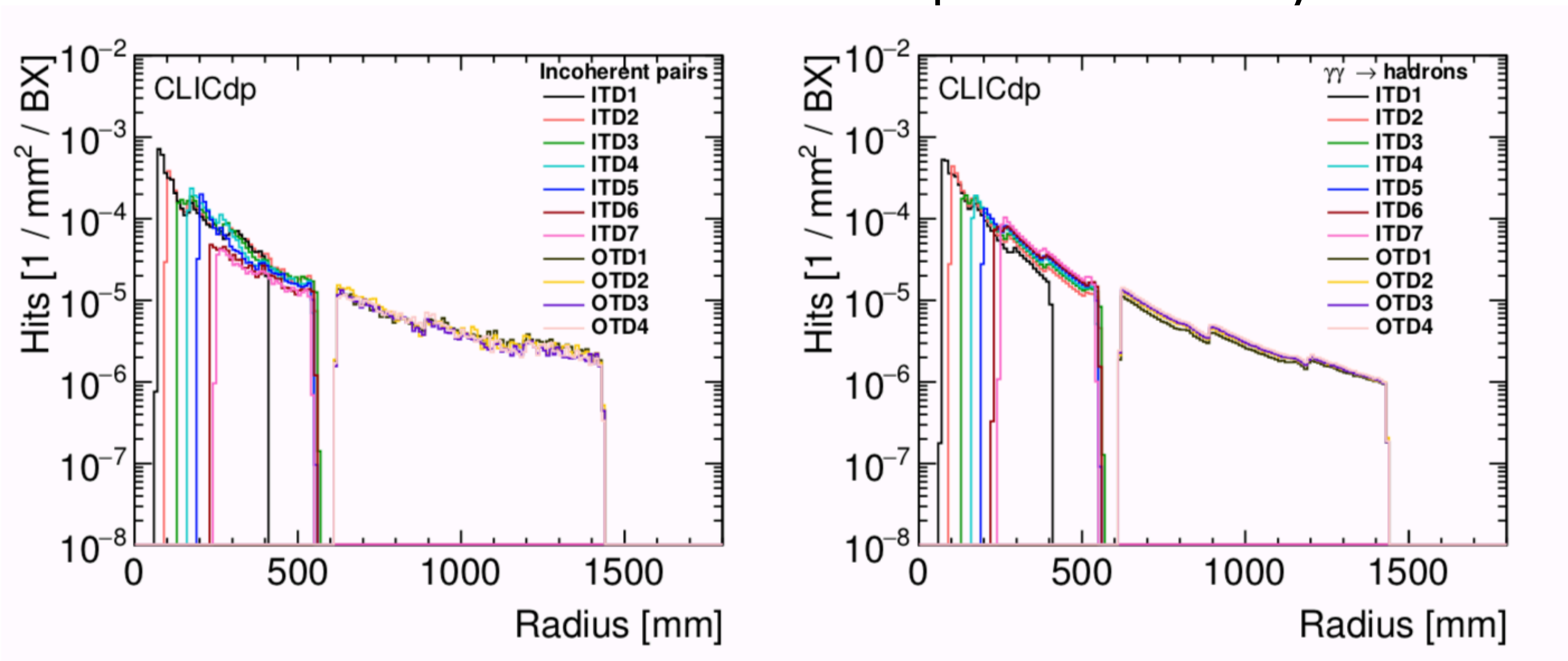


+ requirements from experimental conditions

- Small cell sizes for low cell occupancies in general and for Particle-Flow Analysis
- Accurate hit timing (1 ns in calorimeters, ~5 ns in trackers)

Extra material

CLICdet tracker endcap hit density



(a) Tracker disks hit density (b) Tracker disks hit density

Figure 19: Distribution of the hit densities per bunch crossing in the tracker disks from incoherent electron–positron pairs (left) and $\gamma\gamma \rightarrow$ hadrons (right) at 3 TeV. Safety factors are not included.

Hybrid planar sensor technology

- Planar pixel sensors bump-bonded to r/o ASICs
- Considered for vertex detector

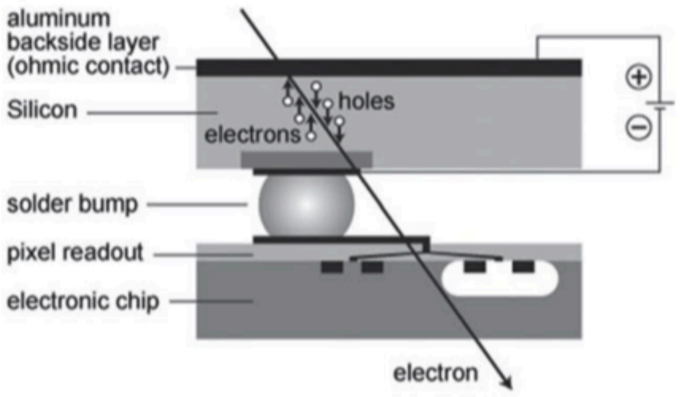
Status:

- Comprehensive thin-sensor studies with slim-edge and active-edge sensors (50-300 μm thickness) on Timepix/Timepix3 readout ASICs
- CLICpix/CLICpix2 prototype r/o ASICs with in-pixel time and energy measurement, 25x25 μm^2 pitch, implemented in 65 nm TSMC process, including full 12" wafer from RD53 prototype run
- Single-chip bump-bonding with 25 μm pitch
- ~100% efficiency, few ns timing, σ_{SP}~7 μm

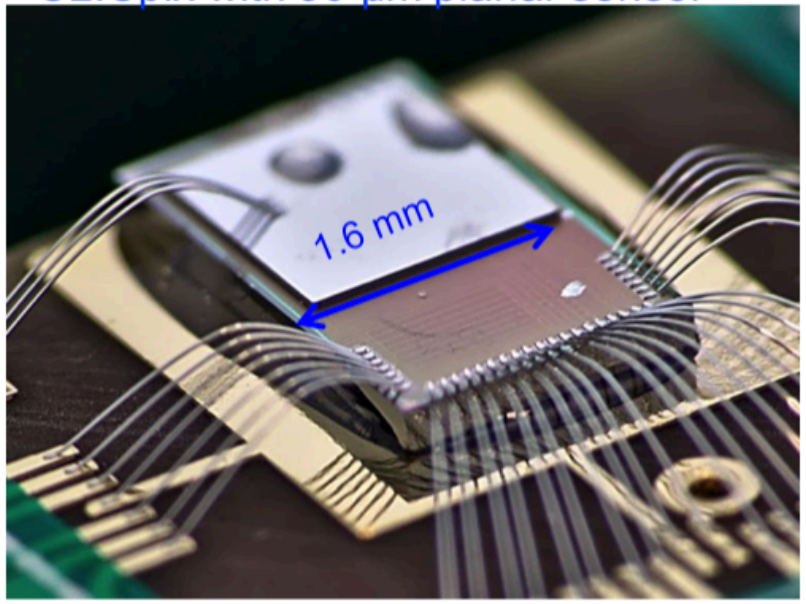
Ongoing work:

- Validation of new single-chip bump-bonding process
- Beam tests for CLICpix2 planar-sensor assemblies
- Reduce σ_{SP}: ELAD sensors with enhanced charge sharing

Hybrid pixel detector



CLICpix with 50 μm planar sensor



Future developments:

- Even smaller pixels (28 nm process technology), lower detection threshold
- New hybridisation methods: Cu pillars, Indium, Anisotropic Conductive Film, …
- Module/stave building studies

CLICdp-Conf-2017-010

Extra material

Capacitively coupled HV-CMOS sensors

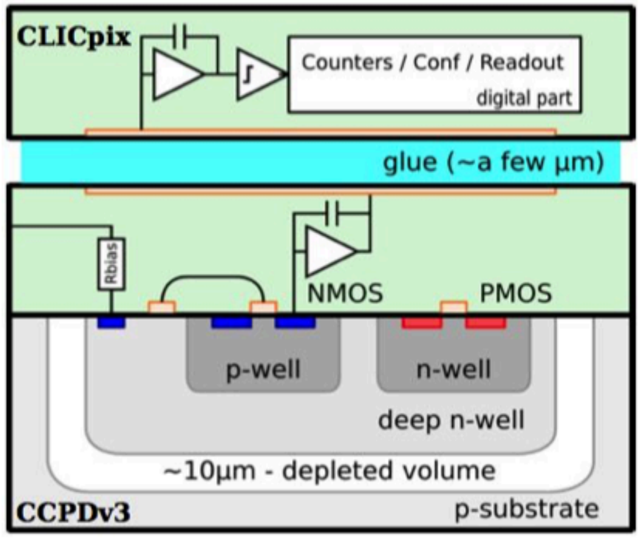
- Active High-Voltage (HV) CMOS sensors, large fill factor: electronics inside charge-collection well, depletion through HV
- Capacitive coupling to r/o ASICs
  → thin glue layer replaces costly small-pitch bump bonds
- Considered for vertex detector

Results:
- Two generations of active sensors (CCPDv3, C3PD) in AMS 180 nm HV-CMOS process, 10-1000 Ohm cm substrates, 25x25 μm^2 pitch
- Glue assemblies with CLICpix/CLICpix2: ~90-100% efficiency, few ns timing, σ_{SP}~6 μm
- Finite-element simulation of capacitive coupling

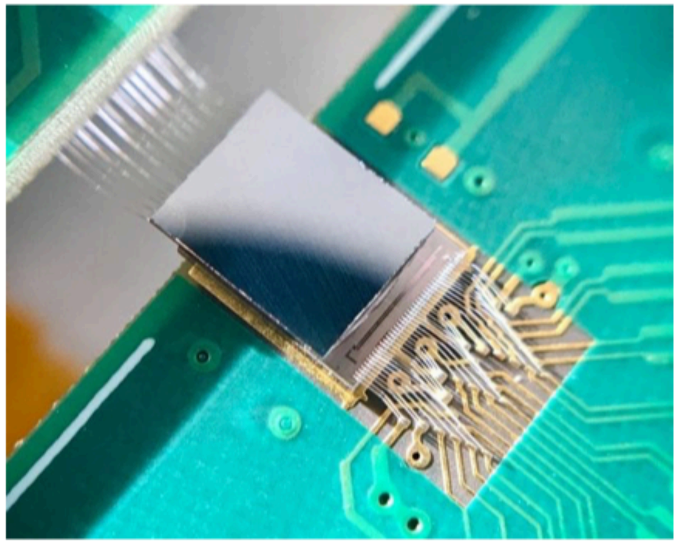
Ongoing work:
- Evaluation of sensors with high-resistivity substrates
- Optimization of gluing process (uniformity, reproducibility)
- Simulation of the entire transfer chain

Future developments:
- Module concept? (difficult!)
- A/C coupling at the fab (wafer) level + TSV
- A/C coupled passive CMOS sensors?

Capacitively Coupled Pixel Detector



C3PD/CLICpix2 glue assembly

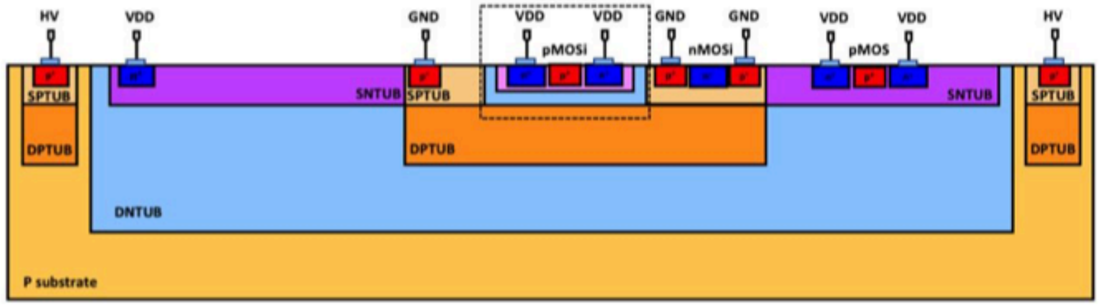


NIM A 823 (2016) 1-8; JINST 12 P09012 (2017)

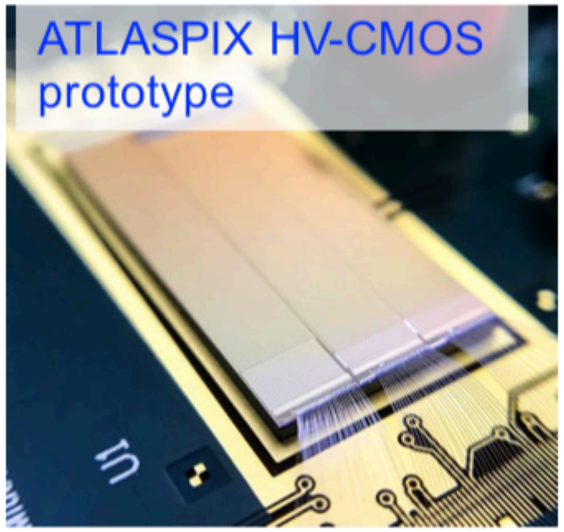
Monolithic HV-CMOS sensors

- Active HV-CMOS sensors with fully integrated readout
- Considered for tracker

AMS 180 HV-CMOS



Results:
- ATLASPIX prototypes in AMS 180 nm HV-CMOS process: 40 x 120 μm^2 pitch, data-driven column-drain readout
- 99.5% efficiency, σ_t~16-20 ns, σ_{SP}~13 μm (almost no charge sharing; timing limited by r/o system)
- Similar developments with LFoundry HV-CMOS process



Ongoing work:
- Beam tests of ATLASPIX with improved readout system (timing, lower threshold, power consumption tests)

Future developments:
- Adapt pixel layout to CLIC requirements (~30 μm pixel width)
- Improve digital design: power pulsing
- Reduce periphery area?

Extra material

Integrated HR-CMOS sensors

- Integrated CMOS sensors on High-Resistivity (HR) substrate
- Small fill factor: electronics outside charge-collection well
- Considered for tracker

Results:

- Tests with INVESTIGATOR analog prototype chip in TowerJazz 180 nm HR-CMOS process (ALICE development), 20x20 - 50x50 μm^2 pitch
- For 28x28 μm^2 pitch, external readout: 99.3% efficiency, σ_t<5 ns, σ_{SP}~4 μm

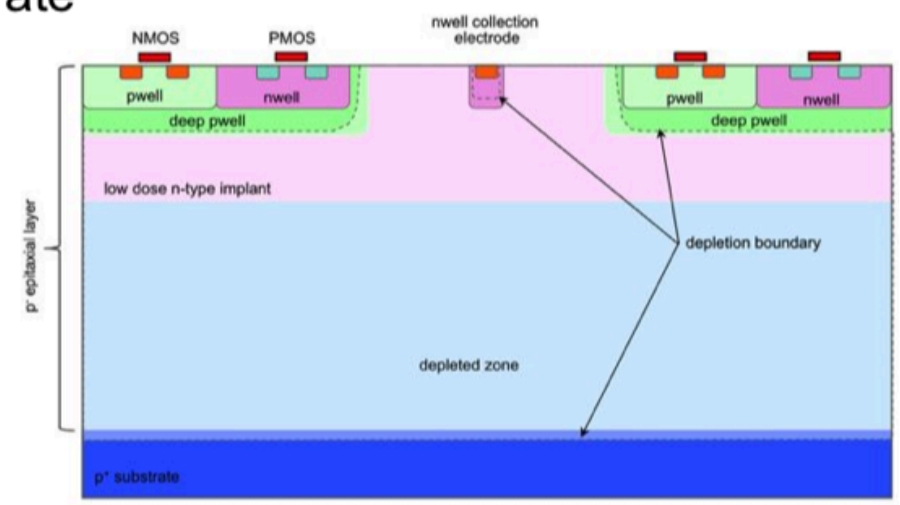
Ongoing work:

- Design of fully integrated CLICTD chip: 30 x 300 μm^2 pitch, segmented electrodes, in-pixel time + charge measurement

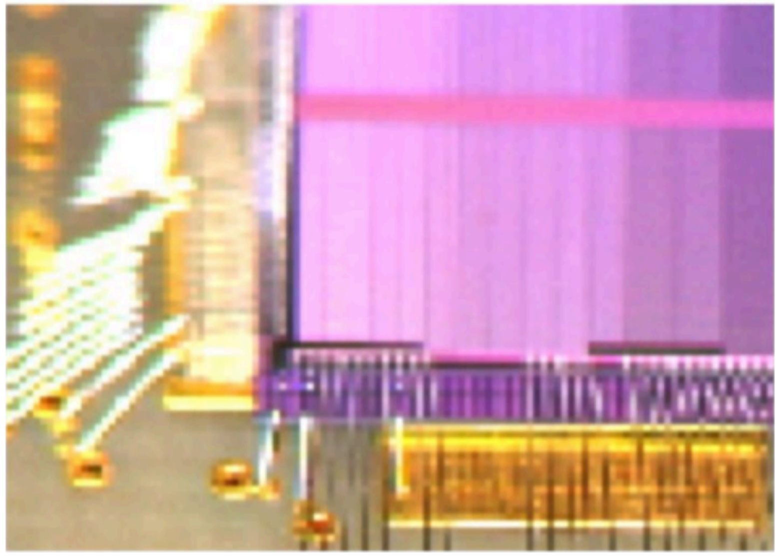
Future plans:

- Thinning to 100 μm
- Larger prototypes
- Further process optimization / smaller feature size? → could also become an option for the vertex detector

HR-CMOS process



INVESTIGATOR HR-CMOS test chip



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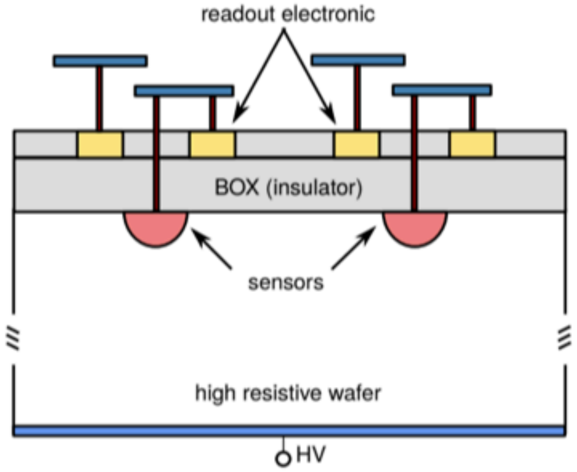
Extra material

Monolithic SOI sensors

- Silicon-On-Insulator (SOI): Sensor and electronics integrated on single wafer with high-resistivity substrate, separated by insulation oxide layer + buried p-wells,
- Considered for vertex and tracker

SOI pixel detector



Results:

- Cracow SOI test chip in 200 nm LAPIS SOI process, with various geometries and technology parameters: >=30x30 μm^2 pitch, single SOI and double SOI, different r/o schemes
- Test results for 500 μm thickness, 30x30 μm^2 pitch, rolling-shutter r/o: >99% efficiency, σ_{SP}~4.5 μm

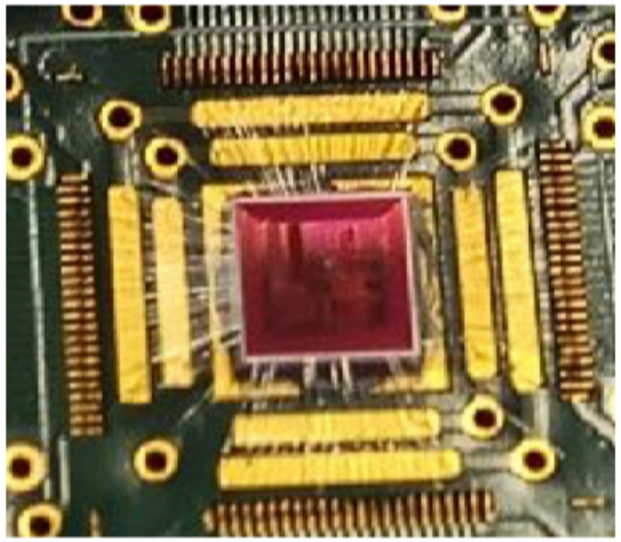
Ongoing work:

- Production of CLIPS vertex test chip, targeted to LC vertex requirements: 20x20 μm^2 pitch, snapshot r/o of analog time and charge measurement, ≧100 μm thickness
- Analysis of first-generation prototype test-beam data
- Development of readout system for CLIPS

Future plans:

- Larger chips, improved readout

Cracow SOI test chip



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