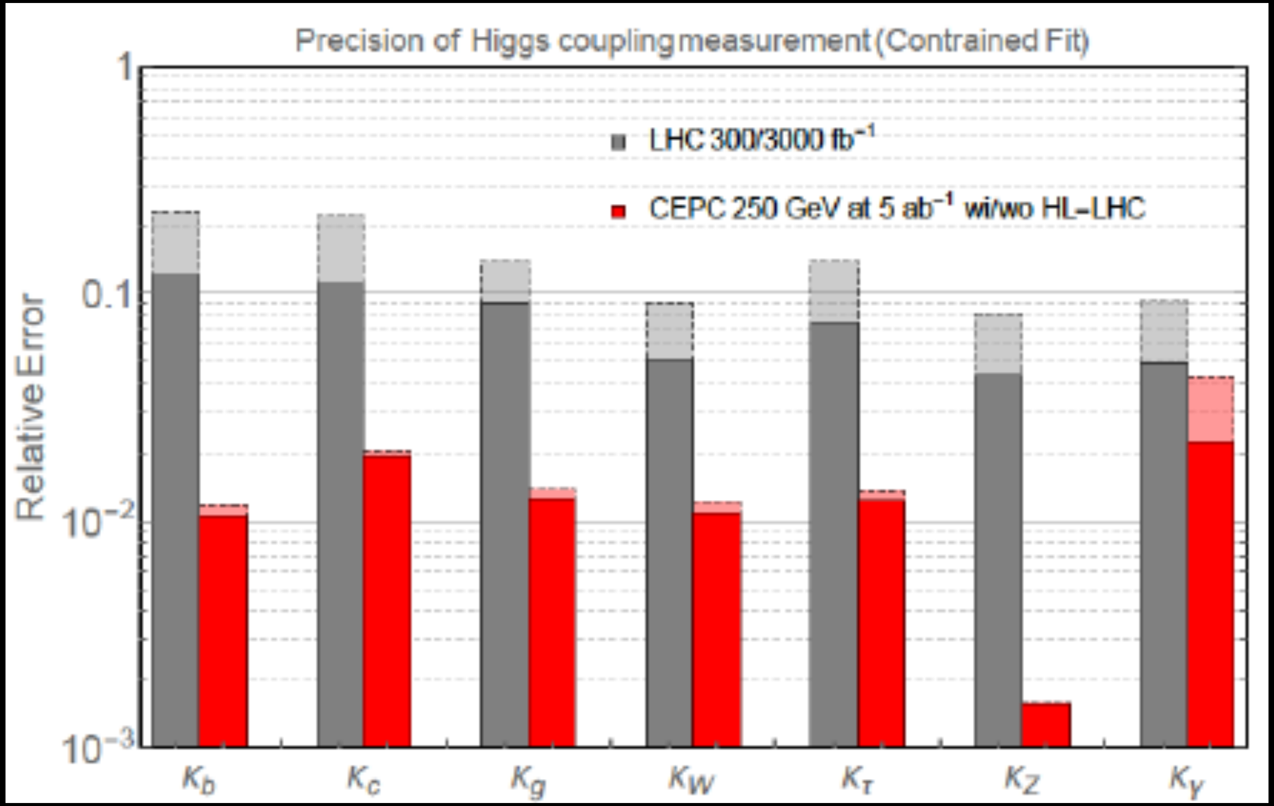
CepC Tracker Summary

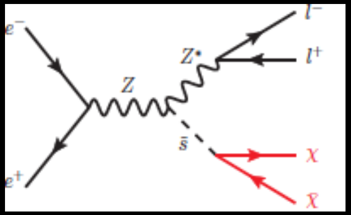
D. Bortoletto
University of Oxford

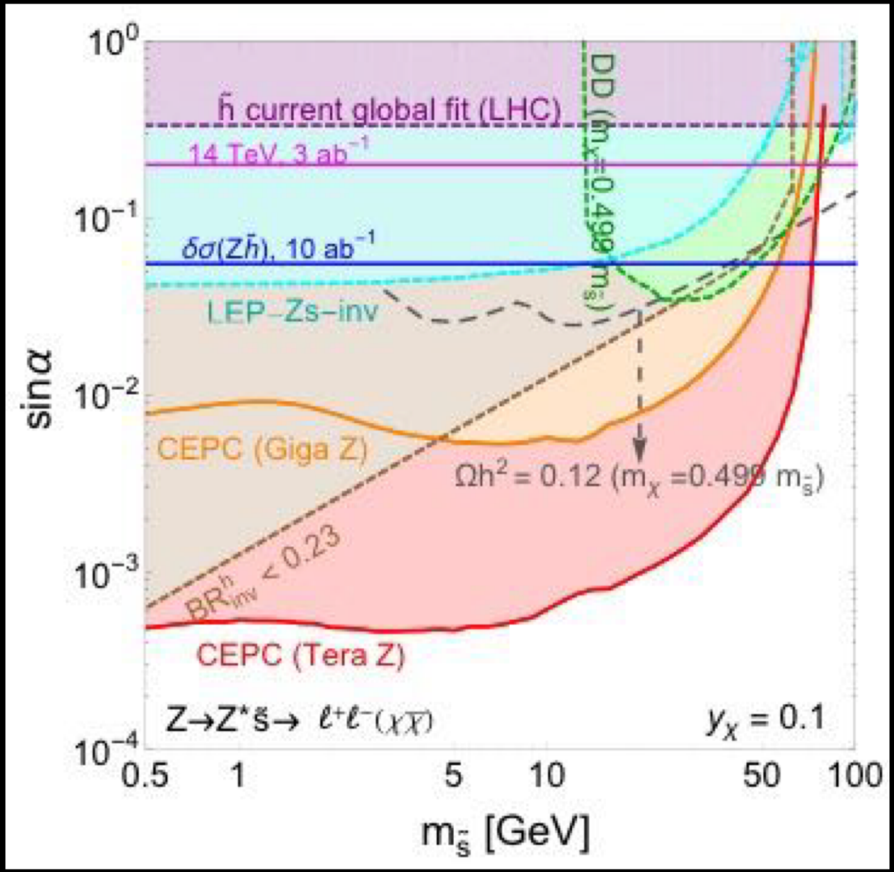
CepC Physics

- Precision Z, W, and Higgs measurements

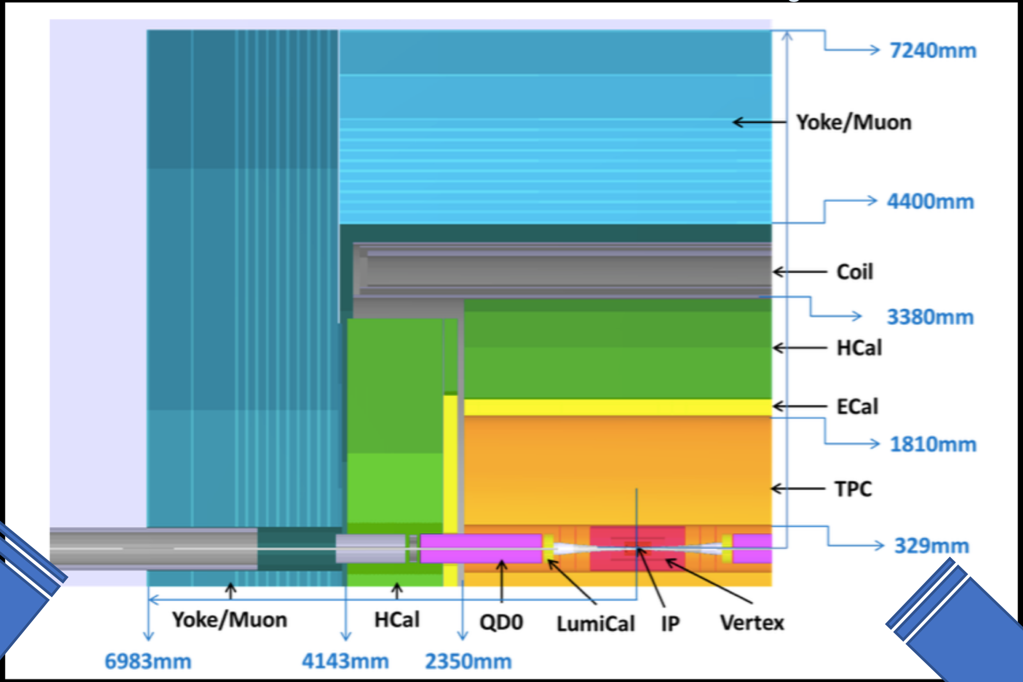


Dark sector search with Z rare decays



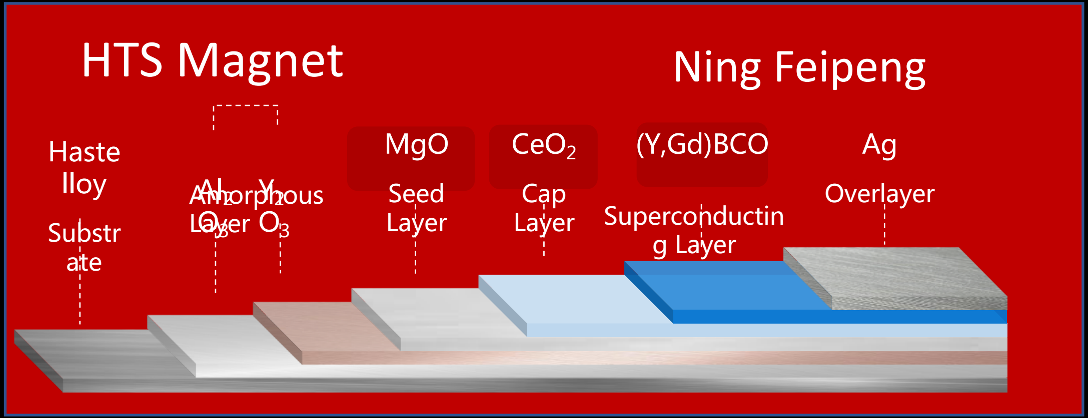


Detector Conceptual Designs (CDR)

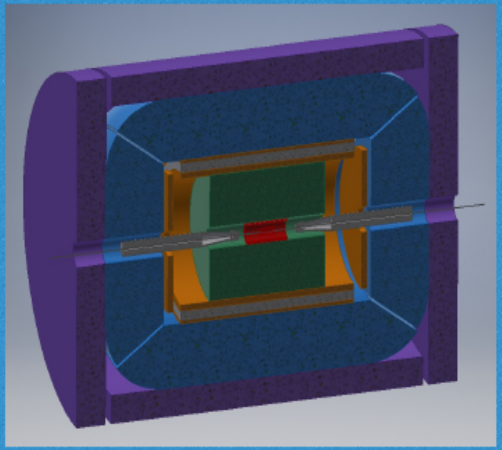


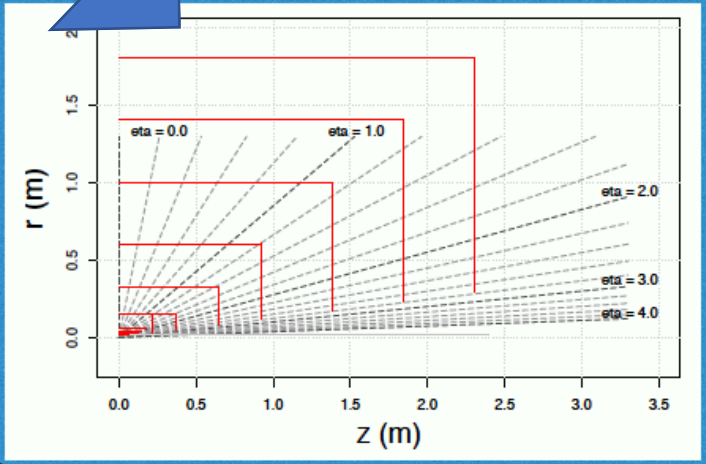
Tracking detectors:

- Vertex identification
- Momentum measurements
- Particle ID



Low magnetic field concept (2 Tesla)





Full silicon tracker concept

Vertex Detector

- Identification of heavy quarks (b/c) is essential to e^+e^- collider physics program
- H→bb, cc requires a=5 μm (intrinsic resolution), b=10 μm (multiple scattering)

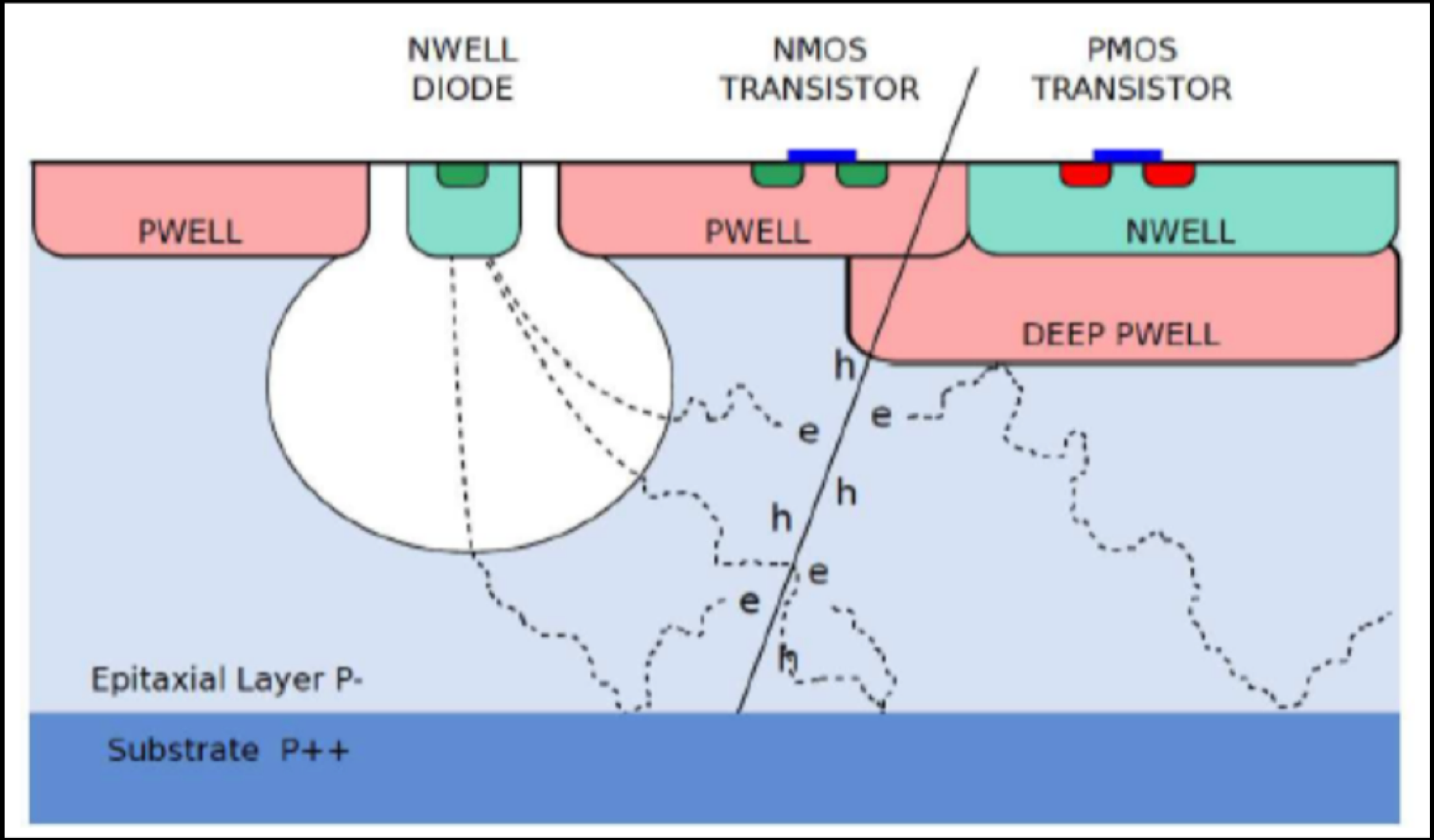
$$\sigma(r\phi) = a \oplus \frac{b}{p(\mathrm{GeV})\sin^{3/2}\theta}\ \mu\mathrm{m}$$

- Space point resolution near IP 3μm
- Material budget <0.15% X_0/layer
- Low Detector occupancy <0.5%
- Radiation tolerance >1MRad/year and 10^{13} 1Mev/n_{eq}/y

CMOS Sensors

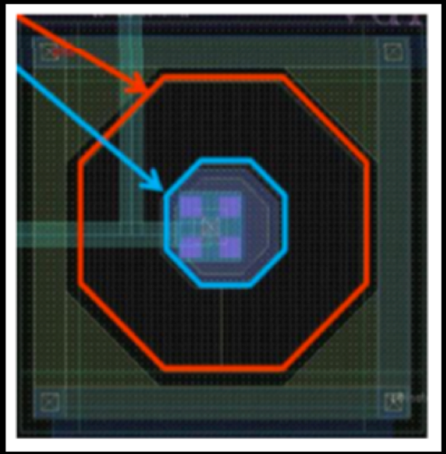
- Monolithic sensors

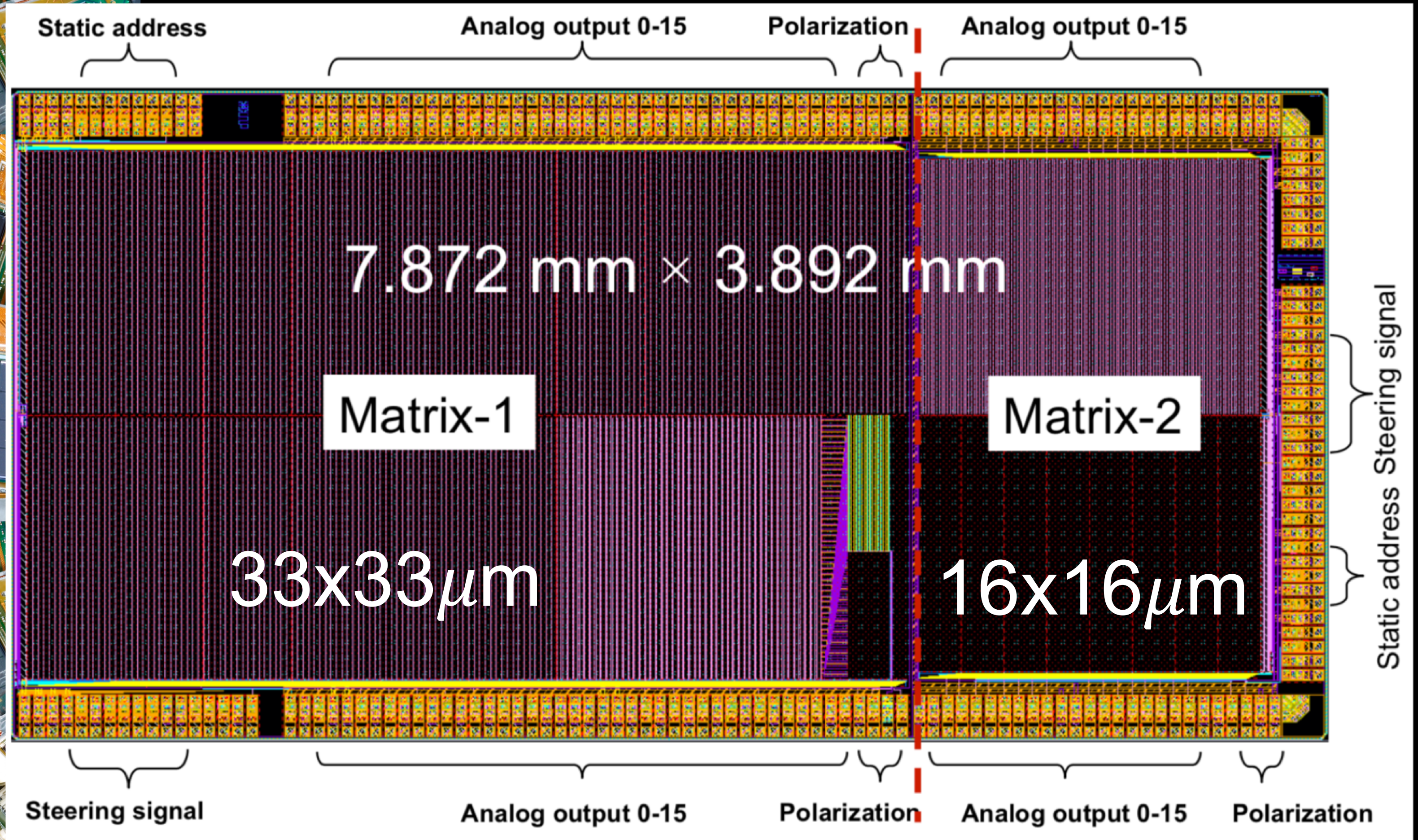
Tower Jazz CIS 180 nm
- Used in ALICE upgrade
- Modified process considered for ATLAS Pixel ITk



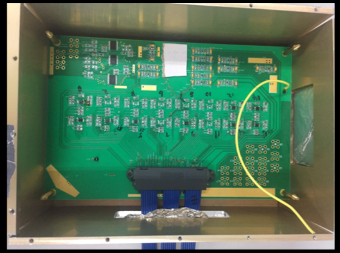
First submission JADEPIX1

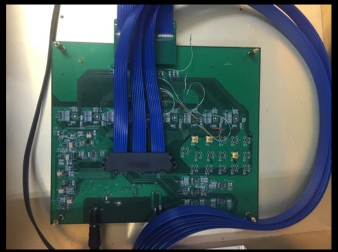
- Join MPW with IPHC in 2015 to understand charge collection performance with different geometries and epitaxial layer properties

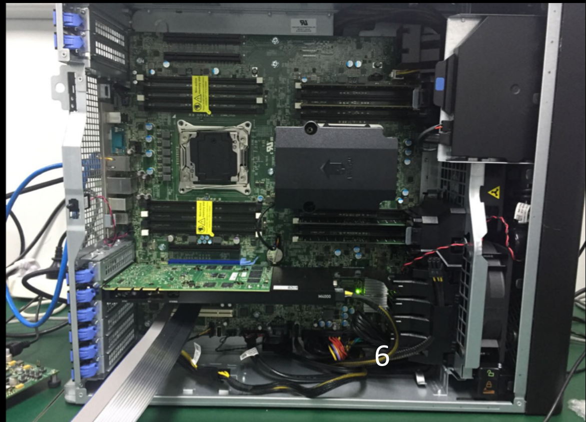




Testing system developed at IHEP

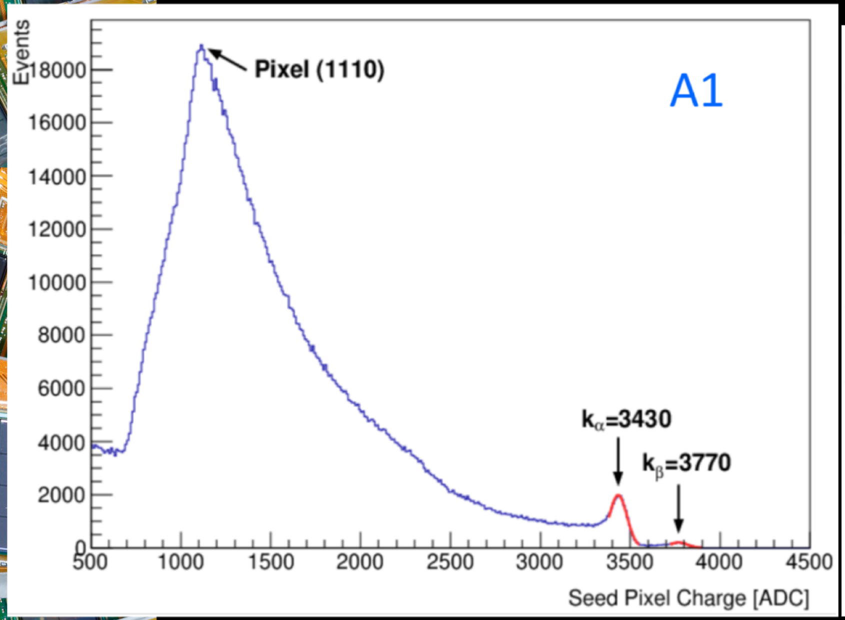




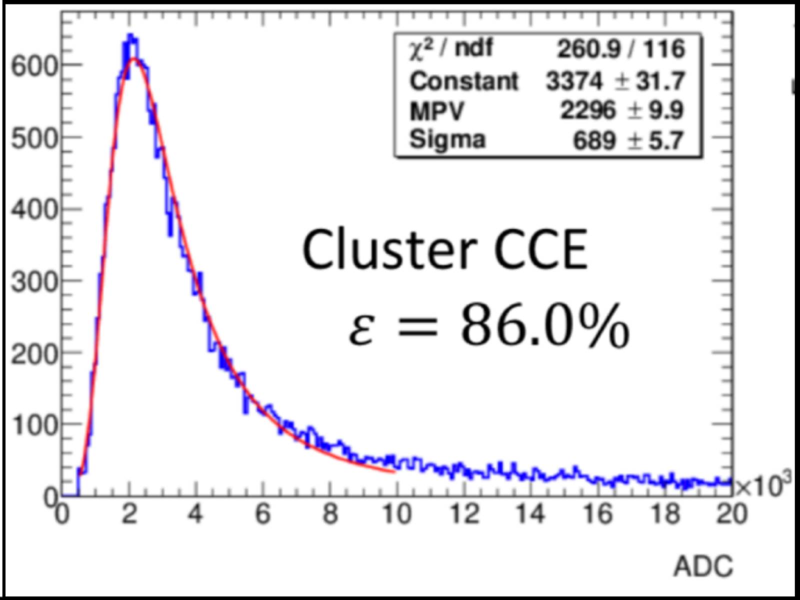


JADEPIX1 studies

- ^{55}Fe



- ^{90}Sr

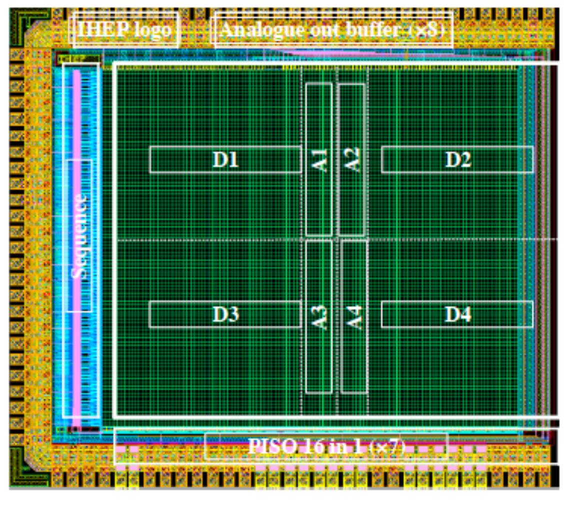


Neutron irradiation at Xi'an pulse reactor to 10^{12}, $5x10^{12}$, 10^{13}

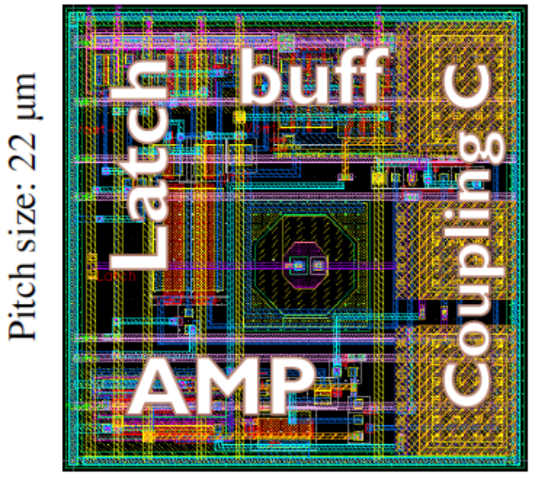
Beam test at DESY august 27, September 2, 2018

JadePix2 in CMOS technology

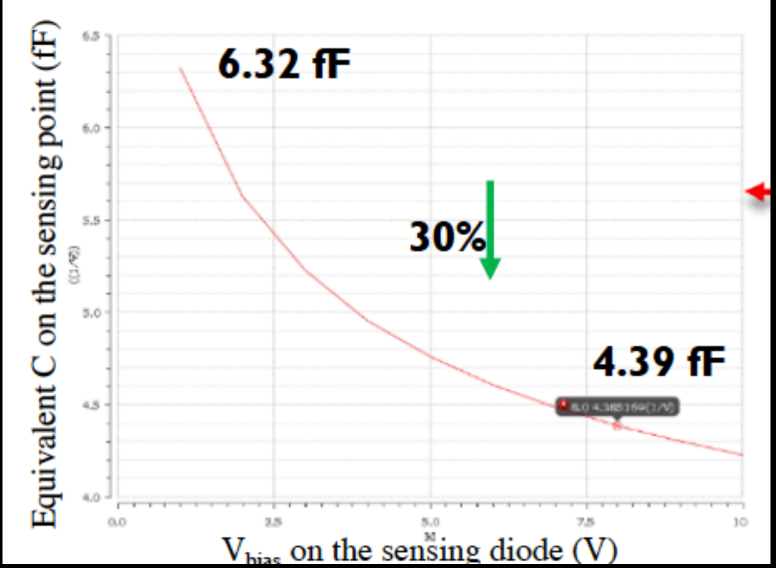
Yang Zhou



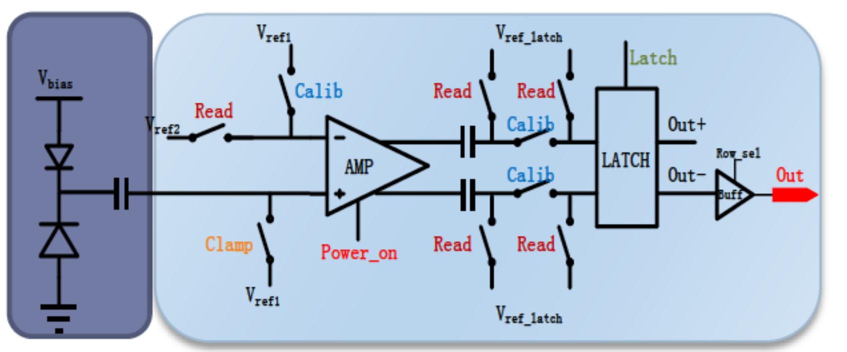
Layout of JadePix2



Layout of a single pixel in JadePix2

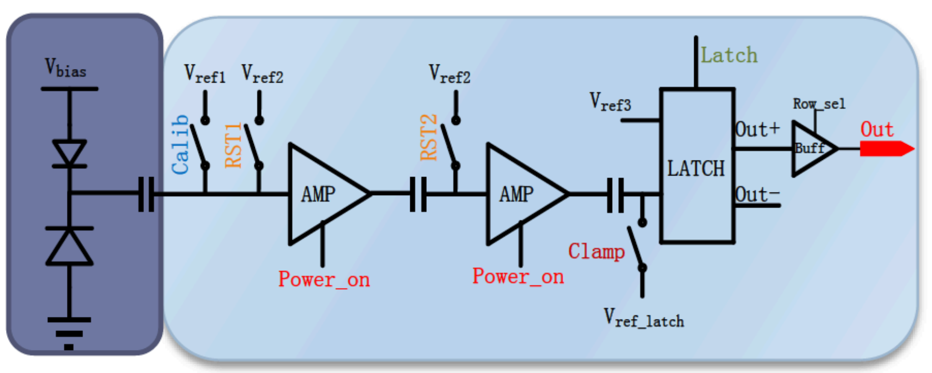


Testing two different amplifiers



Version 1: differential amplifier + latch

Diode 4 μm^2



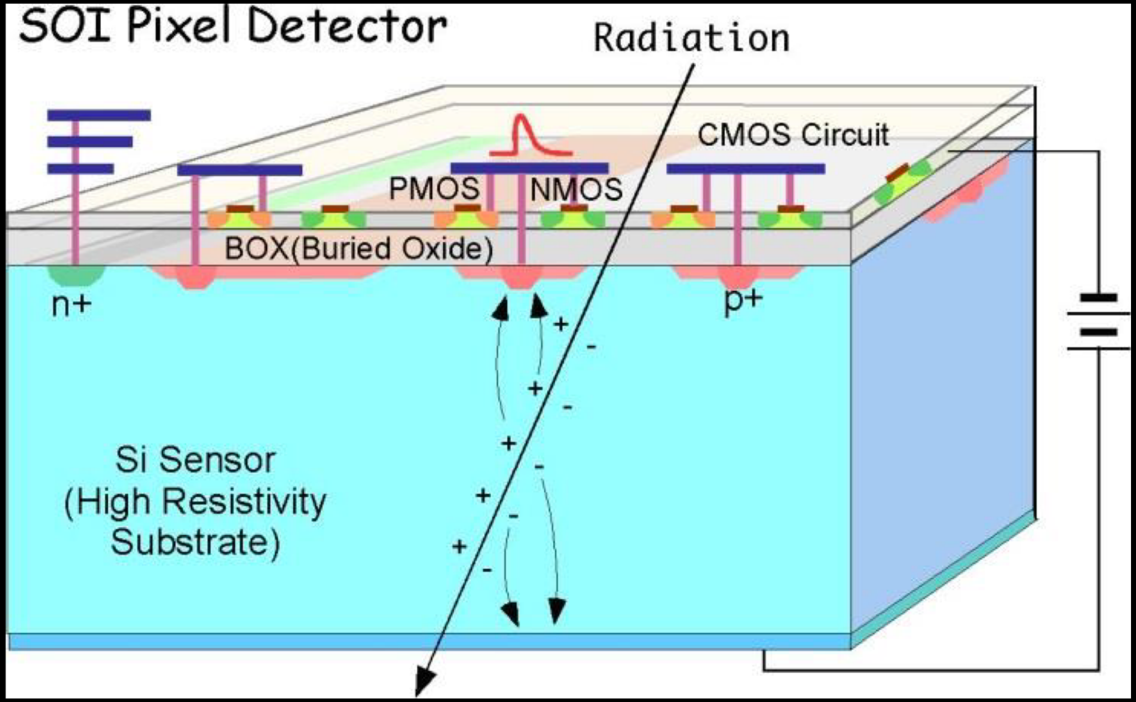
Version 2: two stage CS amplifiers + latch

Testing ongoing

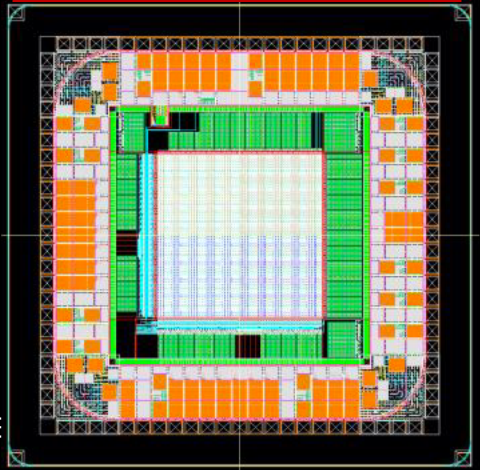
Yang Zhou

SOI

- **SOI: LAPIS 200 nm process**
  - Fully depleted sensor
  - Full in-pixel CMOS
  - 5 Metal layers
  - High resistive substrate(≥1 kΩ•cm)
  - Could be back thinned down to 75 μm
- Thicker sensitive layer: simplify the electronic design
  - 2-3 times signal charges for Minimum Ionizing Particles (MIP) even after the sensor back thinning down to ≈ 50μm
  - More compact layout: shrink the pixel size

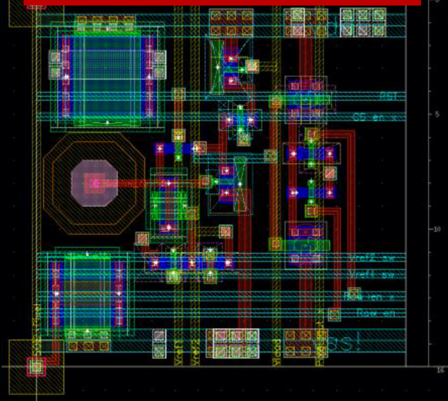


CPV1 3 .3 mm^2

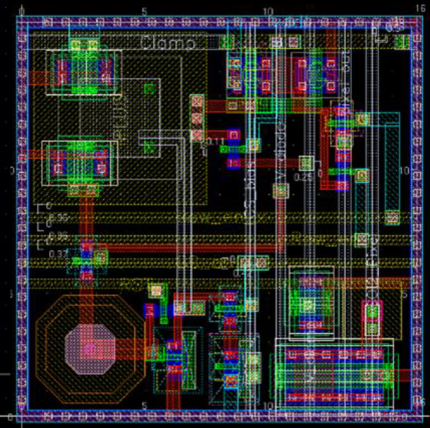


CPV1

16um pitch size



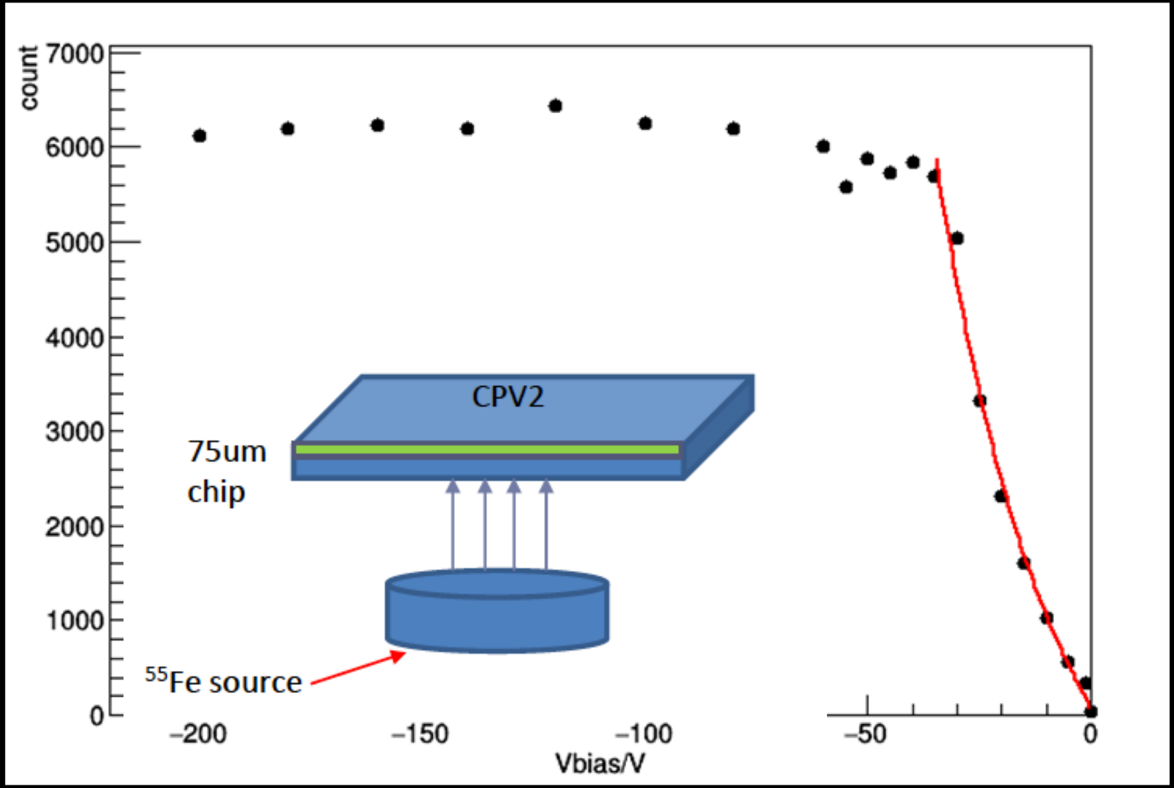
CPV2

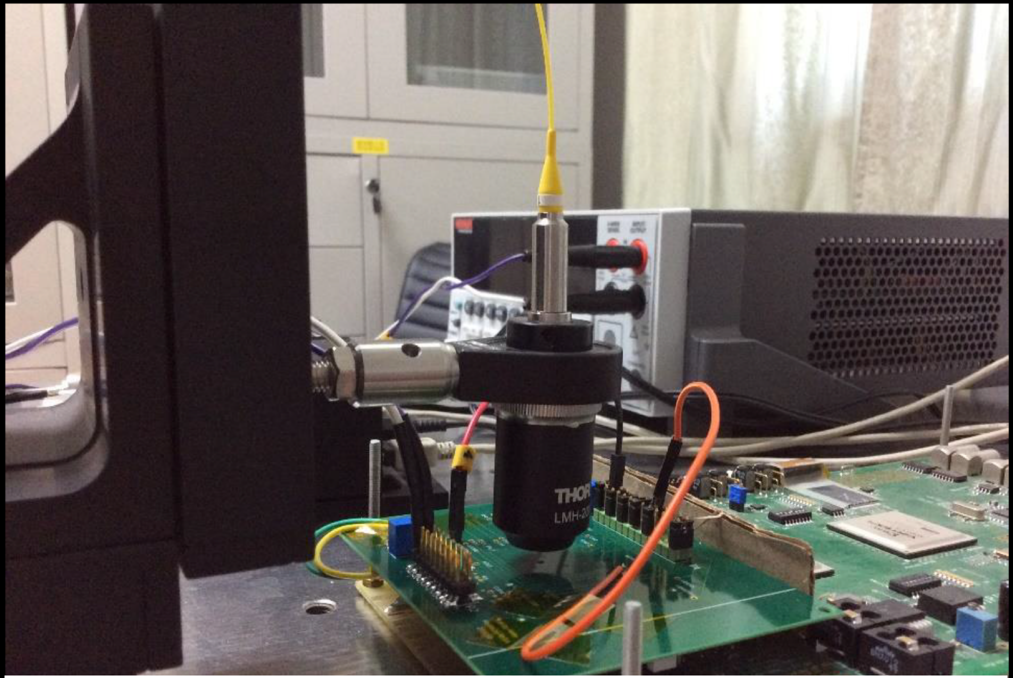


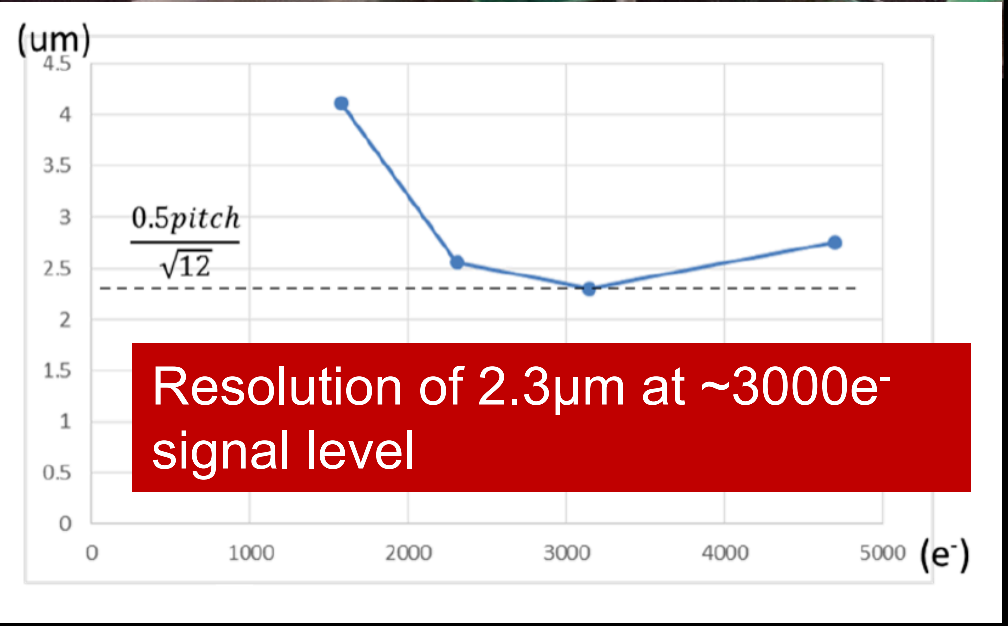
D. I

SOI

- ^{55}Fe signal Efficiency versus bias voltage







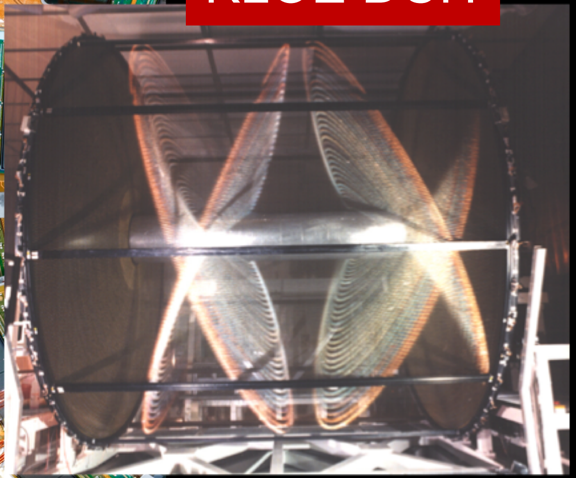
Resolution of 2.3μm at ~3000e$^-$ signal level

IDEA Drift Chamber and Tracking system

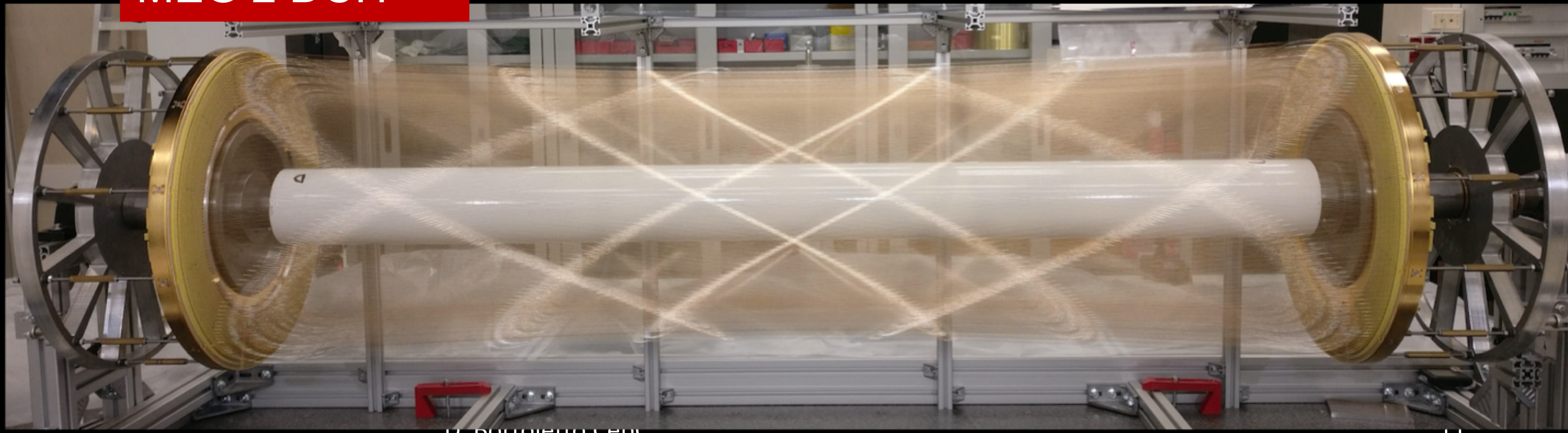
G.F. Tassielli

- IDEA Drift Chamber
  - Novel approach at construction technique of high granularity and high transparency Drift (very low material)
  - Chambers (From KLOE DCH to IDEA DCH)
- IDEA tracking system (DCH+SVX+PSHW)

KLOE DCH

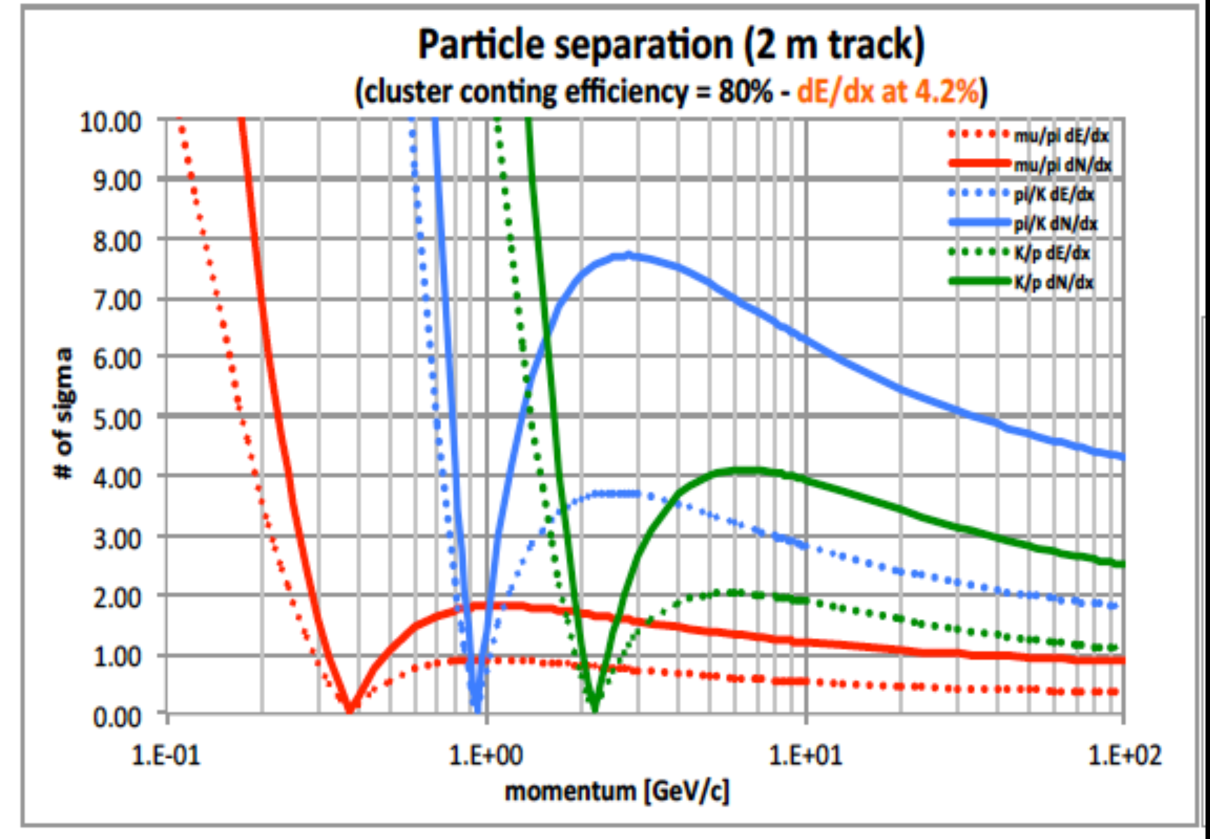


MEG 2 DCH



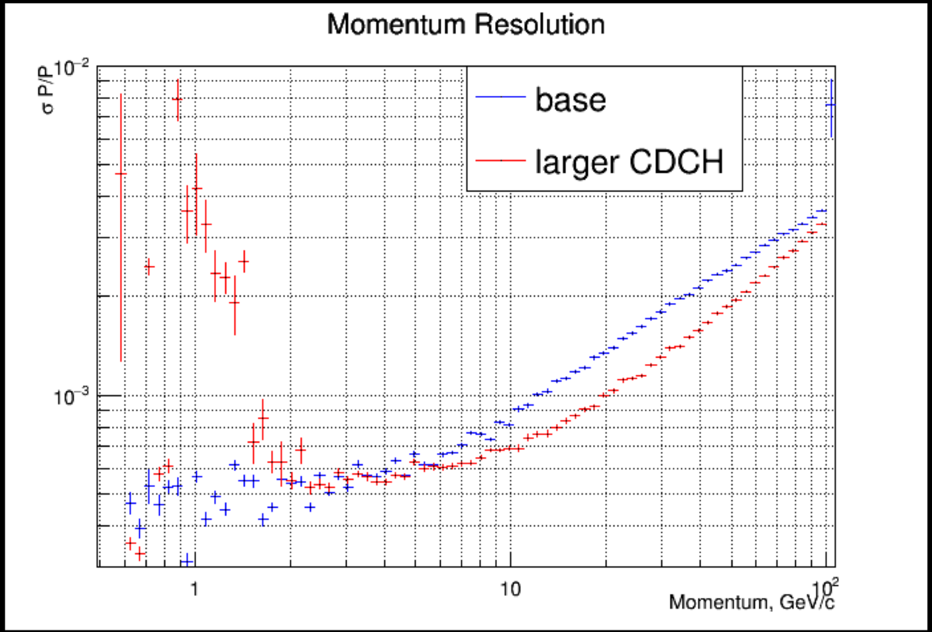
High granularity and high transparency Drift Chambers

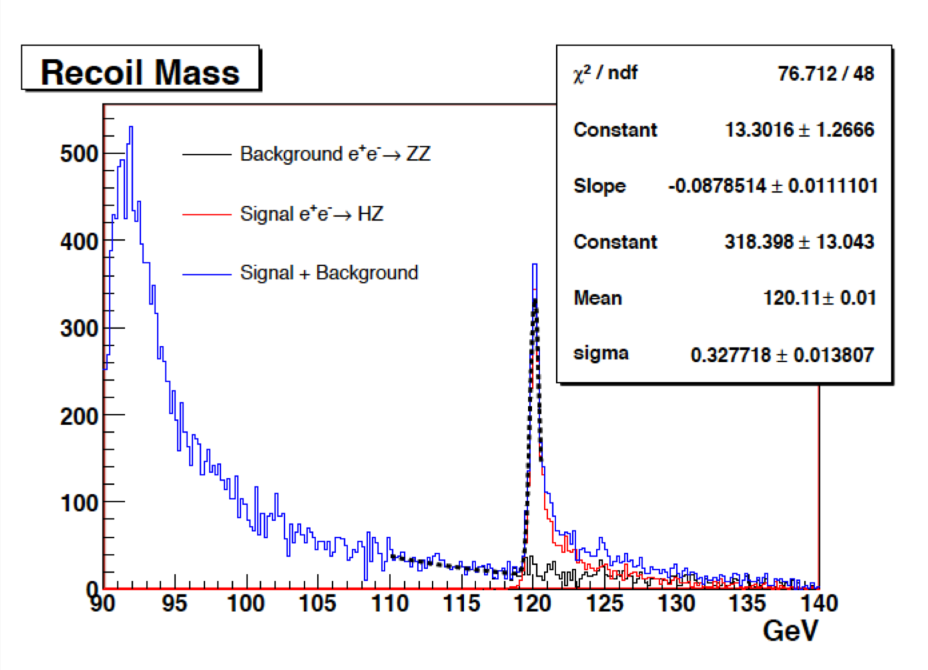
- Material reduction to ≈ 10^{-3} X_0 for the inner cylinder and to a few x 10^{-2} X_0 for the end-plates, including HV supply and signal cables
- Feed-through-less wiring: allows to increase chamber granularity and field/sense wire ratio to reduce multiple scattering and total tension on end plates due to thinner wires
- Cluster timing: allows to reach spatial resolution < 100 μm for 8 mm drift cells in He based gas mixtures
- Cluster counting: allows to reach dN_{cl}/dx resolution < 3% for particle identification (a factor 2 better than dE/dx as measured in a beam test)



IDEA

	Base Line value	Option 1 value	Option 2 value	dim.
R_{in}	345	200*	250	mm
R_{out}	2000	2150	2000	mm
active area length	4000	4000	4000	mm
total length	4500	4500	4500	mm
total cells	56448	34560	52704	n.
layers	112	96	112	n.
Superlayers	14	12	14	n.
Layers per Superlay.	8	8	8	n.
phi sector	12	12	12	n.
smaller cell	11.85	14.2	11.65	mm
larger cell	14.7	22.5	15.25	mm
min. stereo angle	48	25	35	mrad
max. stereo angle	250	240	245	mrad





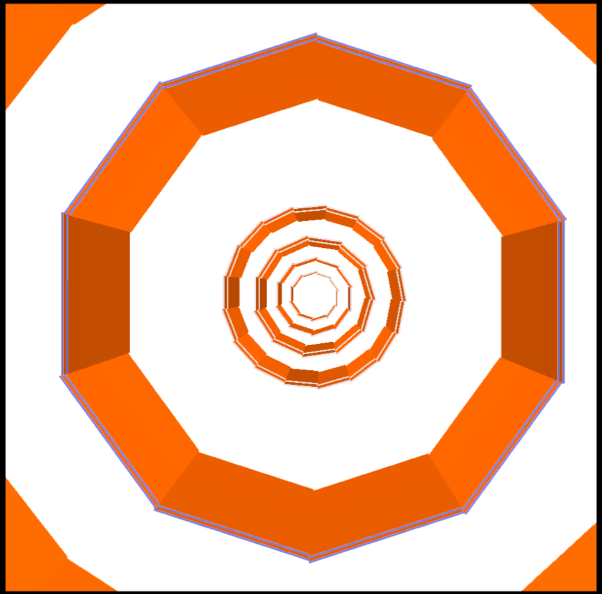
4th-Concept at ILC
ZH → μ+μ− + X

CepC full silicon option

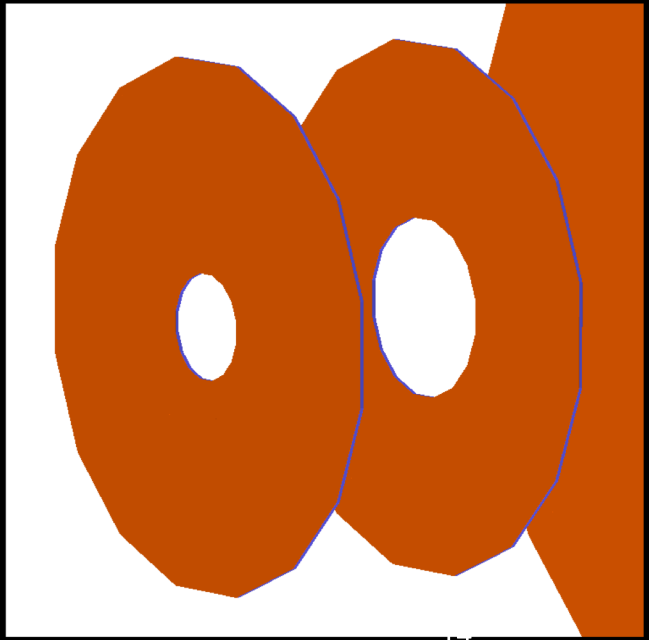
Chengdong Fu

- Two designs for full silicon tracker
- CEPCSID: replacing TPC with extra silicon strip barrel ladders and endcap disks
- SIDB: expanding the SID design to full tracking volume
  http://atlaswww.hep.anl.gov/hepsim/detectorinfo.php?id=sidcc
- B field is assumed to 3.0 T
- The radius of tracking volume is set as 1.87 m, not change the size of calorimeter

- Three options for barrel ladders
  - Detached two layers with overlap
  - Detached two layers without overlap
  - Conjunct layer with two silicon layers

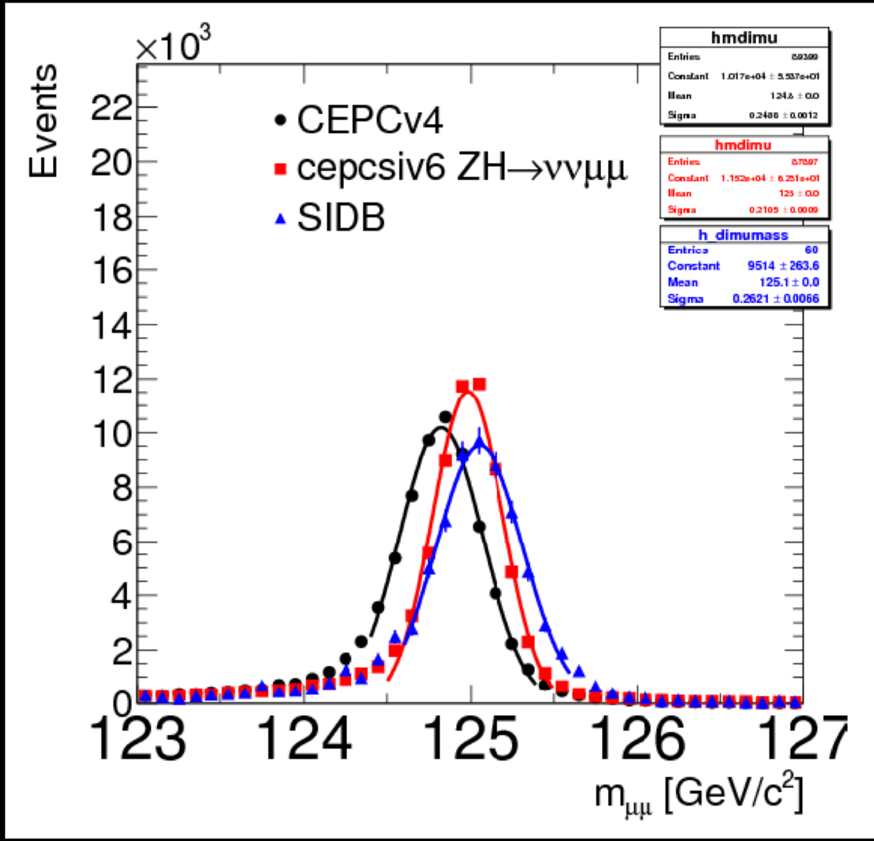


- Two options for endcap petals
  - Detached two layers
  - Conjunct layer with two silicon layers

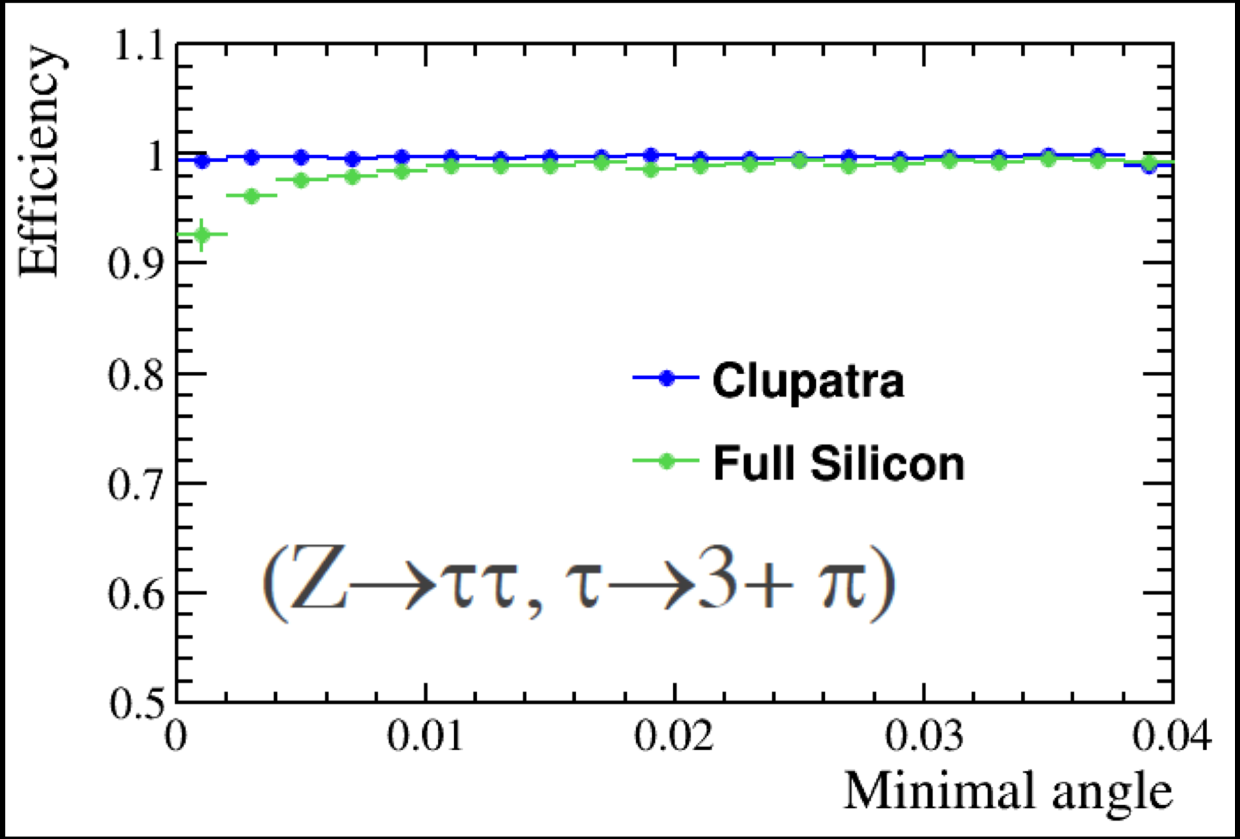


CepC full silicon option

- Many reconstruction tools available
- Tracking and fit
  - SiliconTracking_MarlinTrk
  - Conformal Tracking



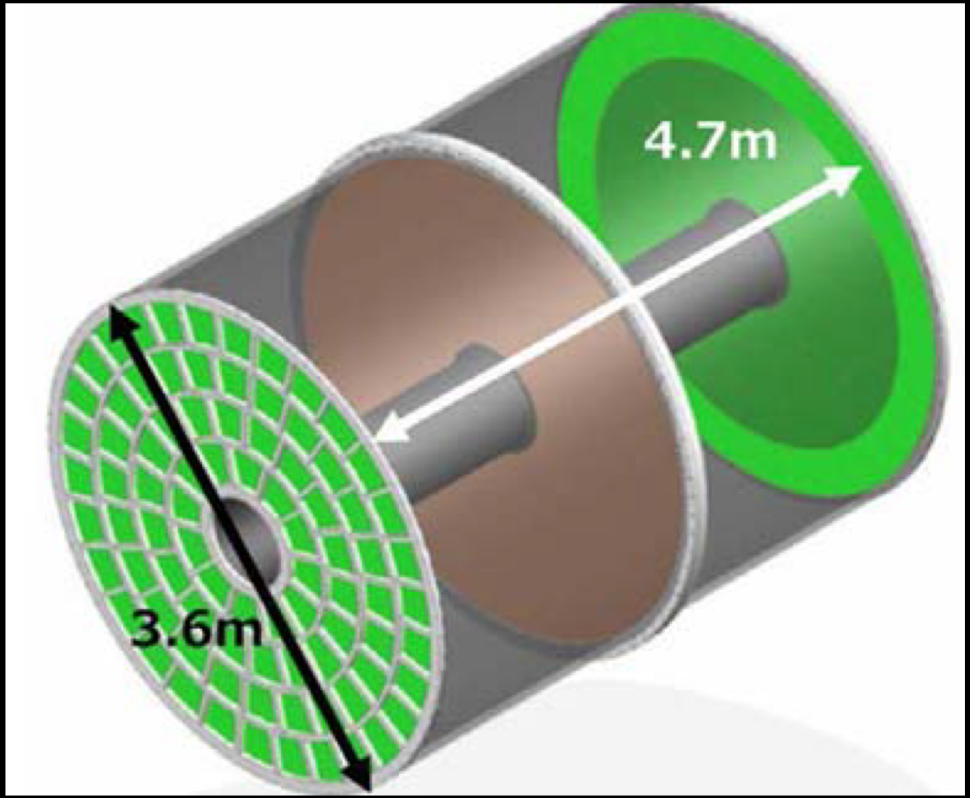
Low efficiency with conformal tracking when two pion are very close



CepC TPC

Huirong Qi

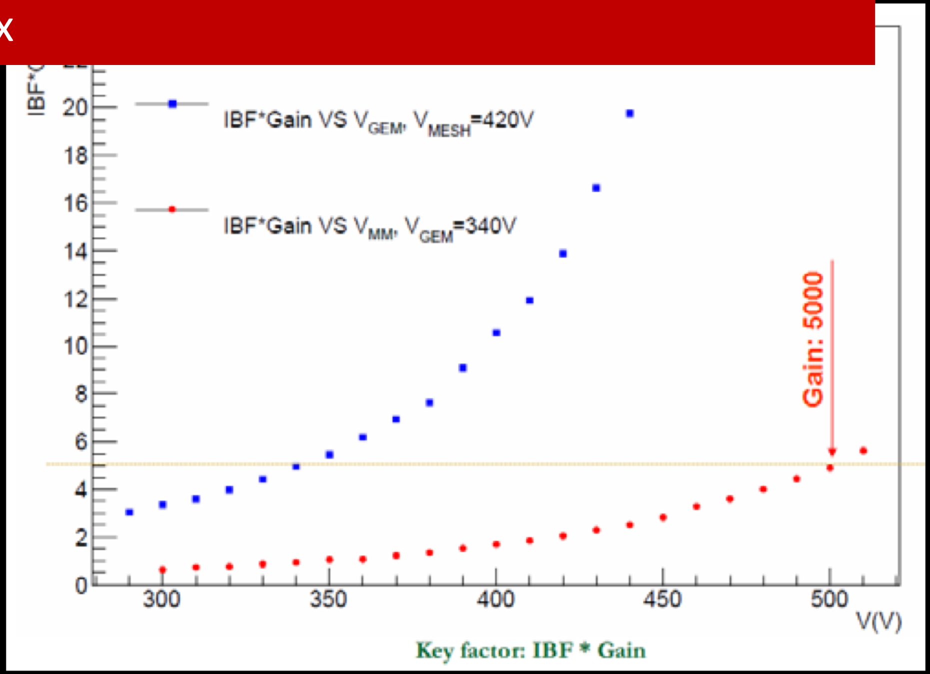
- TPC detector concept:
  - Motivated by the H tagging and Z
  - ~3 Tesla magnetic field
  - ~100 μm position resolution in rφ
  - Large number of 3D points(~220)
  - dE/dx resolution: <5%
  - Tracker efficiency: >97% for p_T>1GeV
  - 2-hit resolution in rφ: ~2mm
  - Momentum resolution: ~10^{-4}/GeV/c



Distortion of the drift field due to secondary ions produced in the amplification region (Ion Back Flow)

CepC TPC

Warning due to ALICE expeirnce that this results could be misleading if measured with x-ray flux



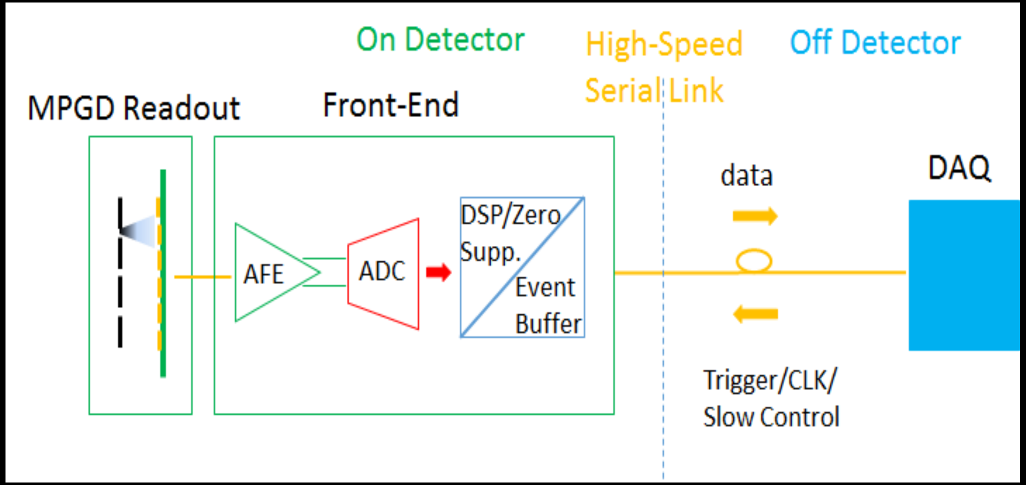
- Continuous IBF module:
  - Gating device may be used for Higgs run
  - Open and close time of gating device for ions: ~ µs-ms
  - No Gating device option for Z-pole run
  - Continuous Ion Back Flow due to the continuous beam structure
  - Low discharge and spark possibility

- Laser calibration system:
  - Laser calibration system for Z-pole run
  - Calibration of the distortion using Nd:YAG laser device@266nm

Liu Wei

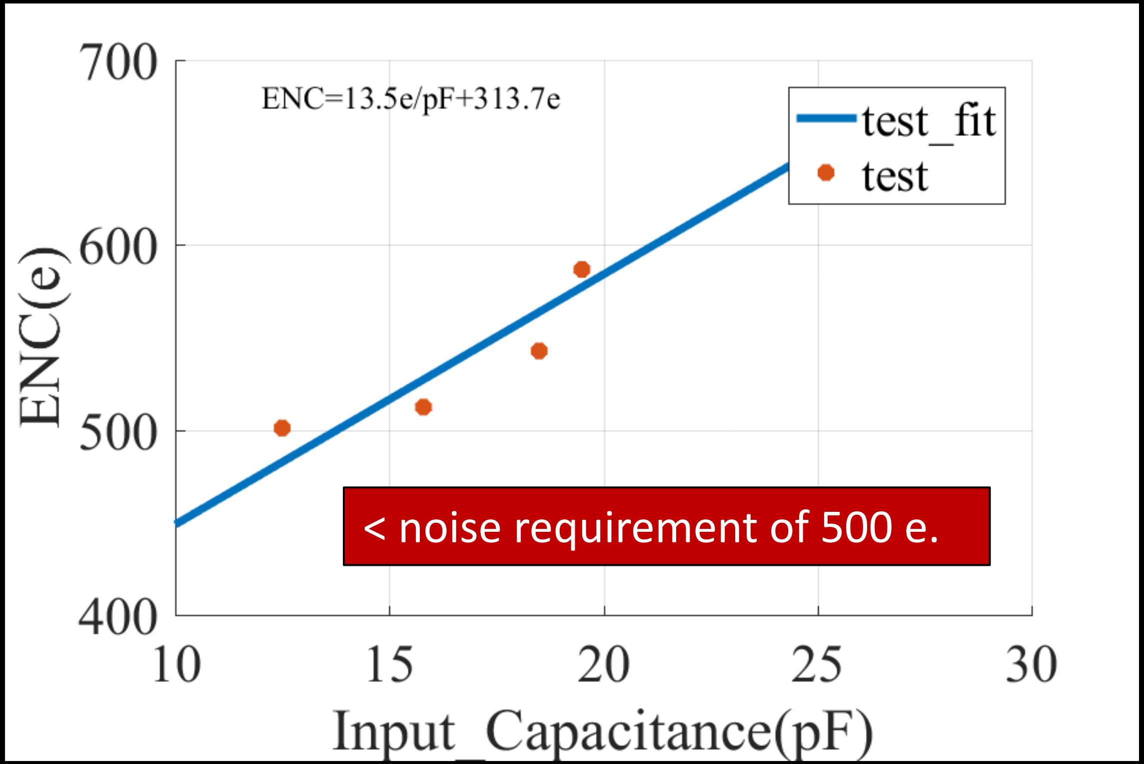
Low Power 65 nm TPC readout

- Low power design is critical for the 1M channel TPC



- Three prototype chips have been designed for the first MPW run
  - Analog Front-end (Charge Sensitive Amplifier + CR-RC shaper) ASIC
  - Lower power SAR-ADC ASIC
  - Analog Front-end +SAR-ADC ASIC

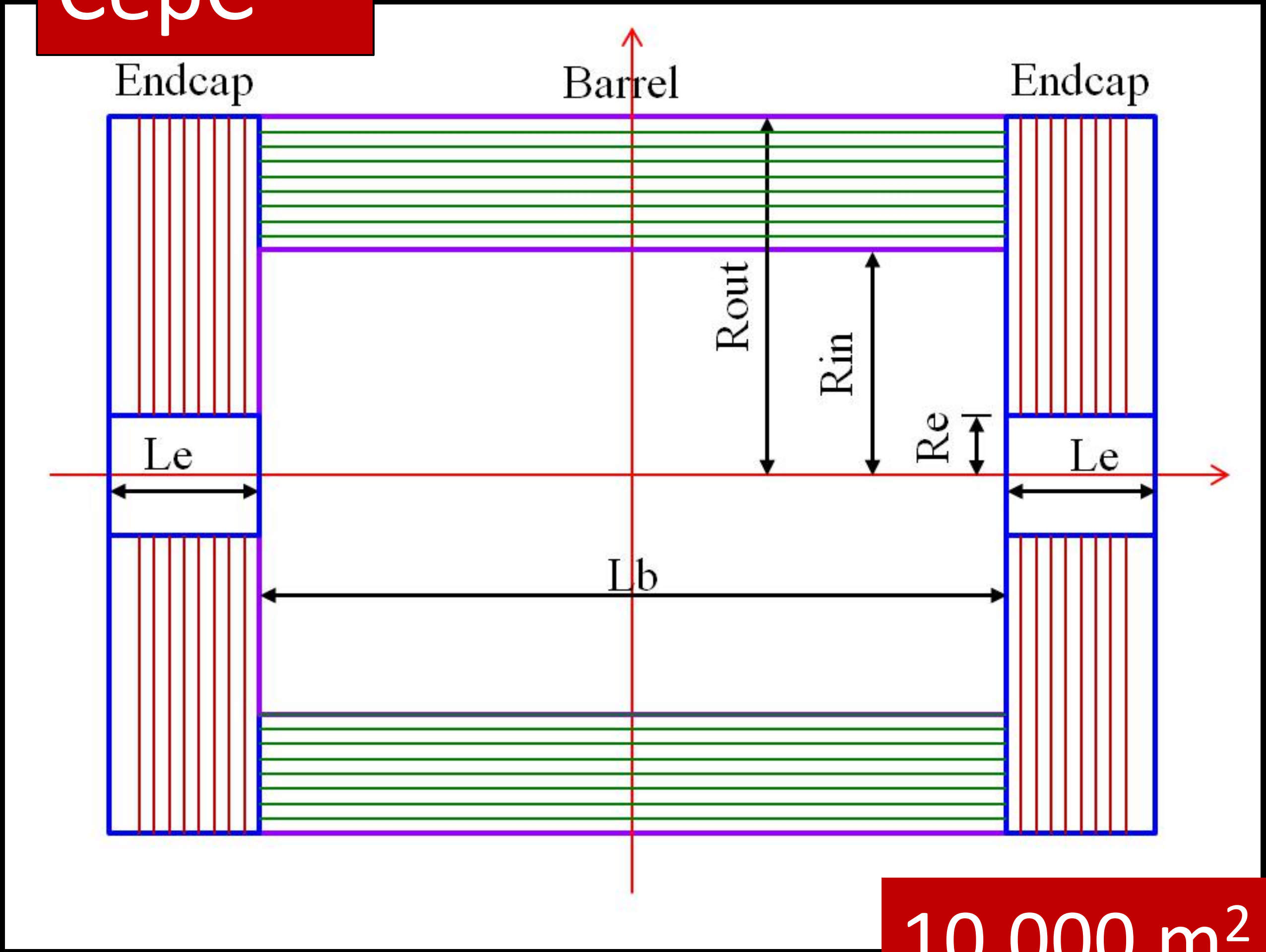
- **The Power consumption : 2.18mW/ch (spec 2.5 mW/ch)**



MUON DETECTORS

Paolo Giacomelli, Marco Poli Lener (, Liang Li (RPC)

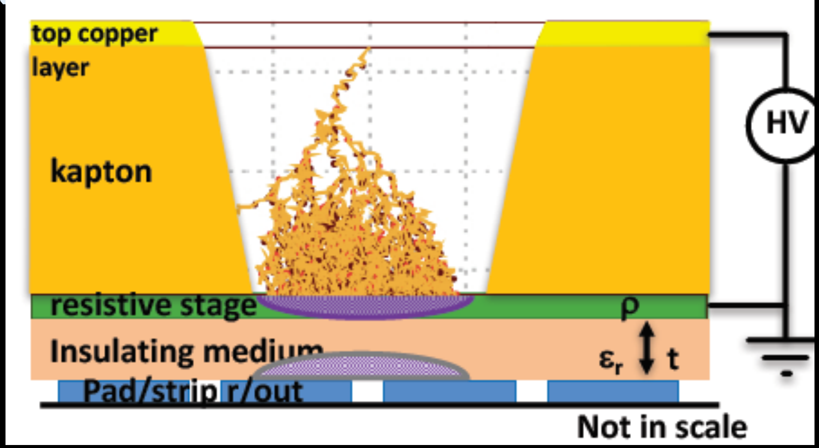
CepC

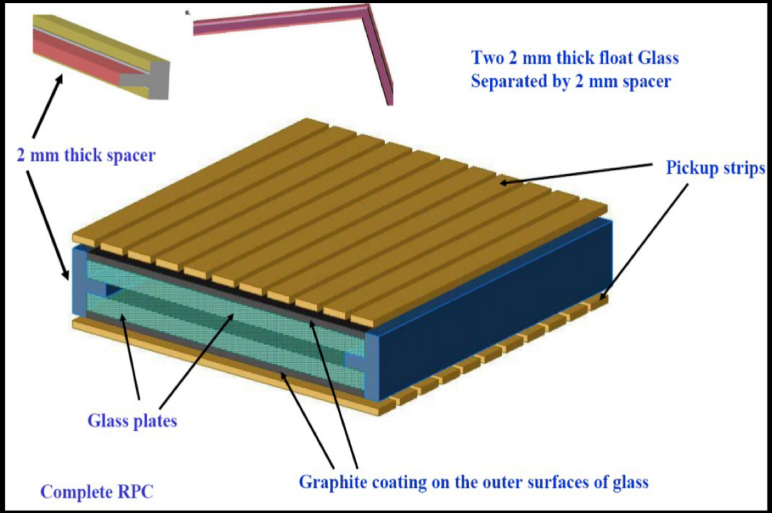


10,000 m^2

- Eight layers of RPC stations.
- Other options:
  - Monitored Drift Tubes
  - Thin Gap Chamber
  - Micromegas
  - GEM

μ-RWELL

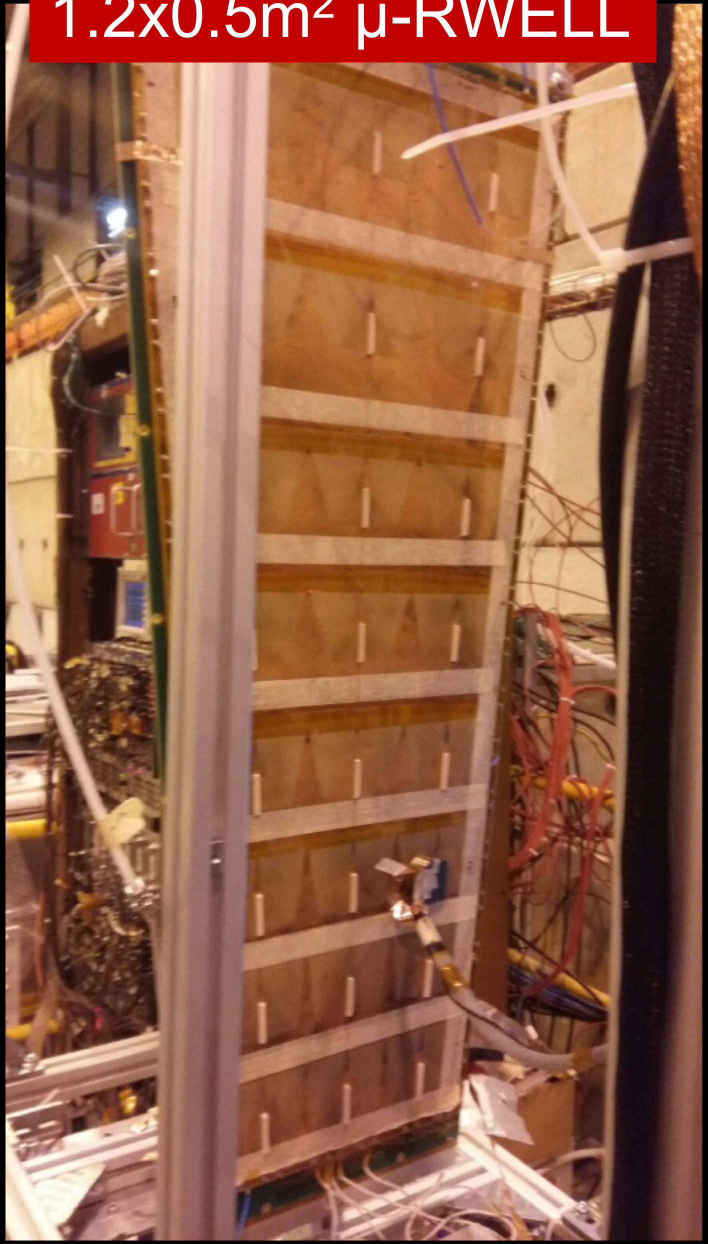




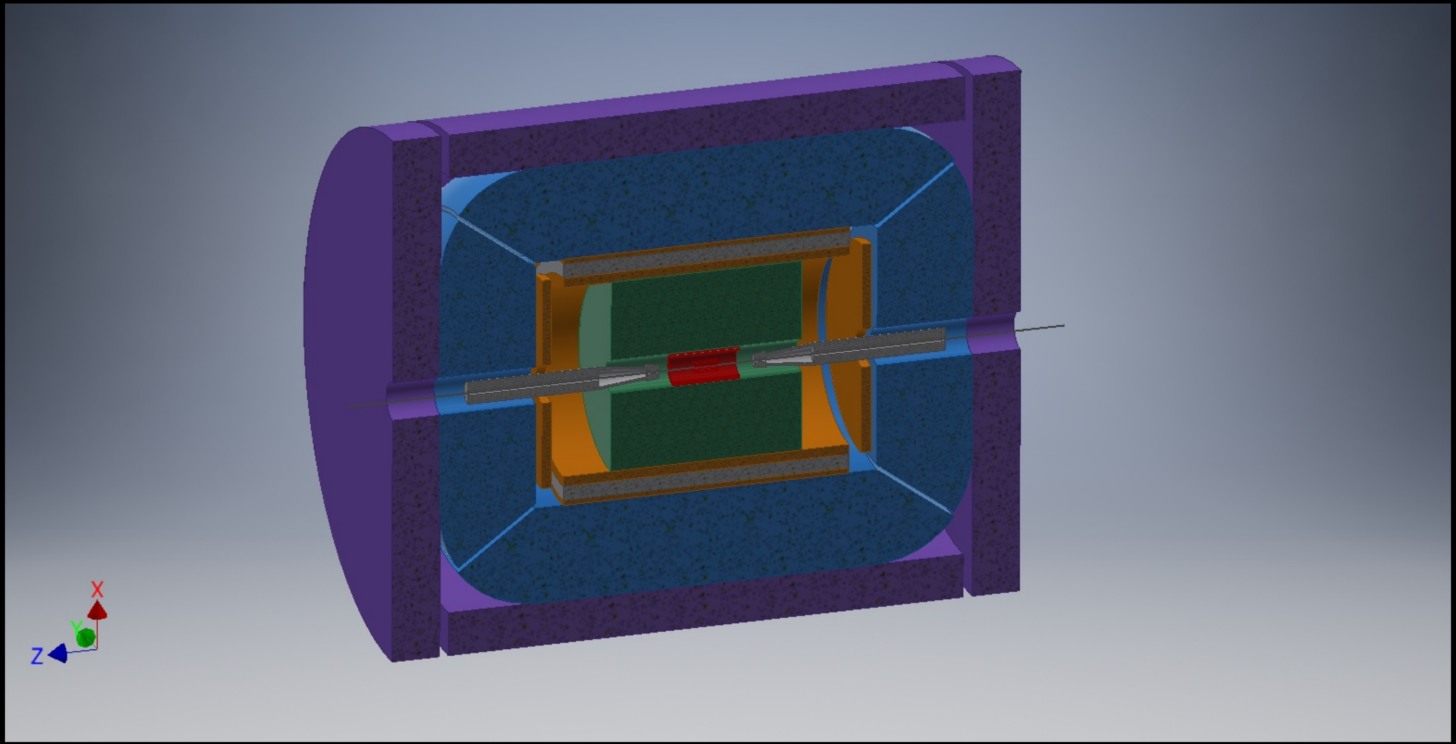
- Low cost, easy construction
- Position resolution: 10-200 μm
- Time resolution: ~ 5-8 ns

Technology transfer ELTOS SpA (http://www.eltos.it)

1.2x0.5m^2 μ-RWELL



MUON DETECTORS - IDEA

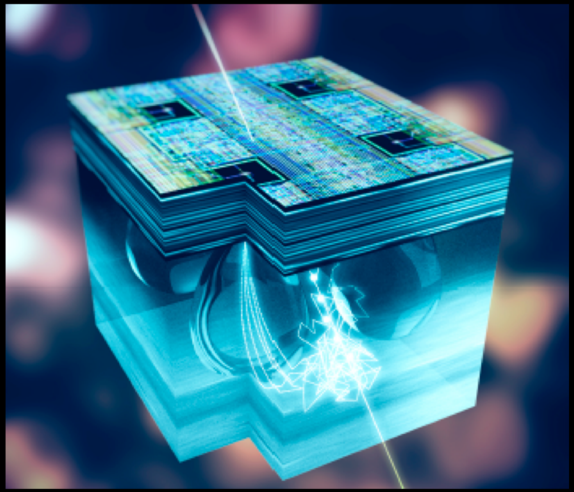


2T B field

CepC and FCC ee

- IDEA detector
- 3-4 MPGD stations interleaved in the iron return yoke.
- The current baseline solution employs μ-RWELL as active detector

ALICE



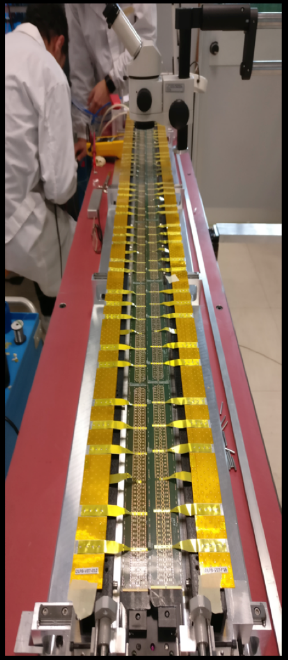
CMOS Monolithic Active Pixel Sensors
in TowerJazz 180 nm technology

Werner Riegler

- Pixel pitch: 29 × 27 μm^2
- Low power consumption ~40 mW/cm^2
- Input capacitance C_{in} = 5 fF
- Input charge Q_{in}(MIP) = 1300 e ⟶ V = 40 mV
- Spatial resolution 5 μm, Event time resolution < 1 μs
- Radiation hardness: expected in Run 3 and 4 < 300 krad (< 2.0×10^{12} 1 MeV n_{eq}/cm^2)

- 7 layers (inner/middle/outer): 3/2/2 from R = 22 mm to R = 400 mm
- Ultra-lightweight support structure and cooling (0.30 % X_0 for innermost layers)
- Possible to remove and re-install the detector for maintenance during the yearly shutdowns

Outer barrel staves

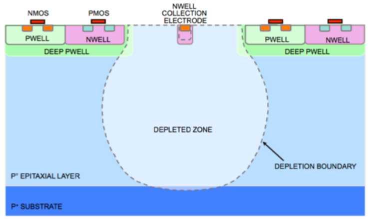


Novel CMOS Pixel Sensors for the ALICE Upgrade

In the framework of the R&D for the ALICE upgrade, CERN has developed in collaboration with Tower Semiconductor a process modification that allows full depletion of the high resistivity silicon layer

- Reduces charge collection time (<1ns)
- Enhances radiation hardness (~10^{15} n / cm^2)

The process modification requires a single additional process mask with no changes on the sensor and circuit layout



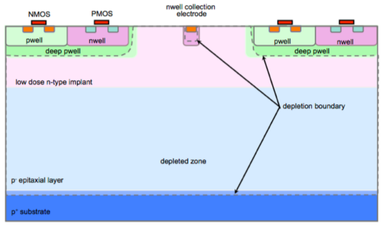
Vertical full depletion

Lateral partial depletion

Collection time < 30ns (V_{bb}=-3V)

Suitable for up to 10^{14} n/cm^2

Foundry Standard Process



Epi-layer fully depleted

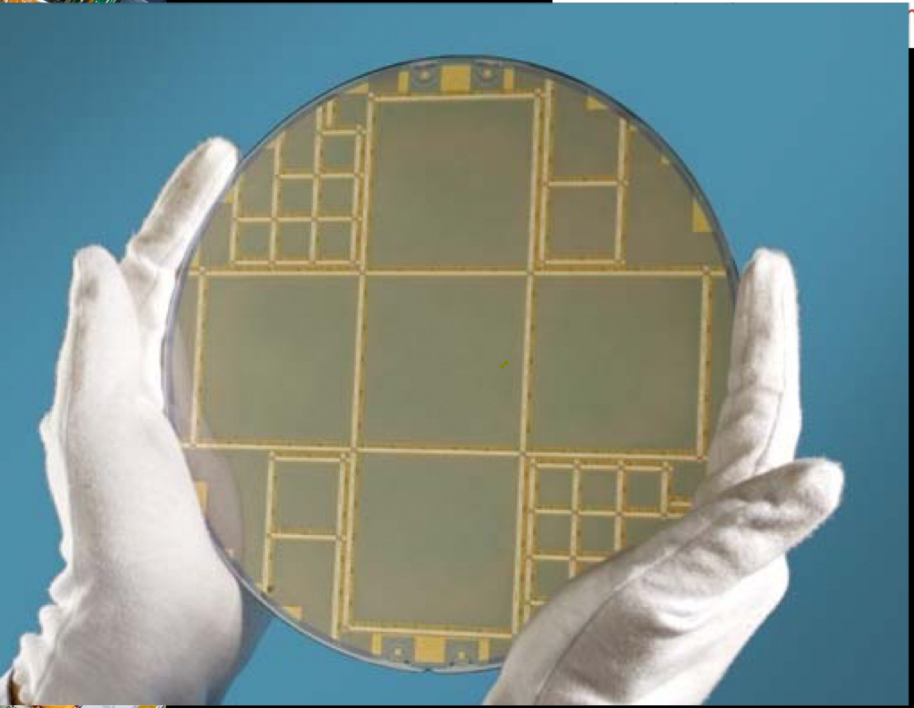
Collection time < 1ns

Operational for up to 10^{15} n/cm^2

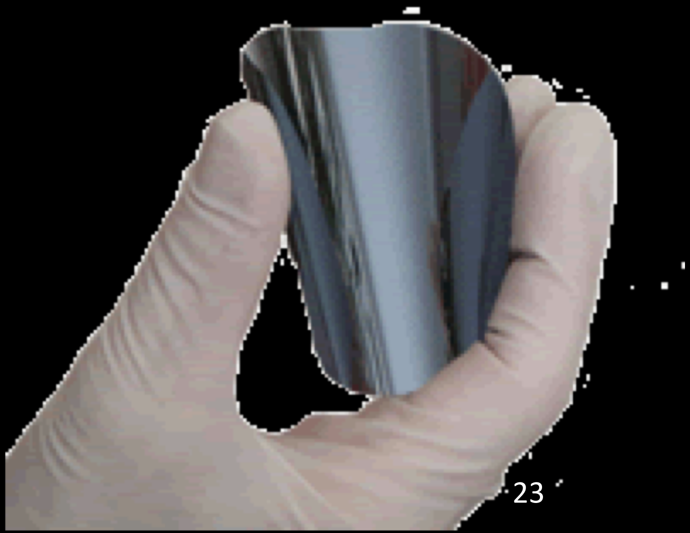
Modified process CERN/Tower

The ALICE test vehicle chip (investigator) and prototype ALPIDE chips exist with both flavors

modification and experimental results see: NIM, A 871C (2017) pp. 90-96



Exploit flexibility of ultra thin silicon

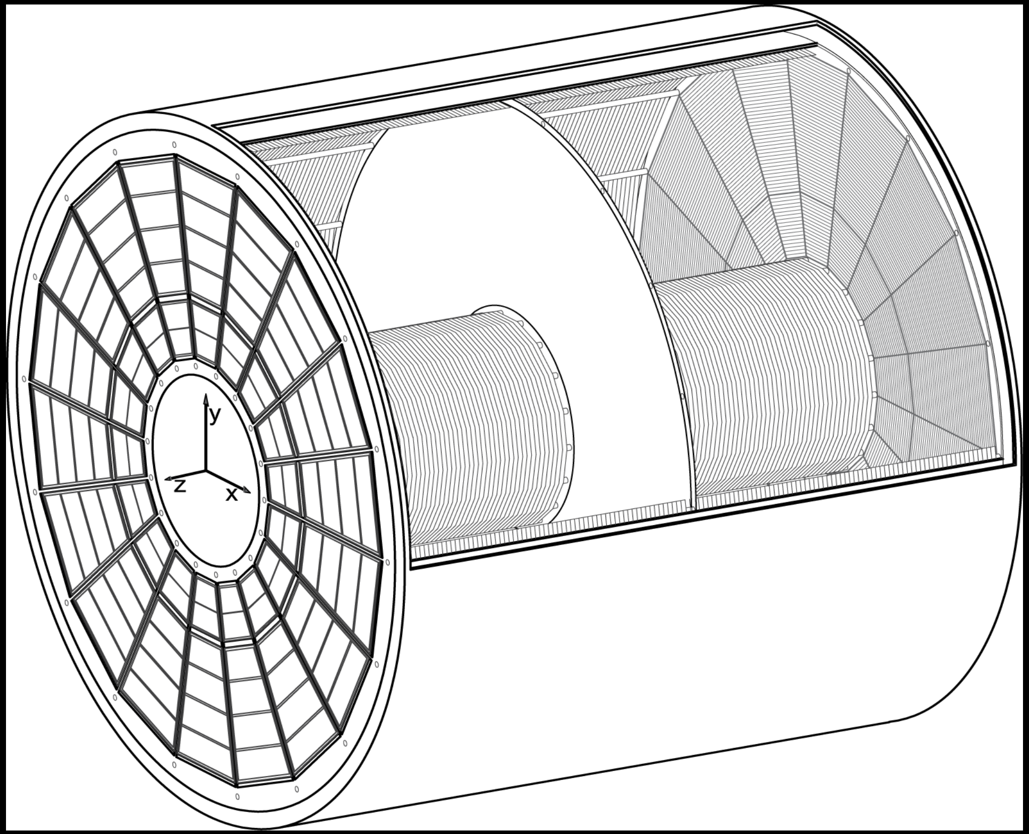


- Stitching to build larger sensors (RAL)
- Migration to 65 nm

ALICE TPC

- Diameter: 5 m, length: 5 m
- Gas: Ne-CO_2-N_2, Ar-CO_2
- Max. drift time: ~100 µs
- 18 sectors on each side
- Inner and outer read out chambers: IROC, OROC

- Current detector (Run 1, Run 2):
  - 72 MWPCs
  - ~550 000 readout pads
  - Wire gating grid (GG) to minimize Ion Back-Flow (IBF)
  - Rate limitation: few kHz



ALICE TPC Upgrade

Production of 40 IROCs and 40 OROCs until September 2018

TPC Upgrade requirements:

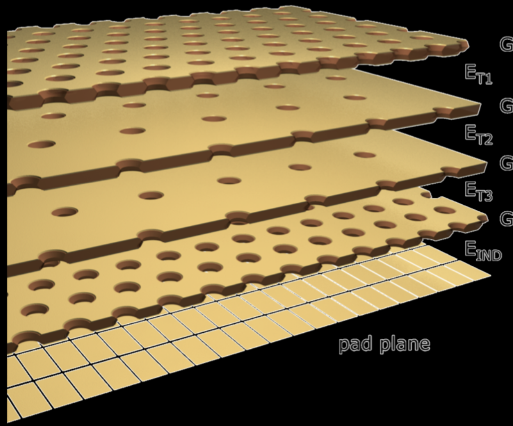
- Nominal gain = 2000 in Ne-CO_2-N_2 (90-10-5)
- IBF < 1% (ε = 20)
- Energy resolution: σ_E/E < 12% for ^{55}Fe
- Stable operation under LHC Run 3 conditions
- Unprecedented challenges in terms of loads and performance

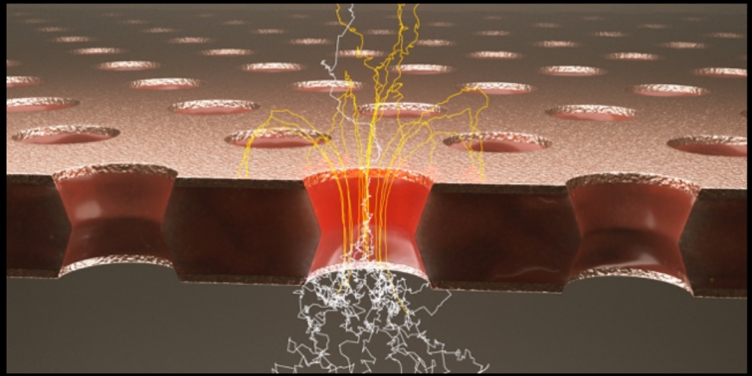
Solution: 4-GEM stack

Combination of standard (S) and large pitch (LP) GEM foils

Highly optimized HV configuration

Result of intensive R&D

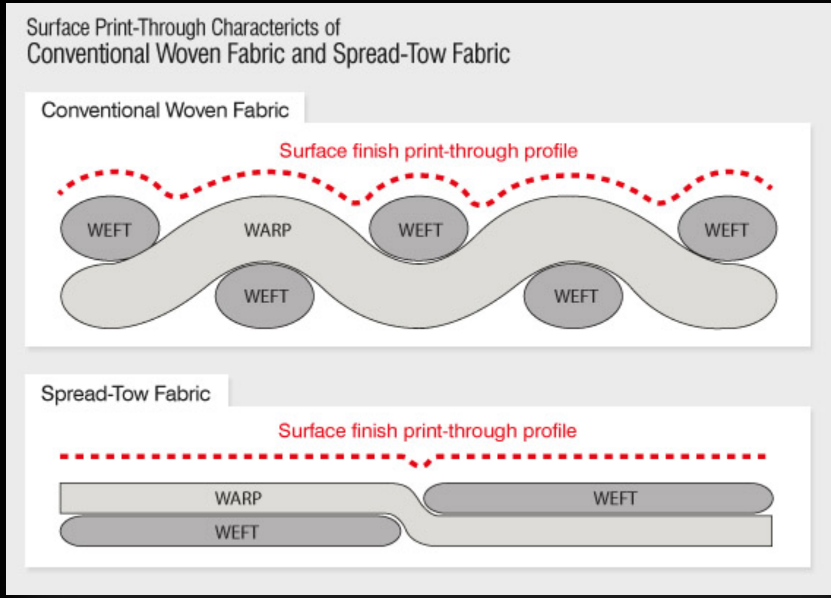


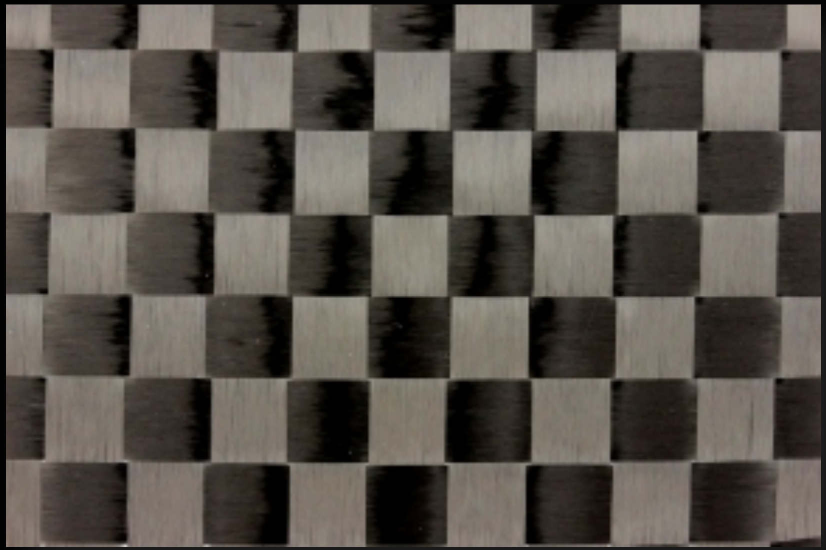


Development of CFRP Structures

Tim Jones

- Most low-mass support structures in PP experiments are made from CFRP.
  - High modulus carbon fibres embedded in a resin matrix
  - Cured under heat (120°C) and pressure (1-7 bar)
  - Laminate built up from several laminae at different angles
- Primary issue
  - CFRP laminates cured at elevated temperature need to be balanced to avoid distortions
    - Balanced: [0], [0/0], [0/90/0], [0/90/90/0], etc…
    - Increased thickness over mono-layer (eg. Kapton
- In Spread-tow pre-preg, the fibre bundles are spread out into strips (typically >15mm wide)
  - Lower areal weight and higher fibre fraction
  - Lower mass for equivalent stiffness
- Developed techniques to manufacture custom spread-tow woven pre-preg with weave ~ 5mm for vertex detector support

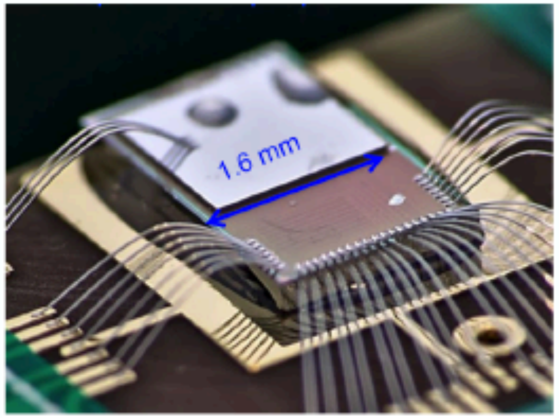


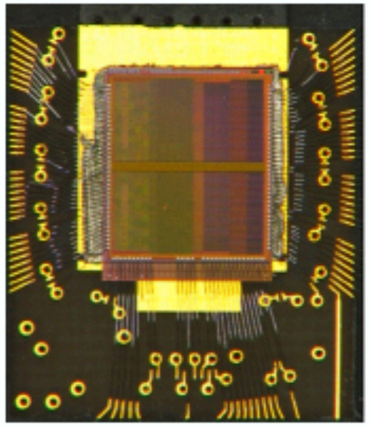


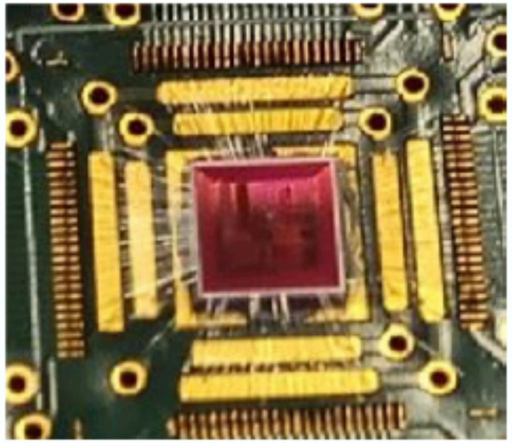
Technology R&D for CLIC & FCC-ee

Emilia Leogrande

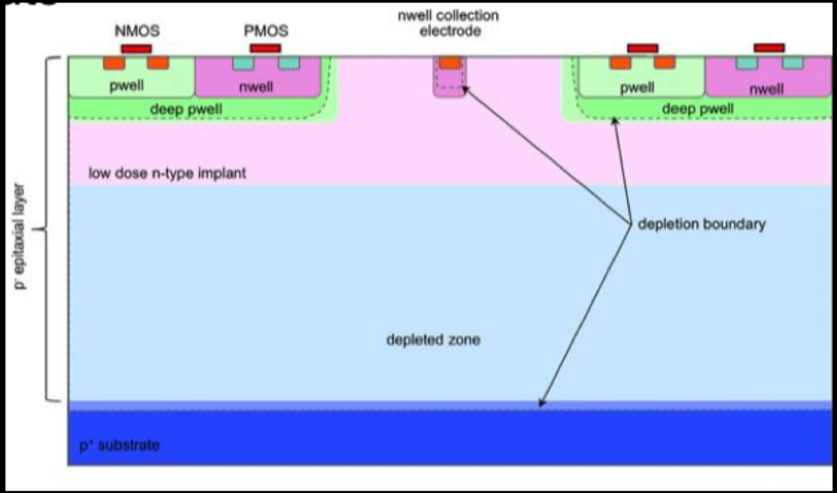
Sensor + readout technology	Currently considered for
Bump-bonded Hybrid planar sensors	Vertex
Capacitively coupled HV-CMOS sensors	Vertex
Monolithic HV-CMOS sensors	Tracker
Monolithic HR-CMOS sensor	Tracker
Monolithic SOI sensors	Vertex, Tracker

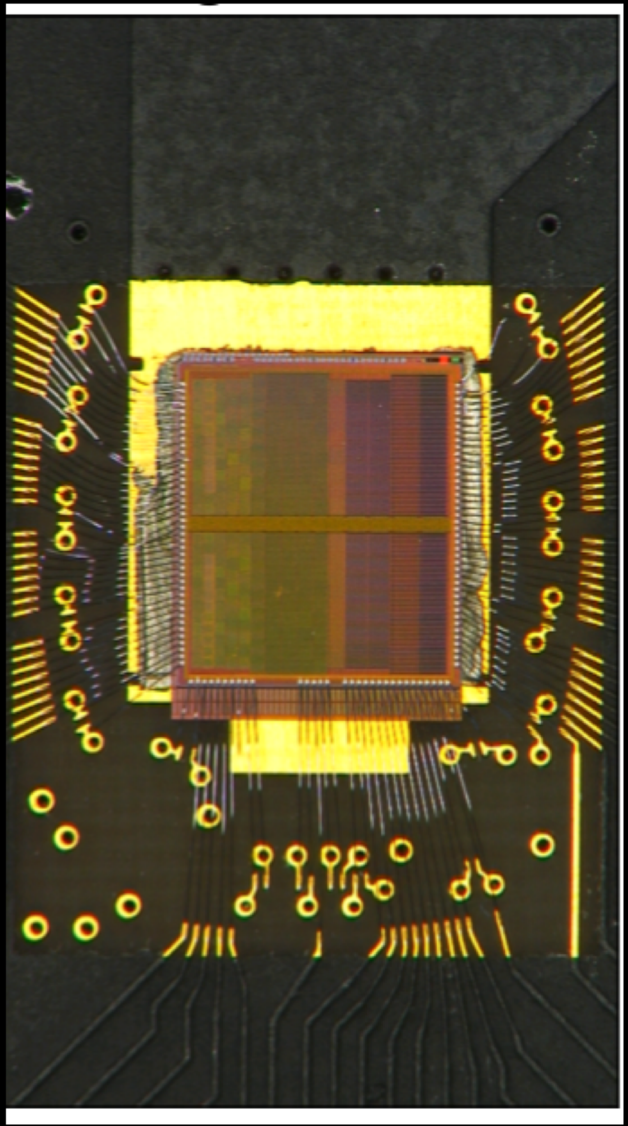






Integrated HR-CMOS sensors



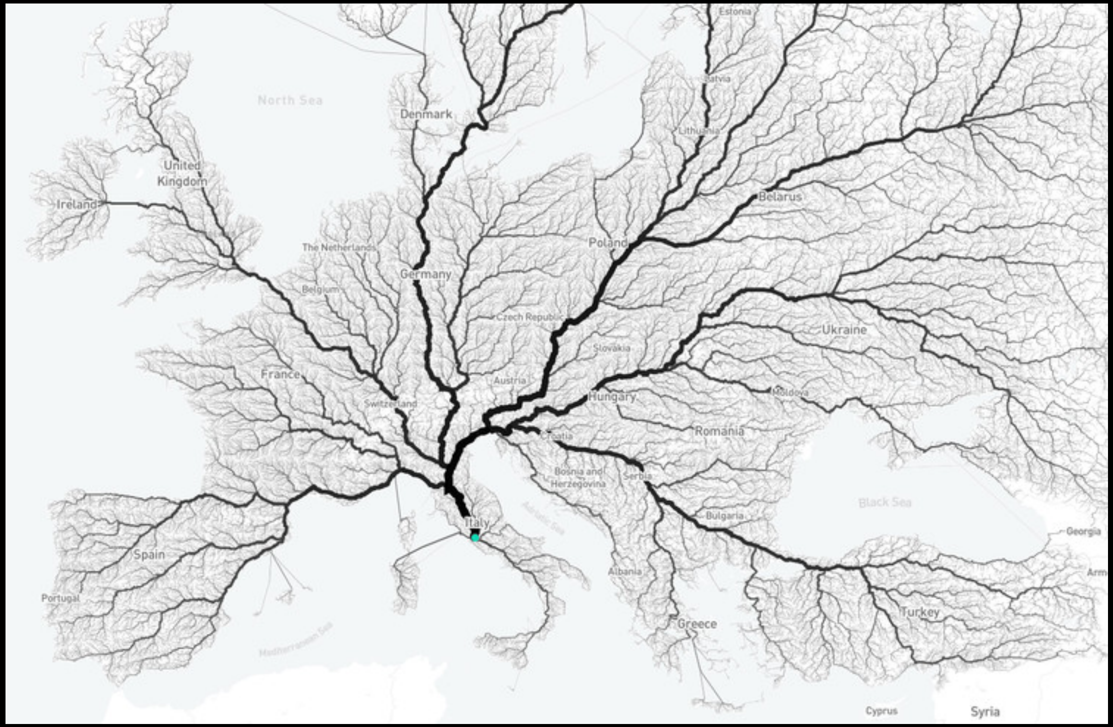


- Integrated CMOS sensor on High-Resistivity substrate
- Tests with INVESTIGATOR analog prototype chip in TowerJazz 180 nm
- HR-CMOS process (ALICE development): 20x20 - 50x50 μm2 pitch for 28x28 μm2, with external readout:
- ~99.3% efficiency, <5 ns timing, σSP ~ 4 μm
- Ongoing work to design fully integrated CLICTD chip: 30x300 μm^2 pitch, be thinned to 50-100 μm
- Plan to use smaller feature size processes in the future

UNIVERSITY OF OXFORD

Conclusions

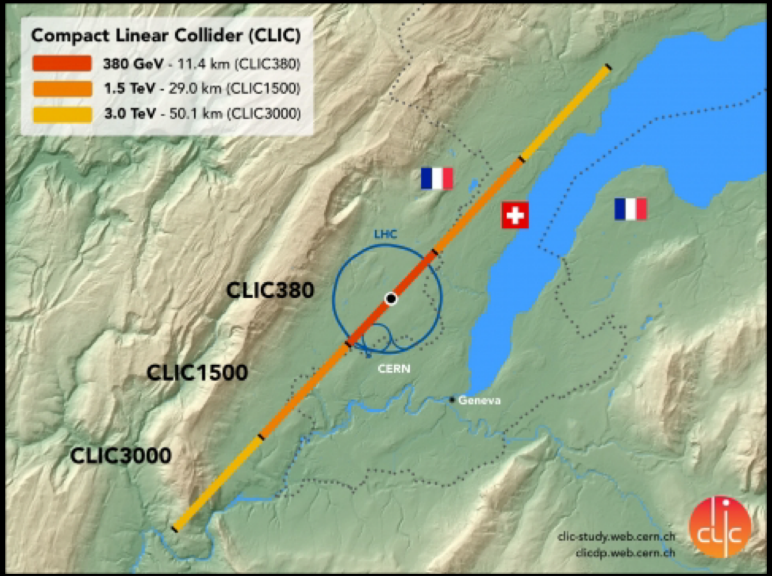
- All road lead to Rome

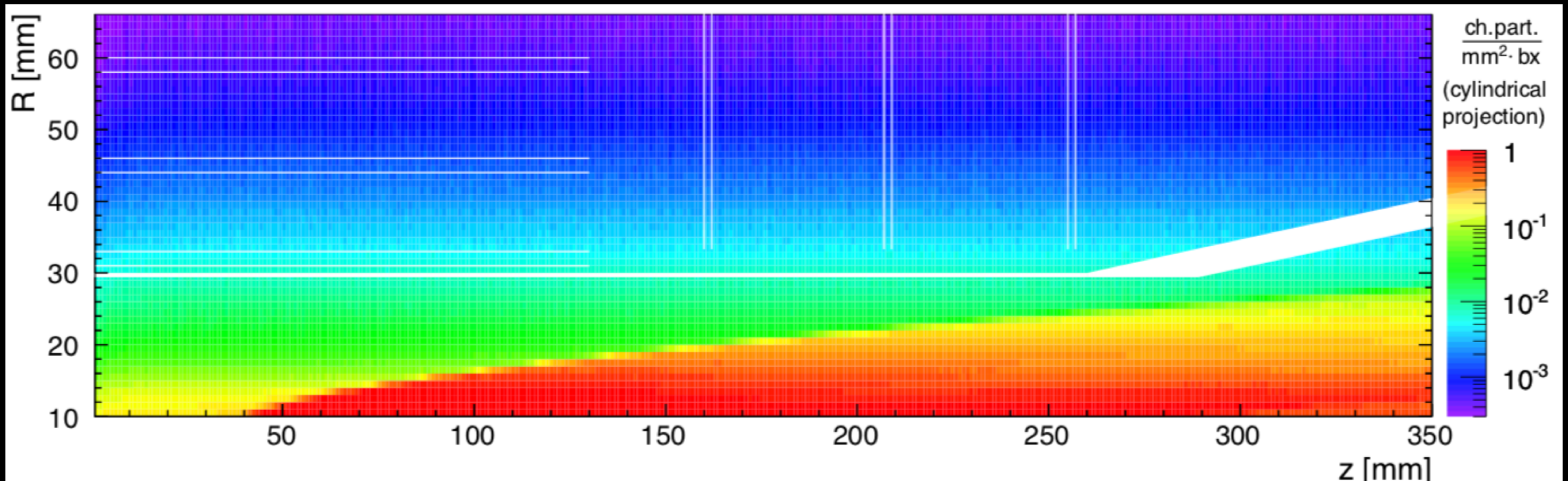


Detector R&D for CepC can benefit from experience gained in the ILC/CLIC/FCC-ee R&D/studies and current experiments/ongoing upgrades (ALICE, LHCb, ATLAS….)

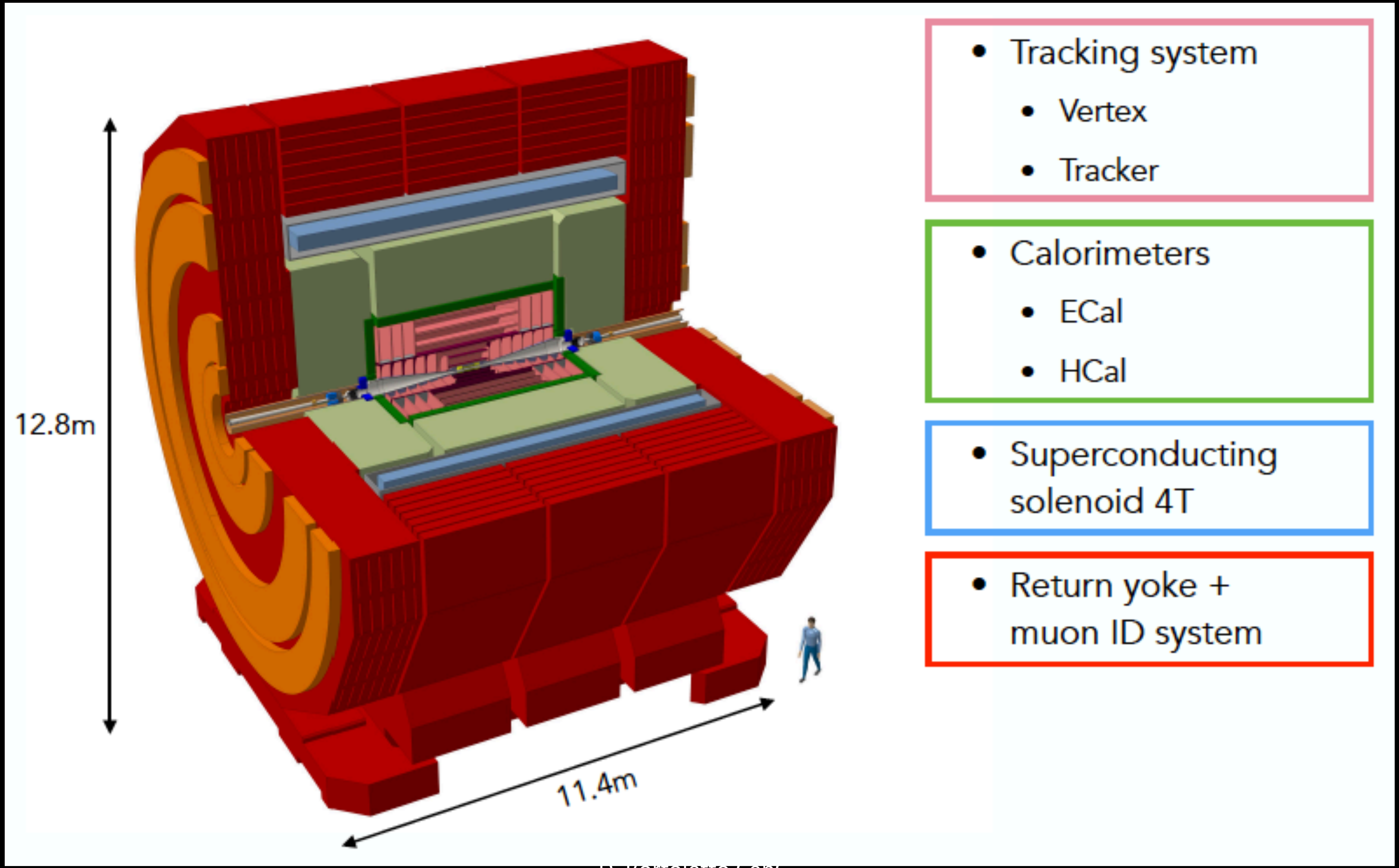
CLICDdet

- Built in stages: 380 GeV, 1.5 TeV, 3 TeV
- Beam structure
  - record data during collision time,
  - *triggerless* readout between bunch trains
  - power pulsing: detector “switched off”
  - between bunch trains
  - crossing angle (20mrad @3TeV) in crab crossing schem





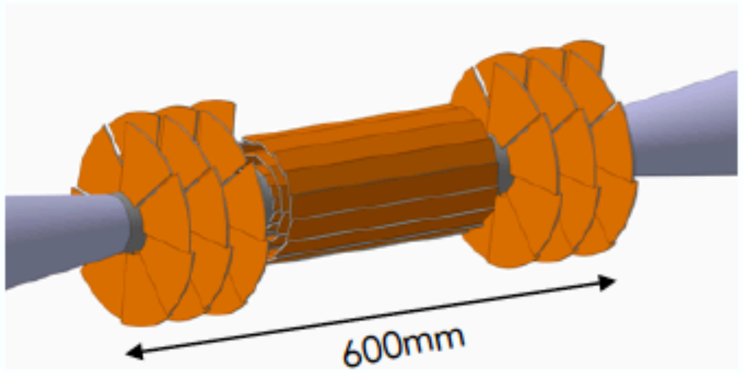
CLICdet



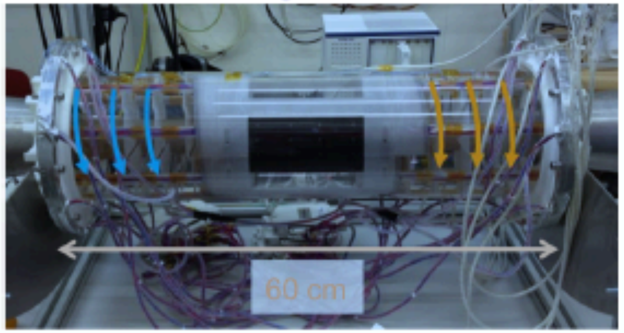
12.8m
11.4m
• Tracking system
• Vertex
• Tracker
• Calorimeters
• ECal
• HCal
• Superconducting solenoid 4T
• Return yoke + muon ID system

The vertex detector

- 3 double layers in the barrel
  - radius from 31** to 58 mm
    **limited by occupancy from pairs
- 3 double-layered forward disks
  - shaped in spirals to allow for air cooling (power-pulsed detector)
  - 50 mW/cm² achievable with power pulsing



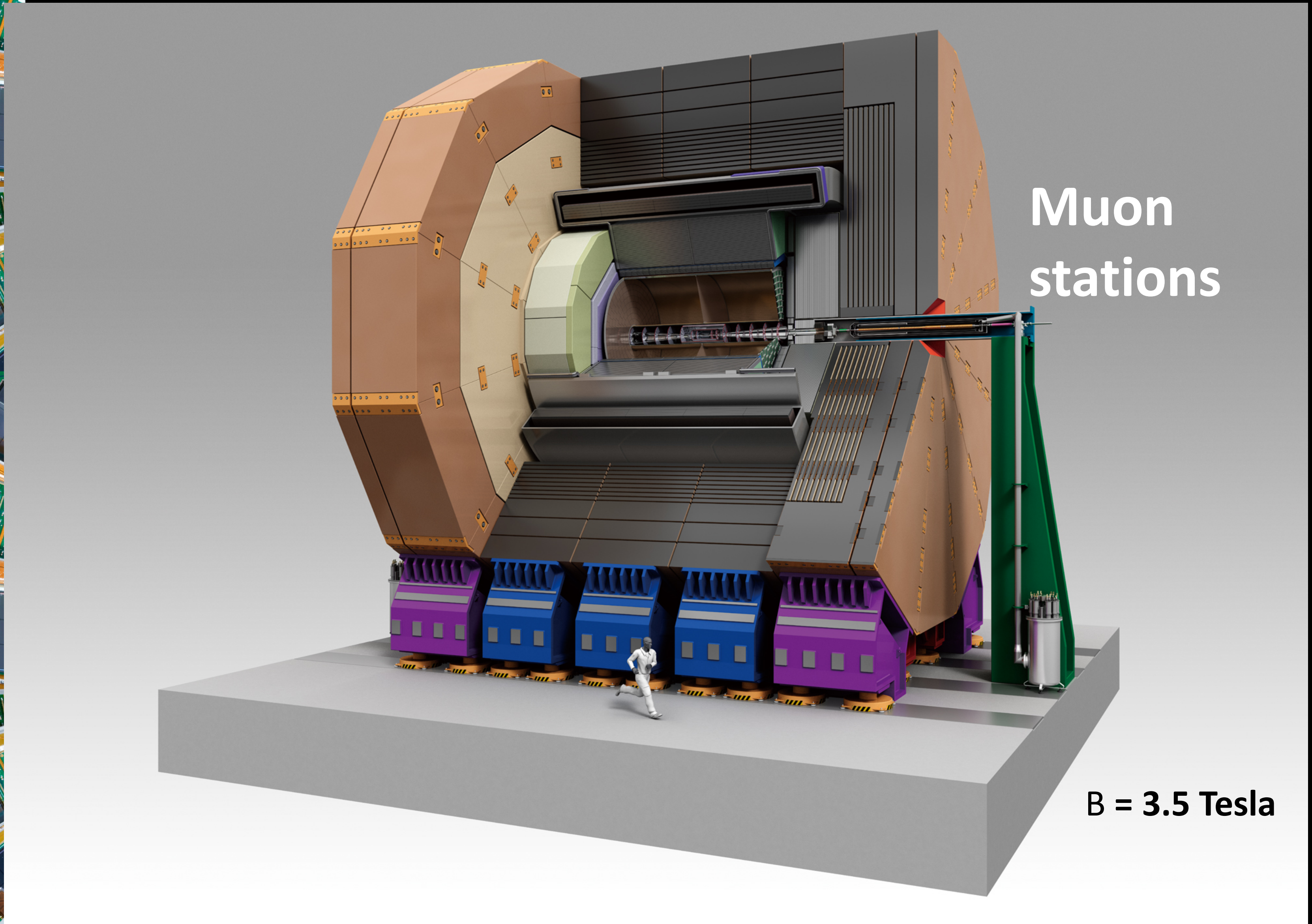
1:1 scale air cooling thermal test setup



- low material budget
  - 50 μm-thick sensors
  - 0.4% X_0 per double layer (0.2% X_0 per layer)
- total sensitive area = 0.84 m²

https://cds.cern.ch/record/2138963?ln=it

MUON Detectors ILC



- 14 layers in the barrel and 12 in the endcaps interleaved in the iron return yoke. The technology adopted is scintillator bars (2.5-3 cm wide, 7-10 mm thick) with wavelength shifting fibres and SiPM. Space resolution O(1 cm).
- RPCs (1x1 cm^2 pads) are considered as a possible option.