中国科学院高能物理研究所
Institute of High Energy Physics Chinese Academy of Sciences

Development of high granularity pixel sensors for CEPC Vertex Detector

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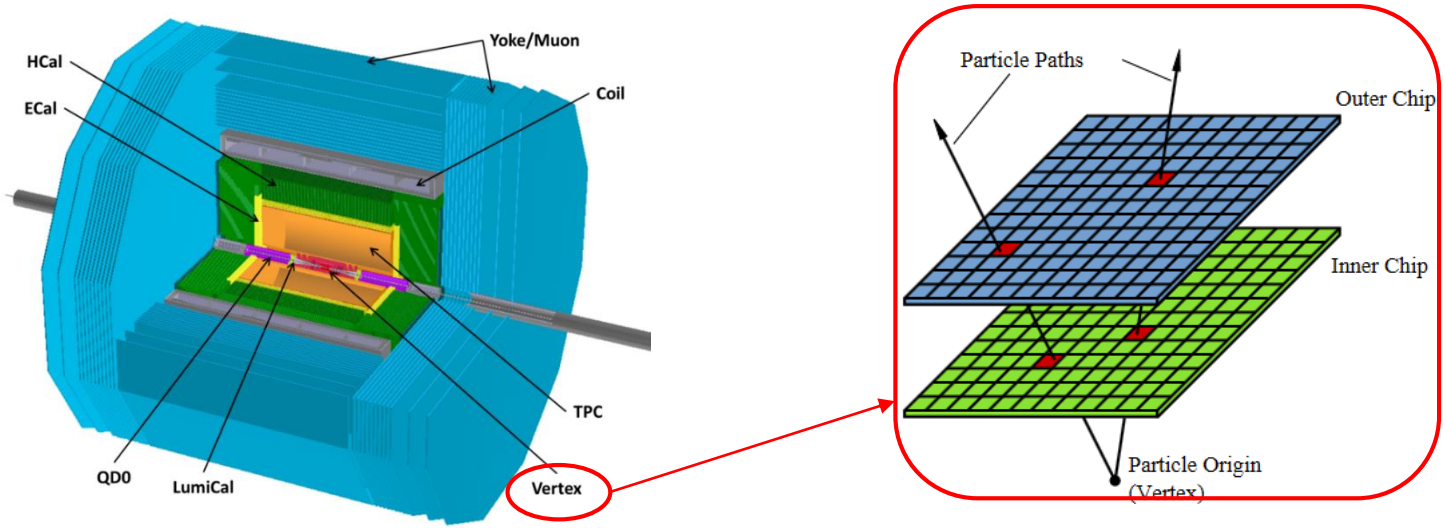
Outline

- Introduction and challenges of the vertex detector for CEPC
  - Specifications and design goal
- Two high granularity Pixel sensor prototypes: *with in-pixel digitization*
  - **JadePix2** in CMOS technology
  - **CPV** (**C**ompact **P**ixel sensors for the **V**ertex detector) in SOI technology
- Summary and outlooks
- Acknowledgement

Part 1: Introduction and challenges of the vertex detector for CEPC

Vertex detector general specifications



Vertex detector:

- *Inner most detector:*
  - *high flux density;*
- *Reconstruct the charm & bottom particle decay vertex:*
  - *Precise spatial & time resolution;*
  - *Thin (minimize scattering effect);*
  - *Low power consumption (simplify cooling system).*

Part 1: Introduction and challenges of the vertex detector for CEPC

Vertex detector general specifications

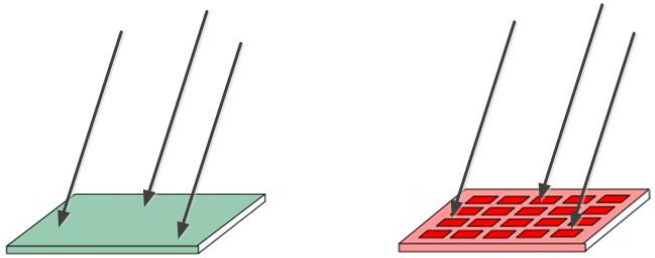
◆ ***General* requirements of vertex detector：**

High granularity, fast processing speed, thin* pixel sensors with *low power consumption

Some characters of promising technologies:

- 100% fill-factor
- Miniaturized: sensor and signal processing integrated in the same silicon wafer
- Low cost: standard commercial technology
- Low power dissipation: monolithic sensor
- Almost dead time free: very short reset time
- Sensitive: low noise; (signal collected by the sensing diode as low as 200 e^-)
- High granularity: pixel pitch on the scale of several tens of μm

High granularity is beneficial for both high flux and precise spatial resolution

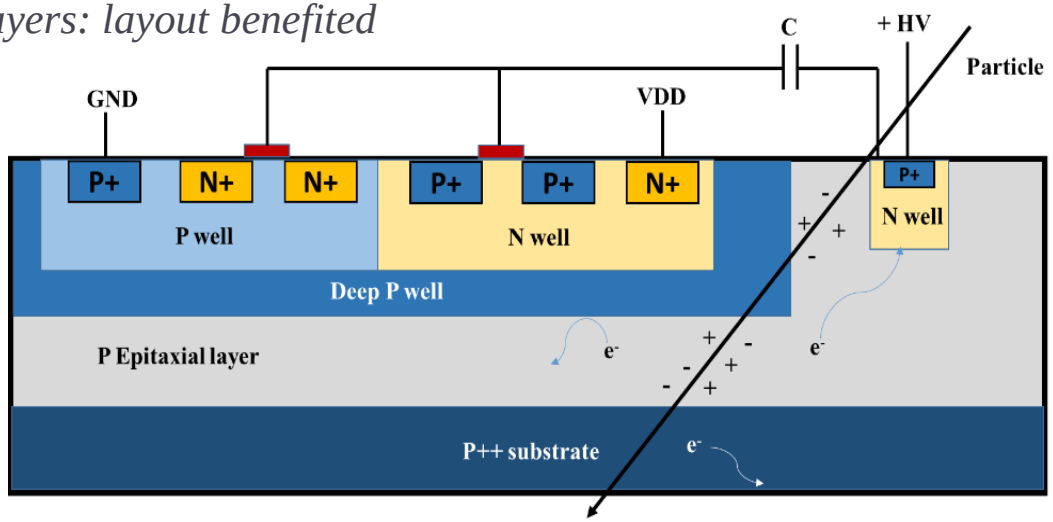


Part 1: Introduction and challenges of the vertex detector for CEPC

Technology options

CMOS technology: *TowerJazz 0.18 μm CIS process for example*

- Quadruple well process, deep PWELL shields NWELL of PMOS: full in-pixel CMOS
- Thick (~20 μm) and high resistivity (≥1 kΩ•cm) epitaxial layer: more depletion
- *Thin gate oxide (<4 nm): robust to total ionizing dose*
- *6 metal layers: layout benefited*



- *Latest Mimosa series @ IPHC for STAR*
- *ALPIDE @CERN for ALICE upgrade*

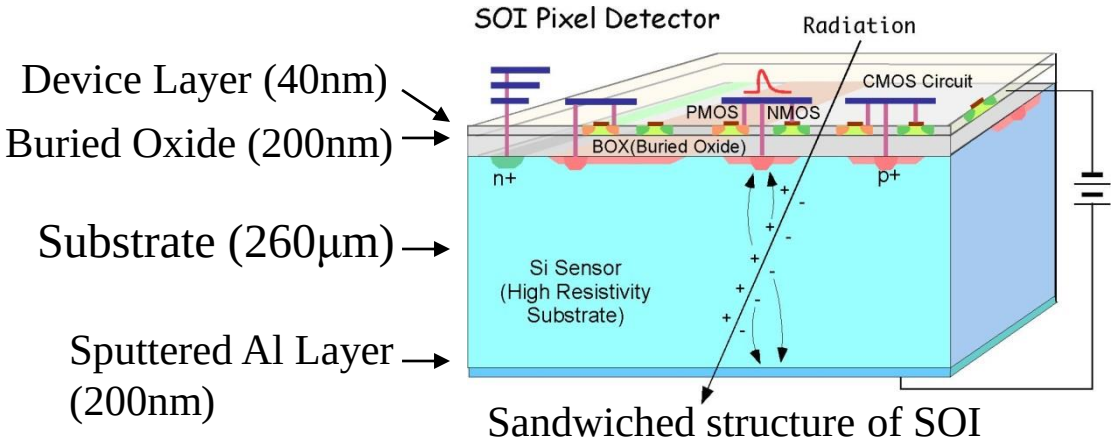
Part 1: Introduction and challenges of the vertex detector for CEPC

Technology options

SOI: *LAPIS 0.2um process*

- Fully depleted sensor
- Full in-pixel CMOS
- 5 Metal layers
- High resistive substrate (≥1 kΩ•cm).
- Could be back thinned down to 75 μm

➢ *SOFIST@KEK for ILC pre-R&D*



Challenges of the vertex detector for CEPC

- Efficient tagging of heavy quarks (b/c) and τ leptons

$$\sigma_{r\phi} = a \oplus \frac{b}{p(GeV)\sin^{3/2}\theta}\,(\mu m)$$

a depends on single point resolution $\sigma_{s.p.}$ & on the lever arm
b depends on the distance between the innermost layer to IP and on the material budget

- to achieve a=5 and b=10 (B=3.5T):
  - Single point resolution near the IP: ≤ 3 μm→ high granularity
  - material budget: $\leq 0.15\% X_0$/layer → Low power dissipation, thinned, monolithic pixel sensor (50μm thick, <50mV/cm^2?)
  - pixel occupancy: ≤ 1% → High granularity & fast processing speed(<20μs/frame ?)
  - Radiation tolerance: ∼1 Mrad/y (TID) and ∼10^{13} N_{eq}/cm^2/y (NIEL)

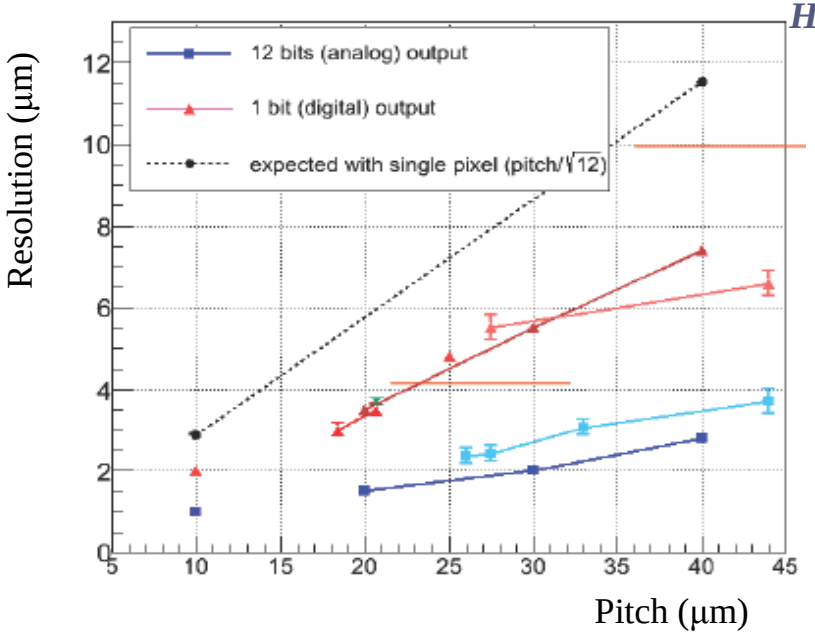
Challenges of the vertex detector for CEPC

Name	Structure	Pixel pitch (μm^2)	Integ.time (μs)	Power density (mW/cm^2)	Spatial resolution
MISTRAL (IPHC)	Column-level comparator, Rolling-shutter	22 × 33	30	200	≈ 5μm
ASTRAL (IPHC)	In-pixel comparator, Rolling-shutter	22 × 33	20	85	
ALPIDE (CERN,INFN,CCNU,YONSEI)	In-pixel comparator, Global-shutter	27 x 29	2	39	

Part 1: Introduction and challenges of the vertex detector for CEPC

Design goal: to reach $\sigma_{sp} < 3\ \mu m$

Spatial resolution vs pitch obtained from Mimosa sensors *



How fine a pixel pitch needed, to obtain a $\sigma_{sp} < 3\ \mu m$? +

① Less than 40 µm with analogue output +12 bits external ADC

- Power pulsing mode in ILC (SOFIST)

② Less than 30 µm with 4 bits digital output

- *Check MIMADC & Mimosa 31*

③ Less than 18 µm with one bit digital output

J. Baudot; **Fully depleted CMOS Pixel Sensors: developments and applications; ANIMMA 2015, Lisbon, 20-24 April 2015.*

*+J.Baudot, "**An ILD vertex detector with CMOS sensor –status report**", in Linear Collider Power Distribution and Pulsing workshop, LAL Orsay, May 2011.*

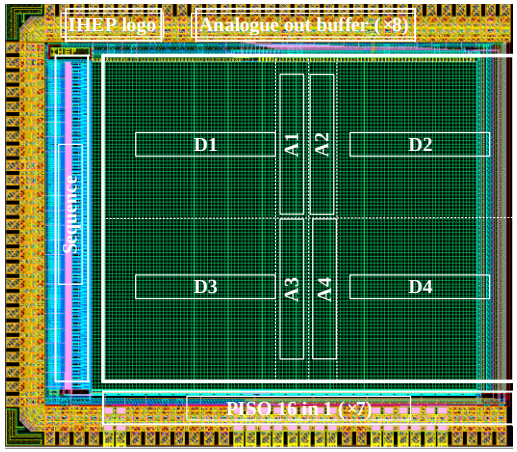
Outline

- Challenges of the vertex detector for CEPC
- High granularity Pixel sensor prototype:
  - **JadePix2** in CMOS technology
  - **CPV** in SOI technology
- Summary and outlooks

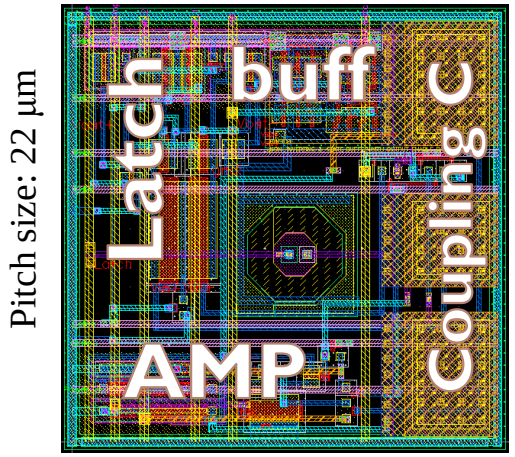
Part 2: High granularity Pixel sensor prototype

JadePix2 in CMOS technology

JadePix2: joint 0.18 μm CMOS process MPW submission with IPHC in May. 2017



Layout of JadePix2



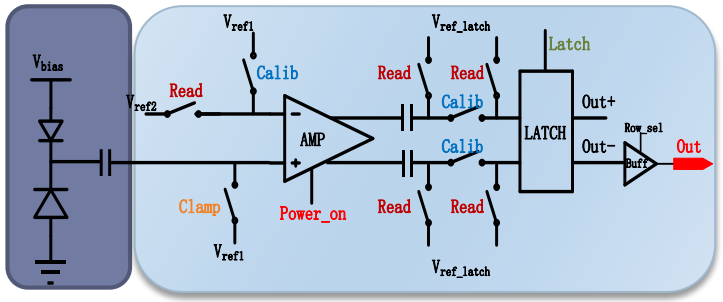
Layout of a single pixel in JadePix2

- *3 × 3.3 mm²;*
- *96 × 112 pixels with 8 sub-matrix*
- Processing speed: 11.2 μs/frame for 80 ns/row;
- Output data speed: 160 MHz;
- Power:3.7 μA/pixel;

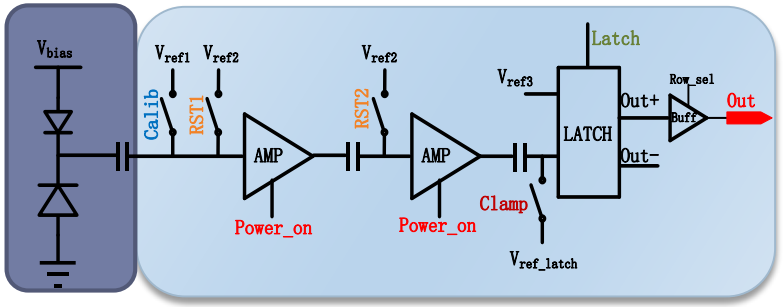
Part 2: High granularity Pixel sensor prototype

JadePix2: in-pixel structure and operation timing

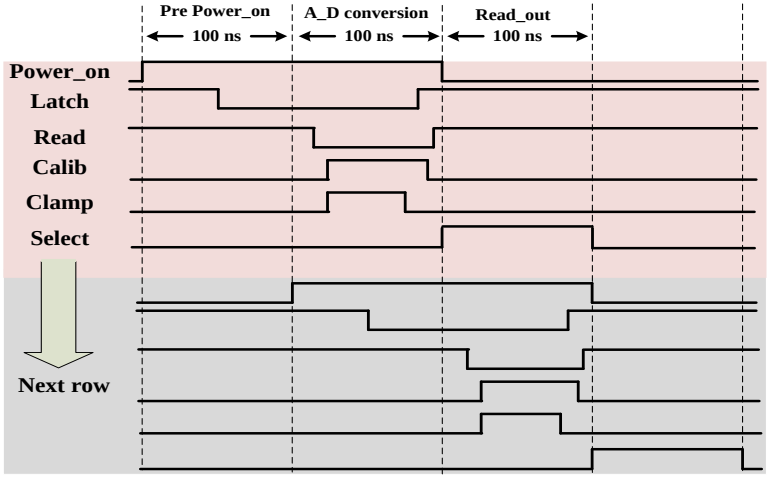
2 pixel versions were proposed in JadePix2:



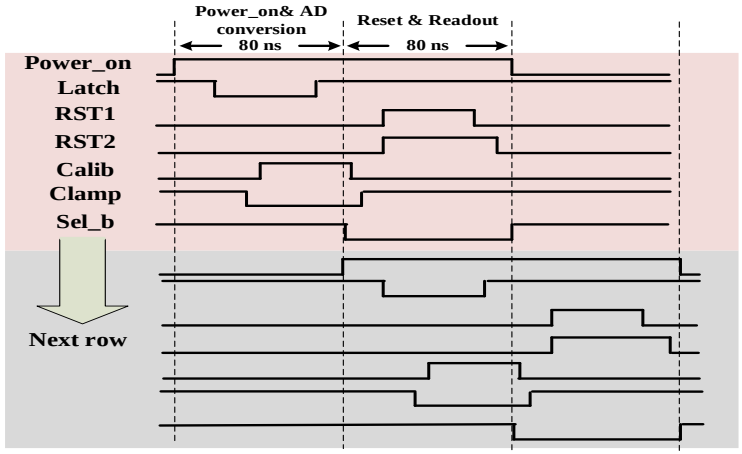
Version 1: differential amplifier + latch



Version 2: two stage CS amplifiers + latch



Operation timing of pixel version 1

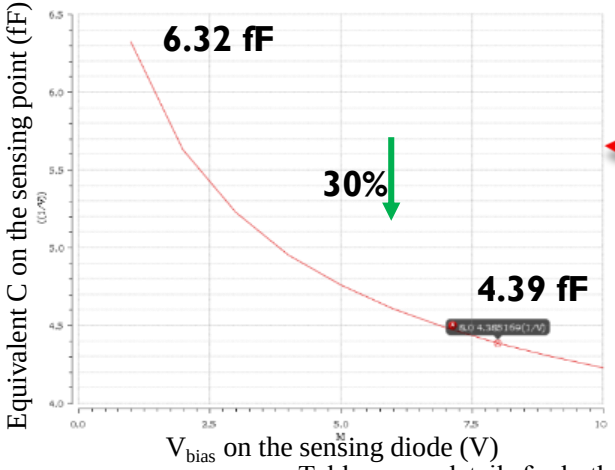


Operation timing of pixel version 2

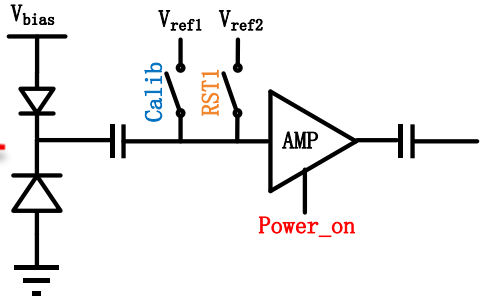
Part 2: High granularity Pixel sensor prototype

JadePix2: sensing point

equivalent C on the sensing point:



For version 2 & diode surface = 4 μm²



*A carefully layout & AMP input transistor size was chosen

Table: some details for both of the 2 versions with different "Bias voltage" and "diode size"

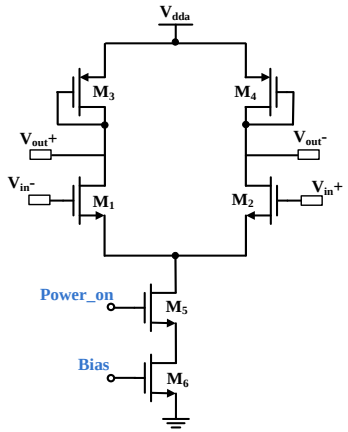
	Diode size (μm²)	Diode Bias (V)	Equivalent C, including AMP input transistors (fF)	Parasitic C (fF)	Total sensing point C (fF)	CVF on the sensing diode (μV/e⁻)	CVF after 1st AMP (μV/e⁻)
Version 1	4	8	3.53 fF	0.786 fF	**4.316 fF**	**37**	**303**
Version 2	4	1	6.32 fF	0.670 fF	6.99 fF	22.9	187.3
		8	4.39 fF		**5.06**	**31.7**	**250**
	8	1	8.13 fF		8.80	18.2	143.8
		8	5.37 fF		6.04	26.5	209.4

"Best case"

Part 2: High granularity Pixel sensor prototype

JadePix2: performances of the in-pixel amplifiers

Version 1: *first stage AMP transient noise* *(sensing part was not included)*

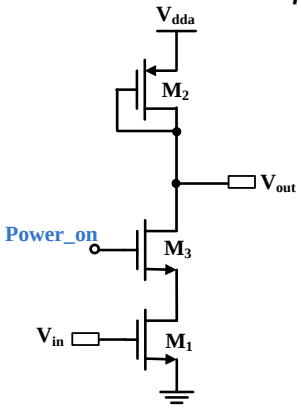


Differential Amplifier Noise simulation:

- Input DC level: 600 mV
- Biasing current: 3.7 μA
- Gain: 8.3
- RMS noise: 1.962 mV

ENC: ≈ 7 e^- (for best case; highly relayed on the equivalent $C_{sensing\ point}$)

Version 2: *first stage AMP transient noise* *(sensing part was not included)*



Single-end CS Amplifier Noise simulation:

- Input DC level: 520 mV
- Gain: 8
- RMS noise: 1.566 mV
- ENC: 6.3 e- (for best case)

Part 2: High granularity Pixel sensor prototype

JadePix2: offsets of the in-pixel amplifiers

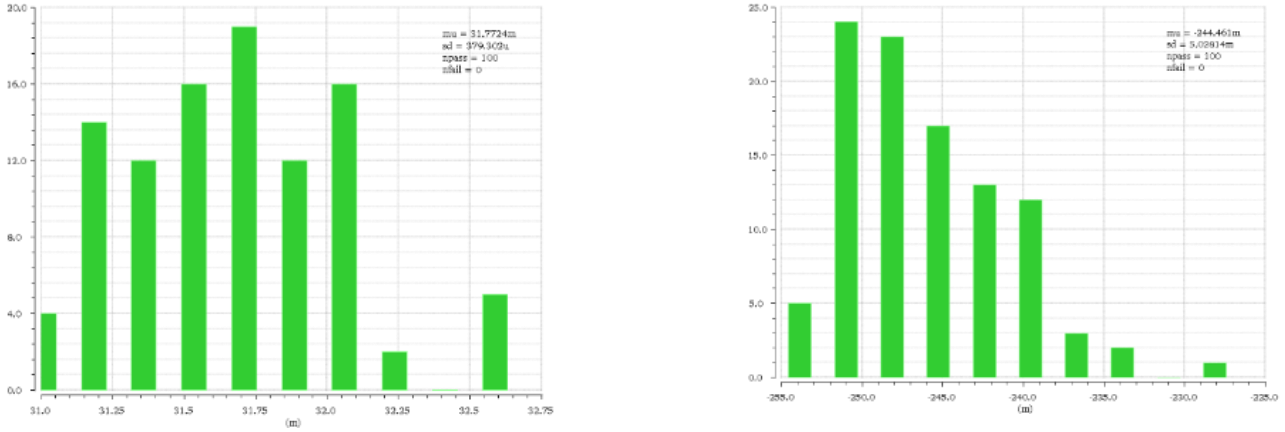


Figure 6: Monte Carlo Simulation of the pixel version2, first stage Amp. offset (process variation + mismatch): input point (left) and outpoint (right).

offset in “best case”	RMS	ENC
AMP input side	379.3 μV	12 e^-
AMP output side	5.028 mV	20 e^-

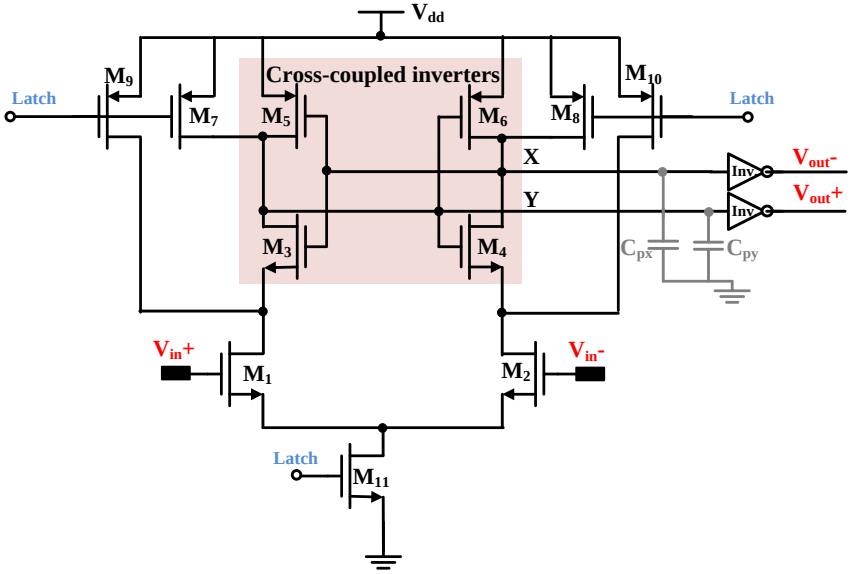
Simulation results show the offsets of the amplifiers are significant, thanks to the in-pixel offset cancellation stage, these offsets are cancelled in the in-pixel CDS process.

Part 2: High granularity Pixel sensor prototype

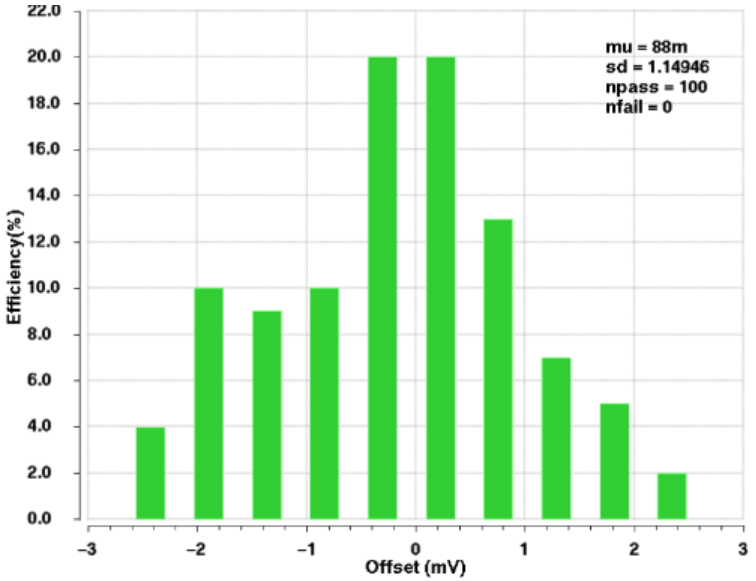
JadePix2: offset of the dynamic Latch

Offset caused by the dynamic Latch:

Monte Carlo Simulation of the dynamic Latch offset : process variation + mismatch



Rising edge



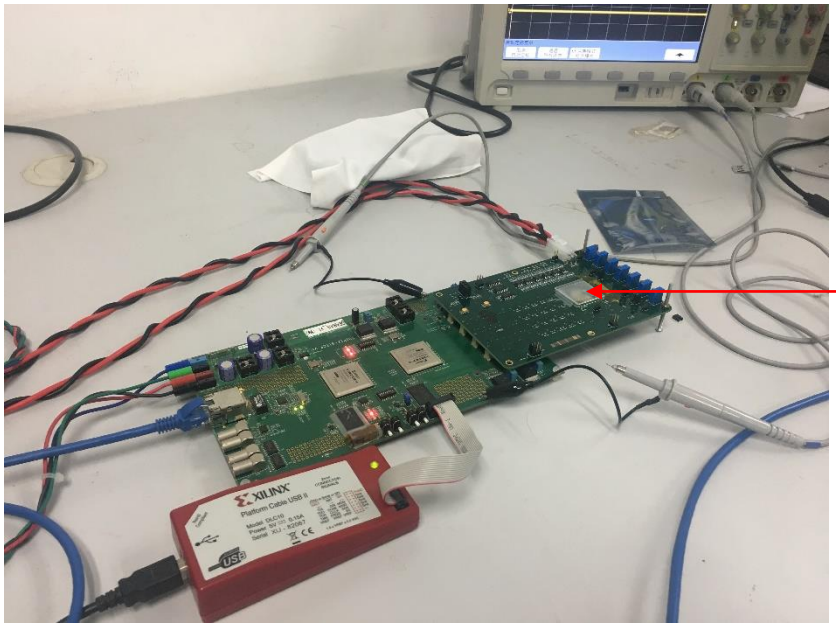
Falling edge

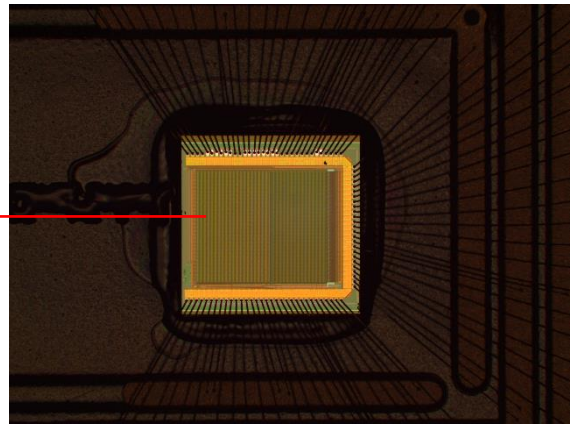
Latch offset in "best case"	RMS	ENC
Version 1	1.15 mV	≈ 4 e^-
Version 2		ignorable

Part 2: High granularity Pixel sensor prototype

JadePix2

Test of JadePix2 is still ongoing……





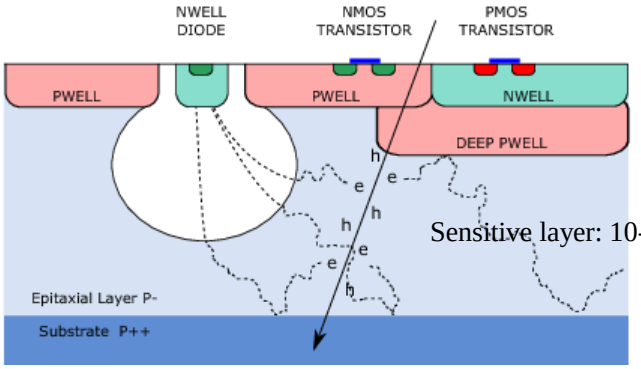
Outline

- Challenges of the vertex detector for CEPC
- Specifications and design goal
- High granularity Pixel sensor prototype:
  - **JadePix2** in CMOS technology
  - **CPV** in SOI technology
    - Design
    - Test results about: CVF, noise, single point resolution results…
- Summary and outlooks

Part 2: High granularity Pixel sensor prototype

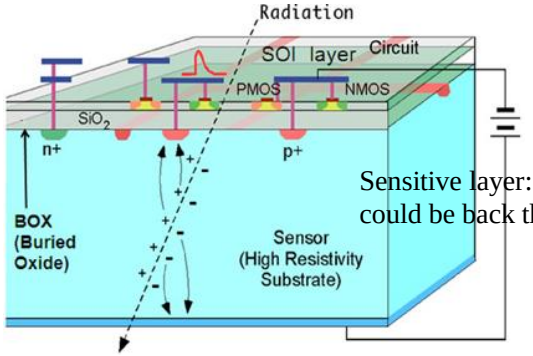
CPV in SOI technology

SOI/CMOS technology: concerning granularity



Sensitive layer: 10-20 µm thick

CMOS



Sensitive layer: hundreds µm, could be back thinned to 50 µm

SOI

SOI pixel technology potential advantages:

- Thicker sensitive layer: *simplify the electronic design*

  - 2-3 times signal charges for Minimum Ionizing Particles (MIP) even after the sensor back thinning down to ≈ 50µm

- More compact layout: *shrink the pixel size*

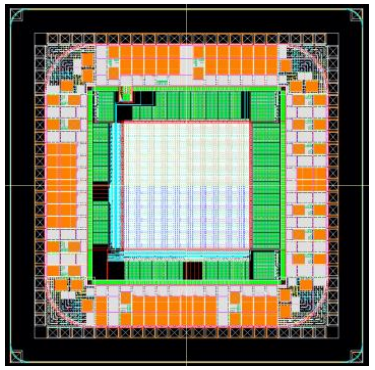
  - PMOS & NMOS transistor could be closer (no NWELL PWELL used for transistors in SOI)

Potentially high granularity

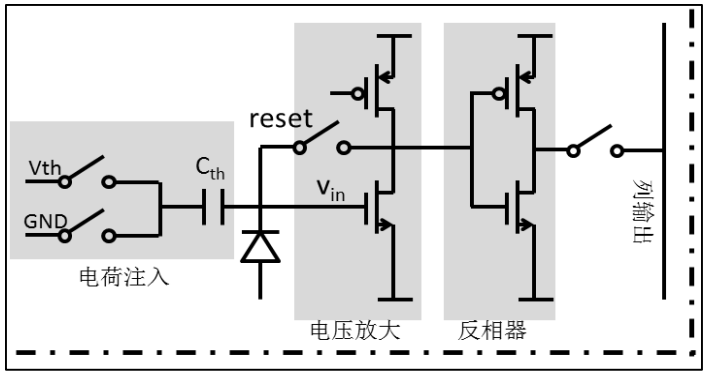
Part 2: High granularity Pixel sensor prototype

Design of CPV1

- First digital pixel of 16um pitch size
- CS voltage amplifier, gain ~ 10
- Inverter as discriminator
- Threshold charge injected to sensing node
- Pixel array: 64*32 (digital) + 64*32 (analog)
- Double-SOI process for shielding and radiation enhancement
- Submitted June, 2015

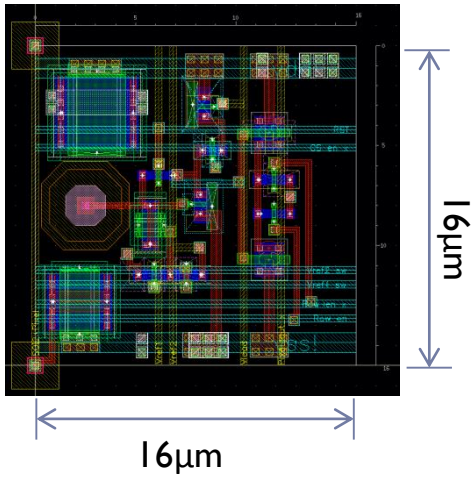


CPV1 prototype layout: $3 \times 3\ mm^2$



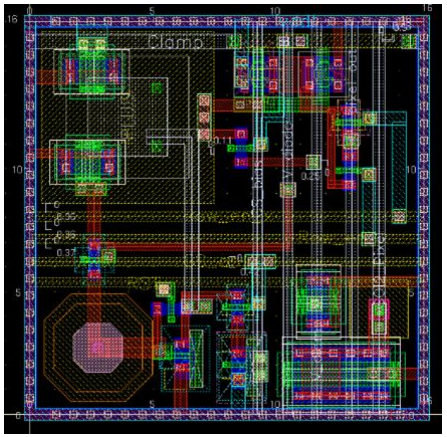
Pixel schematic of CPV1

CPV1 digital pixel layout

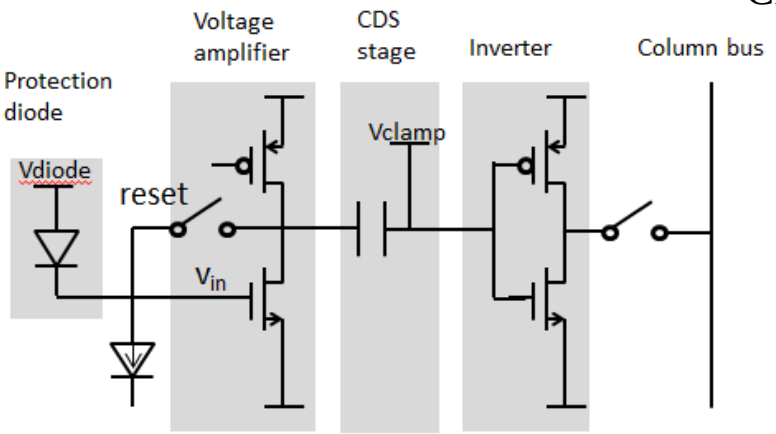


Design of CPV2

- Protection diode added
  - Enable full depletion on sensor
- In-pixel CDS stage inserted
  - improved RTC and FPN noise
  - replaced the charge injection threshold
- Sensor thickness was thinned to 75 μm
- Submitted June, 2016



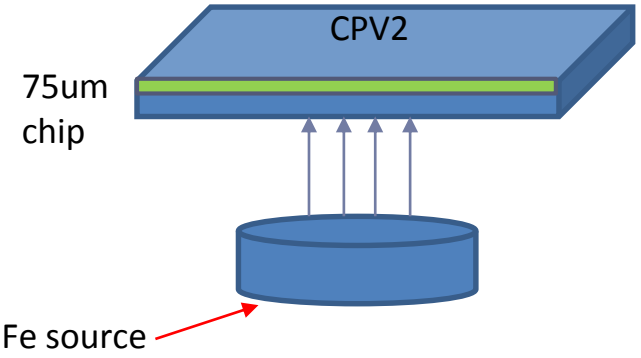
CPV2 digital pixel layout

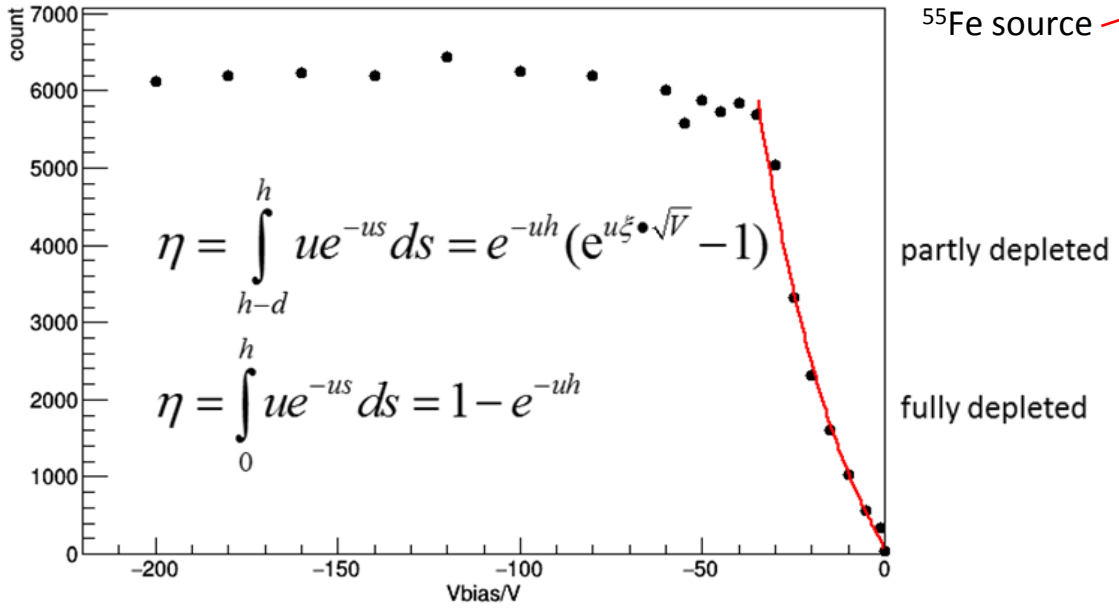


Pixel schematic of CPV2

CPV2 test: fully depleted

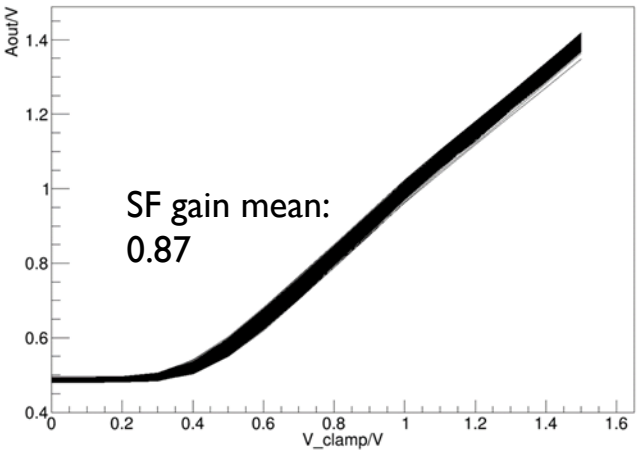
- ^{55}Fe signal Efficiency versus bias voltage
  - x-ray illuminates the sensor from backside
  - plateau reached @V_{bias} = -40V
  - An evidence of fully-depleted sensor

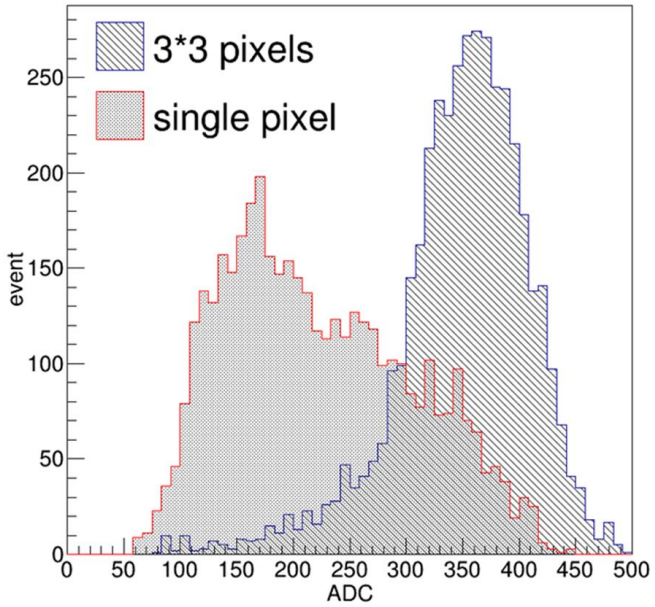




CPV2 test: CVF calibration

- Charge voltage factor (CVF)
  - ^{55}Fe 5.9KeV X-ray@1640e^-
  - SF gain measured 0.87
  - Most probable signal amplitude around 180ADC in single pixel mode
  - A peak at 360ADC in 3×3 pixel cluster mode
  - CVF: 123.3μV/e^- @source follower input

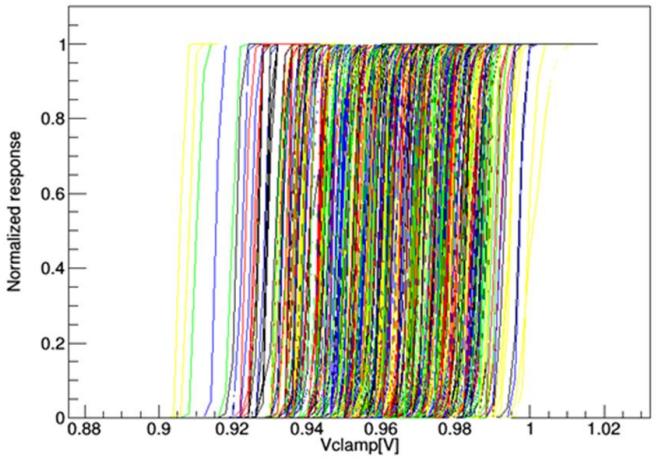


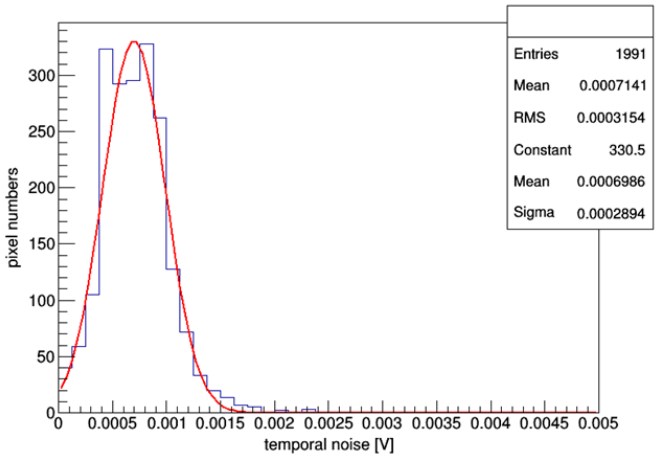


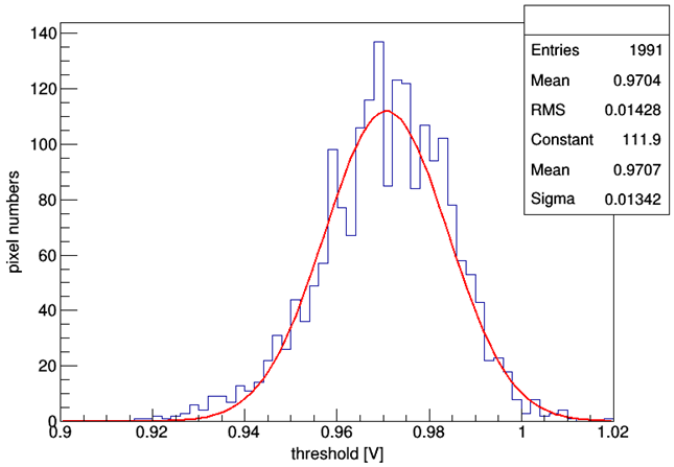
CPV2 test: Noise performances

- Temporal noise and FPN
  - S-curve measured on full pixel array
  - TN: ~6e-
  - FPN:~114e-; need to be improved.

Full array S-Curve



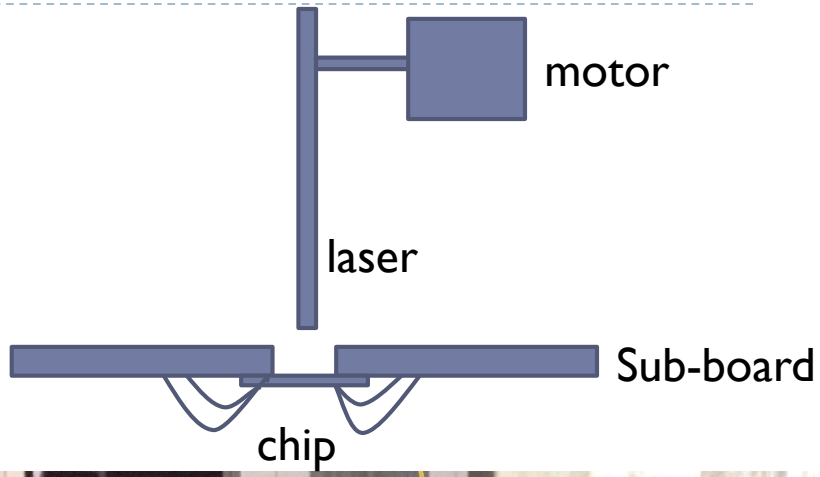


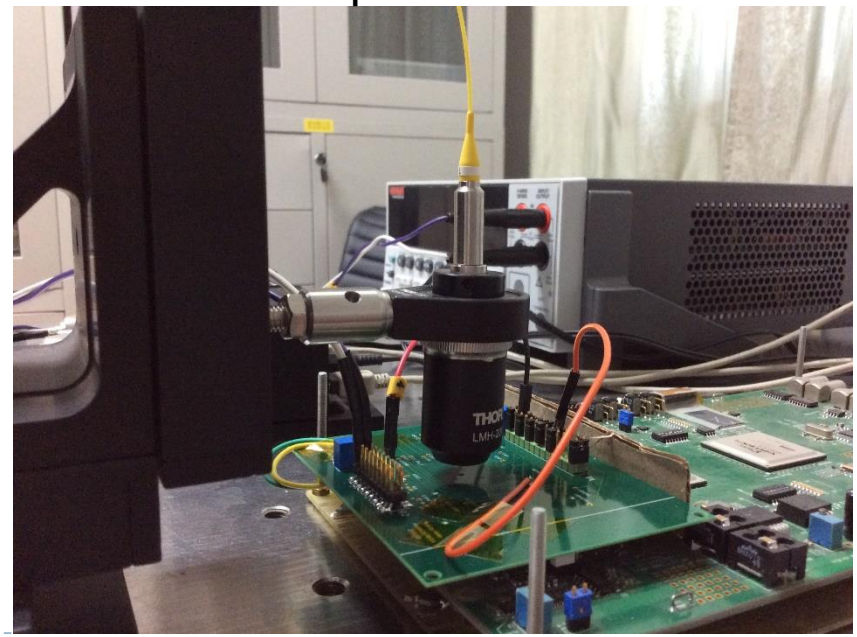


Part 2: High granularity Pixel sensor prototype

CPV2 single point resolution measurement: experiment setup

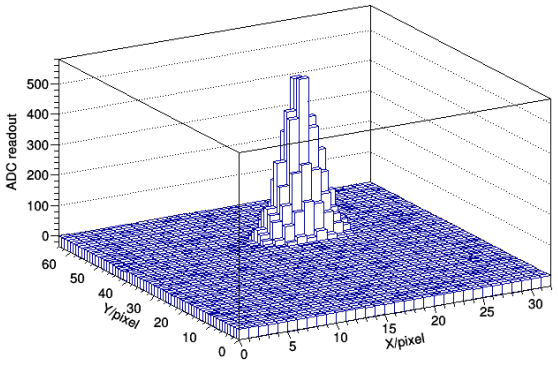
- 1064nm laser beam
  - optical lens to focus laser
- 3-dimensional stepping motor
  - accuracy: 0.1μm
- Thinning chip
  - wire-bonding on sub-board
  - illuminate from backside (no aluminum)



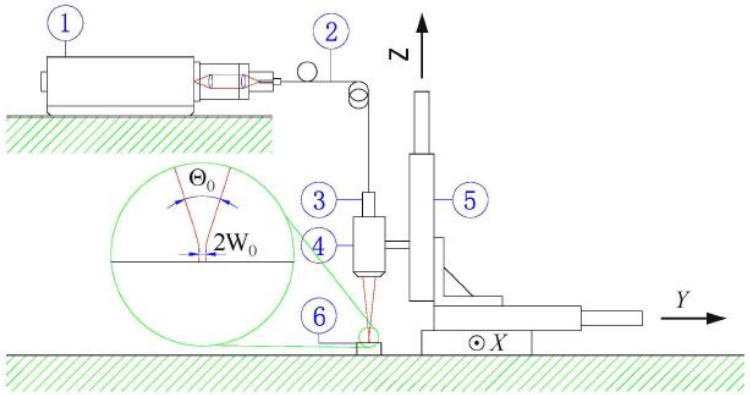


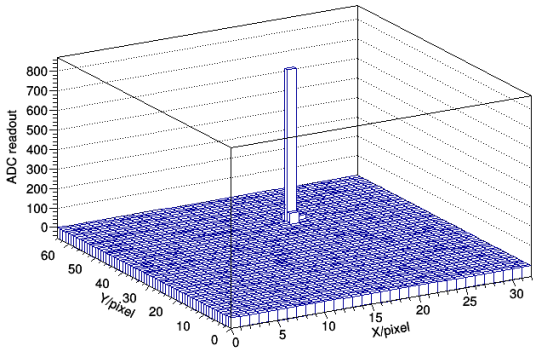
CPV2 single point resolution measurement: laser beam

- Timing
  - Triggered by the frame start signal
  - Synchronized with rolling shutter readout
- Focusing with analog pixel as a monitor
  - Achieve the smallest beam cluster
  - Calibrate the equivalent electron number of laser energy



before focusing

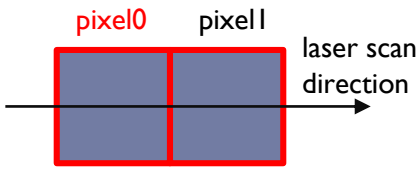


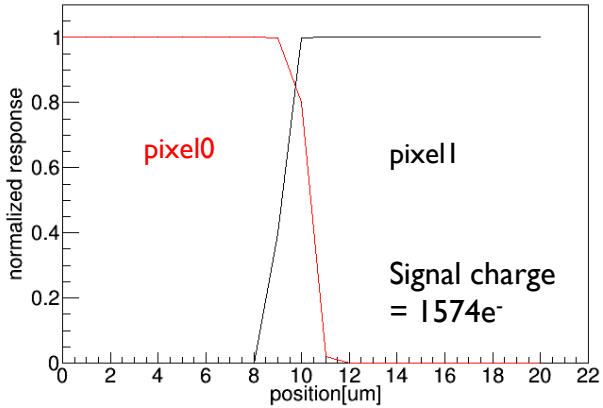


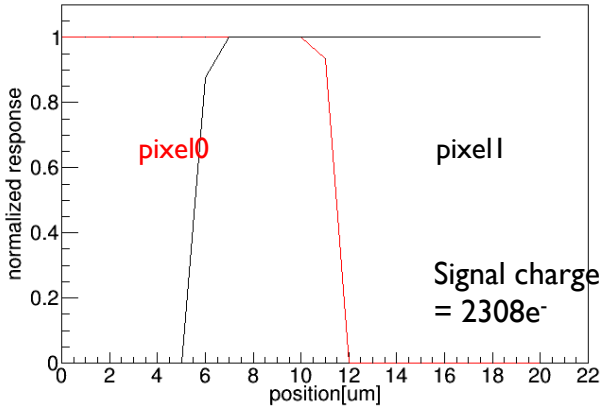
after focusing

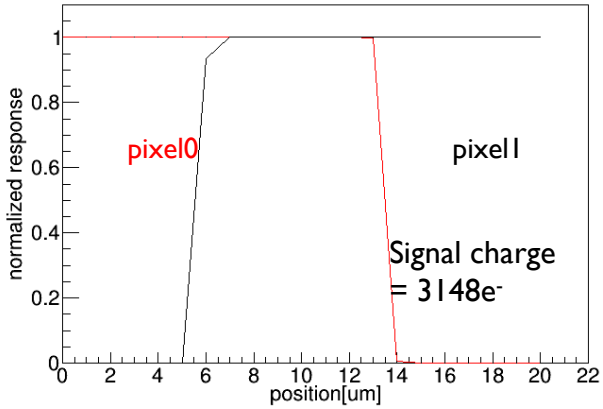
CPV2 single point resolution measurement: laser scan

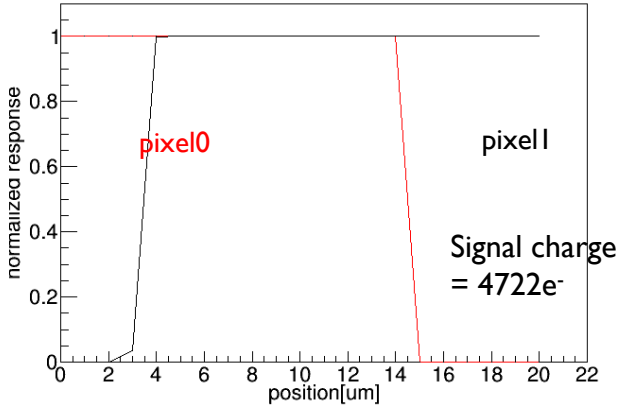
- Scan two adjacent digital pixels
  - Step size of 1μm
  - Threshold is fixed (no noise hits)







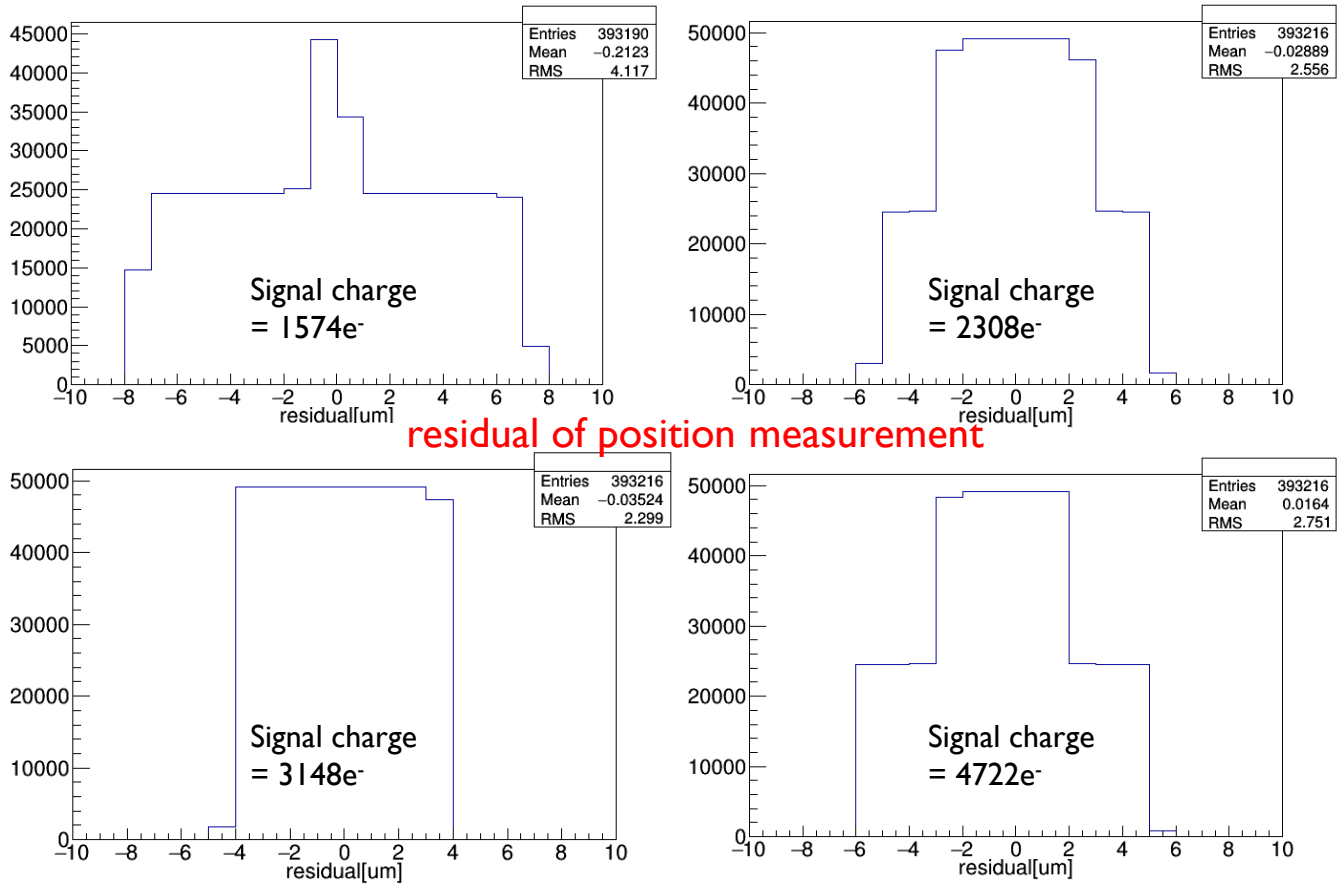




Normalized response =number of hit/number of pulse

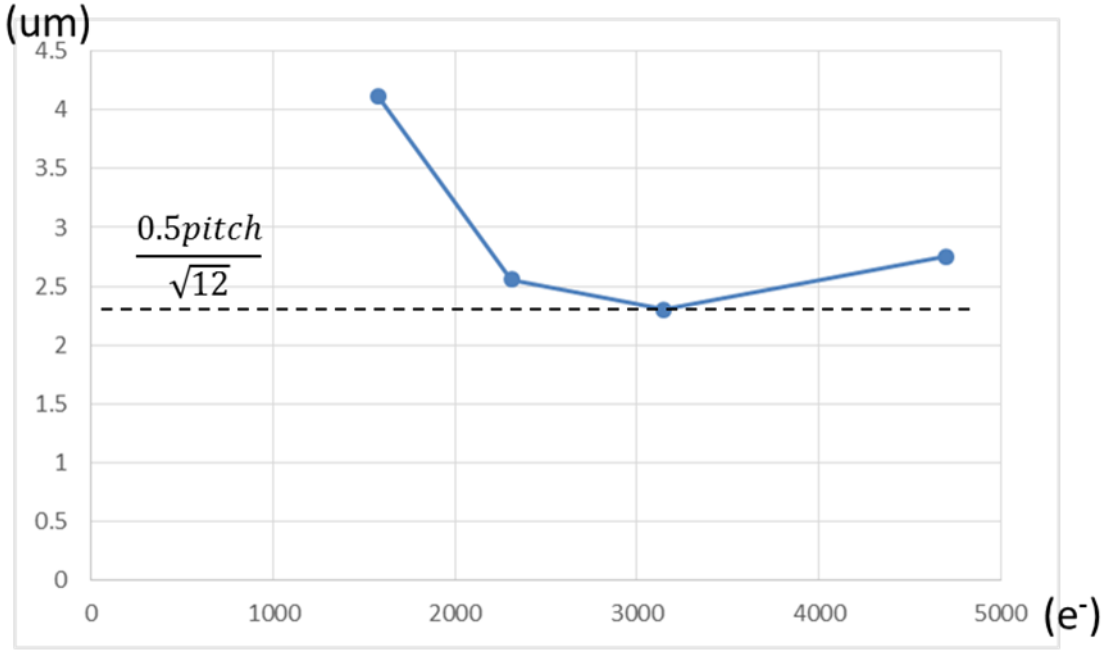
CPV2 single point resolution laser measurement results

- Actual position decided by motor
- Responding position reconstructed by Center of Gravity



CPV2 single point resolution laser measurement results

- Spatial resolution versus signal level
  - Get the best resolution of 2.3μm at ~ 3000e$^-$ signal level



Summary and outlooks

Some features of The two prototype compares with ASTRAL and ALPIDE:

	ASTRAL	ALPIDE	JadePix2	CPV2
Process technology	0.18 μm CMOS			0.2 μm SOI
Readout strategy	Rolling shutter	asynchronous		Rolling shutter
Readout time	20 μs	<2 μs	100ns/row or 80ns/row	50ns/row
Power	85 mW/cm^2	39 mW/cm^2		
Pixel size	22 × 33 μm^2	27 ×29 μm^2	22 ×22 μm^2	16 ×16 μm^2
Spatial resolution	≈ 5μm		Not tested yet	Possibly < 3μm
Total signal for MIP	≈1600 e$^-$ (≈20μm epi-layer)			≈4000 e$^-$ (back thinning to 50μm, fully depleted)

- Demonstrated that a single point resolution <3μm is possible with the method of integrating 1-bit digitization in each pixel
- Perform the test of JadePix2
- Optimize the performances in the following prototypes
- Characterize more features by beam test: Fake hit rate, detection efficiency, radiation tolerance….

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Thanks for your attention!