CEPC Vertex Detector R&D Status

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On behalf of the CEPC VTX R&D Team

IHEP, CAS

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CEPC Workshop at Rome

Outline

- CEPC Vertex detector
- Pixel prototype – JadePix1
- Summary and outlook

Requirement of CEPC Vertex Detector

- The identification of heavy-flavor (b/c) quarks and tau-leptons is essential for CEPC physics program.
- Precision measurement of H→b$\underline{\text{b}}$, c$\underline{\text{c}}$ requires track parameter resolution

$$\sigma(r\phi) = a \oplus \frac{b}{p(\mathrm{GeV})\sin^{3/2}\theta}\ \mu\mathrm{m}$$

  - a: intrinsic resolution of vertex
  - b: multiple scattering effect
  - a=5, b=10 taken as design value

Performance goals for Vertex Detector

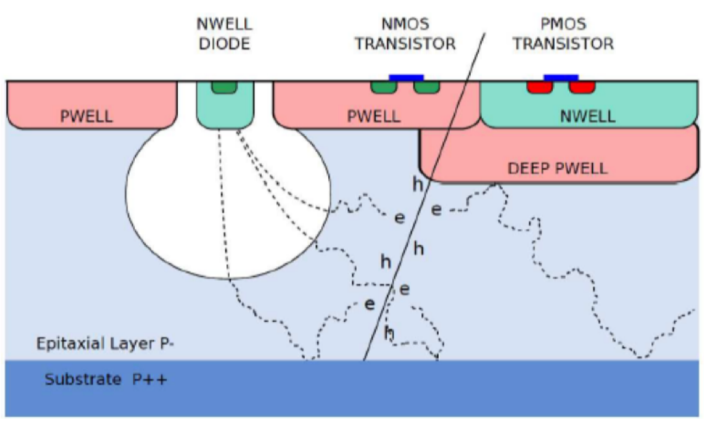
- Spatial resolution near the IP $\sigma_{SP} \leq 3\mu m$
  (high granularity, small pixel size)
- Material budget $\leq 0.15\%$ X_0/layer
  (monolithic pixel sensor thick 50μm
  + air cooling power consumption 50mW/cm^2)
- Low detector occupancy $< 0.5\%$
  (high granularity and/or short readout time)
- Radiation tolerance:
  ~1MRad/y(TID) and 10^{13} 1MeV n_{eq}/cm^2/y(NIEL)

Sensor Options

- No sensor technology satisfies all the requirements of CEPC vertex detector (yet)
- Potential options after extensive R&D
  - Depleted Field Effect Transitor (DEPFET)
    Belle-II vertex
  - CMOS Pixel Sensors (CPS)
    ALICE ITS , STAR PXL, JadePix1 (this talk),
    JadePix2 (see talk by Y. Zhou)
  - Silicon-on-insulator (SOI)
    Explored at IHEP (see talk by Y. Zhou)

CMOS Pixel Sensor – TowerJazz Process

- Integrated pixel sensor and readout electronics on the same silicon bulk with the industry "standard" CMOS process
  -> Low material budget, low power consumption, low cost …



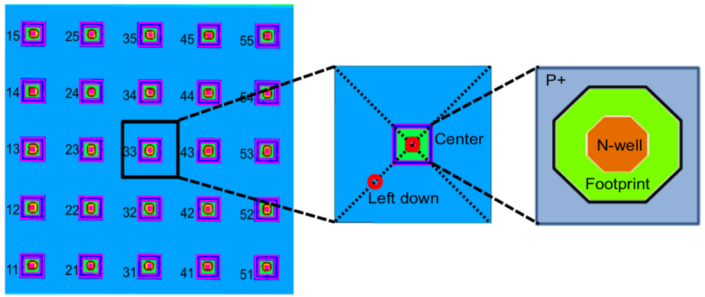
- TowerJazz CIS 0.18µm process features:
  - Quadruple well process: deep P-Well shields N-Well of PMOS transistors, allowing for full CMOS circuitry within the active area
  - Feature size of 0.18um and 6 metal layers: high-density and low power
  - Thin gate oxide (3nm): radiation tolerance
  - Thick (> 20µm) and high resistivity (1kΩ·cm) epitaxial layer: possible improvement of charge collection

Sensor Design & TCAD Simulation

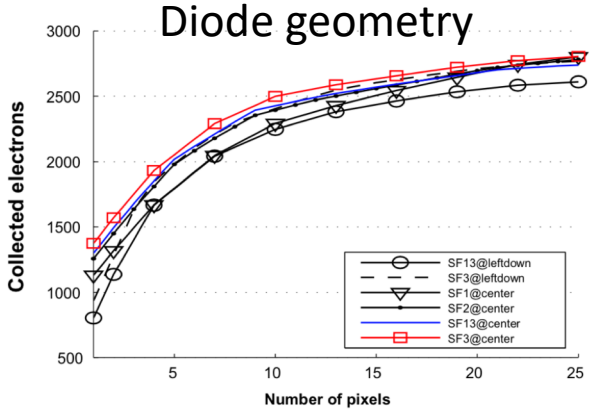
Y. Zhang, M. Zhao

- Charge collection performance with different sensor diode geometries, epitaxial-layer properties and radiation damages evaluated with TCAD simulation

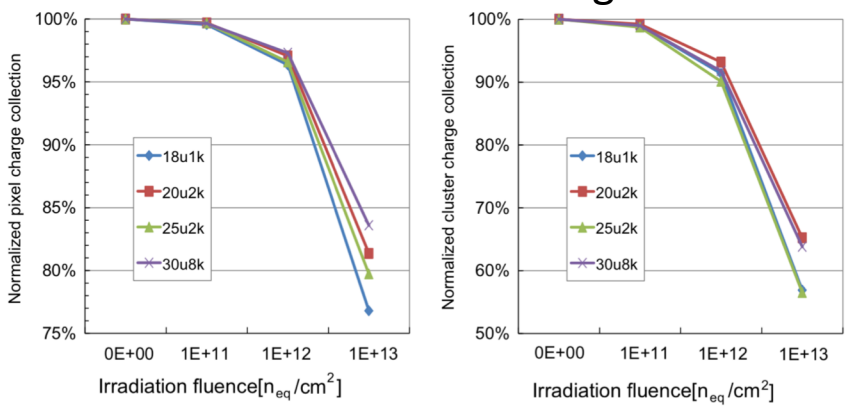
Pixel geometry parameters

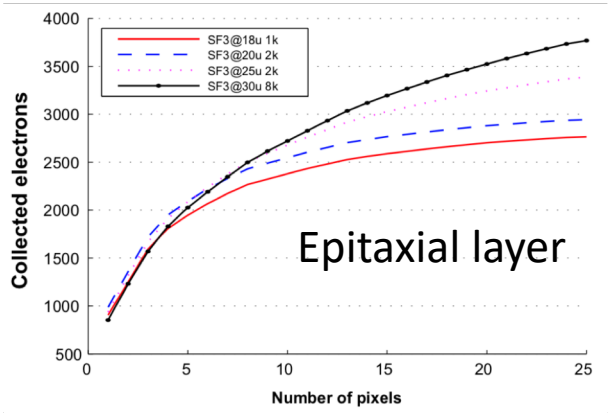


Diode geometry



Radiation damage





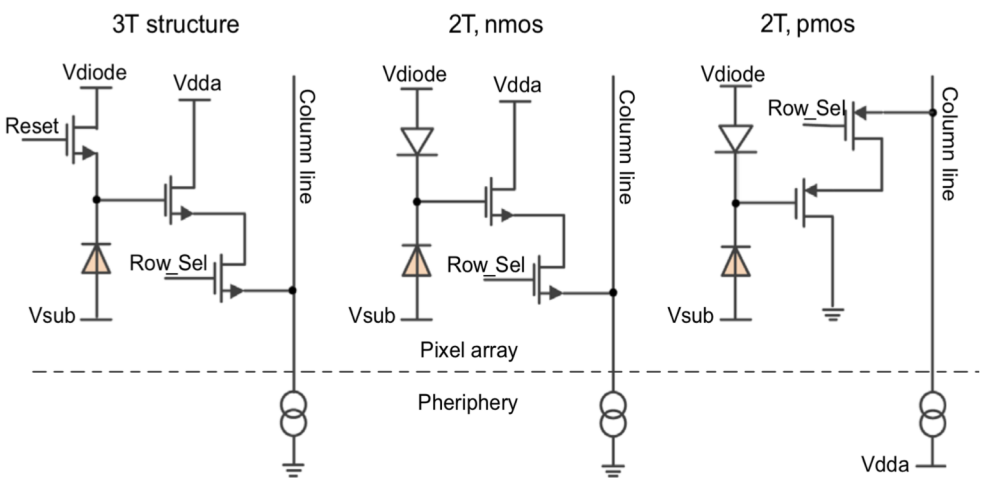
Y. Zhang et. al. NIMA 831 (2016) 99-104

Readout Electronics

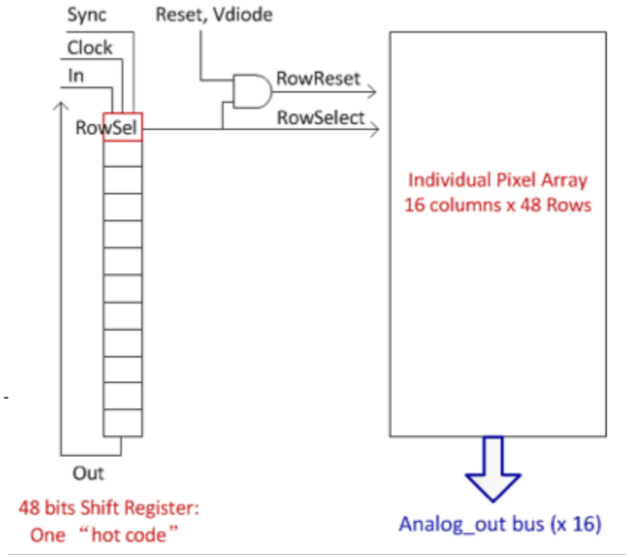
Y. Zhang, Y. Zhou, Y. Lu

- Conventional (simple and robust) 2T/3T in-pixel readout electronics, AC coupling structure with biased voltage up to 10V
  Enlarged depleted region/electric field -> potential improvement in charge collection
- Analog signal readout with the robust rolling shutter scheme

In-pixel readout structures

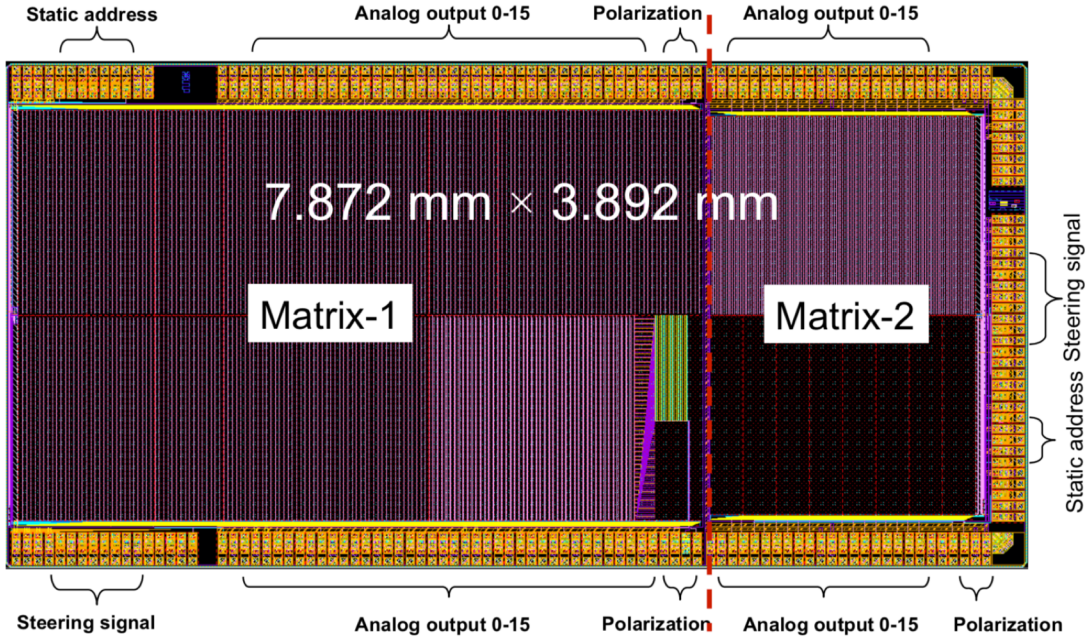


Peripheral circuitry

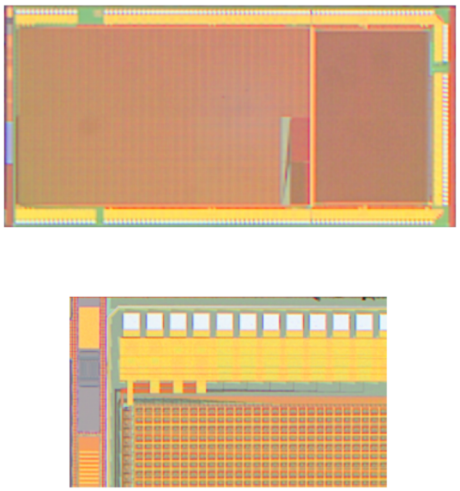


First Submission - JadePix1

- Joint MPW submission with IPHC in November 2015
- Aimed to understand charge collection performance with different diode geometries, epitaxial-layer properties, and potential radiation tolerance
- Diced samples returned to IHEP in June 2016
- Got name “JadePix1” on 29 December 2017 by voting.



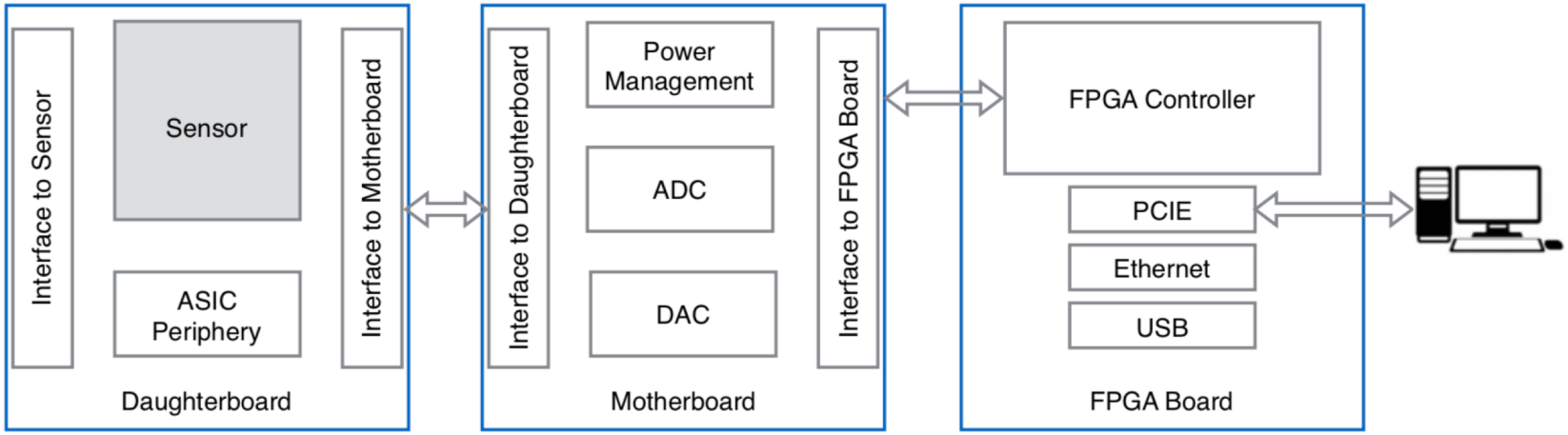
33x33μm^2 (Matrix-1) 16x16μm^2 (Matrix-2)



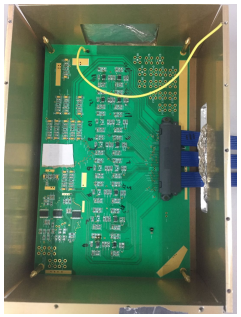
Diced pixel sensor

JadePix1 Test System

- Test system developed to characterize JadePix1 at IHEP

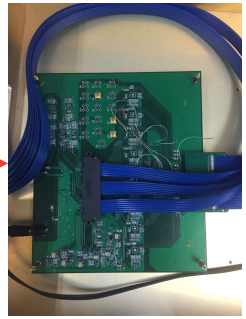


Sensor + Daughterboard



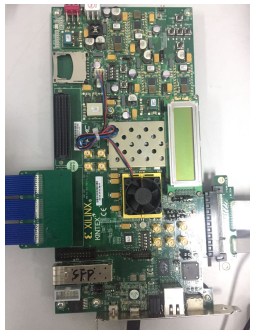
FMC

Motherboard



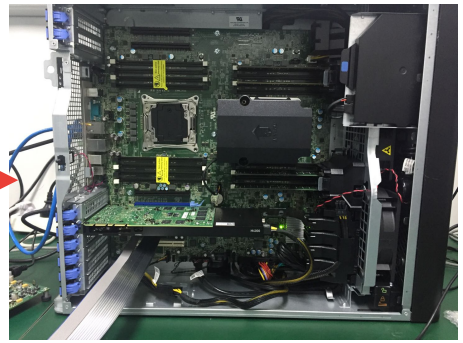
FMC

FPGA board



PCIeX8

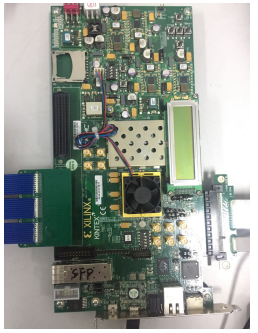
PC

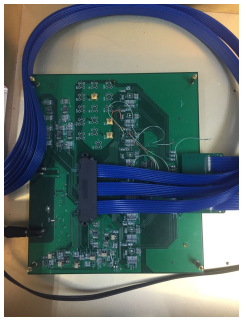


Test System Hardware Design

K. Wang, N. Wang, J. Tao

- FPGA board： control, data handle, data transmission
  - Xilinx KC705 FPGA board with mature technology
  - Data transmission with PCIe, close to 6Gbps
  - Main readout function of firmware：
    - Control CMOS sensor: initialize, address selection, clock
    - Control ADC sampling, serial data read
    - Data conversion: from serial to parallel, transmit to downstream
- Mother board: low noise stable power supply, AD conversion
  - Use 16 bit ADC，high resolution; support 8Vpp differential input, large dynamical range
  - Maximum support 16 ADC simultaneous readout
  - Provide low noise power supply and many types of bias voltage, support all matrix readout from sensor
- Daughter board： Good shield with strong anti-interference ability
  - Signal amplification with low noise
  - Standalone front-end suitable for radiation test

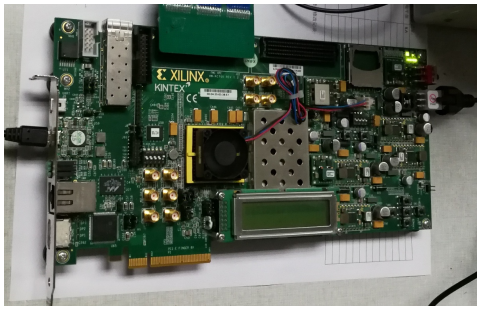


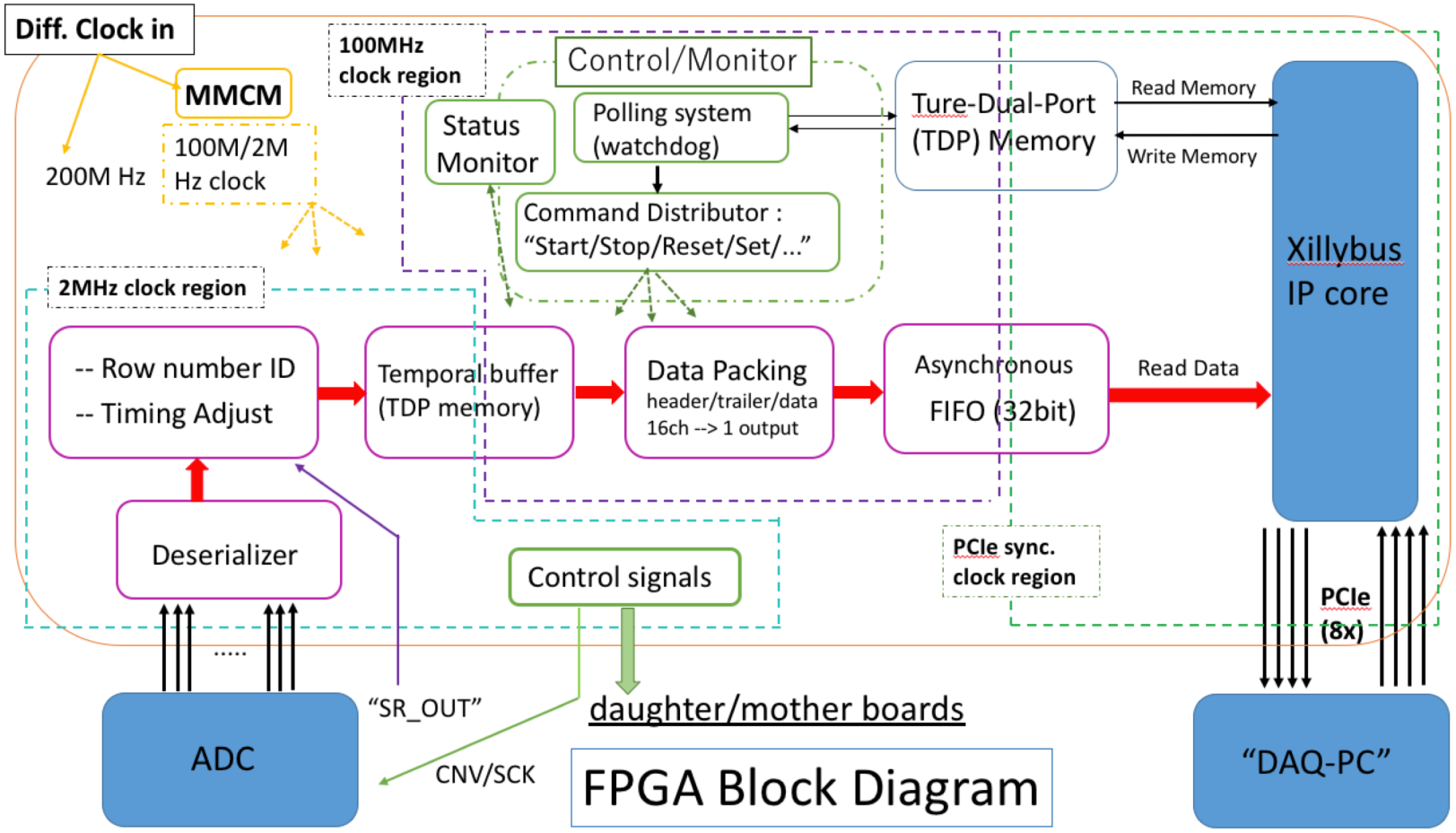


R. Kiuchi, J. Tao

FPGA Firmware

- Xilinx Kintex-7 FPGA
- Receive 16bit ADC 2MHz clock / control PC



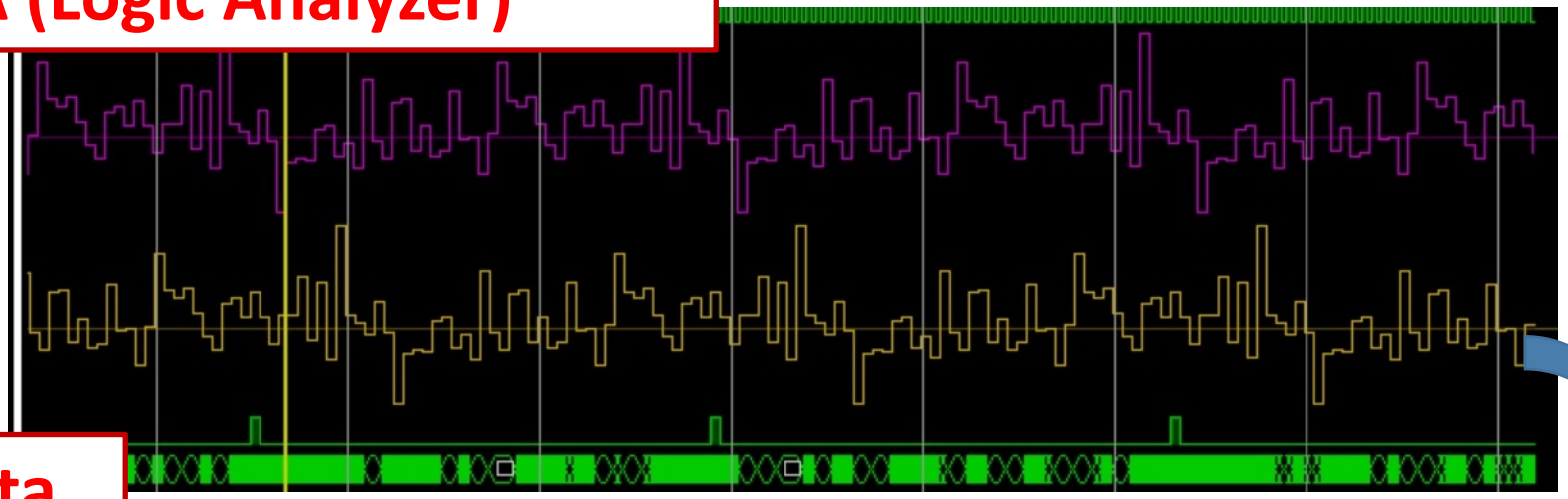


FPGA Block Diagram

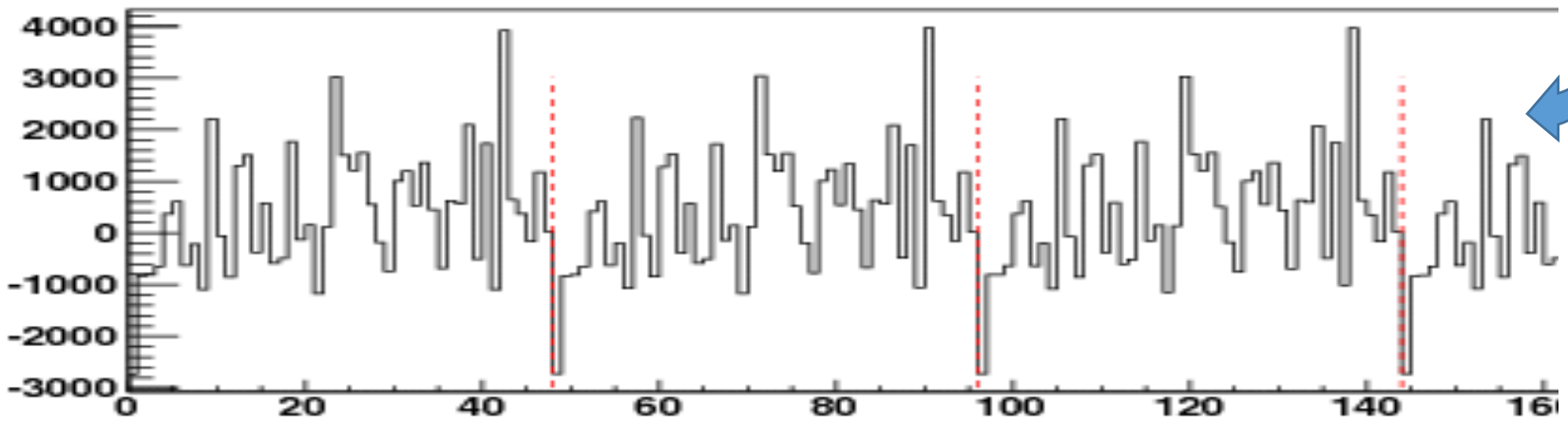
FPGA Firmware Development

R. Kiuchi

ILA (Logic Analyzer)



Data



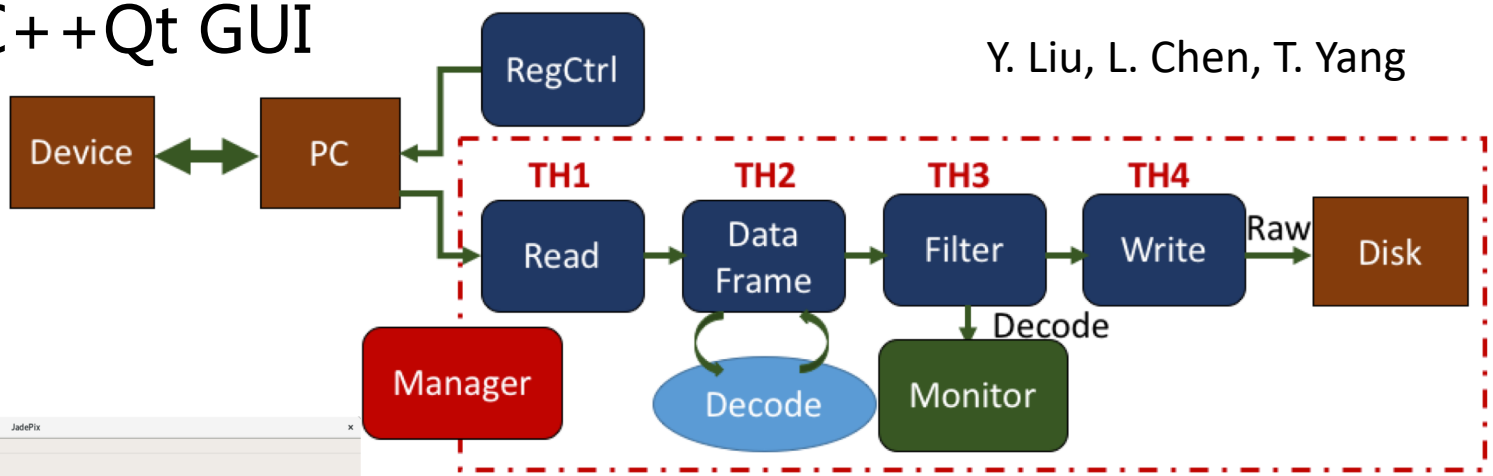
Clock validation

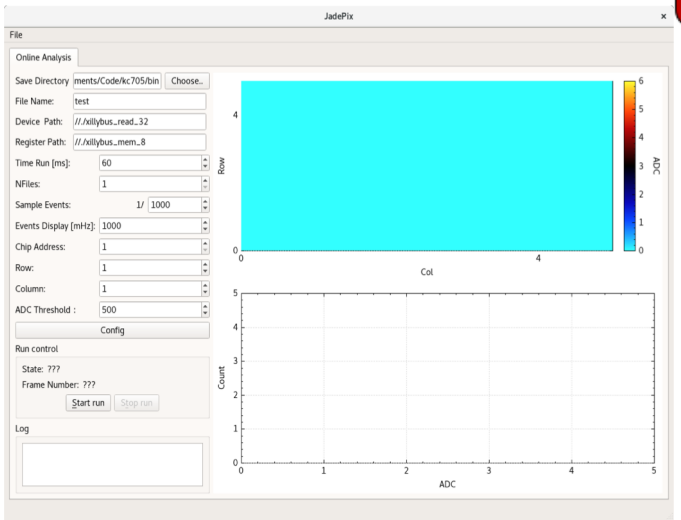
DAQ Software

- Version 1 : C++ core with Python Qt GUI
- Version 2 : Restructured C++ , multi-thread, C++Qt GUI

X. Lu, F. Gao,
J. Mansour,
T. Yang, X. Ju

Y. Liu, L. Chen, T. Yang

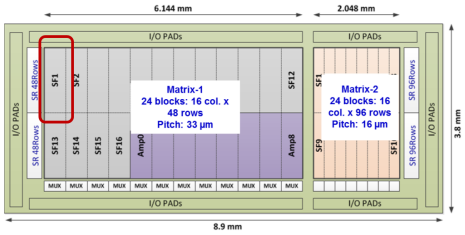




- Cross-platform, multi-thread
- C++/Qt GUI
- 80 MB/s data transmission
- Stable operation, accumulated >10 TB data on disk

Data structure

R. Kiuchi, T. Yang



- Define data structure for each pixel matrix frame, with header and footer

(1536 bytes + 48*(4+4)bytes = 1920 bytes)

\Row header\ + \Row data\ + \Row footer\ + ...

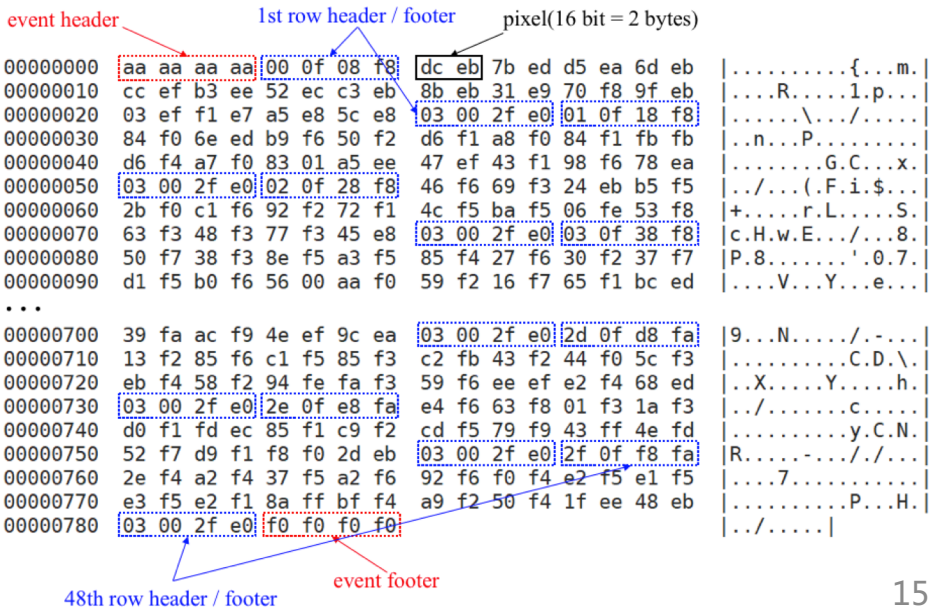
\Event header\ + \Event data\ + \Event footer\

\0xaaaa_aaaa\ (1920 *16 bit) \0xf0f0_f0f0\

(32 bit = 4 bytes) (32 bit = 4 bytes)

1 Event : 1928 bytes

- Check data structure correct in raw format

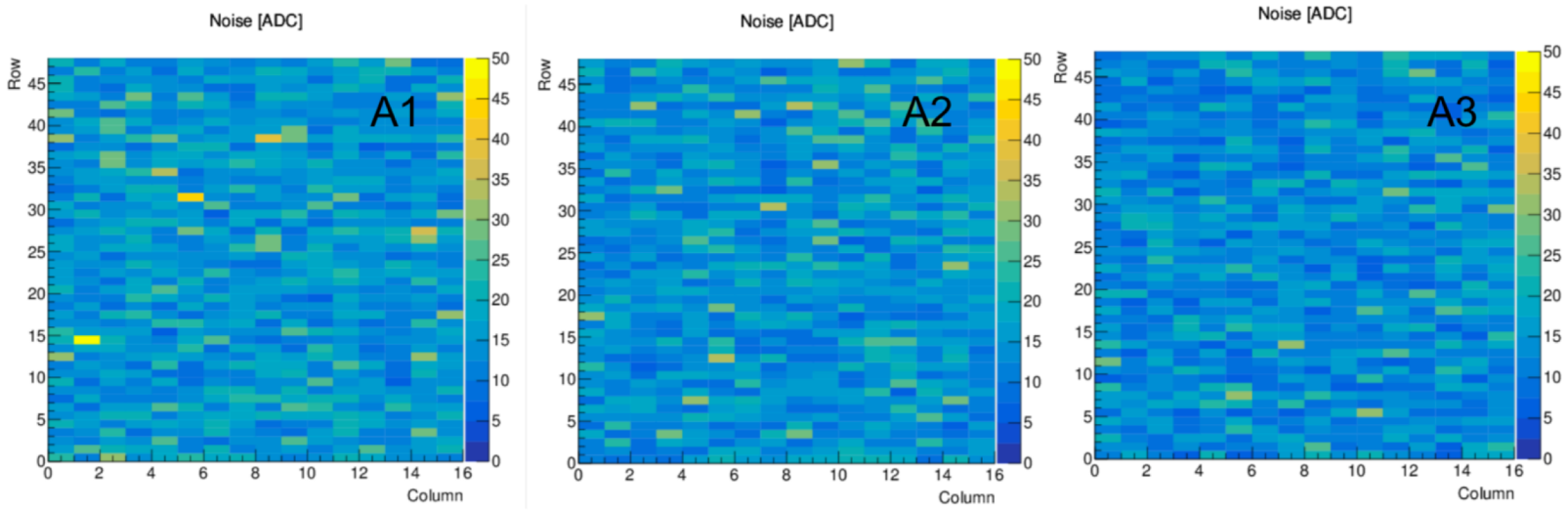


Noise Level (Preliminary)

L. Chen , H. Zhu

- Scan A1-A10 pixel matrix (33μm, 16x48) , Correlated Double Sampling（CDS）, subtract adjacent frame to suppress noise.

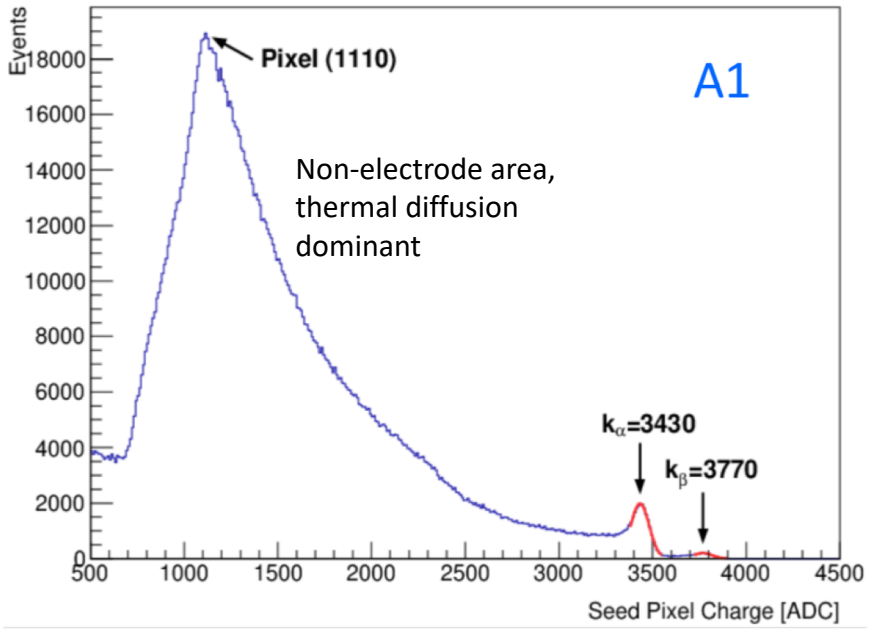
ENC~ 7.5 e^- ENC~ 8 e^- ENC~ 10 e^-

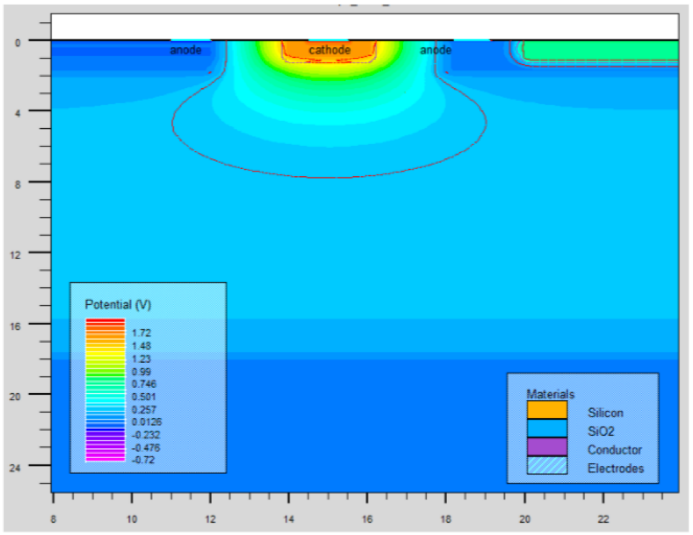


^{55} Fe Radiation test (Preliminary)

L. Chen , H. Zhu, R. Kiuchi

- Use ^{55} Fe for pixel gain calibration





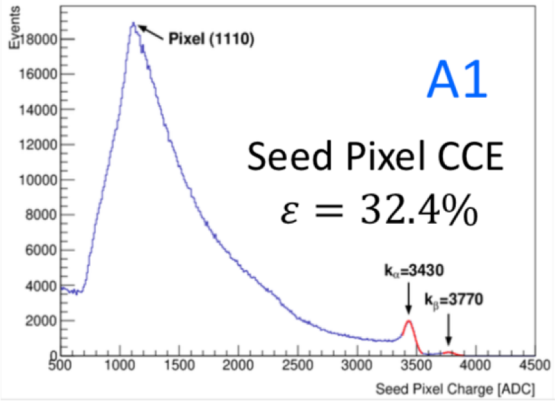
- $k_\alpha k_\beta$ peak can be recognized clearly

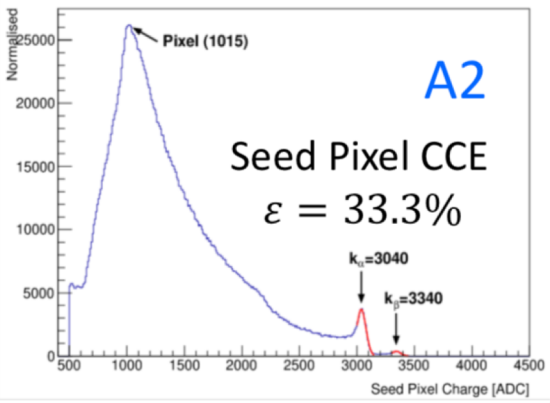
Electrode Size (Preliminary)

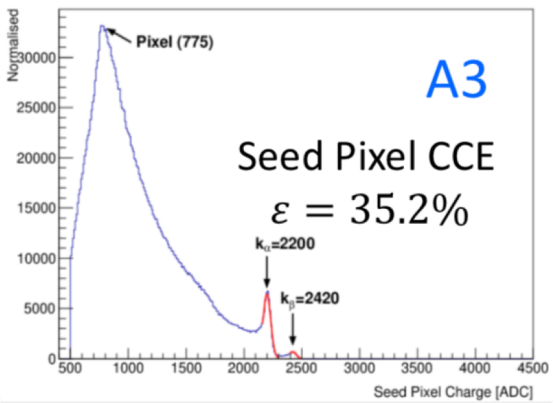
L. Chen , H. Zhu

- Larger electrode size -> better charge collection, but larger capacitance, low gain and higher noise

Sector	*Diode surface*	*Footprint*	*Structure*
A1	4 μm²	30 μm²	2T_nmos
A2	8 μm²	30 μm²	2T_nmos
A3	15 μm²	30 μm²	2T_nmos





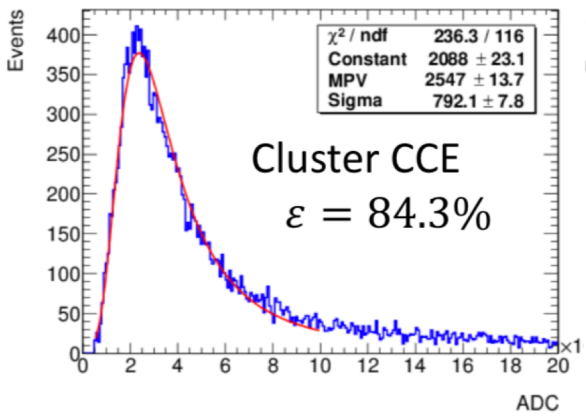


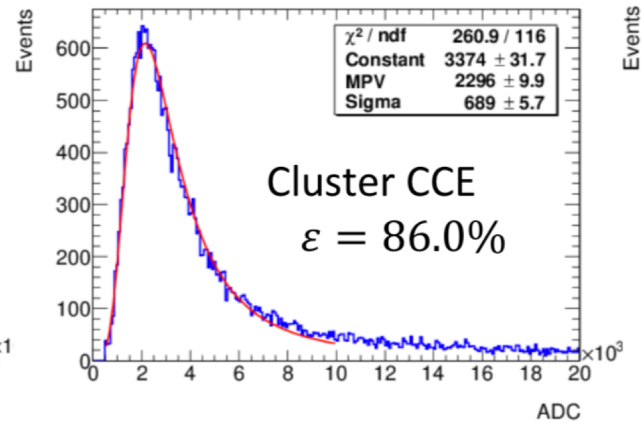
- Optimization: Q/C (analog power consumption), S/N (spatial resolution)

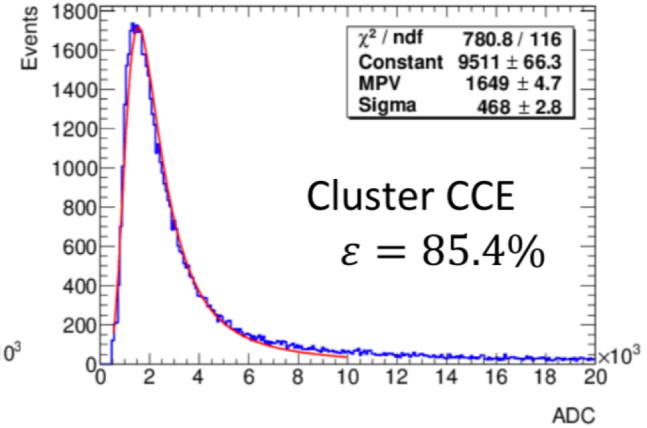
^{90}Sr Radiation test (Preliminary)

L. Chen , H. Zhu

- Use ^{90}Sr to measure the charge collection efficiency for MIP





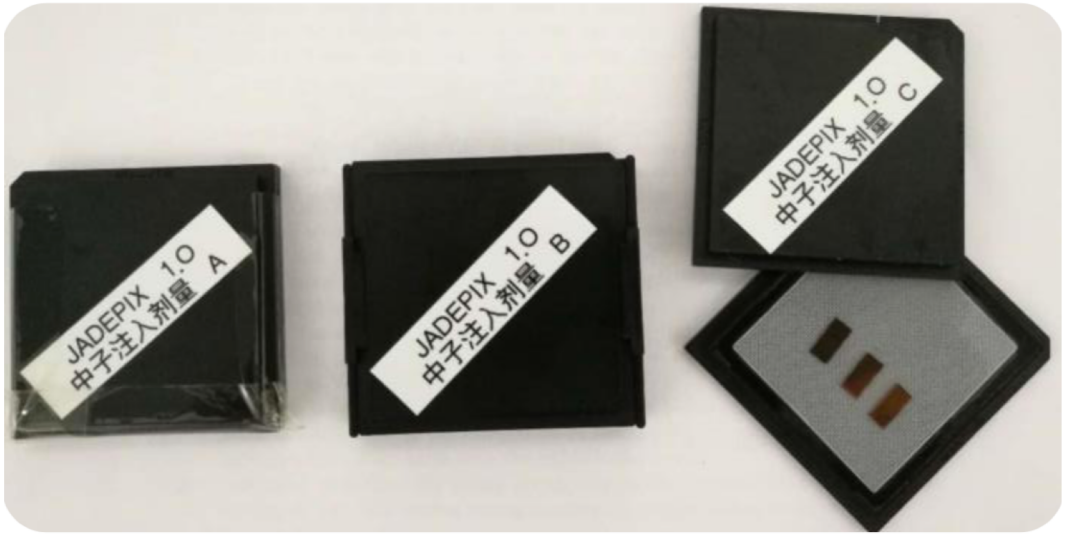


- Cluster with Landau distribution, use MPV for CCE calculation
- Uncertain of radiation angle, will use electron beam for better CCE
- Optimization: Q/C (analog power consumption), S/N (spatial resolution)

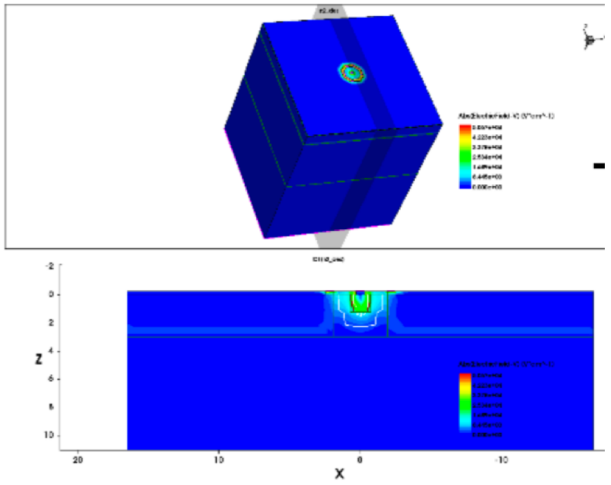
Irradiation with neutron

- Three batches of neutron irradiation with Xi'an pulse reactor : 10^{12}, $5x10^{12}$, 10^{13}.
- Build TCAD simulation with radiation damage model

H. Zhu

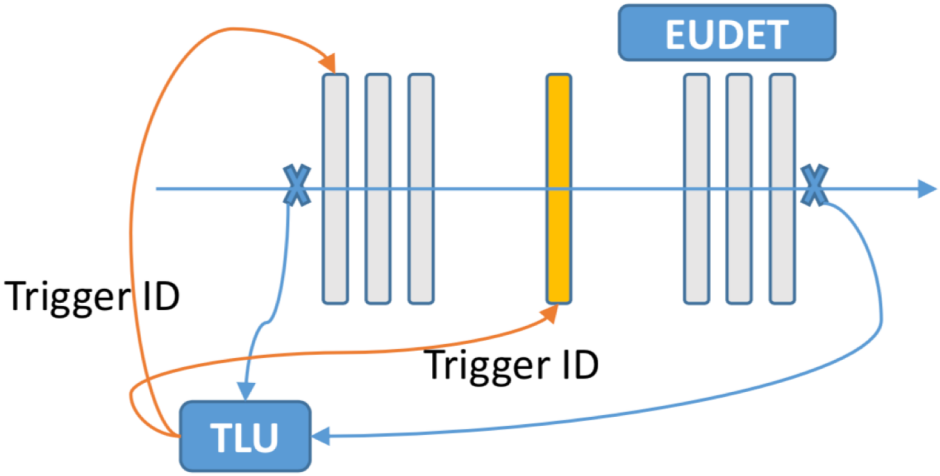


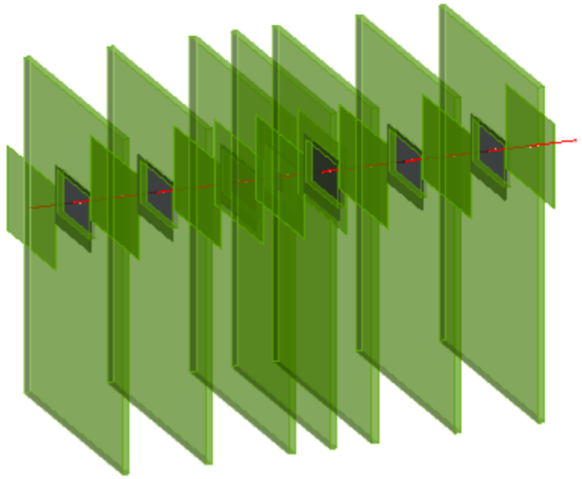
L. Chen



DESY test beam

- Reserved DESY test beam (Aug. 27- Sep. 2, 2018) , characterize pixel special resolution and detector efficiency.
- Preparing: new firmware, EUDAQ plugin, offline reconstruction software, etc.





Summary and outlook

- To fulfill the CEPC physics program, the Vertex detector has to be built with high resolution, low material budget and radiation hard.
- The first pixel prototype – JadePix1 has been built and tested with radiation sources.
- Test beam will be carried out in August for spatial resolution and detector efficiency characterization.