FATIC characterization

(FAst Timing Integrated Circuit)

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Schematic (single channel)

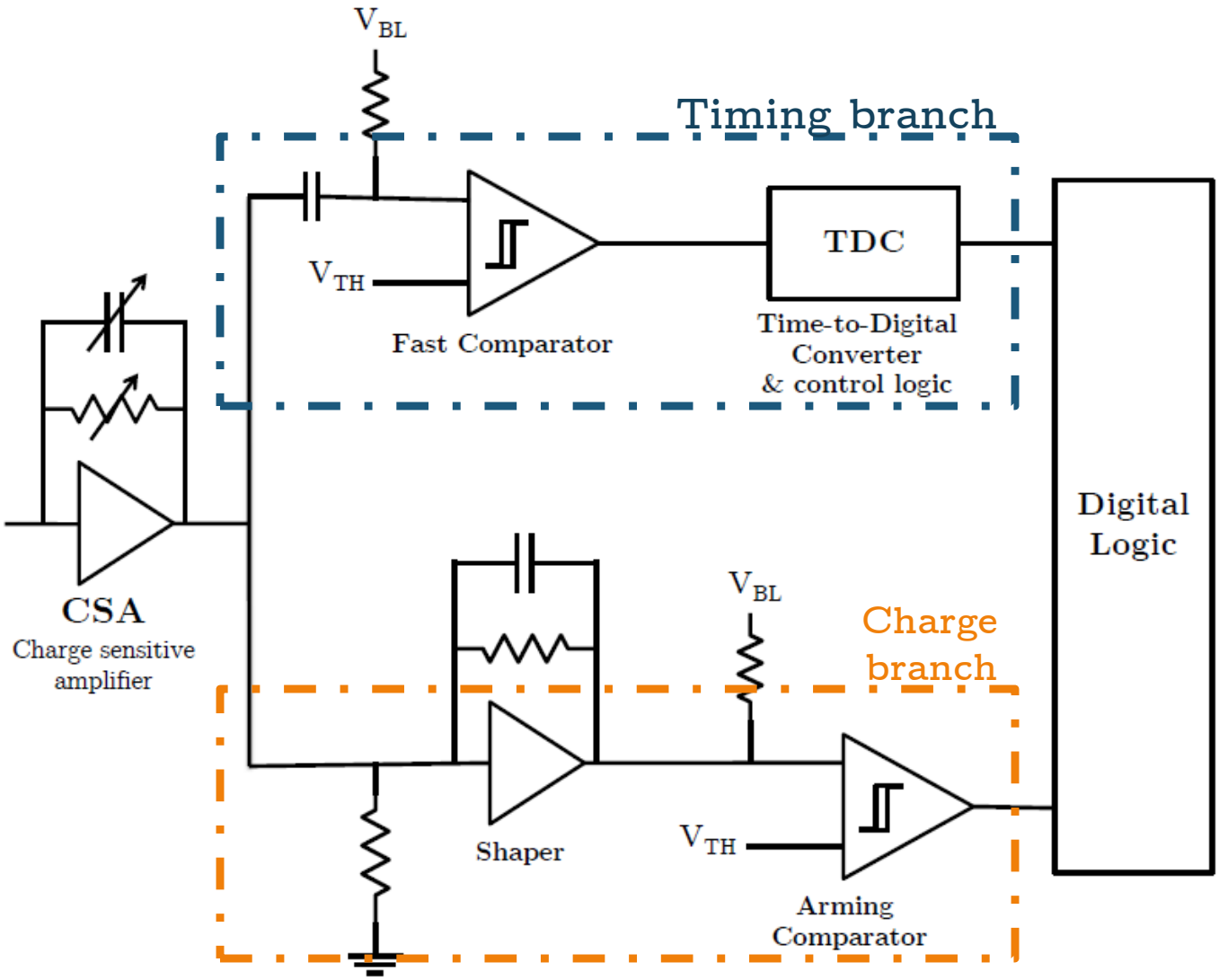
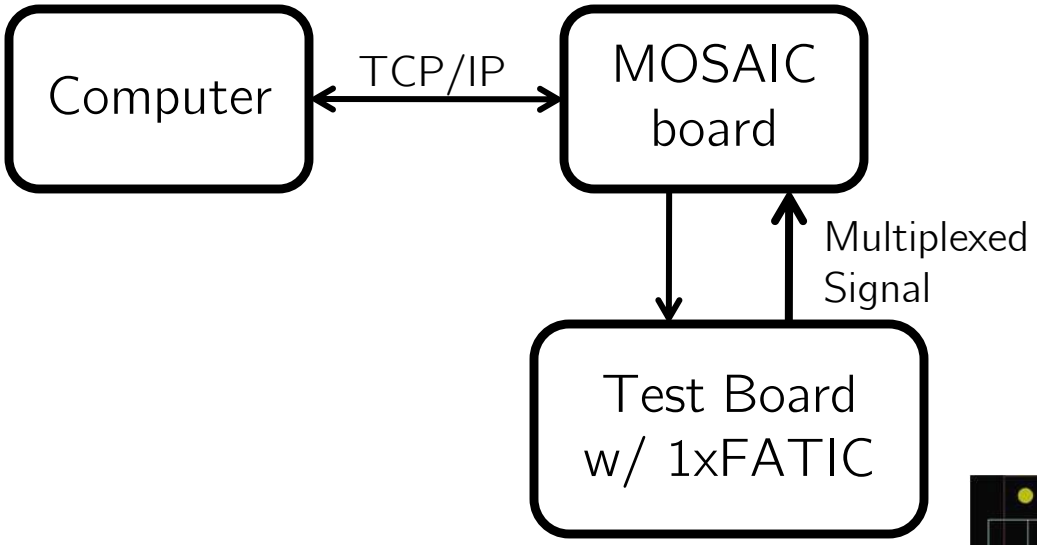


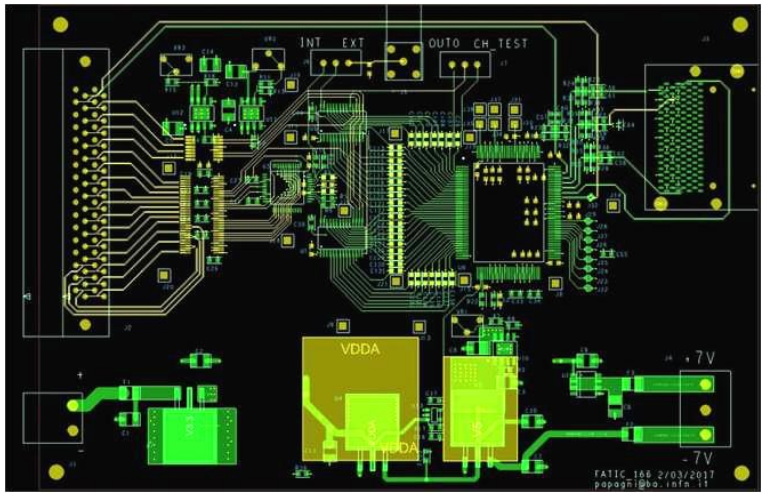
Table 1.1: FATIC features

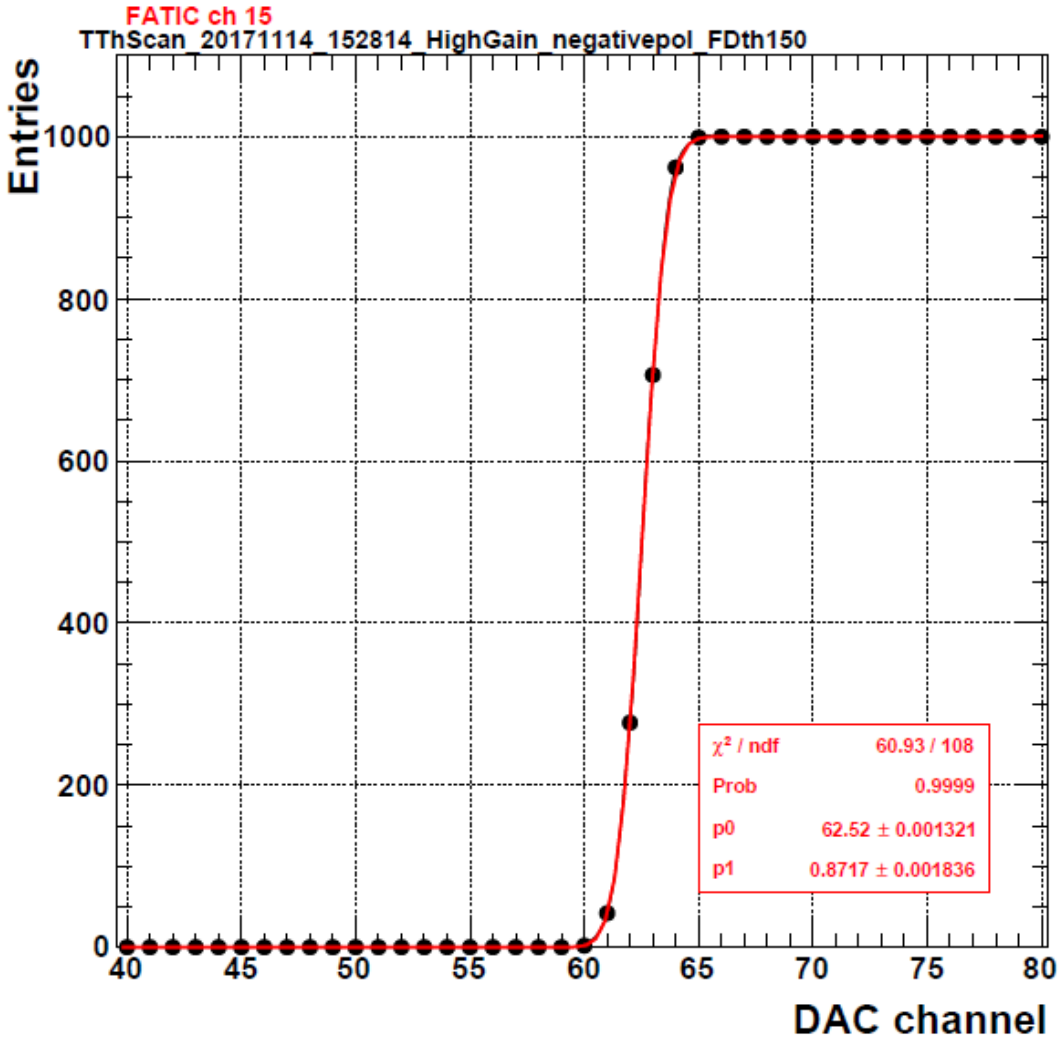
CSA		**TDC**	
Peaking time*	7.3 ns	Resolution	5-bit fine / 16-bit coarse
Time jitter*	300 ps @ 1 fC input charge	Reference Clock	320 MHz
ENC*	18.2e-*Cin (pF) + 235.5e-	Time resolution	100 ps
Current Cunsuption*	1.3 mA	**Shaper**	
Signal Polarity	positive & negative	Peaking time	100 ns
Gain	High gain mode: 50mV/fC	**Fast Comparator**	
	Low gain mode: 10 mV/fC	Threshold	[0 - 76.5]ke-, step 300e-
*simulation in high gain mode w/ Cin = 15 pF		**Arming Comparator**	
		Threshold	[0 - 58.65]ke-, step 230e-

Test Setup



$$Q = 0.1\ \mathrm{mV/unit} * C * \mathrm{ADC\_units}$$
$$C = (1 \pm 0.25)\ \mathrm{pF}$$



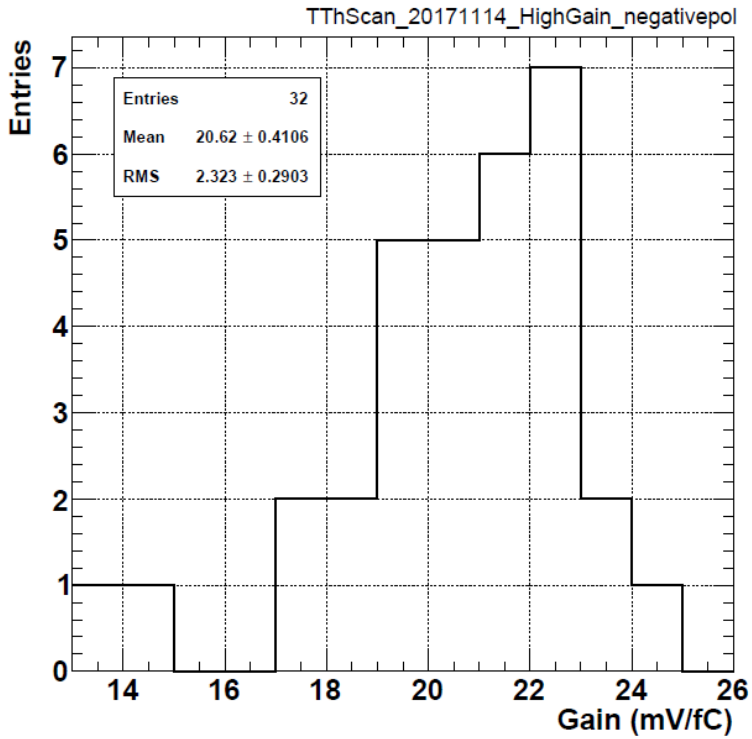


$$\Phi = \frac{1}{\sigma\sqrt{2\pi}} \int_{-\infty}^{x} e^{\frac{-(z-\mu)^2}{2\sigma^2}} dz =$$

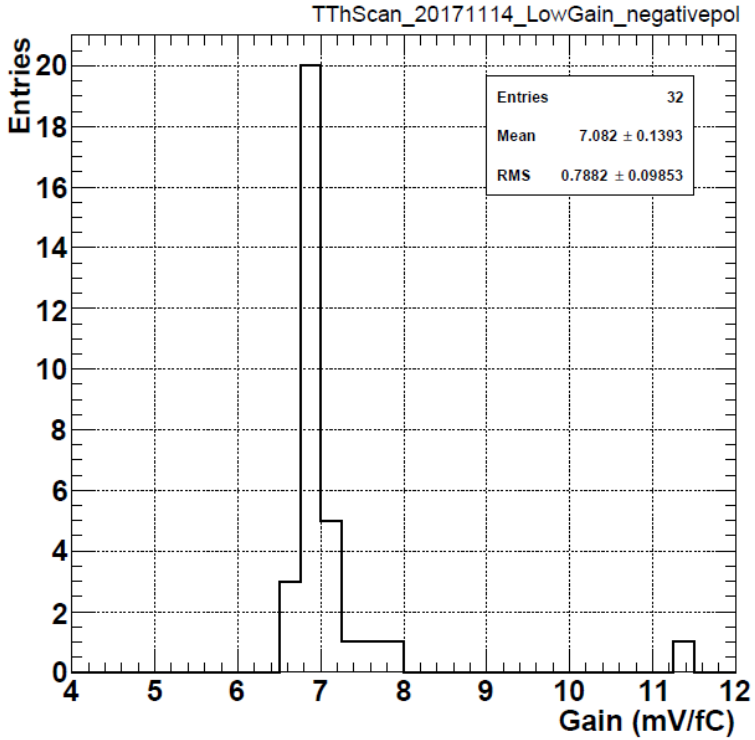
$$= \frac{1}{2}\left[1 + erf\left(\frac{x-\mu}{\sigma\sqrt{2}}\right)\right]$$

Single channel response fitted with function Φ.
CSA in High Gain Mode. Arming comparator disabled.

CSA Gain



(a) CSA in High Gain mode



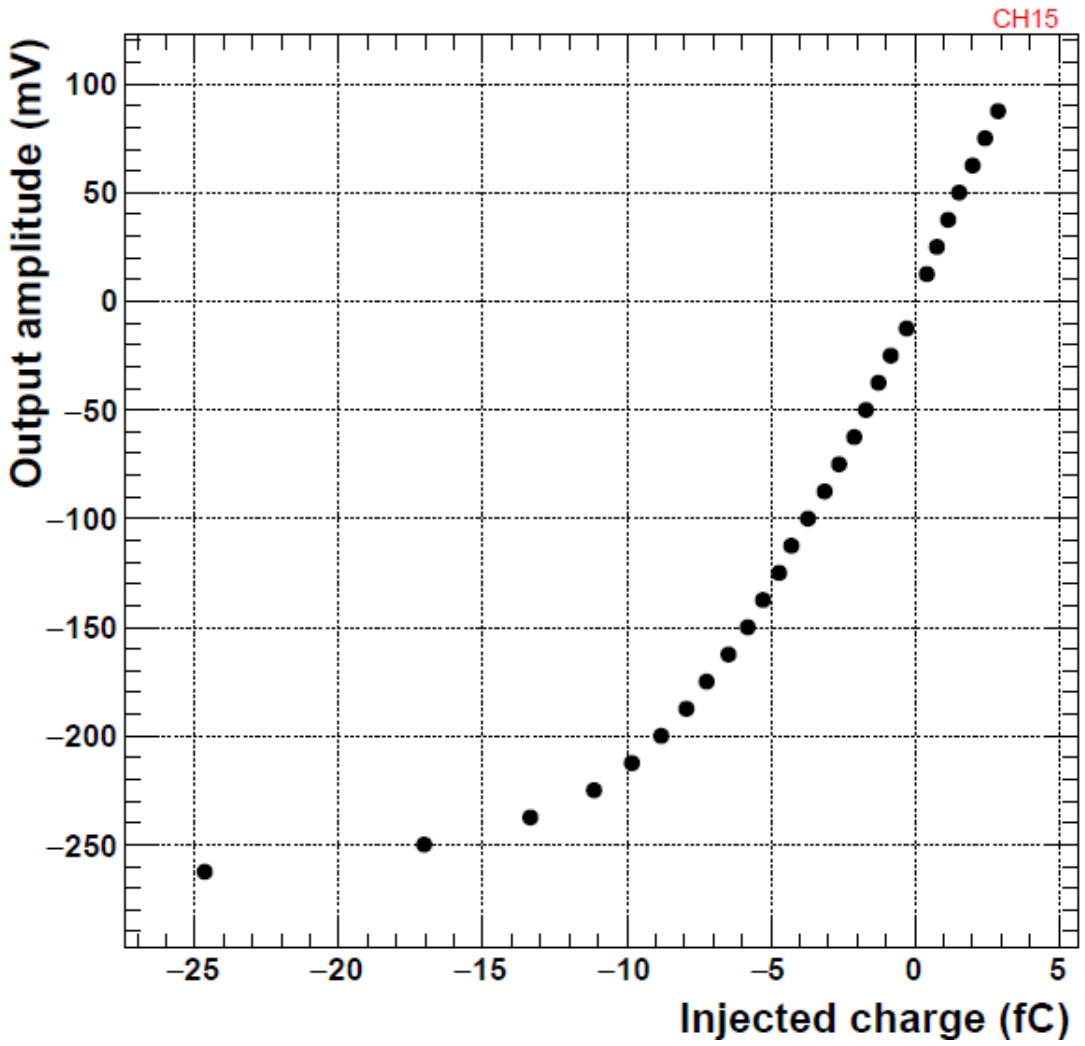
(b) CSA in Low Gain mode

$$G = \frac{Th_1 - Th_2}{\mu_1 - \mu_2}\left(\frac{mV}{fC}\right)$$

$$\langle G \rangle_{\text{high gain}} = 20.62\frac{mV}{fC} \pm (0.41\frac{mV}{fC})_{stat} \pm (3.56\frac{mV}{fC})_{sys}$$

$$\langle G \rangle_{\text{low gain}} = 7.082\frac{mV}{fC} \pm (0.139\frac{mV}{fC})_{stat} \pm (1.24\frac{mV}{fC})_{sys}$$

CSA linearity



Single channel response varying the injected charge.

Note:
Baseline ≈ 220 ADC units

Arming comparator

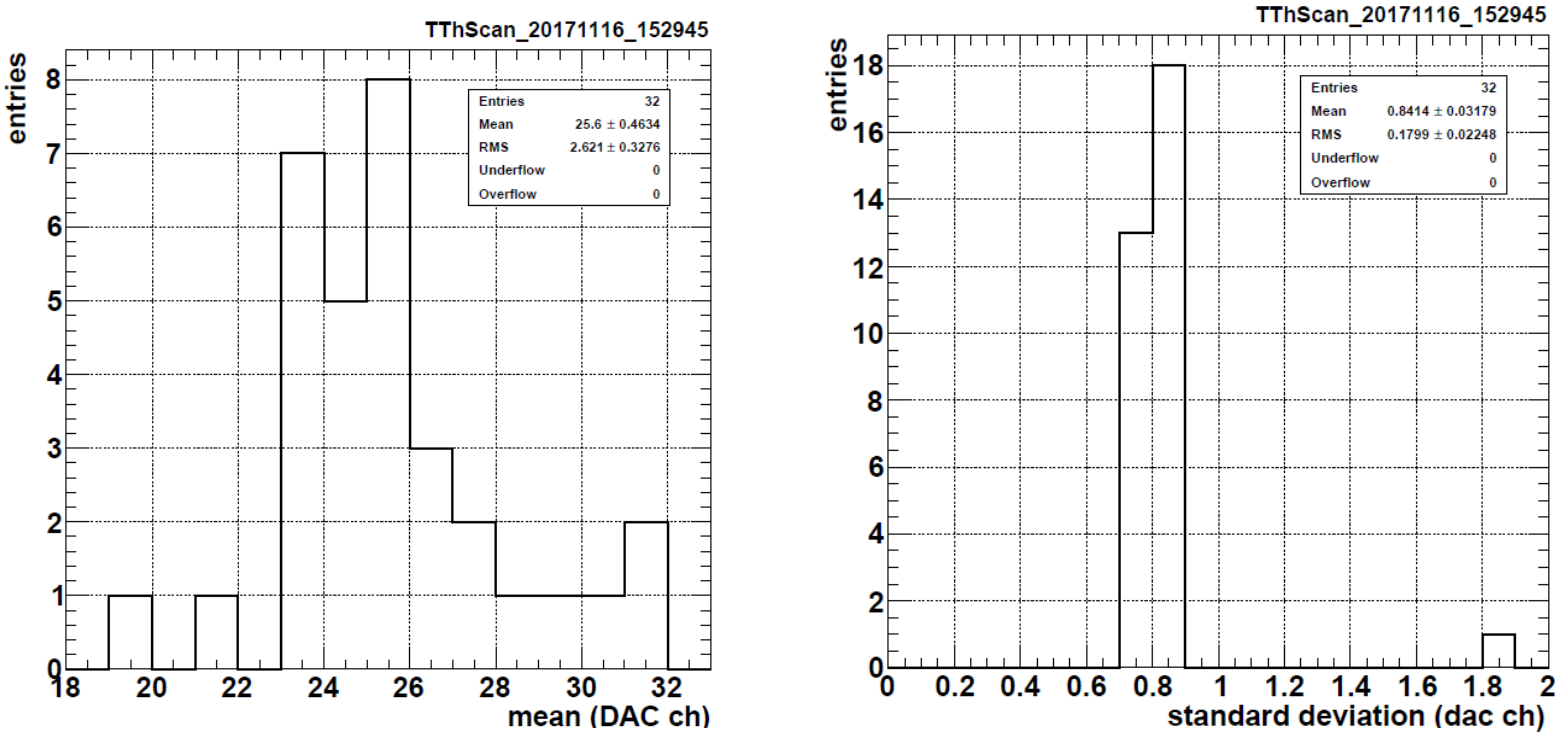
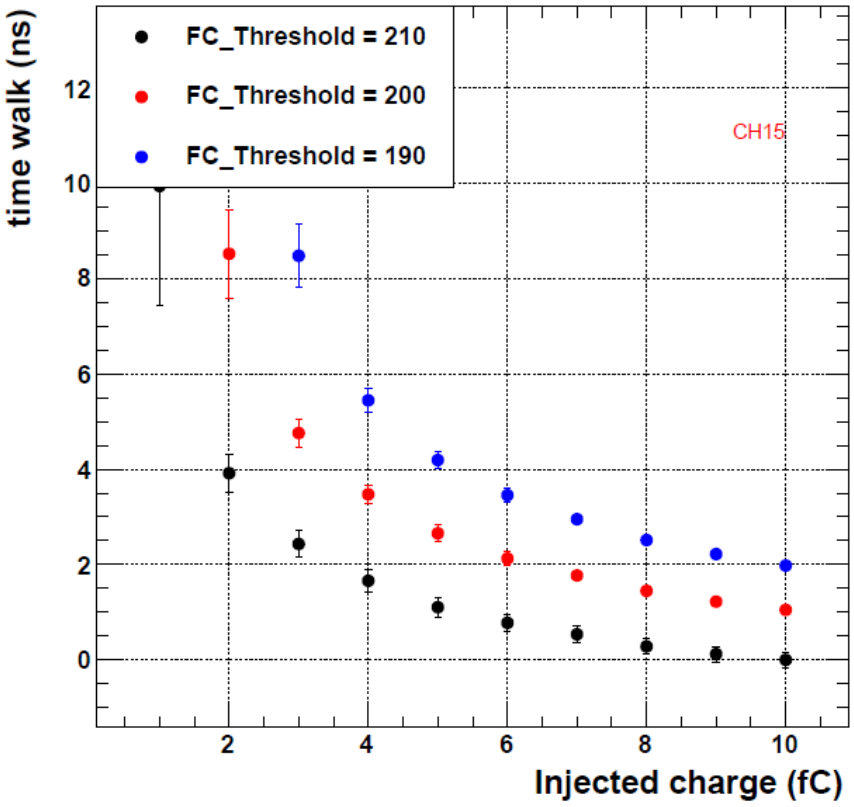
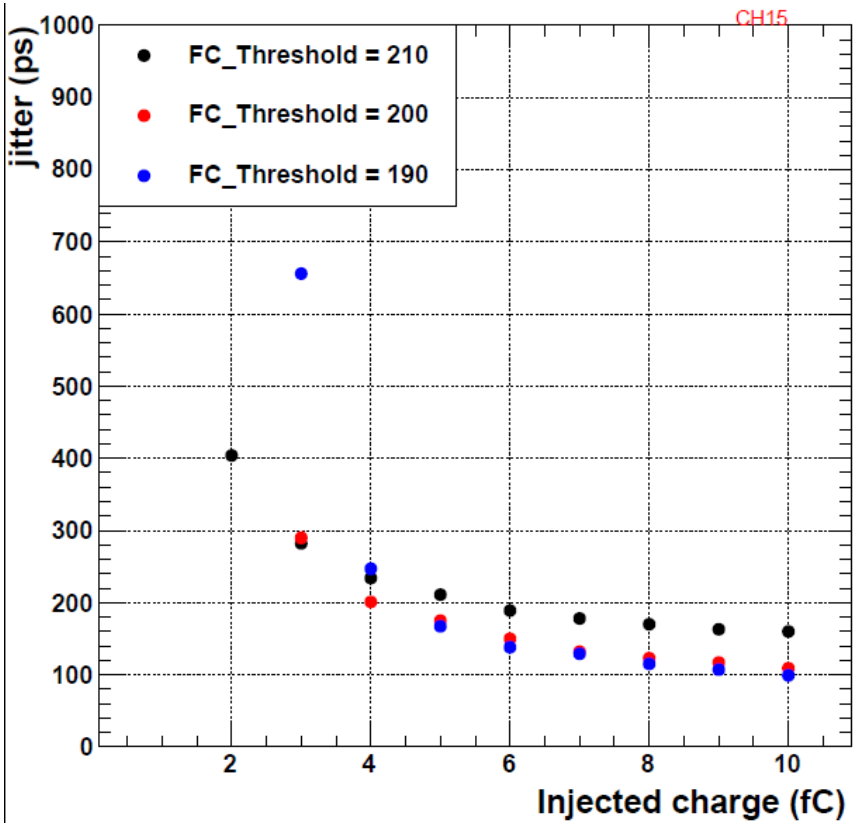


Figure 1.9: μ and σ fit values for all channels. CSA in High Gain mode, Arming Comparator enabled, FC Threshold = 200, AC Threshold = 40 ($LSB_{ACth} = 2.3mV$)

$$\sigma_{timing} = 1.026 \pm 0.045$$
$$\sigma_{arming} = 0.841 \pm 0.032$$
$$\%ENC_{reduction} = [\sigma_{timing} - \sigma_{arming}] \,/\, \sigma_{timing} \approx 18\%$$

Timing





- Input trigger and the fast-OR signal sent to the scope
- Average delay = time walk
- Delay std deviation = time jitter

Upgrade ideas for FATIC v.2

- Internal circuit for threshold matching
- Investigate CSA gain (lower than expected)
- Symmetric dynamic for positive and negative signals