Assembly and preliminary tests on the new prototype for the fast timing mpgd (FTM)

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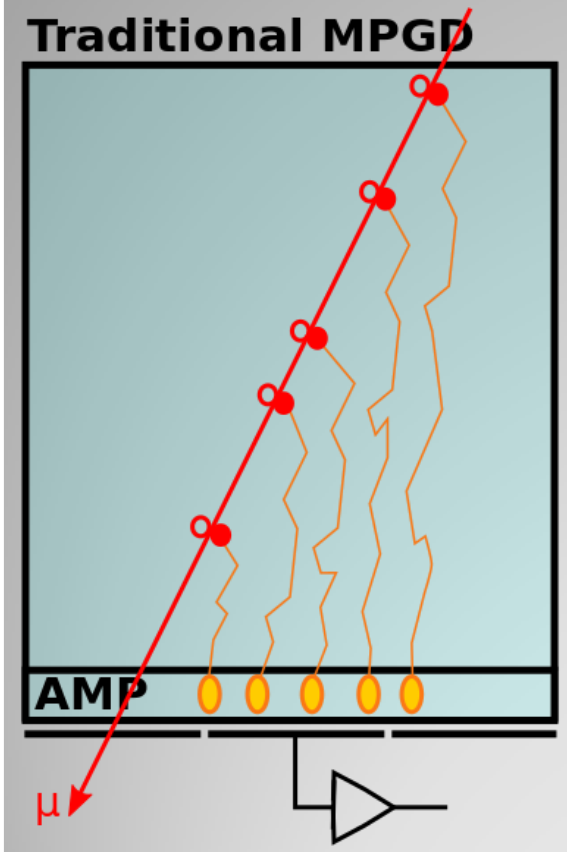
Fast Timing MPGD Principle



σ_t driven by distance fluctuactions.

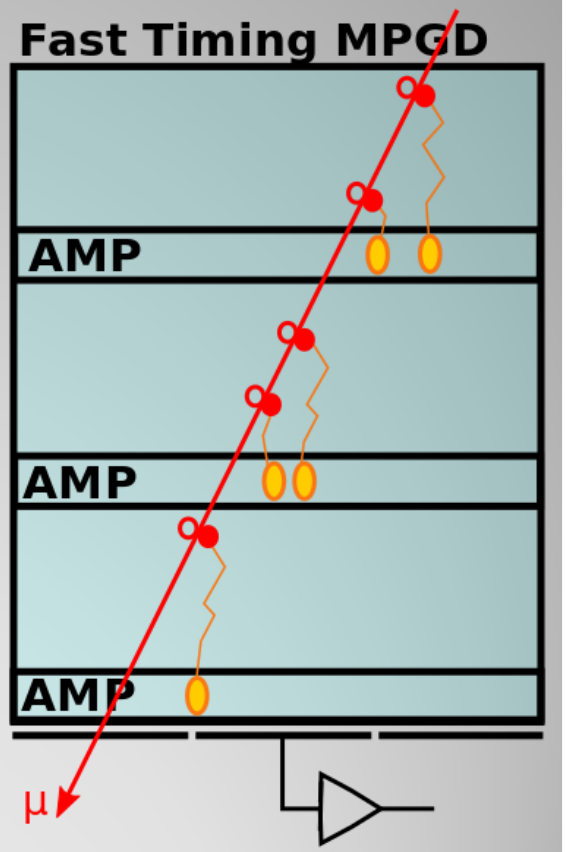
$\sigma_t \propto 1/\lambda v_{drift}$

λ = # primary cls

electron-ion pairs created **close** to the amplication structure result in fast signals

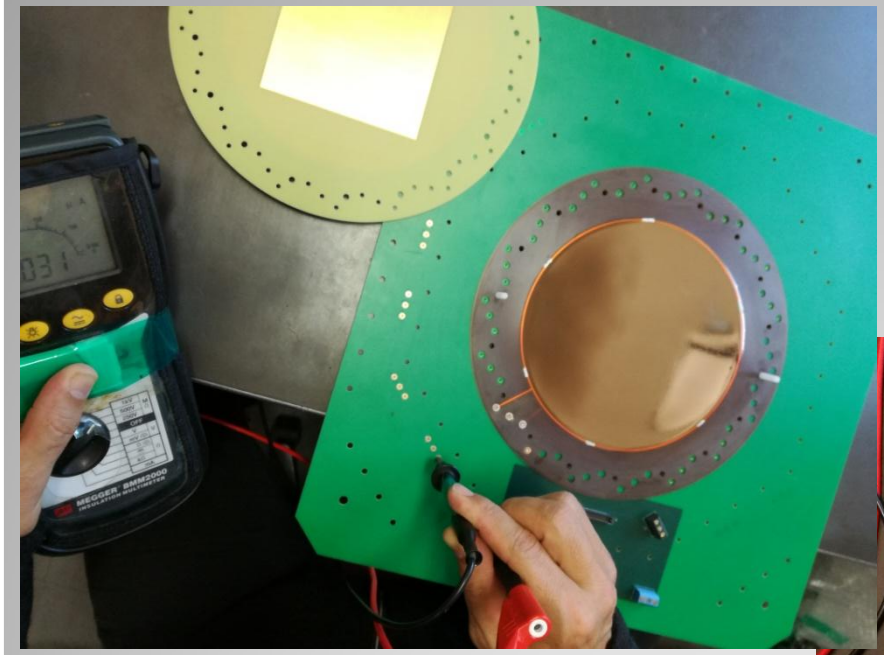
Fast Timing MPGD: split drift volume in **N** layers, each with own amplication structure

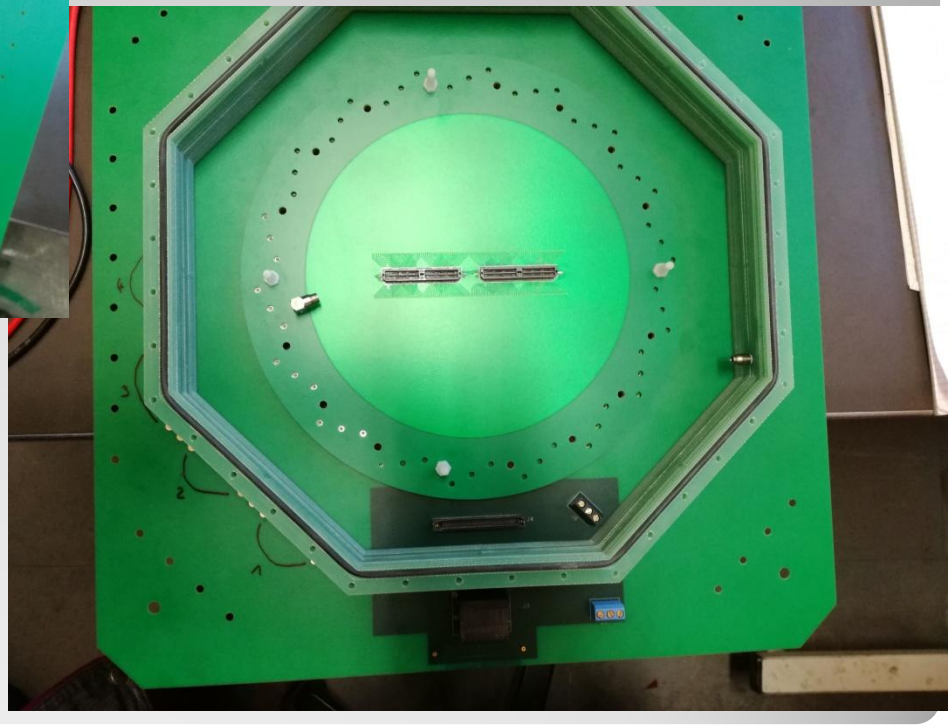
$\sigma_t \propto 1/\lambda v_{drift}$ **N**



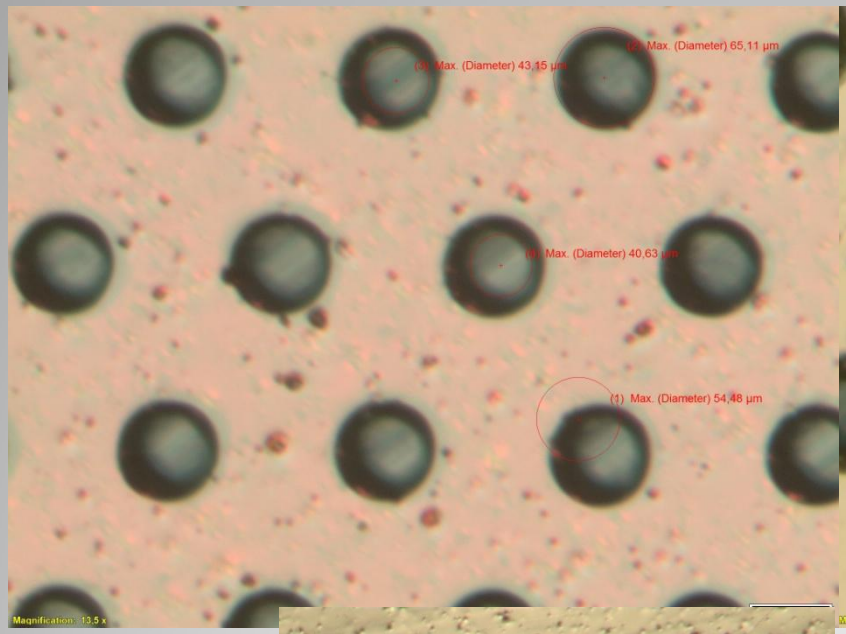
- Resistive structure → transparency → signal from any layer induced in readout
- Time resolution should improve with **N** = number of layers

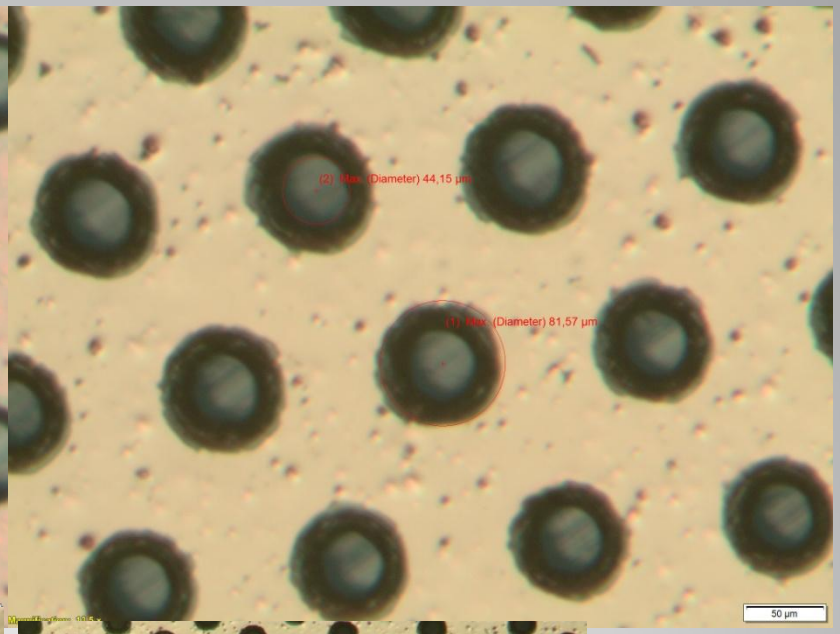
FTM v4: assembly

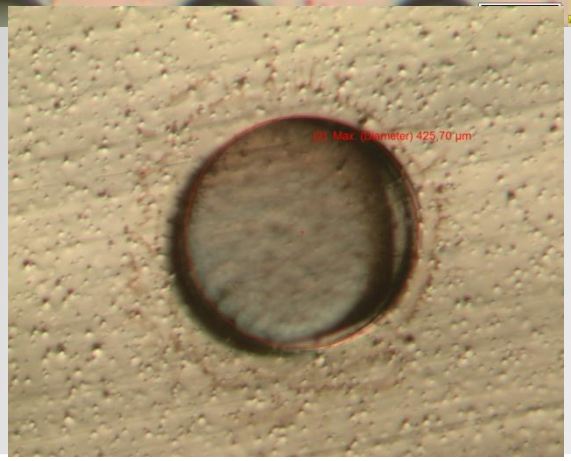


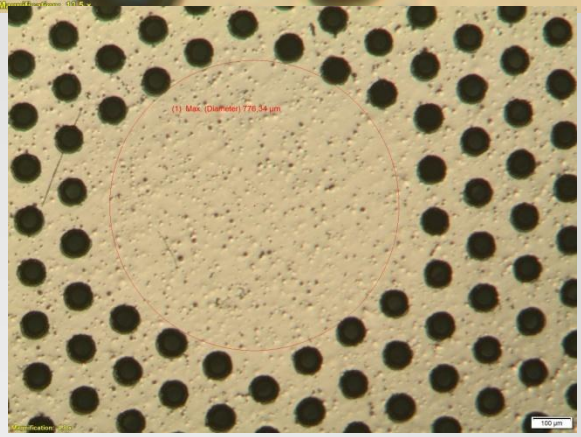


FTM v4: foils

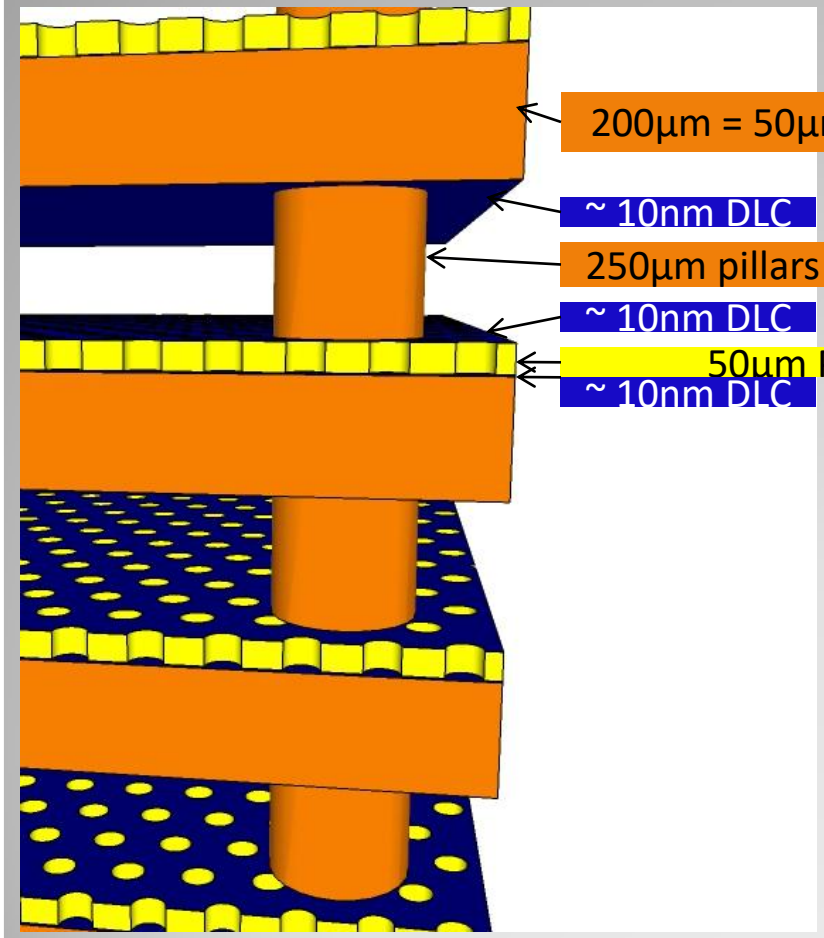

(3) Max. (Diameter) 43,15 µm
(2) Max. (Diameter) 65,11 µm
(4) Max. (Diameter) 40,63 µm
(1) Max. (Diameter) 54,48 µm
Magnification: 13,5 x


(2) Max. (Diameter) 44,15 µm
(1) Max. (Diameter) 81,57 µm
50 µm

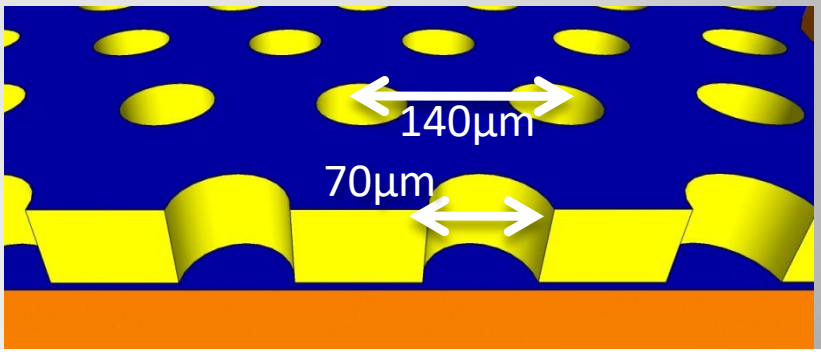

(2) Max. (Diameter) 425,70 µm


(1) Max. (Diameter) 776,34 µm
100 µm

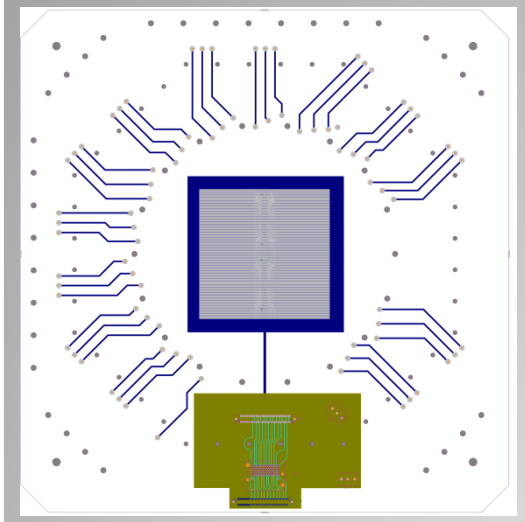
FTM v4: design



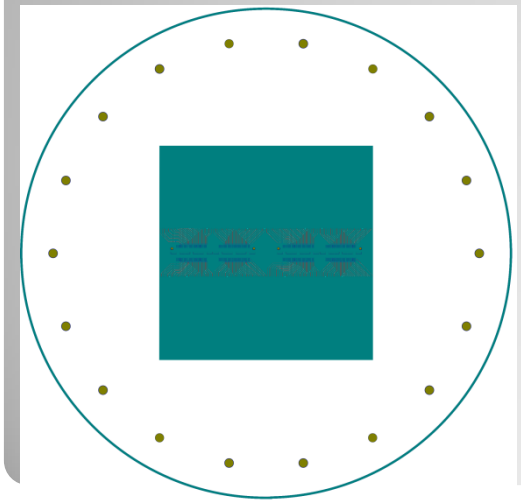
- 4 independent drift – amplification layers
- 250µm drift gap
- "GEM-like" amplification foils



FTM v4: specs

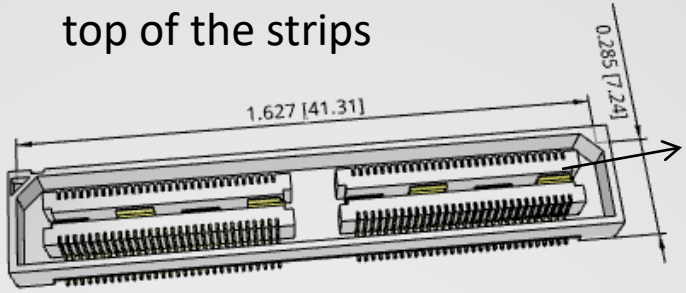


Bottom PCB design



Top PCB design

- **Modular design**
- Forced **gas circulation** through all layers
- Signals are read capacitively both on top and bottom, each **readout** board has 200 strips of 500um width
- Preserve fast pulse: Panasonic →**SAMTEC**
  - QSH-060-01-L-D-A high-speed connector
  - massive central ground pin close to each channel
- **Reduce noise** pick-up:
  - Connector directly on middle of strips → no long vias
  - Large ground plate, grounded connectors
  - Discriminators (fatic chip) as close as possible to the readout strips; front end board directly mounted on top of the strips



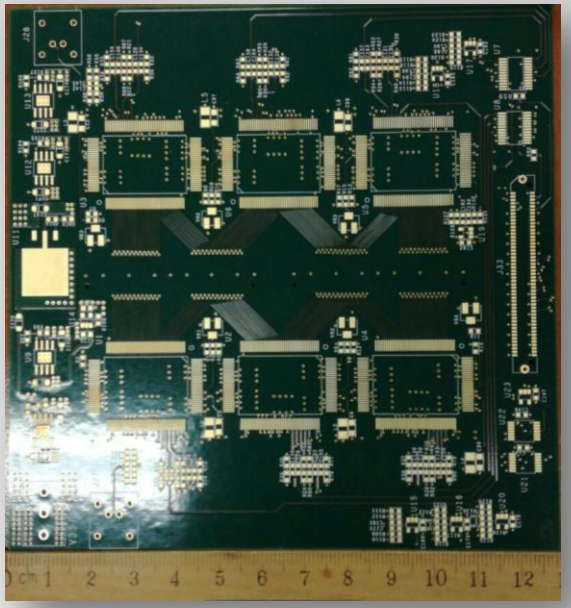
SAMTEC QSH-060-01-L-D-A (120 pins)

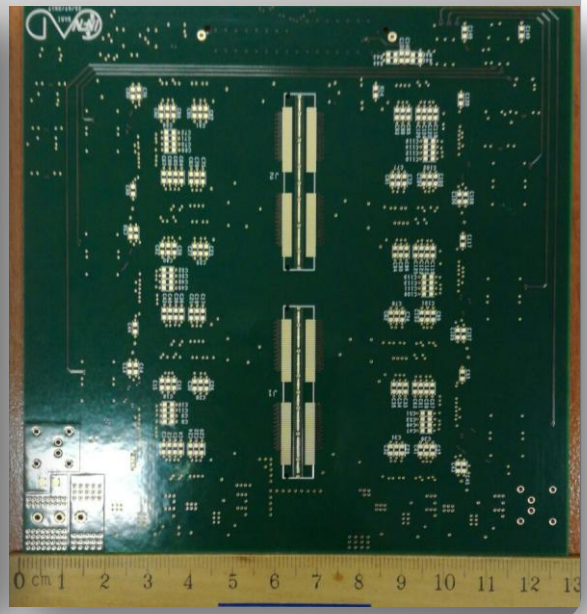
FTM v4: frontend and DAQ

- **Fast Timing Integrated Circuit (FATIC) chip:** 32 channel CSA + Comparator + TDC (100ps resolution)

CSA: high gain 50mV/fC;
low gain 10mV/fC;
risetime of 7.5ns

- **High speed Digital output** (320 Mbps): Frontend board mounted on top of connector (in gas box) containing 6 FATIC chips (low noise fast discr.) -> 182 channels
- **DAQ** with MOSAIC board (INFN Bari design)





Test Setup

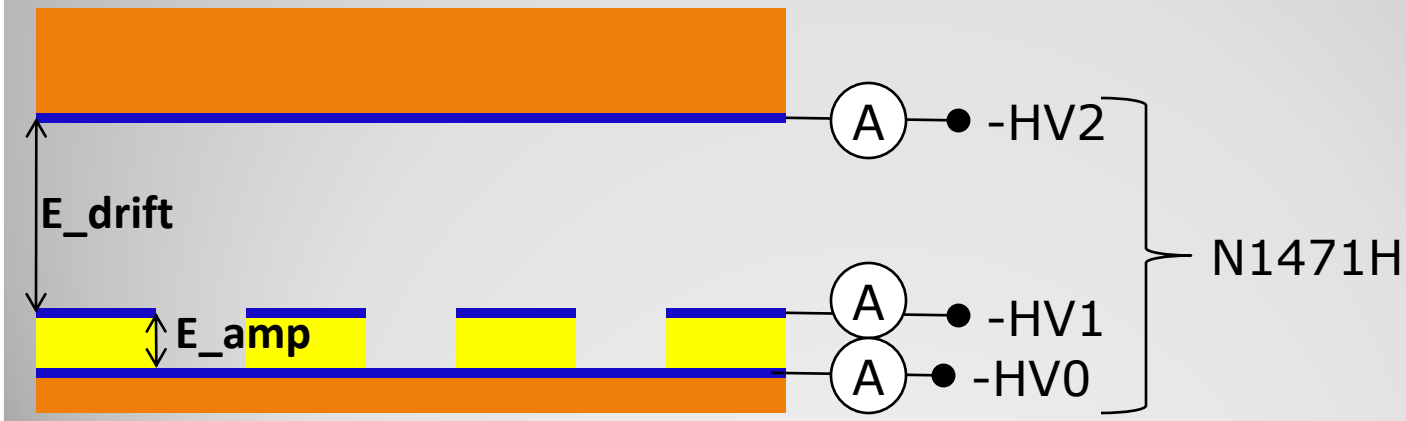
- Gas mixture: Ar/CO2 70/30
- HV Power supply w/ high resolution current monitoring (50pA, e.g. CAEN 1471H)
- Source: X-ray tube

Single layer:

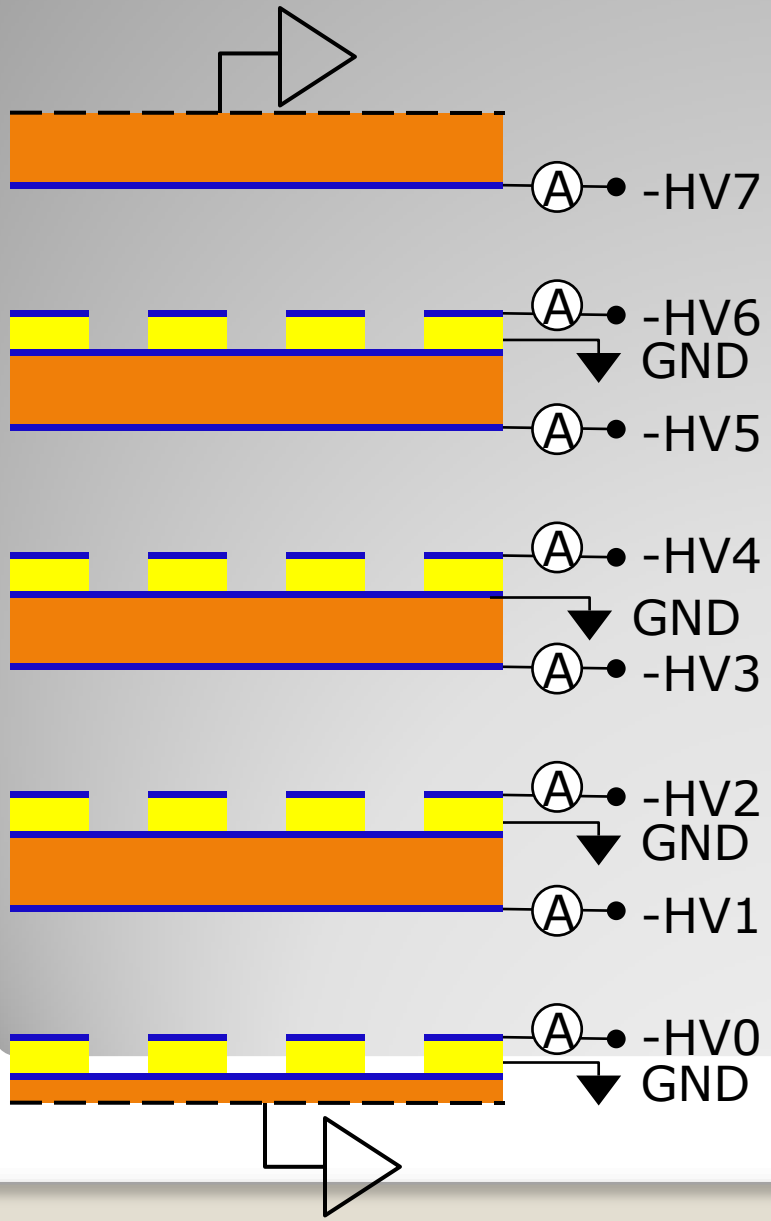
- HV slow ramp up (→ E_drift = 3kV/cm, E_amp = 10 ÷ 100kV/cm
- Linearity test (All currents vs source power)
- Gain estimation

Repeat for all layers

$$G = \frac{I_{ON} - I_{dark}}{I_{ON,drift} - I_{dark,drift}}$$



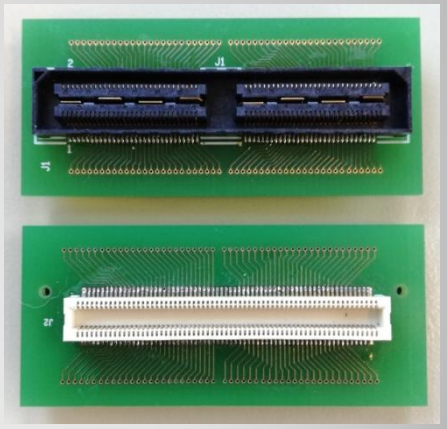
First tests without frontend board



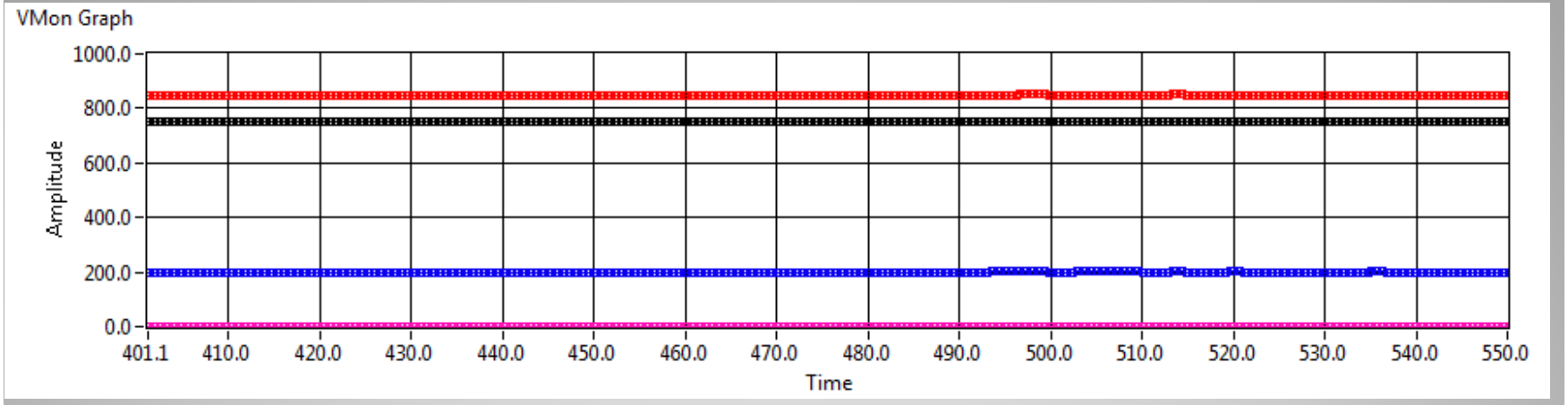
All layers powering scheme

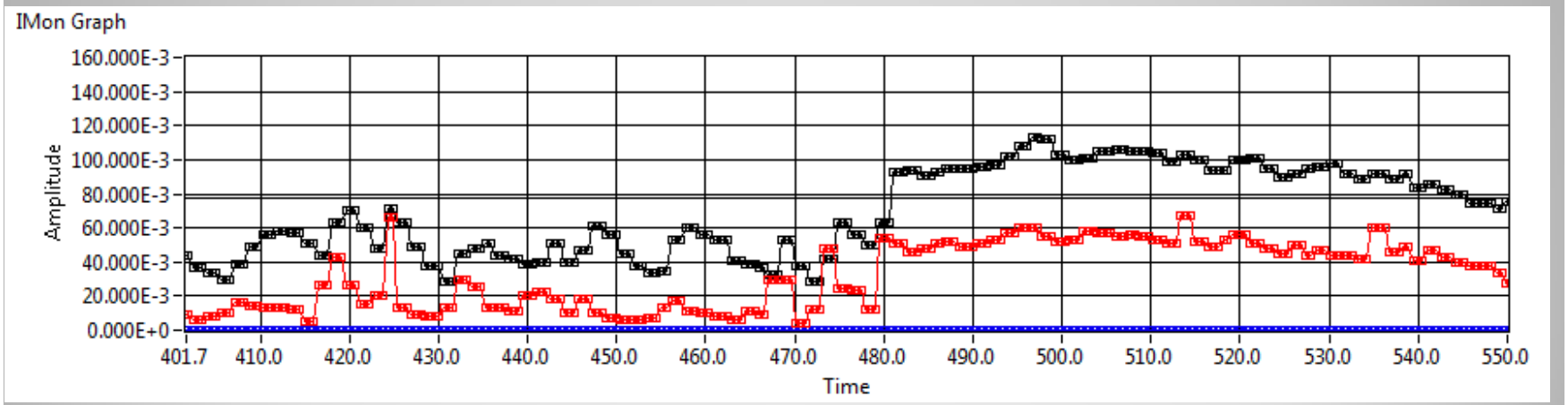
In order to see the signal from one layer or a group of layers:

- SAMTEC-to-Panasonic→ Panasonic-to-Lemo →pre-amp →scope
- Signal = OR of all the strips at the bottom



FTM powering



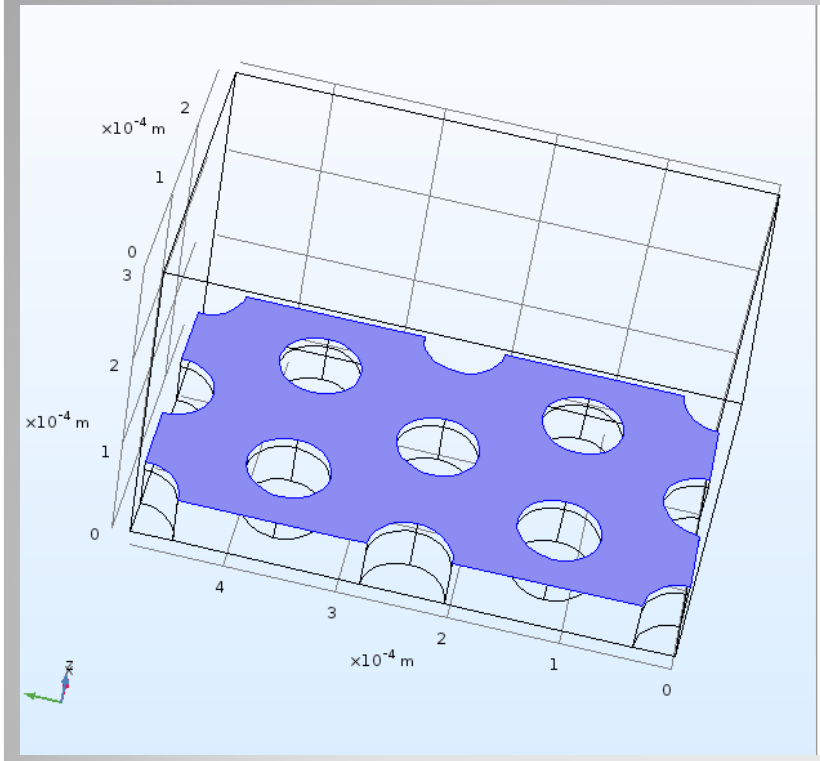


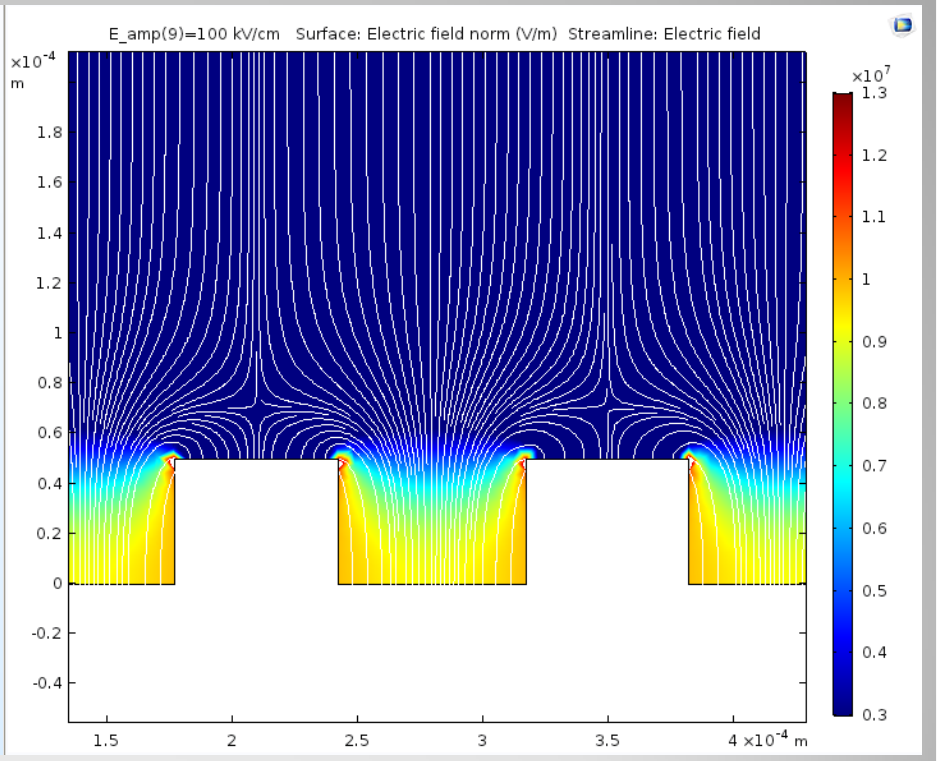
- Current fluctuations (≈ 10 nA) with peaks of μA
- 4° layer is drawing current (N1471H overload)

Backup

- Gain estimation
- E_Field simulation

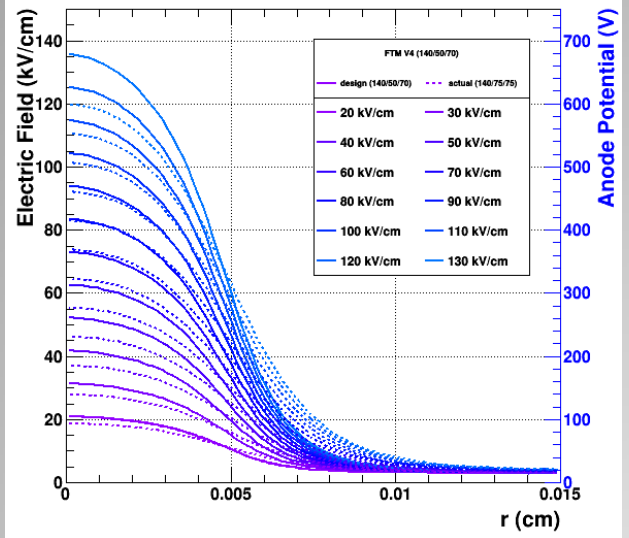
FTM v4: E field simulations



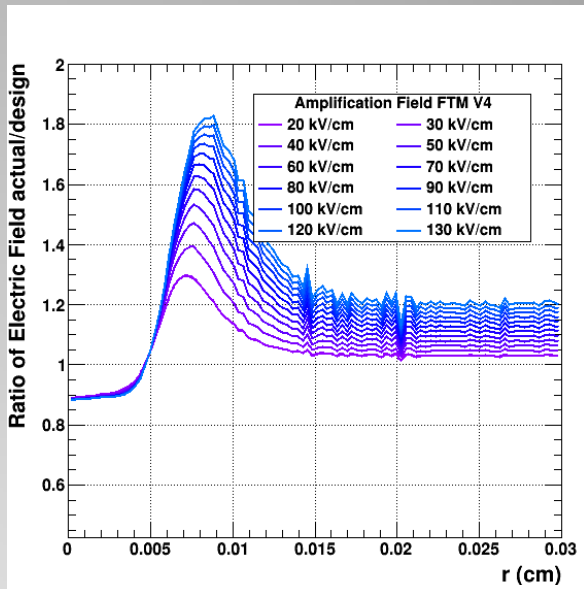


FTM v4: Gain estimation

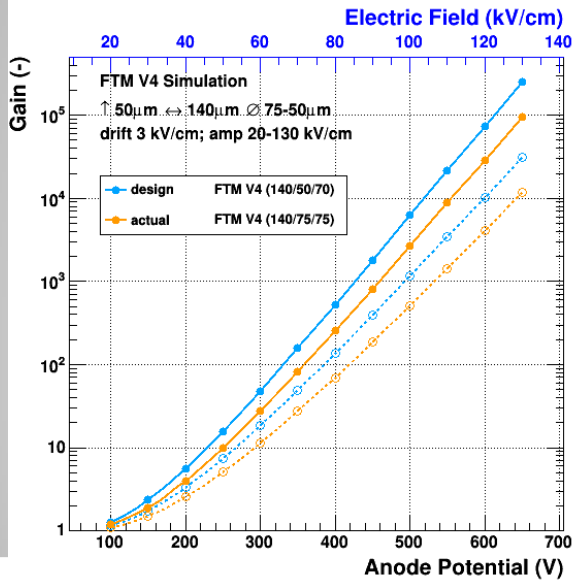
E Field in Center Hole



Ratio of E field Hole



Gain Estimate



Ratio of Gain