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Study of I-V curves on 2D simulations and update on the 3D one



Where we were

- a first 3D geometry designing;
- a study of the 2D simulations with optical beams;

- labVIEW activities.



Where we are

- a new geometry more similar to the real one;
- a study of the 2D simulations in the static case;
- a first study of 3D simulations with optical beams.





Statical study of 2D devices

A study of the statical electrical response of 2D devices of the same structure as in other presentations was performed. V_{Gs} at the silicon dioxide level V_{GS} gate ambiguity: two routes taken \overline{V}_{GS} at the bottom contact level

Graphical explation of $V_{\rm GS}$ and $V_{\rm TS}$



I-V curve choosing V_{GS} at silicon dioxide level



I-V possible interpretation

The strange shape of the I-V curve, with $V_{TS} = 0$ and $V_{GS} = 20$ in the case examined can be due to the presence of the kink-effect [1].







Quantum capacitance

The asymmetry in the plot is due to an asymmetry in the values of V_{GS} respect to the zero of V_G (graph obtained using formula developed by Thiele et al.).

$$V_{ch} = \frac{-\frac{C_{ox}}{2} + \sqrt{(-\frac{C_{ox}}{2})^2 + (V_{GS} - V(x))C_{ox}\alpha}}{\alpha}$$





Quantum capacitance

There is a good accordance of the quantum capacitance value versus V_{GS} with the results founded in literature if V_{GS} is chosen as the external one. The plot below was obtained using V_{GS} equal to $V_{GS-external}$



$I_{DS} - V_{DS}$ characteristic

Using V_{GS} as the average value of the potential at the level of silicon dioxide below the graphene's layer was obtained the I-V curve at various V_{TS} external. Now the saturation seems to be achieved for V_{TS} greater than 1.



$I_{DS-}V_{DS}$ after depleting $(V_{GS}=75V)$

The general behavior seems to respect the results

obtained in the article in the reference[2]. The graph

on the right correspond to a p-channel G-FET.



Charge neutrality point

In an ideal graphene's layer the Dirac point coincides with the point where the concentration of free carriers in the material is 0. In a real graphene's layer since the presence of defects the Dirac point is the position where the concentrations of carriers of n and p type coincide and is called CNP. This position can be determined in principle changing V_{top} and looking at the resulting current

$V_{_{TS}}$ vs $I_{_{DS}}$ at $V_{_{GS}}$ fixed at 75V

These plots don't coincide with the results obtained in the article provided by Thiele et al. . That can be an effect due to our different geometry respect to the one used in the article: our source contact seems to "shield" the negative values of V_{TS}



V_s effect?

 V_s contact in this case may not allow the potential below graphene's layer to go to high negative values. In the geometry presented in the article this is not expected since it's a standard G-FET as shown in the sketch on the right. The electrostatical potential in our device at V_{TS} =-5V is shown on the left (dioxide thickness 100 nm).





3D devices update

A new geometry more correspondent to the one will be tested in lab has been designed. The greater difference is the presence of two regions at top where is present an implant of p+ carriers.





Mesh refinement

Mesh was chosen in order to be more dens in regions of interest, not too dense in other points in order to grant convergence in reasonable time (total mesh elements around 220.000).



Optical beam study

As in the 2D case an optical beam was used to induce the concentration of carriers in the bulk expected for a MIP particle. The interest on the 3D study is necessary each for a realistic optical beam excitation and for 2D Extrusion: Full 3D **Unphysical Track** Realistic Track taking into account border effects.

Optical beam excitation

An optical source was used in order to induce carriers in the silicon bulk. In the figure below the optical beam is hitting the device at position ($0\mu m$, 150 μm , -20 μm).



Space charge

The space charge at T=1ns (on the left) after the beam hit and after 5ns (on the right) is reported below.





Convergence time

The convergence in the region near the middle of the device requires a lot more time than in other positions due to the electrical fields of the two top p+ implants that creates two competing electrical field. The time for a complete simulation (from steady situation to the steady one again) is of the order of 14h for a hit in the middle position of the device and of around 5h shifting 10-20 micrometers from the previous case.

Voltage increasing trough time

The voltage in the channel seems to have the expected behavior after the optical beam hit with a maximum value after around 6ns.



BACK-UP



I-V in the depletion region









Zoom at $V_T = 10$ and $V_T = -10$ -160 -150 Electrostatic Potential (V) 1.000e+01 8.338e+00 6.675e+00 5.013e+00 -140 3.351e+00 1.689e+00 2.631e-02 ° X 10 -20 -10 20 -150 Υ ElectrostaticPotential (V) -145 4.847e-01 -1.359e+00 -3.202e+00 -140 -5.045e+00 -6.888e+00 -8.732e+00 -1.057e+01 -135

-20

-10

0

10

20

I-V curve for V_{D} that goes from -5V to 5V I_{DS} vs V_{DS} at V_{G} =75V and V_{D} =variable 100 l_{os} [μ A] 80 60 40 20 0 -20 -40 -60 -80 -100 5 V_{DS} [V] -3 -2 0 3 4



Missing plot

Last time I didn't achieve to show the plot about the delta I/I_0 for the 2D simulated prototype. The results are similar to the one founded in past works.





3D device

Device designed is constitute by:

- 300 micrometer of Silicon n doped;
- 100 or 300 nm of Silicon dioxide;
- 4 graphene layers 0.05 nm thick (base sizes: 10x10, 20x20, 30x30 micrometer²);
- 2 p+ top implant distant 4 micrometer from the 2 adjacent graphene's layers.

Sentaurus workbench

Sentaurus workbench is a program provided by synopsys that allows to use consequently the three main family of Sentaurus TCAD that are mostly used: SDE, SDEVICE and SVISUAL. In principle is possible to use also matlab in order to directly analyze directly results



Sentaurus Workbench environment

In the SWB environment developed is possible to choose in a direct way the thickness of silicon dioxide and of the graphene's layer without directly manipulating the code.



	SDE			SNMESH	SH SDEVICE		No Variables		36	
		GW	GI	tox			Vg			
1 2 3 4 5 6 7 8 9 10 11 11 12 13 14 15 16 17 18 19 20 21 22	[n2]:	[n4]: 10	[n24]: 10	[n1]: 0.1	[n64]:	[n5464]:	[n144]: 0 [n5504]: 10 [n5784]: 20 [n6064]: 30 [n6344]: 40 [n6624]: 50 [n6904]: 60 [n7184]: 70 [n7464]: 80 [n7744]: 90			0 720
				[n44]: 0.3	[n65]:	(n5465):	[n145]: 0 [n5511]: 10 [n5791]: 20 [n6071]: 30 [n6351]: 40 [n6631]: 50 [n6911]: 60 [n7191]: 70 [n7471]: 80 [n7751]: 90 [n8031]: 100			
23 24 25 26 27 28 29 30 31 32 33			[n25]: 20	[n6]: 0.1	[n66]:	[n5466]:	[n146]: 0 [n5518]: 10 [n5798]: 20 [n6078]: 30 [n6358]: 40 [n638]: 50 [n6918]: 60 [n7198]: 70 [n7478]: 80 [n7758]: 90 [n8038]: 100			
34 35 36 37 38 39 40				[n46]: 0.3	[n67]:	[n5467]:	[n147]: 0 [n5525]: 10 [n5805]: 20 [n6085]: 30 [n6365]: 40 [n6645]: 50 [n6925]: 60			2

Droject Lochestule

Details on the Mesh

The mesh defined is more dense in the regions of the contacts and of the graphene's layers where an accurate measure is required. In the Silicon bulk the average element has a size 10-20 times grater than in the region of interest.

Problems using V_{GS} at the contact position

1) current between Drain and Source became independent on the Silicon thickness;

2) $1/v_{sat}$ integrated in V could become higher to L of graphene giving as a possible result a negative current between drain and source.

A possibility could be using V_{GS} as $V_{GS} - V_{GS0}$ where V_{GS0} is calculated at Dirac points (it seems the approach in the article provided by Meric et al. [1]).

Depletion voltage

The depletion voltage for a resistivity of $6k\Omega cm$ and a silicon thickness of 300 mµ is expected to be of the order of 20V in our case that resistivity is for a n implant in the bulk of 7.10¹¹ [1/cm³] carriers. Since there are other implants the complete depletion is reached for V=70-80V in simulations. That can be corrected adding all the correct values of doping used in the real devices.

Resistivity relation with carrier density

The relation between resistivity and carrier density for silicon devices n and p doped is well known. A plot of this is reported on the right.



Resistivity and $V_{\mbox{\tiny depletion}}$

For n and p type doped materials there is a correlation between the depletion voltage and the resistivity of the material. In our case V_{bi} has a lower value respect to the other quantities and can be neglected. $V_{dn} = 4 \left[\frac{\Omega \cdot \text{cm}}{(\mu \text{m})^2} \right] \cdot \frac{d^2}{\rho_n} - V_{bi}$

$$V_{dp} = 11 \left[\frac{\Omega \cdot \mathrm{cm}}{\left(\mu \mathrm{m} \right)^2} \right] \cdot \frac{d^2}{\rho_p} - V_{bi}$$

Thiele formula

$$V_{\rm ch} = \left[V_{\rm GS-top} - V(x)\right] \frac{C_{\rm ox-top}}{C_{\rm ox-top} + C_{\rm ox-back} + \frac{1}{2}C_q} + \left[V_{\rm GS-back}\right]$$

$$-V(x)]\frac{C_{\text{ox-back}}}{C_{\text{ox-back}} + \frac{1}{-}C_a}$$
(14)

$$C_q = \frac{2q^2k_{\rm B}T}{\pi(\hbar v_{\rm F})^2} \ln \left[2\left(1 + \cosh\frac{qV_{\rm ch}}{k_{\rm B}T}\right) \right].$$

$$v_{\rm sat} = \frac{\Omega}{(\pi \rho_{\rm sh})^{0.5 + AV^2(x)}}.$$

$$I_D = q \mu W \frac{\int_0^{V_{\rm DS}} \rho_{\rm sh} dV}{L - \mu \int_0^{V_{\rm DS}} \frac{1}{v_{\rm sat}} dV}$$

We can see that when V_{GS} has a too high value C_a can increase a lot and consequently V_{ch} will drop in value, this two behaviors should limit the increasing in the carrier density (proportional to both).

Equations from Thiele's et al. article

$$V_{ch} = (V_{GS} - V(x)) \frac{C_{ox}}{C_{ox} + \alpha |V_{ch}|};$$
(1)

$$V_{ch} > 0 = > V_{ch} = (V_{GS} - V(x)) \frac{C_{ox}}{C_{ox} + \alpha V_{ch}},$$
(2)

$$\alpha V_{ch}^2 + V_{ch}C_{ox} = (V_{GS} - V(x))C_{ox}$$
(3)

$$V_{ch} = \frac{-\frac{C_{ox}}{2} + \sqrt{(-\frac{C_{ox}}{2})^2 + (V_{GS} - V(x))C_{ox}\alpha}}{\alpha}$$
(4)

In the other case

$$V_{ch} < 0 => V_{ch} = (V_{GS} - V(x)) \frac{C_{ox}}{C_{ox} - \alpha V_{ch}},$$
(5)

(6)

$$V_{ch} = \frac{-\frac{C_{ox}}{2} \pm \sqrt{(-\frac{C_{ox}}{2})^2 + (-V_{GS} + V(x))C_{ox}\alpha}}{-\alpha}$$

 $I_{DS-}V_{DS}$ at $V_{GS}=20$





References

[1] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, Nat. Nanotechnol. 3, 654 2008.

[2] S. A. Thiele, J. A. Schaefer, and F. Schwierz. Modeling of graphene metal-oxide-semiconductor field-effect transistors with gapless large-area graphene channels.
Journal of Applied Physics, 107(9), 2010.