WP4 fast track finding device: organisation of activities

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People

WP4: Design and implementarion of fast tracking devices				
Resp: N. Neri (MI)		FT	m/pers 018	Activity in 2018
People	RU			
A. Carbone	BO	0,2	2,2	design
A. Sidoti	BO	0,2	2,2	design
L. Frontini	MI	0,3	3,3	design/tests
P. Gandini	MI	0,2	3,3	design/tests
N. Neri	MI	0,3	3,3	design/tests
M. Petruzzo	Mi	0,3	2,2	design/tests
Total		**1,5**	**18,7**	

- 1 PhD student joined the group: Elisabetta Spadaro Norella

Tasks

1. Optimisation of the 4D fast tracking algorithm and tracking detector layout based on high-level simulations (6 months) [Nicola, Marco, Elisabetta, Paolo, altri?]
2. Design of fast track finding device architecture based on a realistic tracking detector and running conditions of the HL-LHC (6 months) [Nicola, Marco, Stefano, Paolo, altri?]
3. Study of the performance of the device based on low-level simulations (6 months) [Marco, Elisabetta, Paolo, altri?]
4. Implementation of the firmware in fast track finding boards based on Bologna (ATLAS) and Milano (Retina) boards. Four boards developed in Bologna will emulate hits of the detector and perform stub reconstruction. The Retina board will receive the stubs and perform the track reconstruction (6 months) [Marco, Elisabetta, Paolo, Stefano, altri?]
5. Emulation of a realist tracking detector at HL-LHC and study of the performance of the device based on simulated data on optimise board to be designed and constructed in Timespot (6 months) [Marco, Elisabetta, Paolo, altri?]
6. Study the performance of the fast track finding device using a multilayer pixel prototype in a test beam (6 months) [All]

Milestones & deliverables

Milestones

1. Dec. 2018: document with the specifications for the fast track finding device for a realistic tracking detector for the HL-LHC phase
2. Sept. 2019: Test of the performance of the device using emulated tracks on existing boards developed in ATLAS and Retina experiments
3. June 2020: Test of the performance of the device using a emulated data using an optimised board to be developed in Timespot
4. Dec. 2020: Test of the performance of the device on beam using a multilayer pixel detector prototype

Deliverables

1. Dec. 2018: document of specifications for fast track finding device
2. Dec. 2020: Prototype optimised fast track finding board

Timeline

Timeline

Task	2018	2019	2020
Optimisation 4D algorithm and detector layout			
Device architecture			
Low-level simulations			
Test using simulated tracks with existing DAQ and Retina boards			
Test using simulated tracks at high rates with optimised board and track processor			
Integration with the prototype pixel detector and test on beam			