STATUS OF **F**AS**T** TRAC**K**ER (**FTK**) AND FUTURE **H**ARDWARE **T**RACKER FOR THE **T**RIGGER (**HTT**)

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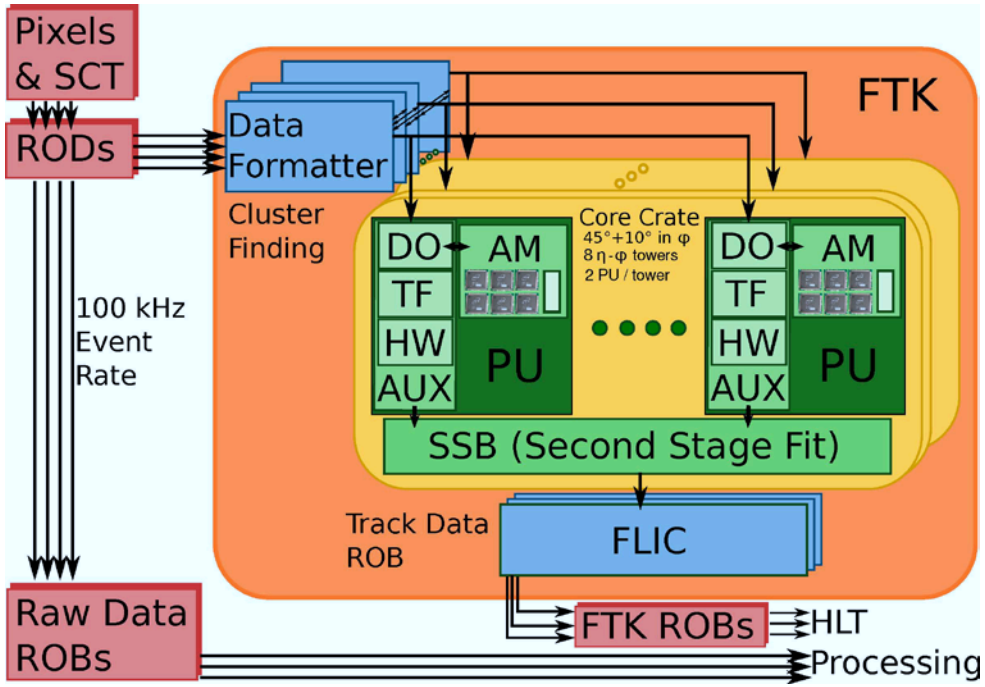
STATE-OF-THE-ART: THE FTK SYSTEM

The whole FastTraKer (FTK) system stores **one billion (10^9) patterns**

- **8 Mpatterns** per board (128 boards)
- **128 kpatterns** per chip (64 AM chips / board)
- A pattern is composed by 18 bits × 8 words

Major concerns:

- high pattern density
  - **large silicon area**
- I/O signal congestion at board level (**solution: 2 Gbit/s serial links**)
- Maximum power limited by cooling (because we are fitting 8192 AMchips in 8 VME crates): **250 W per AM board**

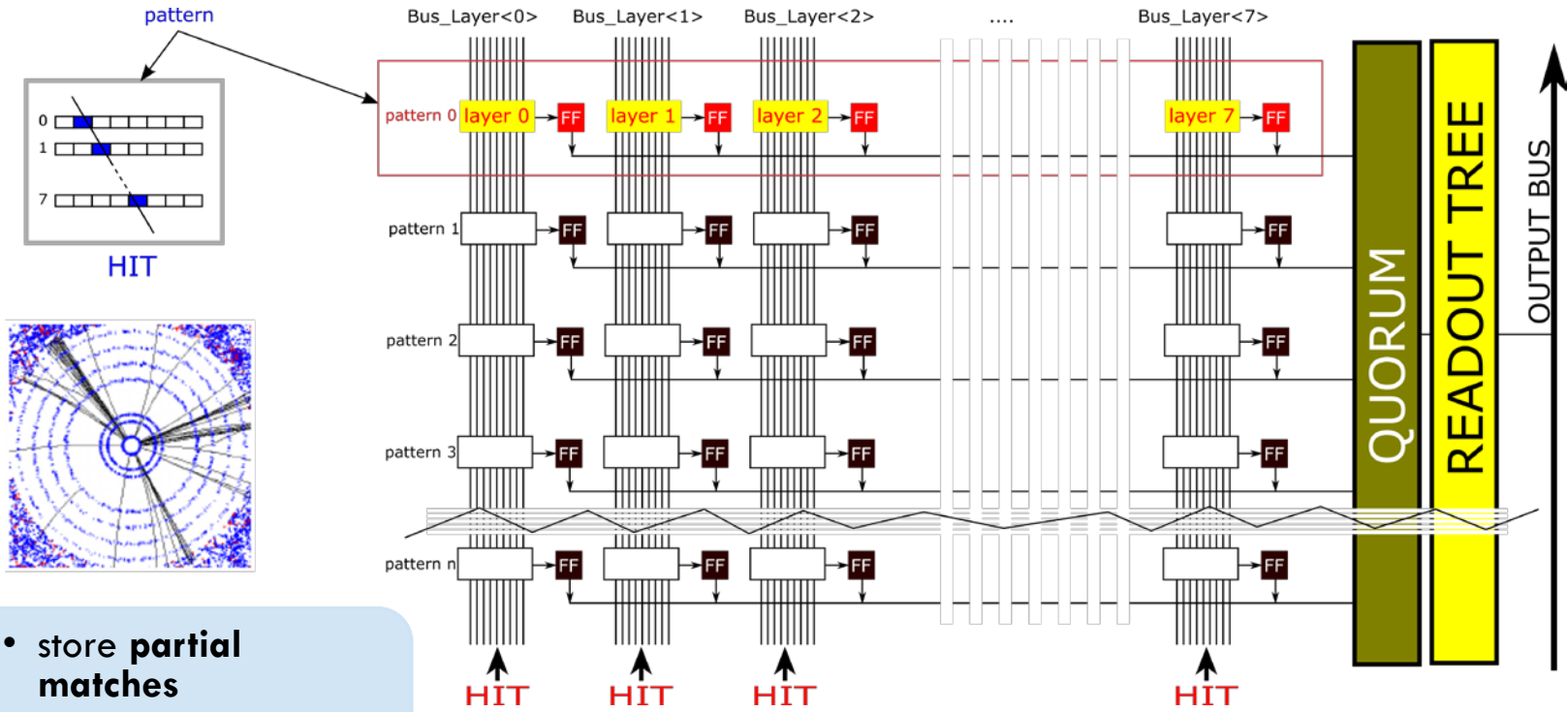


[1]A. Andreani et al., \The AMchip04 and the processing unit prototype for the FastTracker," *IOP J. Instr. 7* (2012) C08007

THE AM CHIP ARCHITECTURE

For each bus and for each pattern there is a small **CAM cell array (layer x)**

- It compares its own content with all data received. If it matches a **memory is set (FF)**
- The partial matches are analyzed by **Quorum logic** the and compared to the desired threshold
- A **readout encoder (Fischer Tree)** reads the matched patterns in order



The AM and commercially available CAMs differs substantially

The AM provides the unique capability:

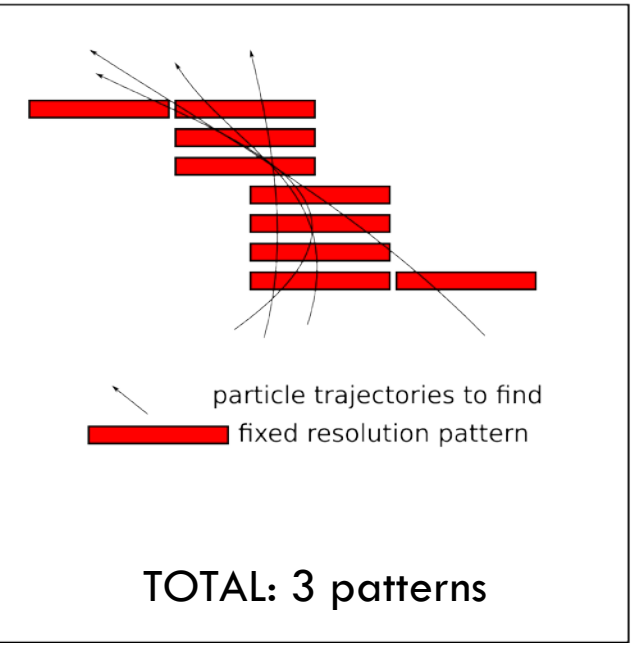
- store **partial matches**
- find correlations at **different times**

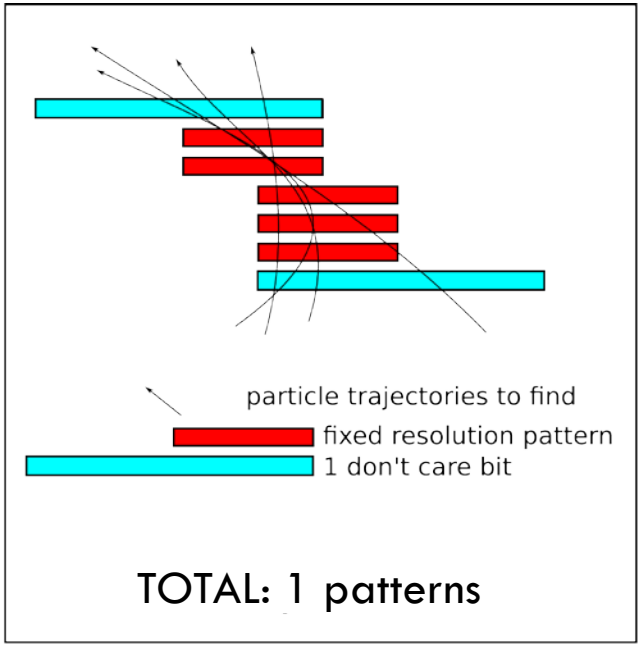
VARIABLE RESOLUTION

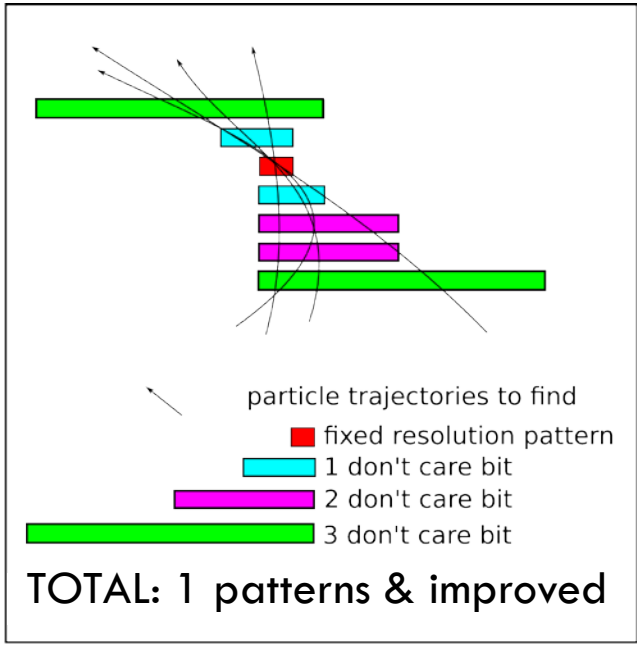
Smart approach: consists in performing pattern matching at **reduced and variable resolution first,** and then to **refine** matching resolution using a FPGA.

- A **"don't care" bit** is used to increase the pattern recognition efficiency at different resolutions.

At high efficiency: number of fakes, required patterns, and power consumption decrease.







HL-LHC REQUIREMENTS

Big challenges from phase-II conditions

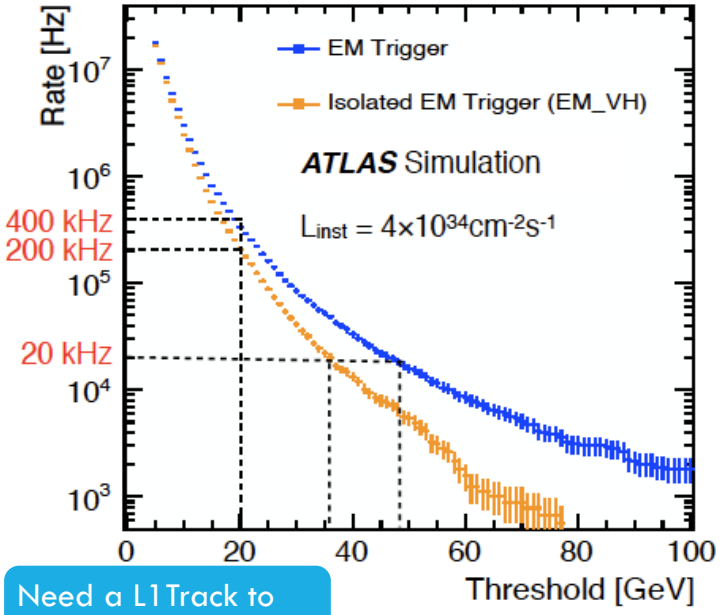
- Pileup 140 (max 200)

Track Triggers are a crucial piece of the phase-II upgrade plan

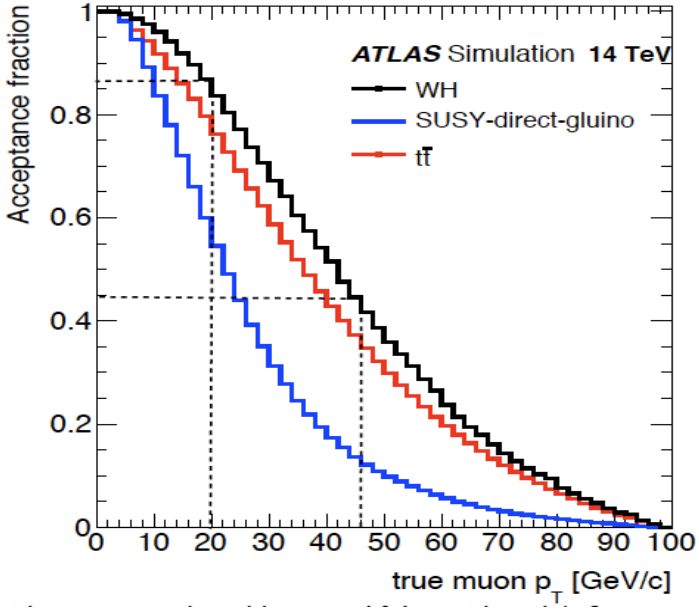
- **ATLAS:** L1Track and L2 upgrade
- **CMS:** L1Track Trigger is the baseline

Goal: evolve the system design to phase-II environment

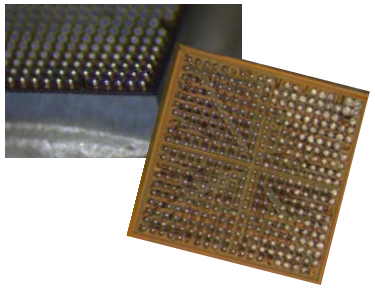
- **AM chip R&D**
- Fully exploit **ATCA** potentialities



Need a L1Track to save EM pt>20 GeV



AMCHIP TREND



Since 2010:

- **AM chip v. 4** designed and characterized 2012 – area: 14 mm² – cost: 50 k€ – 8 kpattens

65 nm

65 nm

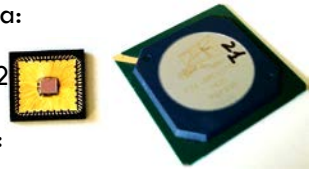
28 nm + FPGA

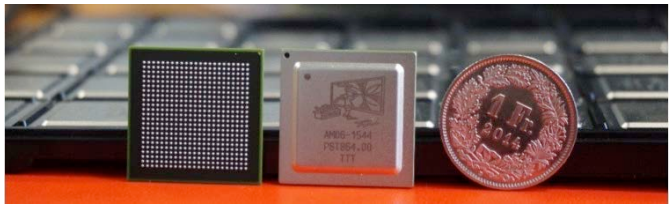
2015-2017
IMPART+RDPHASE_2

- **AM07 chips will be** designed and characterized within the project for several disciplines:
  - **Image analysis**
  - **DNA sequencing**
  - **Trigger DAQ**

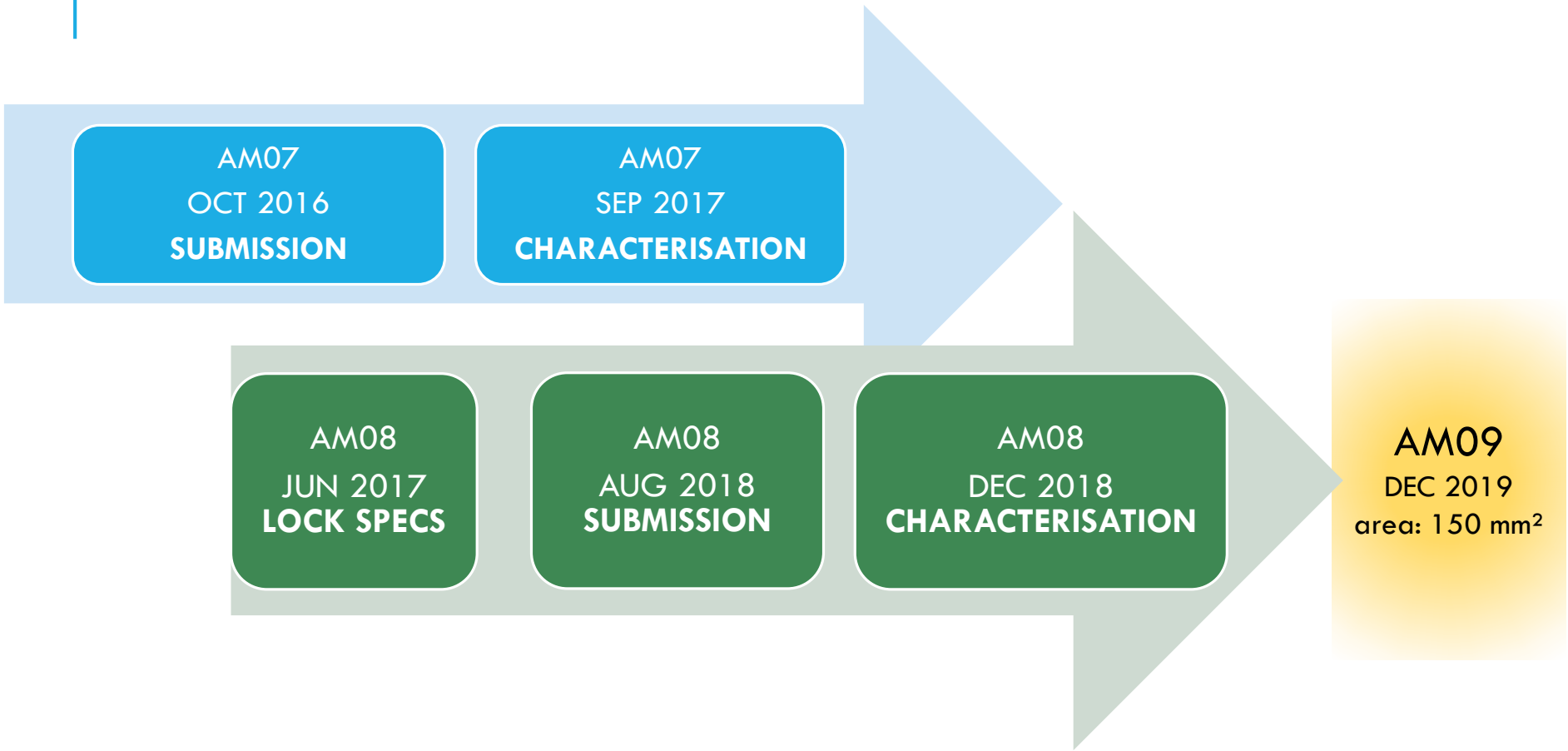
Since 2011:

- **AM chip v. 5-mini@sic** designed and characterized 2012 – area: 4 mm² – cost: 20 k€ – 256 pattens for cell test
- **AM chip v. 5-mpw** designed and characterized 2013 – area: 12 mm² – cost: 75 k€ – 5 kpattens
- **AM chip v. 6** under design; to be submitted in Dec. 2014 – area: 160 mm² – cost: 550 k€ – 128 kpattens - **421 millions transistors**





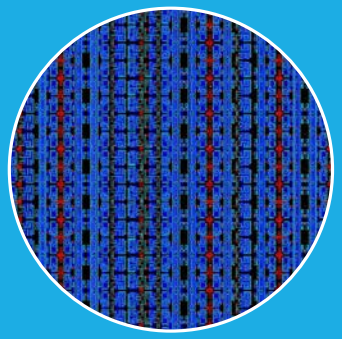
SCHEDULE FOR THE NEXT CHIPS



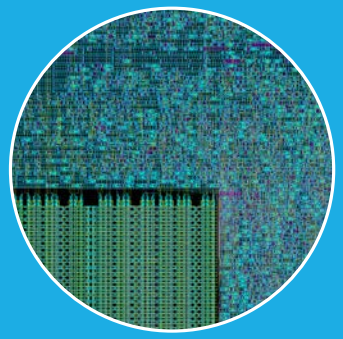
AMCHIP DESIGN COMPLEXITY VS CPUS

Chip name	*Transistor count*	*Year*	*Brand*	*Technology*	*Area*
Core 2 Duo Conroe	291,000,000	2006	Intel	65 nm	143 mm²
Itanium 2 Madison 6M	410,000,000	2003	Intel	130 nm	374 mm²
Core 2 Duo Wolfdale	411,000,000	2007	Intel	45 nm	107 mm²
AM06	**421,000,000**	**2014**	**AMteam**	**65 nm**	**168 mm²**
Itanium 2 with 9 MB cache	592,000,000	2004	Intel	130 nm	432 mm²
Core i7 (Quad)	731,000,000	2008	Intel	45 nm	263 mm²
Quad-core z196[20]	1,400,000,000	2010	IBM	45 nm	512 mm²
Quad-core + GPU Core i7 Ivy Bridge	1,400,000,000	2012	Intel	22 nm	160 mm²
Quad-core + GPU Core i7 Haswell	1,400,000,000	2014	Intel	22 nm	177 mm²
AM09	**1,684,000,000**	**2019**	**AMteam**	**28 nm**	**150 mm²**
Dual-core Itanium 2	1,700,000,000	2006	Intel	90 nm	596 mm²

DESIGN METHODOLOGY

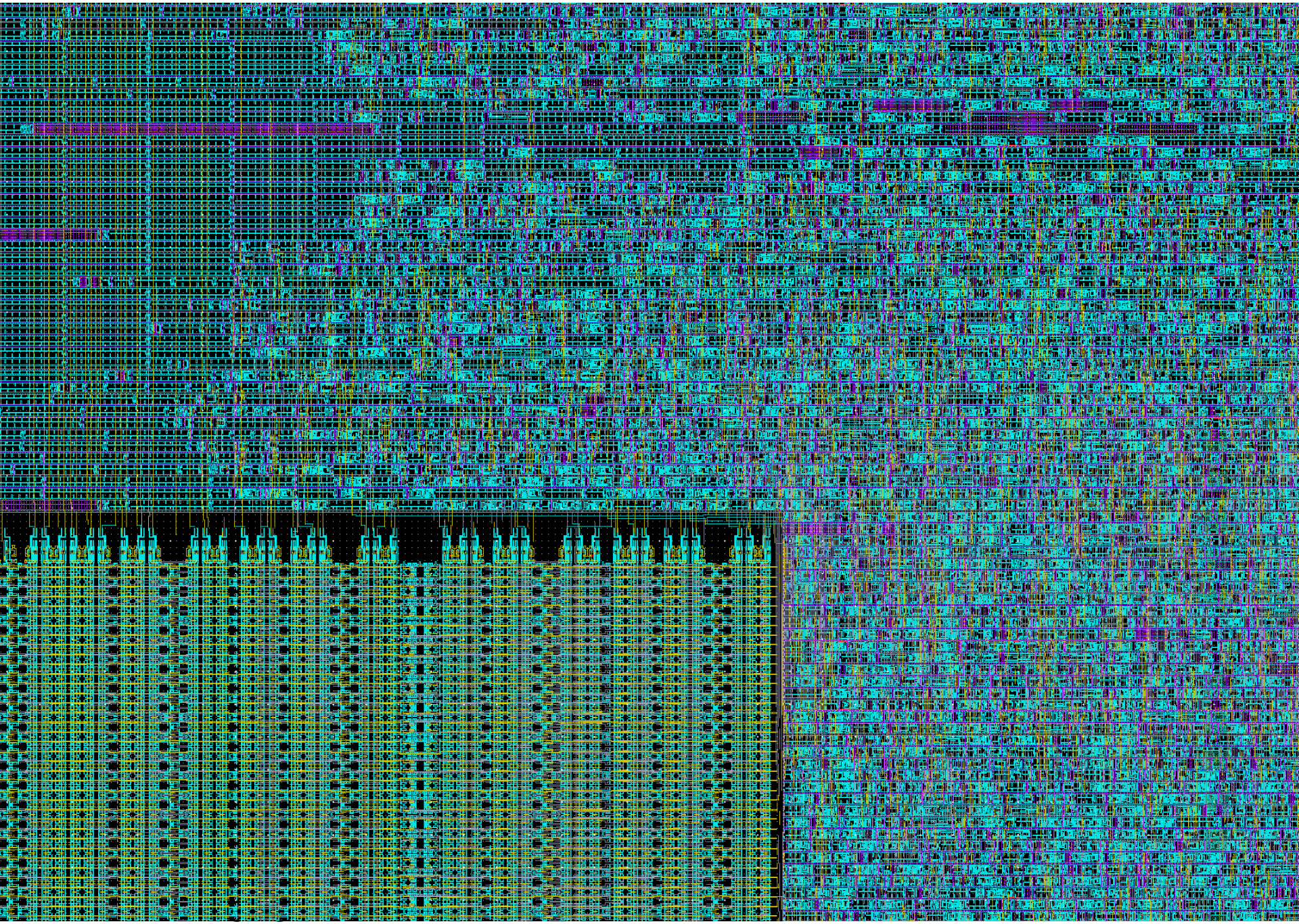


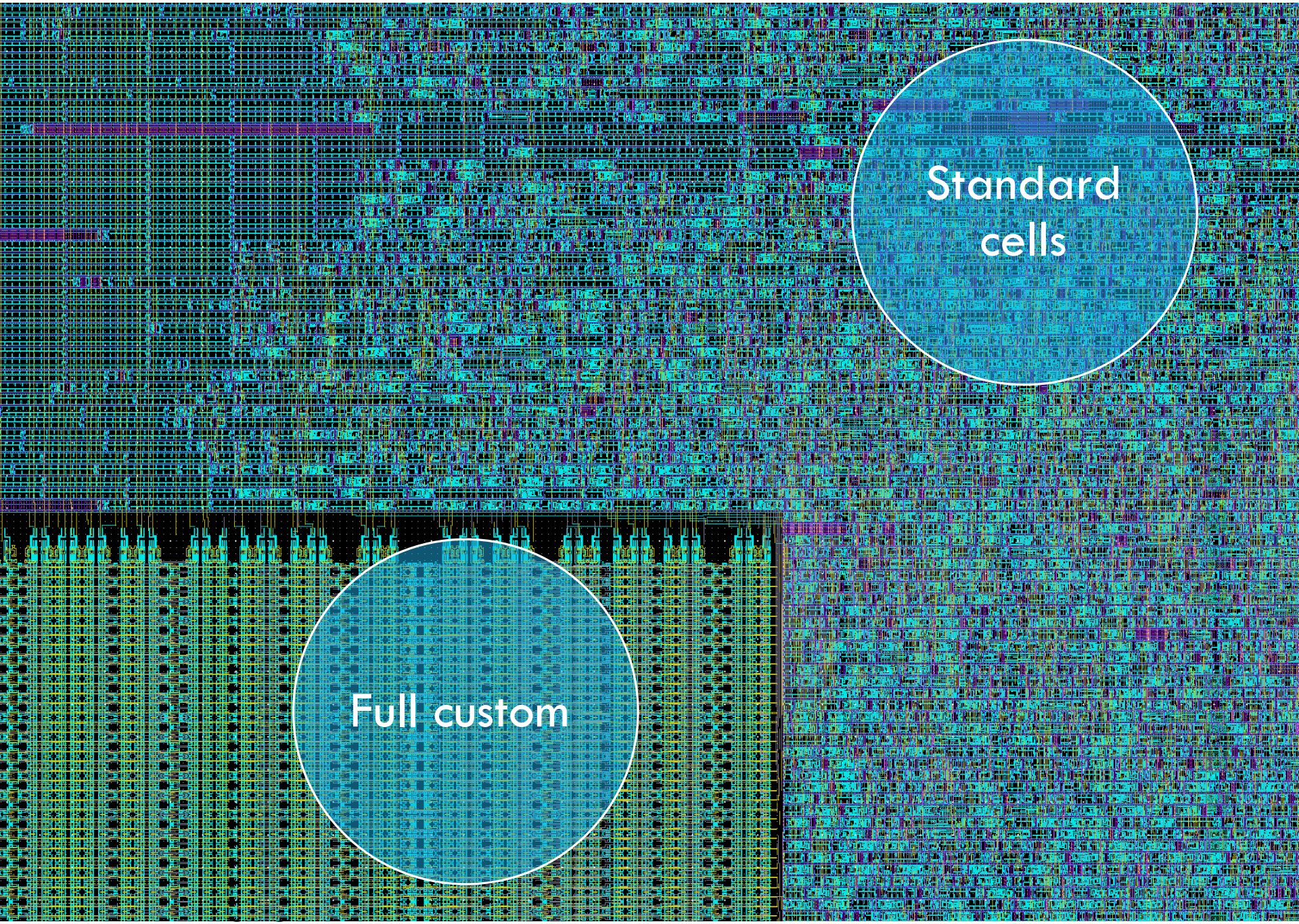
More repetitive parts have been design “by hand” with a full custom approach

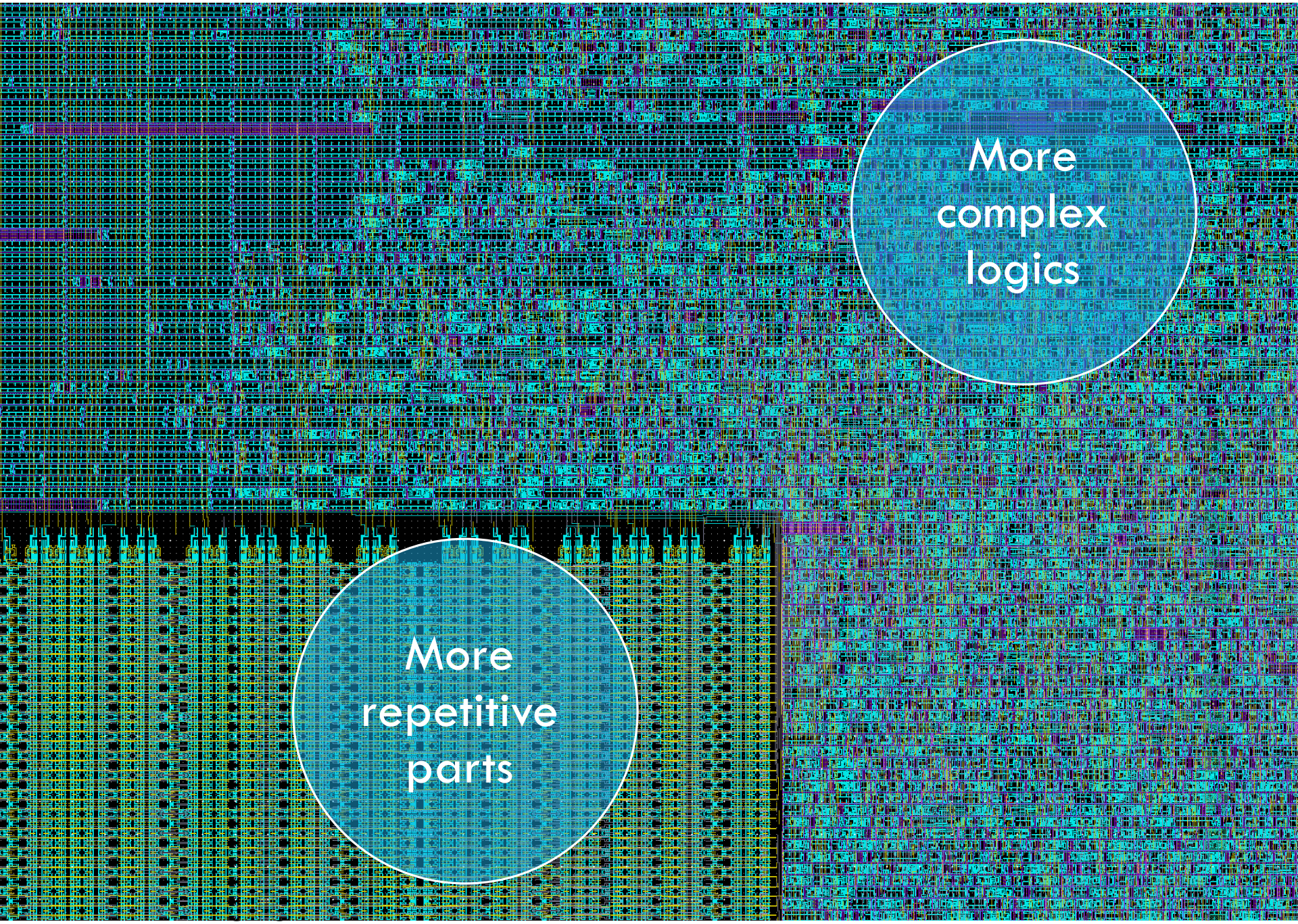


More complex logics have been design with automatic tools based on standard cells (synthesis, place & route)

MIXED APPROACH




Standard cells
Full custom


More complex logics
More repetitive parts

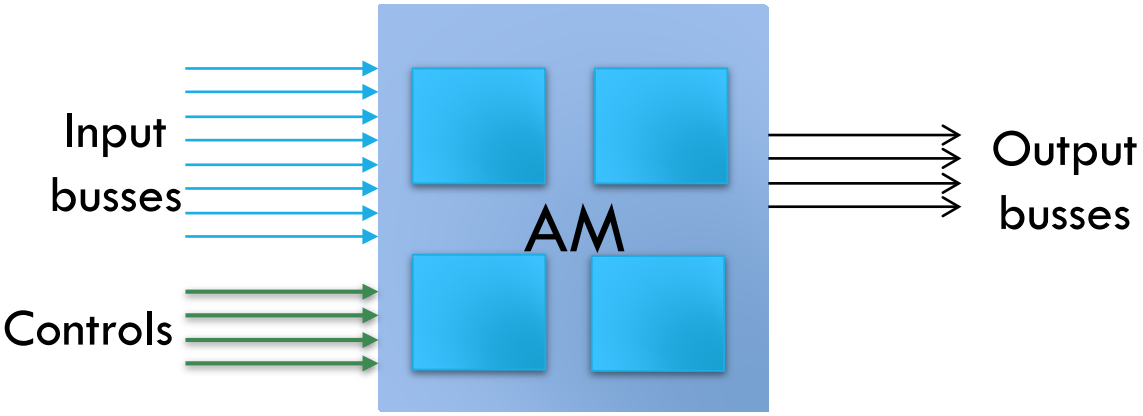
AM09 COMPLEXITY

AM09 will be one of the most complex chips designed within CERN collaboration

Comparison rate:

about 30 peta comparisons per second per chip

MULTI-CORE ARCHITECTURE



Chip will be composed by few **cores**

Outputs could be merged or independed

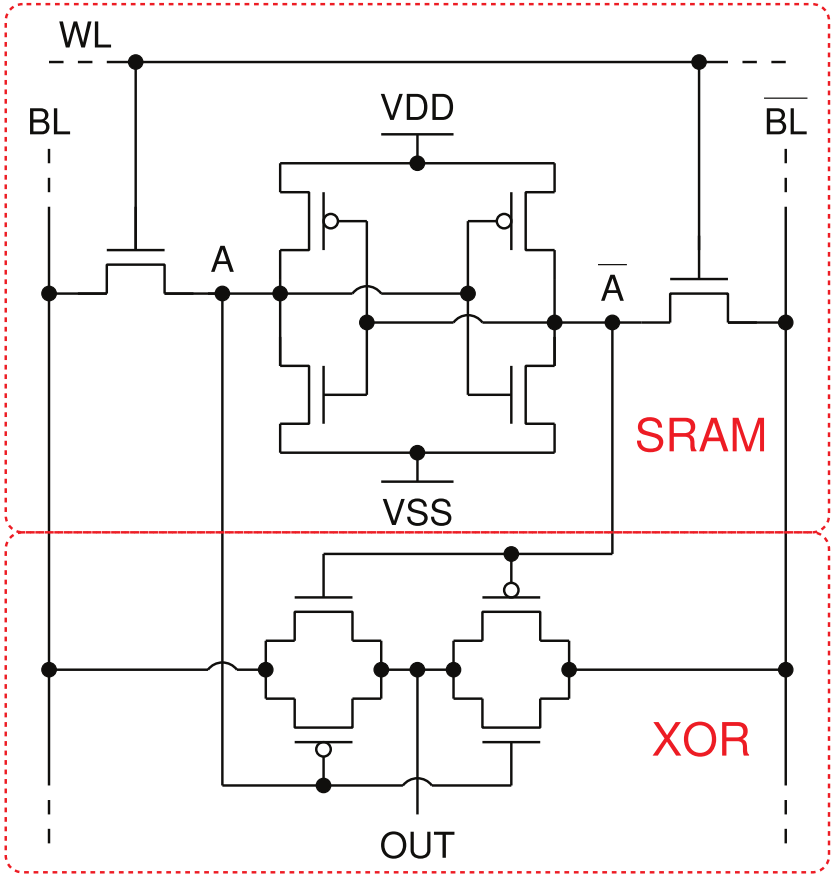
- Choice depending on required output bandwith

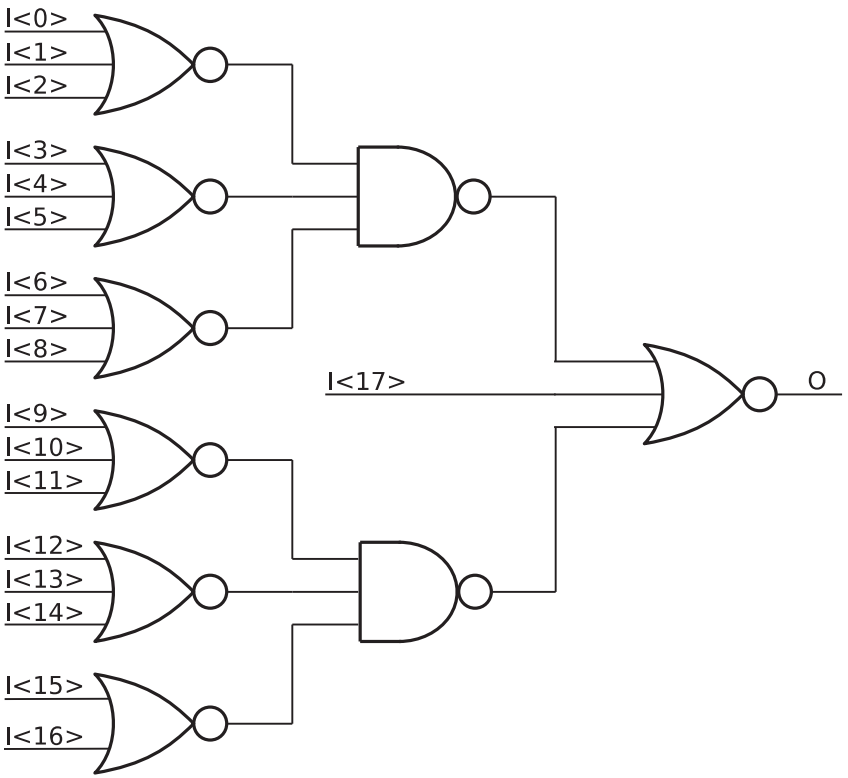
THE XORAM CELL

Based on the previous 65 nm XORAM cell

Based on the XOR boolean function, instead of the NAND and NOR functions

Is made of a 6T SRAM cell connected to a 6T-XOR gate





NEW OPTIMIZED CELLS

With similar power save methods we designed two new cell tech:

- DOXORAM
- KOXORAM

Italian Patent: A. Annovi, L. Frontini, V. Liberali, A. Stabile, "MEMORIA CAM", UA2016A005430

In this week INFN will decide for the internationalization

FULL CUSTOM CELL:
ENERGY CONSUMPTION VS AREA