28 nm Technology

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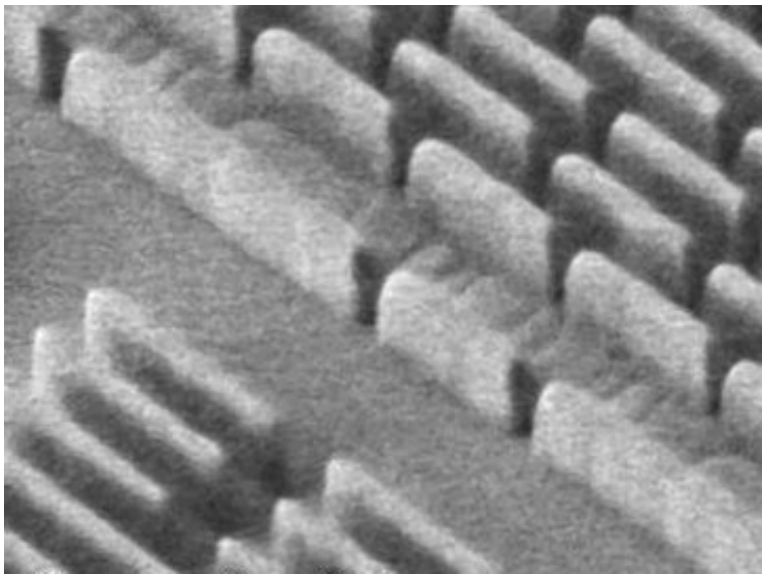
28 nm technology: overview

28 nm is a common and mature technology
(Xilinx Kintex-7, Nvidia 600-700-900 series)

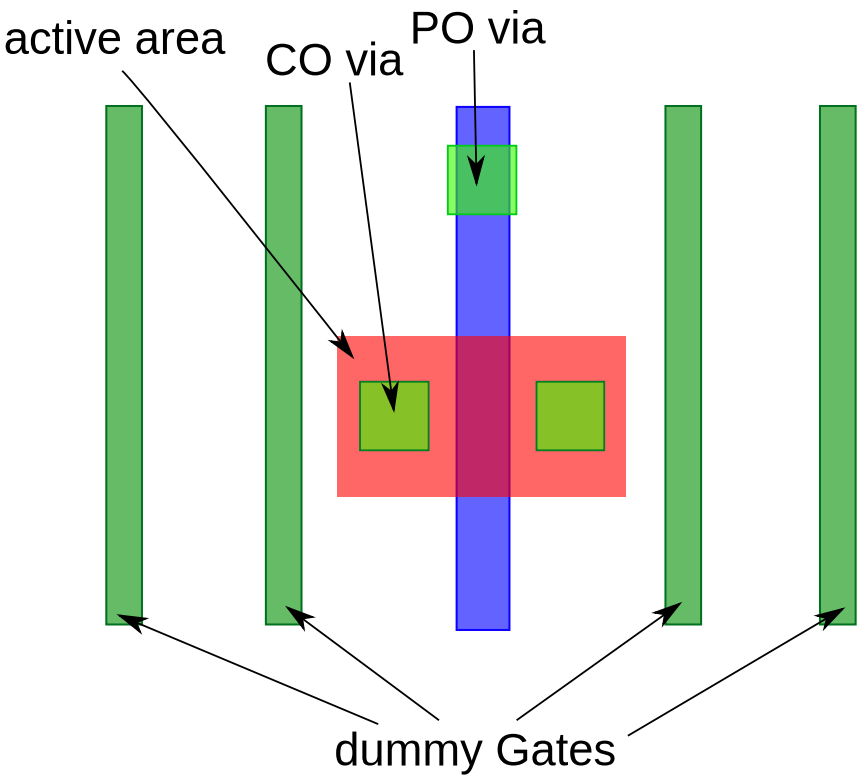
- Minimum gate length 28 nm
- Minimum gate pitch 130 nm

- UV $\lambda >$ gate lenghth

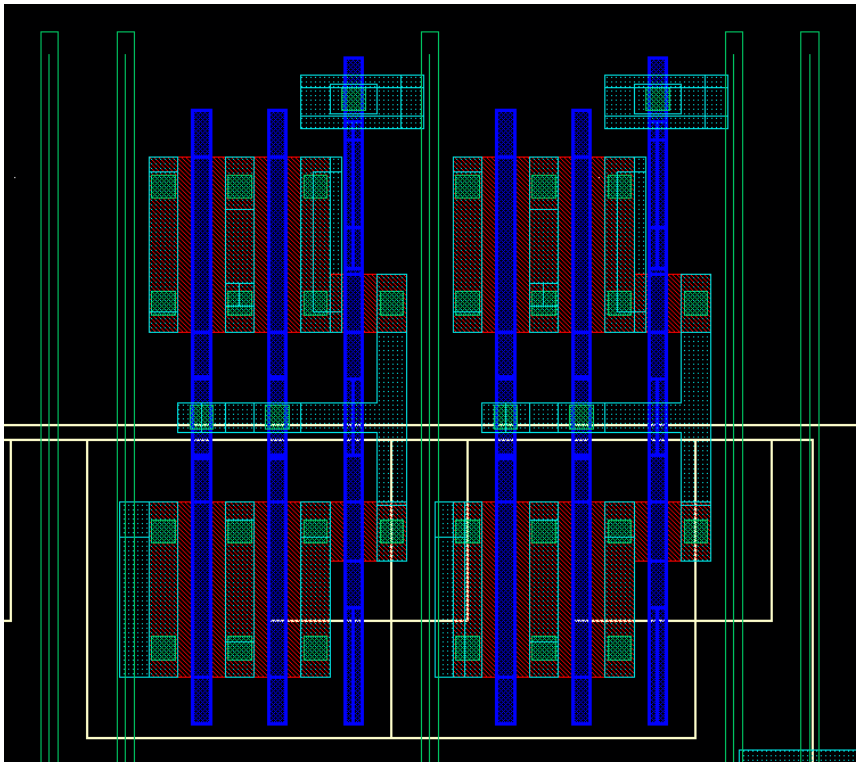
- Interference figure needed to fabricate transistors
- Ordinate and regular design
- More design rules



28 nm technology: MOSFET and dummy gates



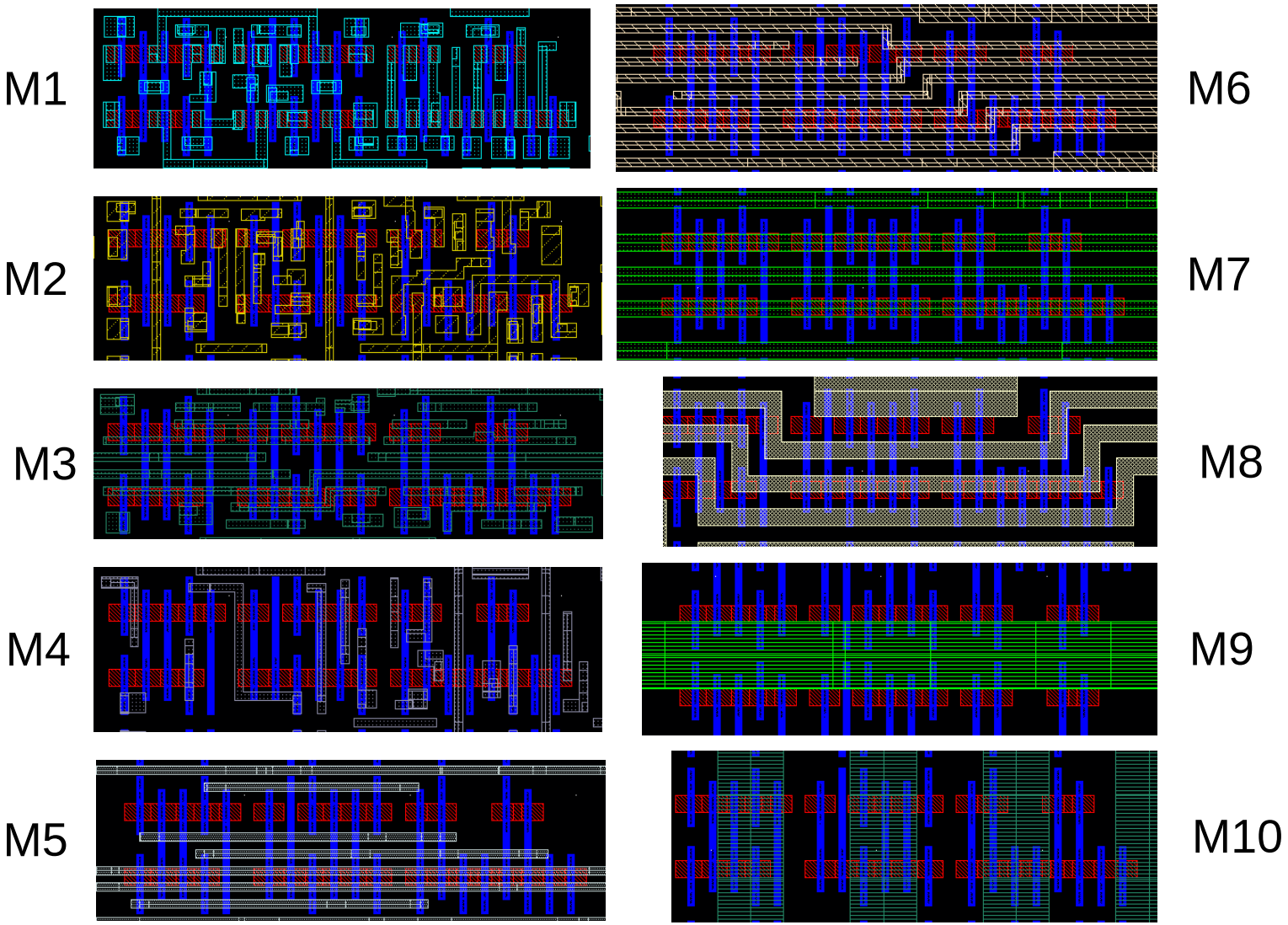
Two buffer (muti-finger transistors)



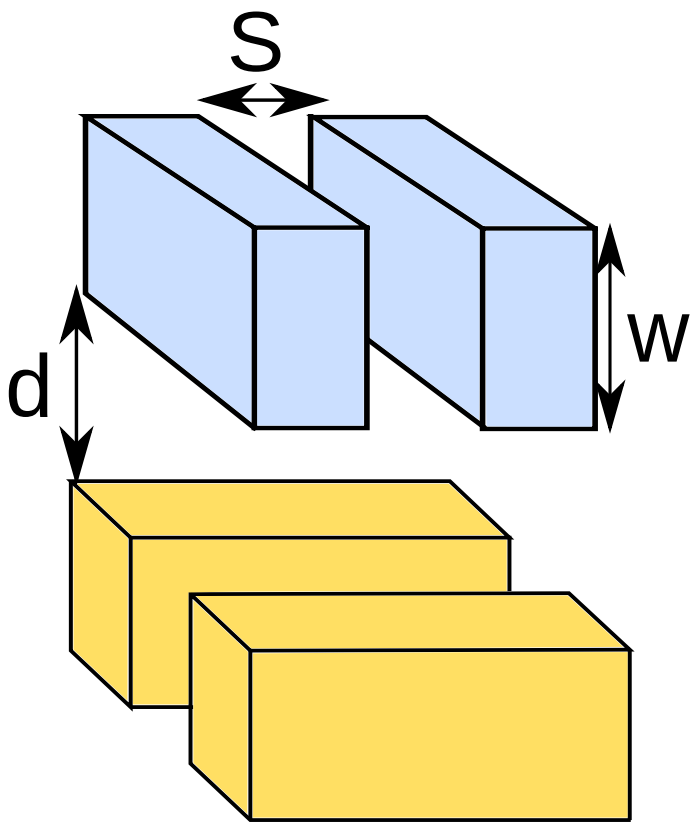
- Two dummy gates per side
- Space between gates strictly fixed
- No L-shaped gates
- PO-via larger than min. PO-w

Metals

18-bit associative memory cell



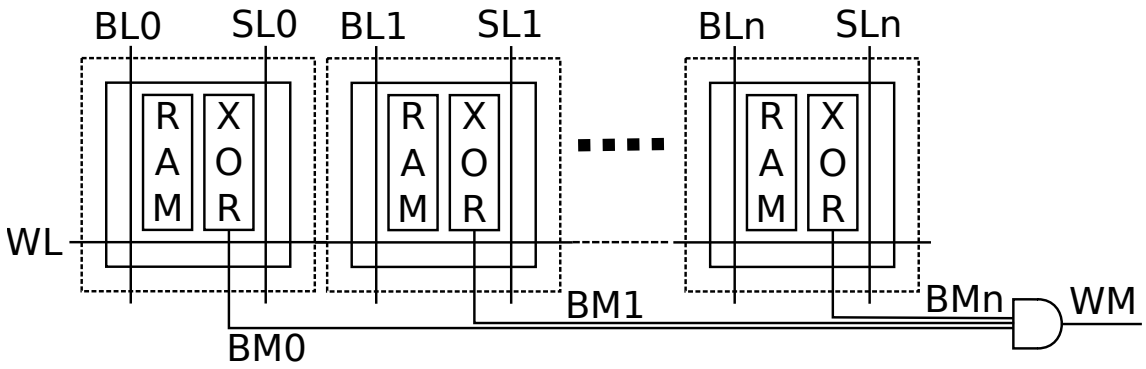
28 nm technology: interconnection capacitances

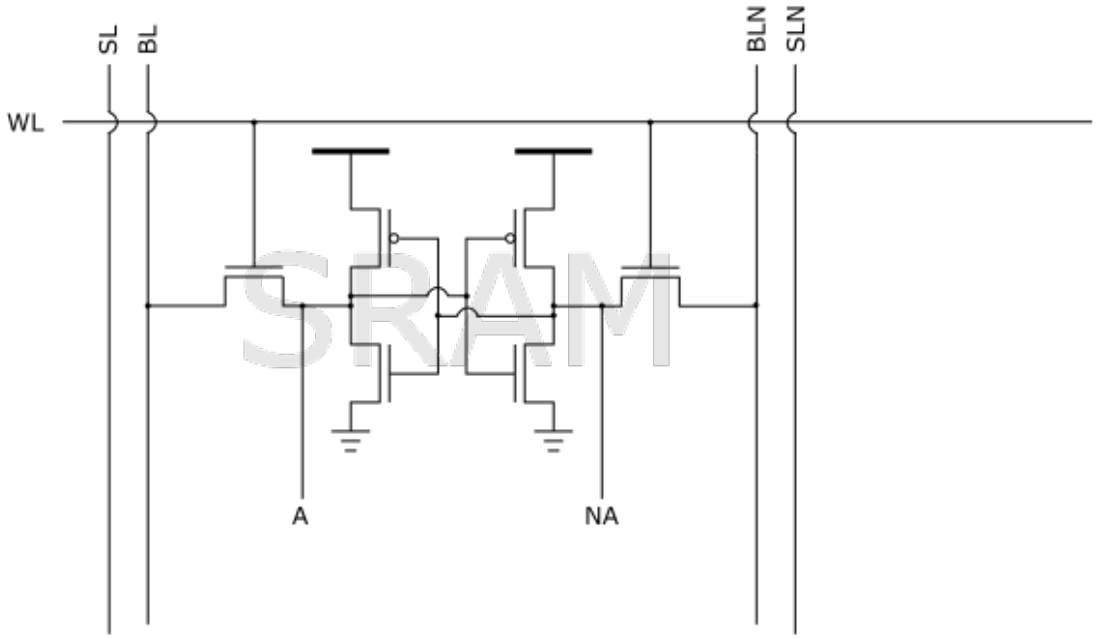


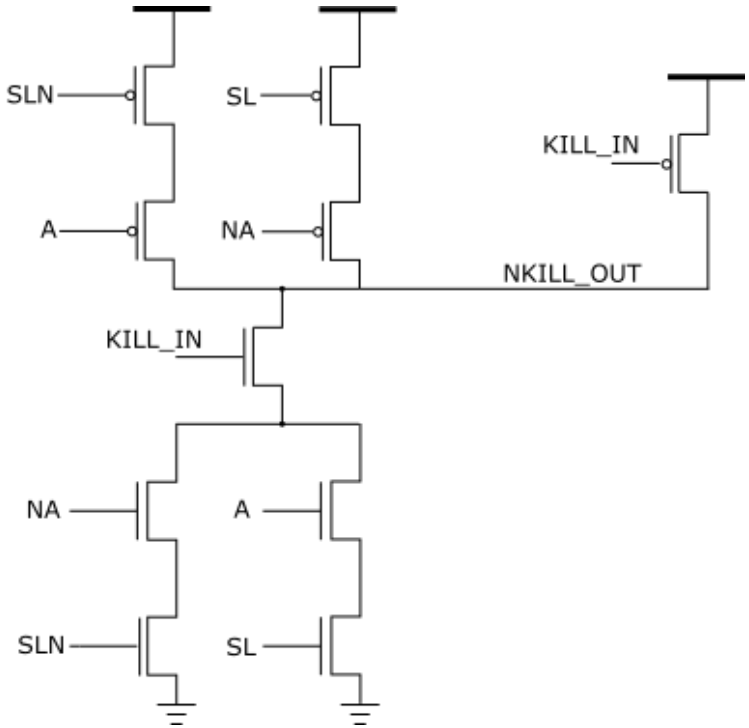
- $2 \times \mathrm{W} \approx \mathrm{S}$
- $\mathrm{S} < \mathrm{d}$

Design performance and power consumption are affected by the capacitance of interconnections

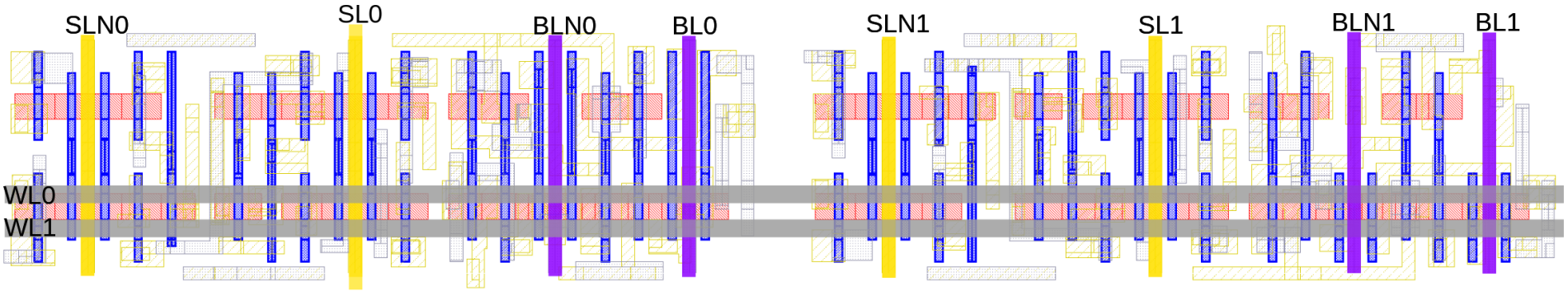
KOXORAM single cell schematic







KOXORAM cell



M2 SL and SLN, M4 BL and BLN, M5 WLs

Design goals:

- Reduce as much as possible the capacitance on SLs without increasing the cell area
- Reduce the switching activity of the transistors during comparison

Results

- The capacitance associated to the search lines is 0.27 fF for two cells (0.20 fF due to gate capacitances, and 0.07 fF due to metal-metal capacitances)
- The average energy per comparison is 0.3 fJ/bit,

Analog design: DCO

- In the previous AMchip (AM06) power consumption can raise from 0.1 A to 2.2 A in 0.1 ns when it changes state from 'idle' to 'compare'
- Current peaks are synchronous with the 100 MHz CLK
- This power consumption generates a ripple on supply voltage

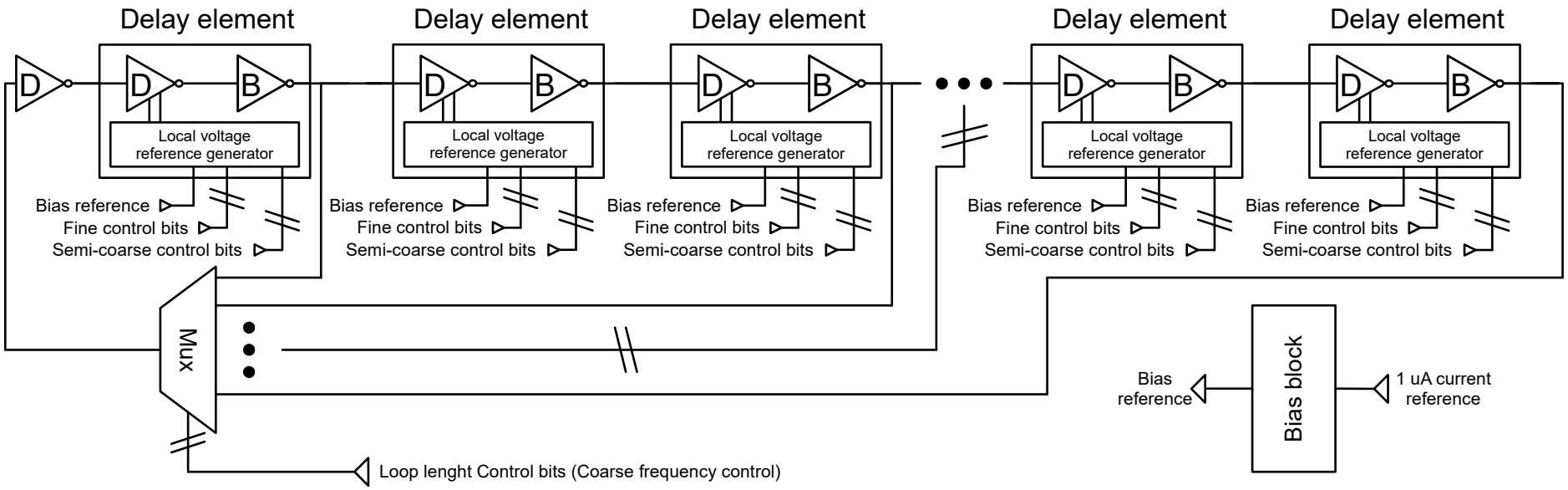
- Divide the total number of memory cells into eight groups
- Spread the power consumption of these groups along the reference clock cycle with eight phase-shifted replicas of the original clock
- Use a digital PLL produce a clock signal locked in phase with the incoming one, but with a frequency that is 8 times higher.

Oscillation frequency:

- Typical and FastFast 1 GHz up to 3.2 GHz
- Slow Slow at least 1 GHz up to 2 GHz

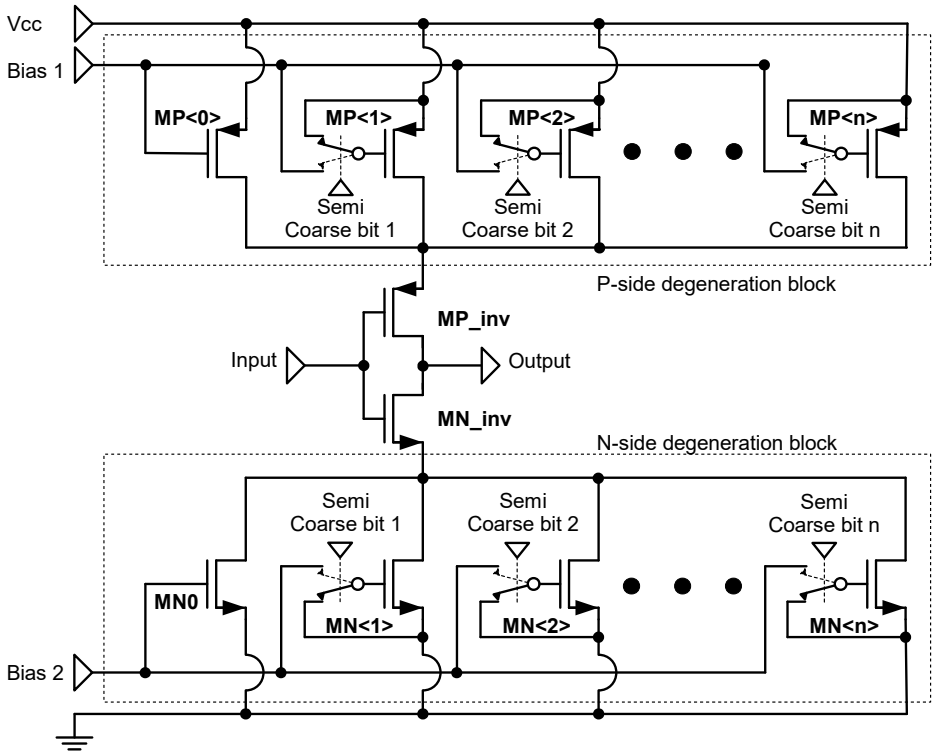
DCO Schematic

Resistors and capacitors in 28 nm technology have a variability of $> 30\%$, we decide to design a delay element only with MOS.



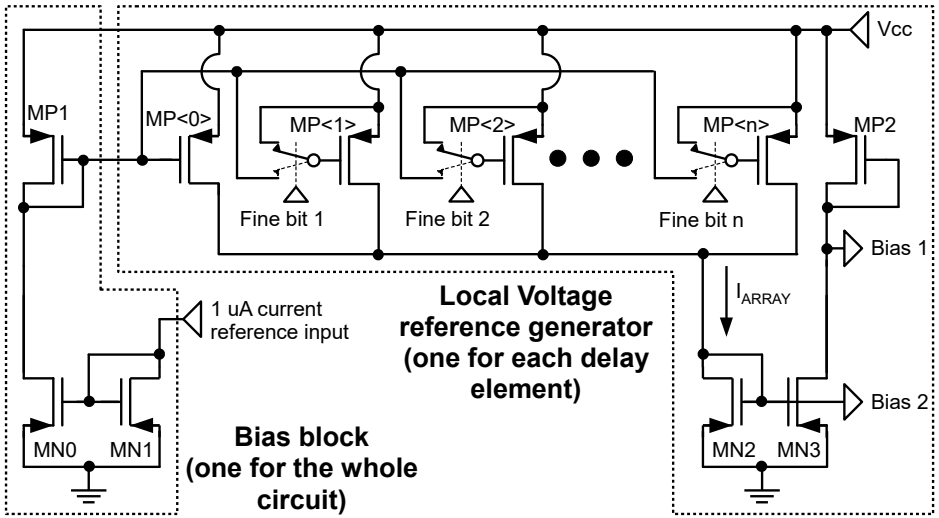
- All controls are thermometric
  - 12bit broad controls
  - 7bit medium controls
  - 64bit fine controls
- 1 µA current reference
- Delay element interleaved with Buffers
- Local and global polarization

DCO Delay element



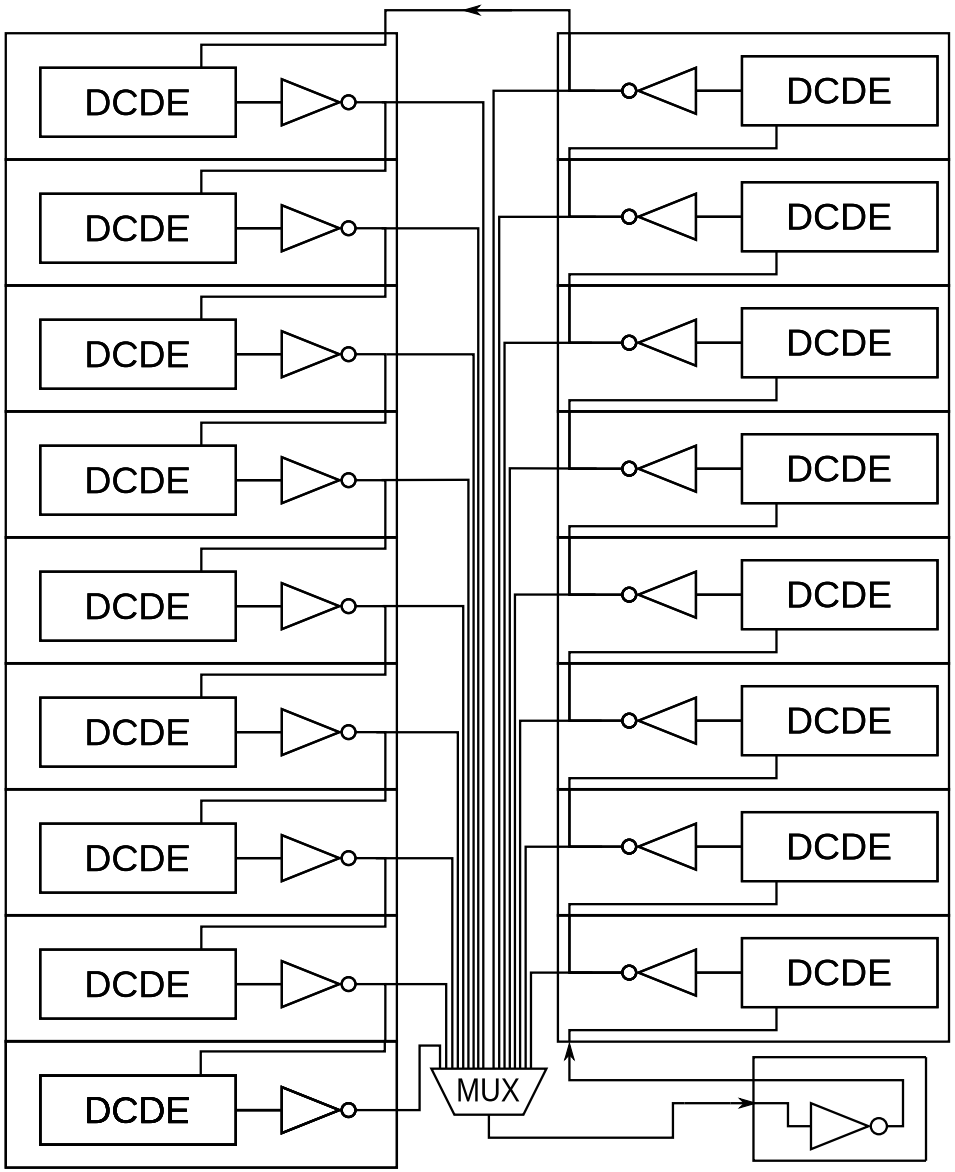
- Based on a current starved inverter
- Each mos of MP<7:1> and MN<7:1> is controlled by control bits
- MN and MP are the output of a current mirror

DCO Local reference generator



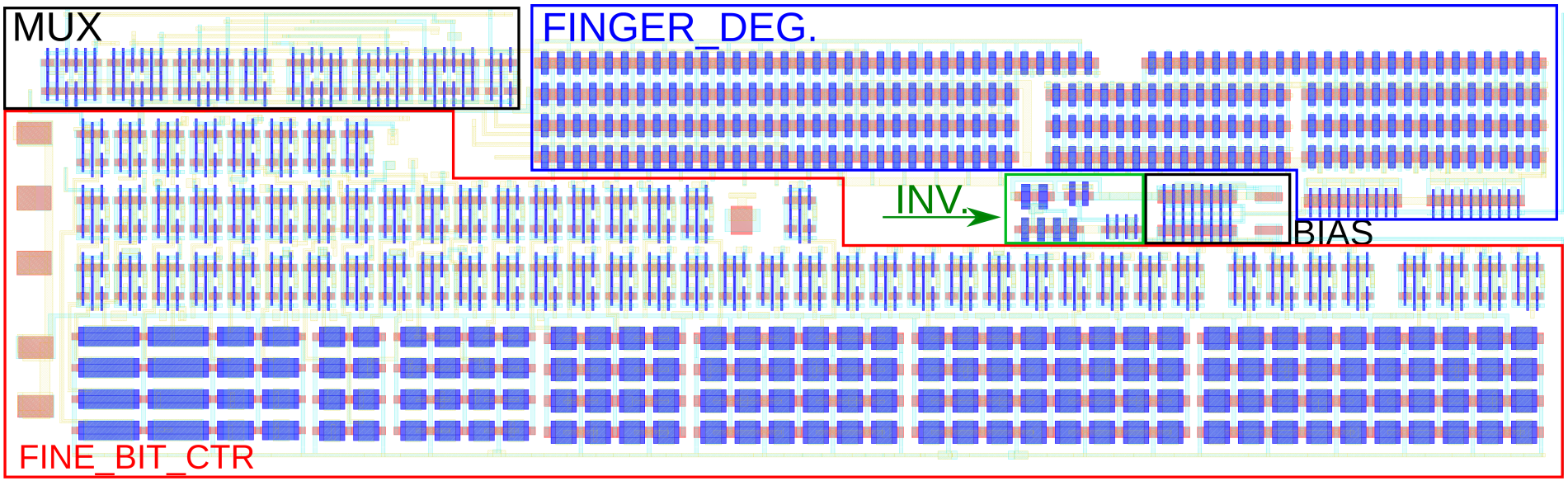
- MP<0:64> have different dimensions to improve linearity the DCO frequency
- Current mirrors to polarize the circuit

DCO Layout – top block



- dimensions: 44×83 µm
- composed by 17 delay blocks
- the returning path is design to reduce parasitic capacitances

Delay element layout



- We made a start-up simulation an the DCO starts
- Performing a post-layout simulation we discover a great dependency from fabrication corners, with the same control set(12/6/32):
  - tt = 2.2 GHz
  - ss = 1.8 GHz
  - ff = 3.3 GHz