TIC
electronics and DAQ

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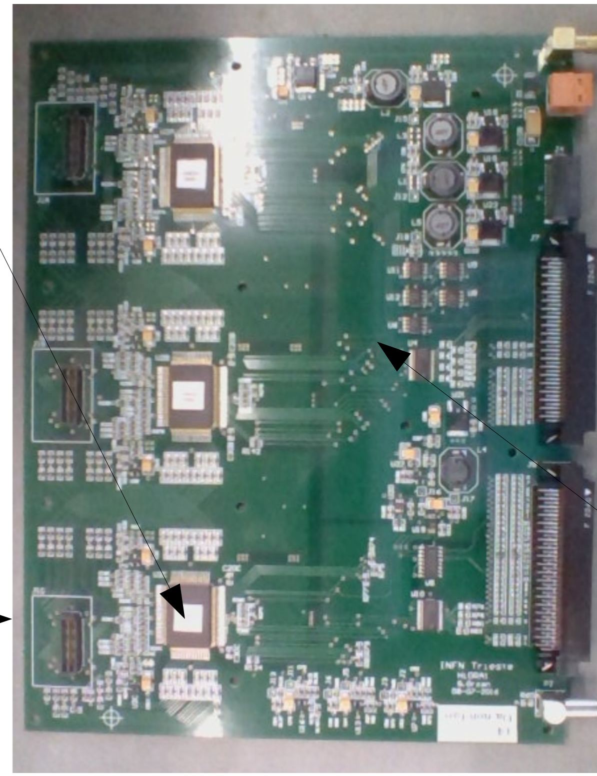
Outline

- Calocube electronics
- Front End chip
- DAQ Status

Calocube electronics Part 1

Each **HiDRA chip** reads two consecutive columns of cubes (both Large and Small PD)



ROC

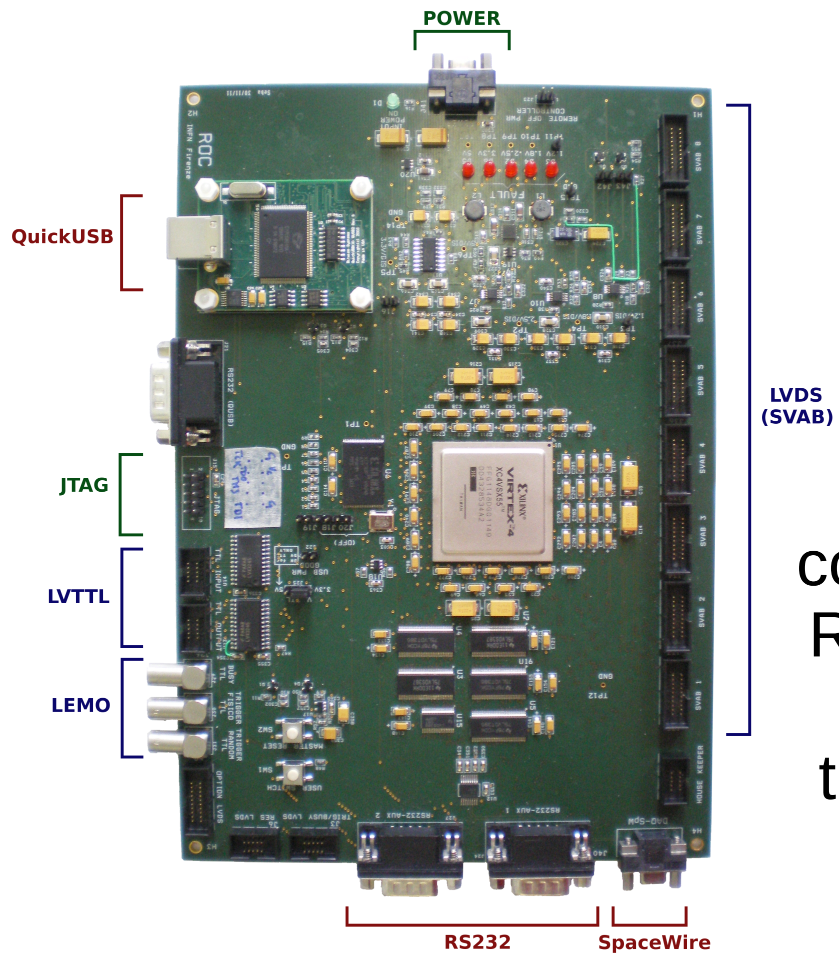
Each HiDRA board is made of 3 HiDRA chip

Front-End electronics

Each 6x6 tray is connected by a **Scolopendra** (kapton cable) to the same HiDRA board

Calocube electronics
Part 2

PC



HiDRa

ROC board communicates with the PC through the QuickUSB device

Acquisition is handled using simple C++ QuickUSB libraries

Read-out controller

HiDRa are connected to the ROC board that drives them though 8 LVDS connectors

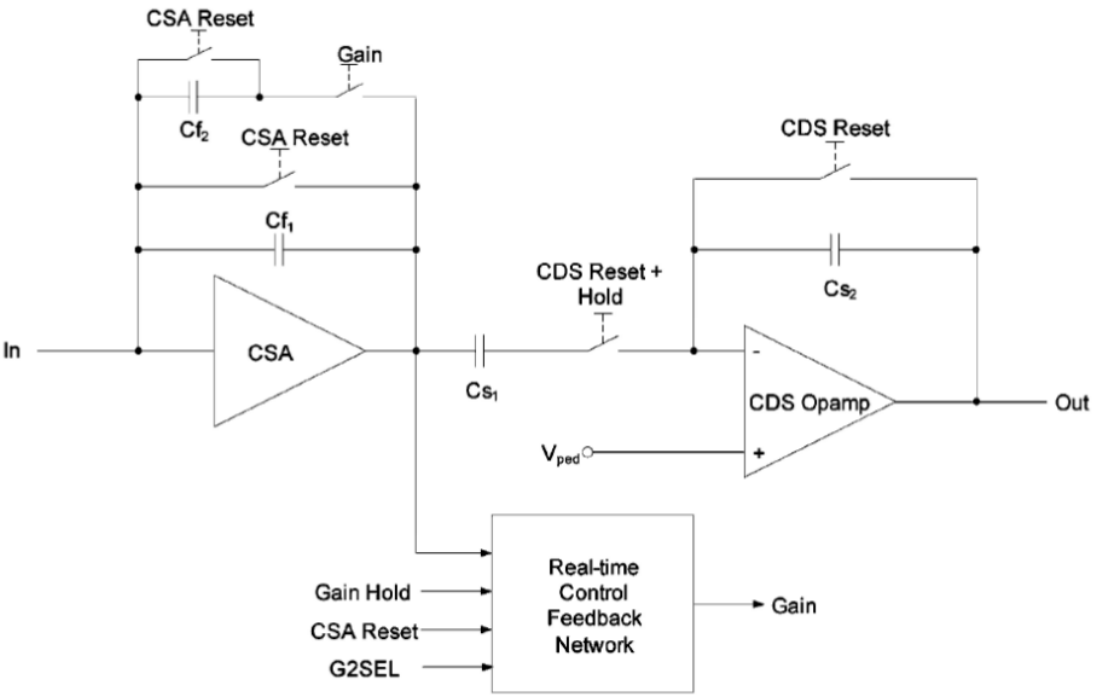
HiDRa chip
Overview

HiDRa chip
- R&D project by INFN
- Developed by INFN-Trieste
- Designed for silicon calorimetry in space

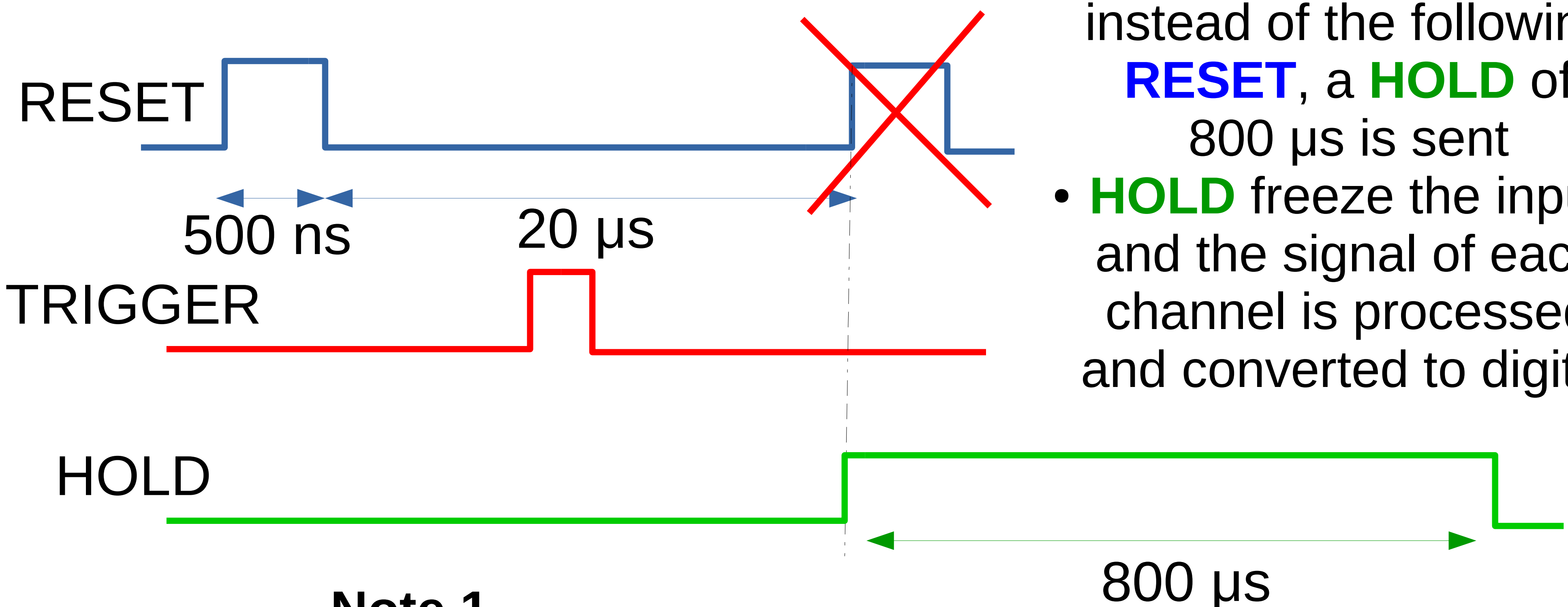
Future Development
- HiDRa chip with auto-trigger by INFN-Trieste (end of 2017)
- ROC to drive the new HiDRa boards by CIEMAT (end of 2018)

Specification
- 28 channels
- charge sensitive amplifier + correlated double sampling
- double gain (1:20)
- automatic gain control

Performances
- High Dynamic range = 52.6 pC
- Low ENC = $2280e^{-} + 7.6e^{-}$ /pF
- Low Consumption = 2.8 mW/ch



HiDRa chip
How it works



Simple description

- The chip is **RESET** with a period of 20 µs
- If a **TRIGGER** arrives, instead of the following **RESET**, a **HOLD** of 800 µs is sent
- **HOLD** freeze the input and the signal of each channel is processed and converted to digital

Note 1

Taking into account CsI response, only triggers arriving before 14 µs from RESET are correctly integrated so **only 70% of events are good for the analysis**

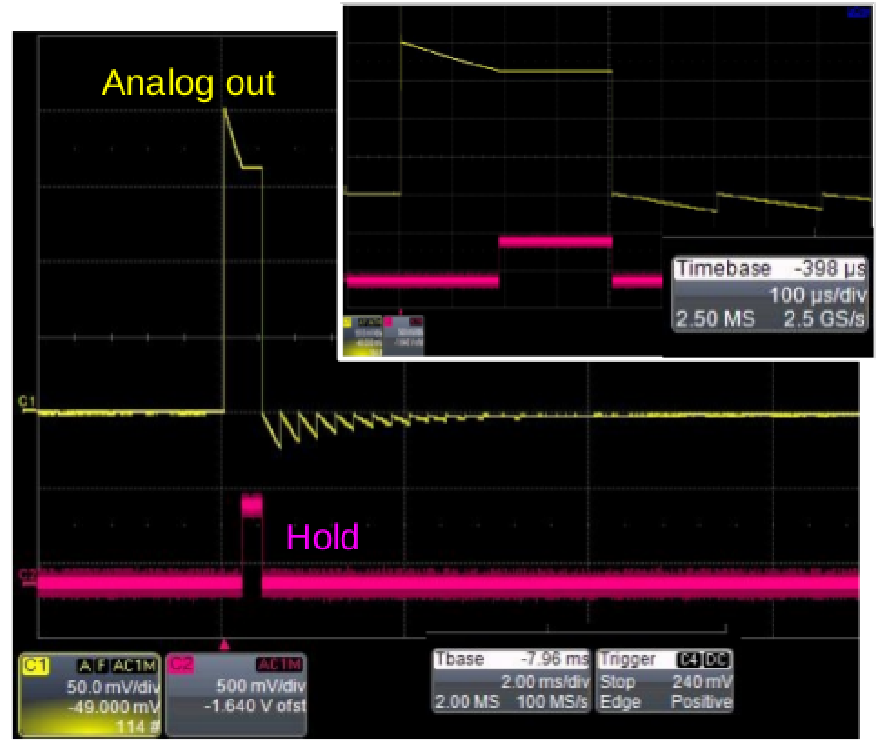
Note 2

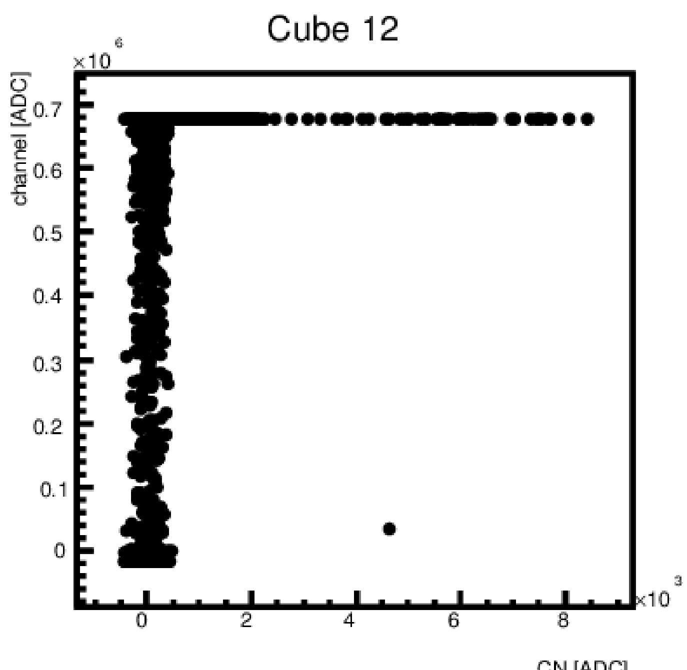
The time required to process and transfer one event to PC is about 1 ms, so **DAQ is limited to 1 kHz**

HiDRa chip Critical points

Input capacitance discharge

The RESET signal resets the capacitor in the CSA, but not the input capacitor, so that this is discharging with a time constant τ = 10 ms (1 ms in the old design): i.e., to avoid pile-up **the beam rate must be of the order of 100 Hz**.





Electrical Cross Talk

When Large PD saturates, there is an electrical crosstalk with other channels connected to the same half-Scolopendra (1 disconnected channel, 1 channel for CN computation, 6 Large PD and 6 Small PD), so that **we need to study in laboratory how much is this effect and eventually to apply correction for it**

ROC firmware

The ROC firmware did **NOT** have any problem so far, **BUT**...:

- <u>the HiDRa calibration mode has not been implemented</u>
- <u>the usage of memory is really inefficient</u>

If, for some reason, we really want to **change the firmware** we need to write it again from the beginning, but this work can require **at least one full month of work.**

Considering that **this is not a critical point** and that we will have to write again the firmware once the new CIEMAT ROC will be available, **it doesn't worth the effort to do it now**.

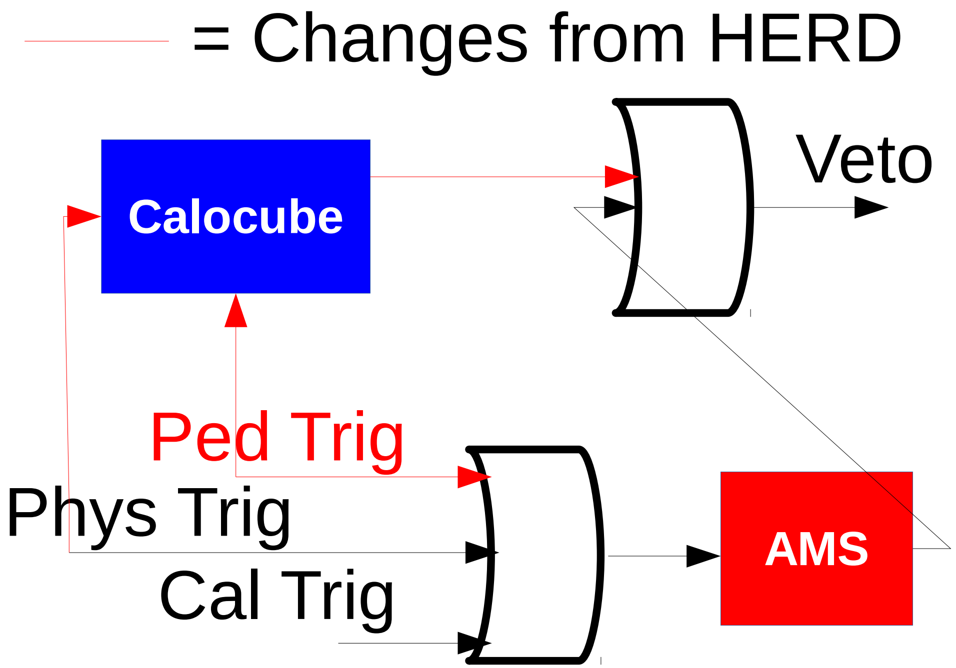
One important point is instead to **make new cables between ROC and HiDRA** because we observed that some connection is critical

DAQ

The Calocube-AMS common DAQ was tested during November 2017 SPS Beam Test.

Acquisition software

The Calocube acquisition software was inserted inside the AMS acquisition software



Trigger Logic

The trigger logic was slightly changed respect to the one used for HERD:

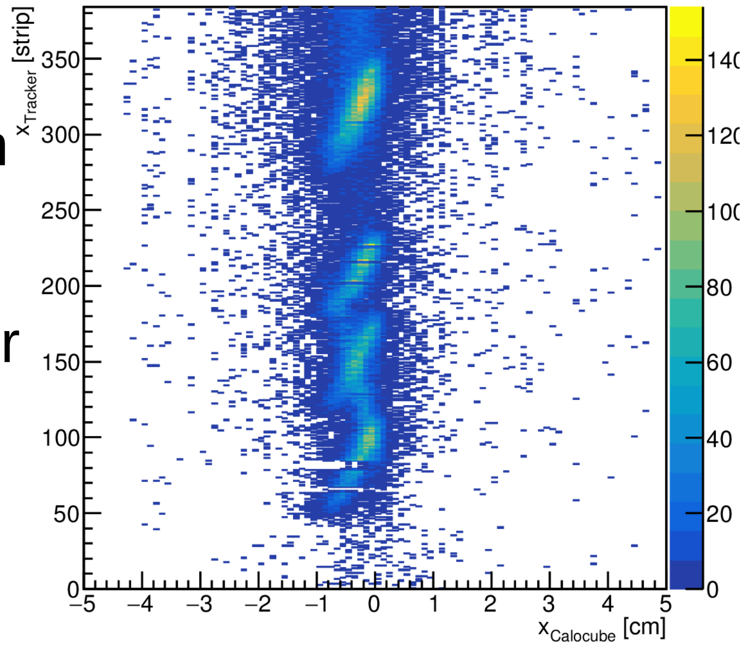
- add a 1 Hz pedestal trigger
- split pedestal and particle trigger entering the ROC
- add the ROC busy to make veto of the following triggers

Confirmation of event alignment

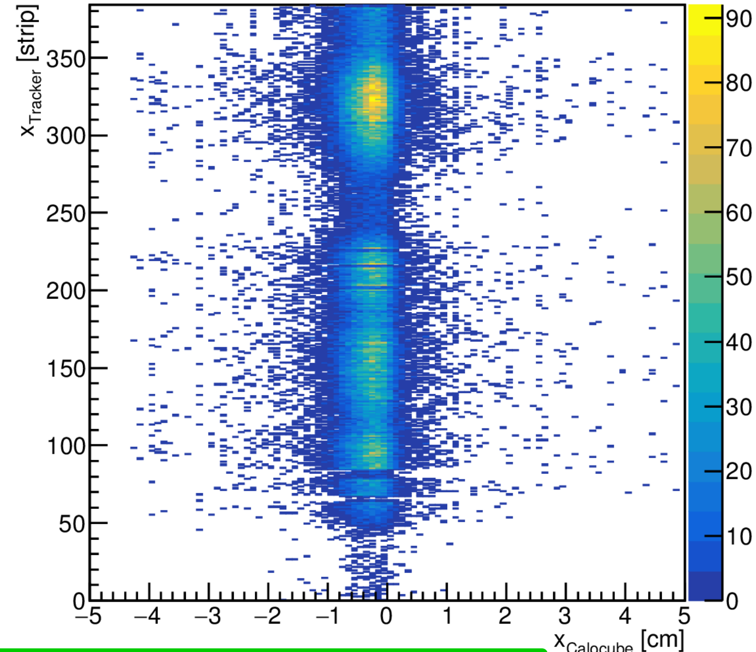
During data taking we observed a few events (<1%) with large delay (<10 ms) between AMS and Calocube trigger time. Even if we still have to check the alignment of these events, **the alignment was confirmed for the majority of events**.

Correlation between X position: AMS Strip VS Calocube Barycenter

The same event



One event offset



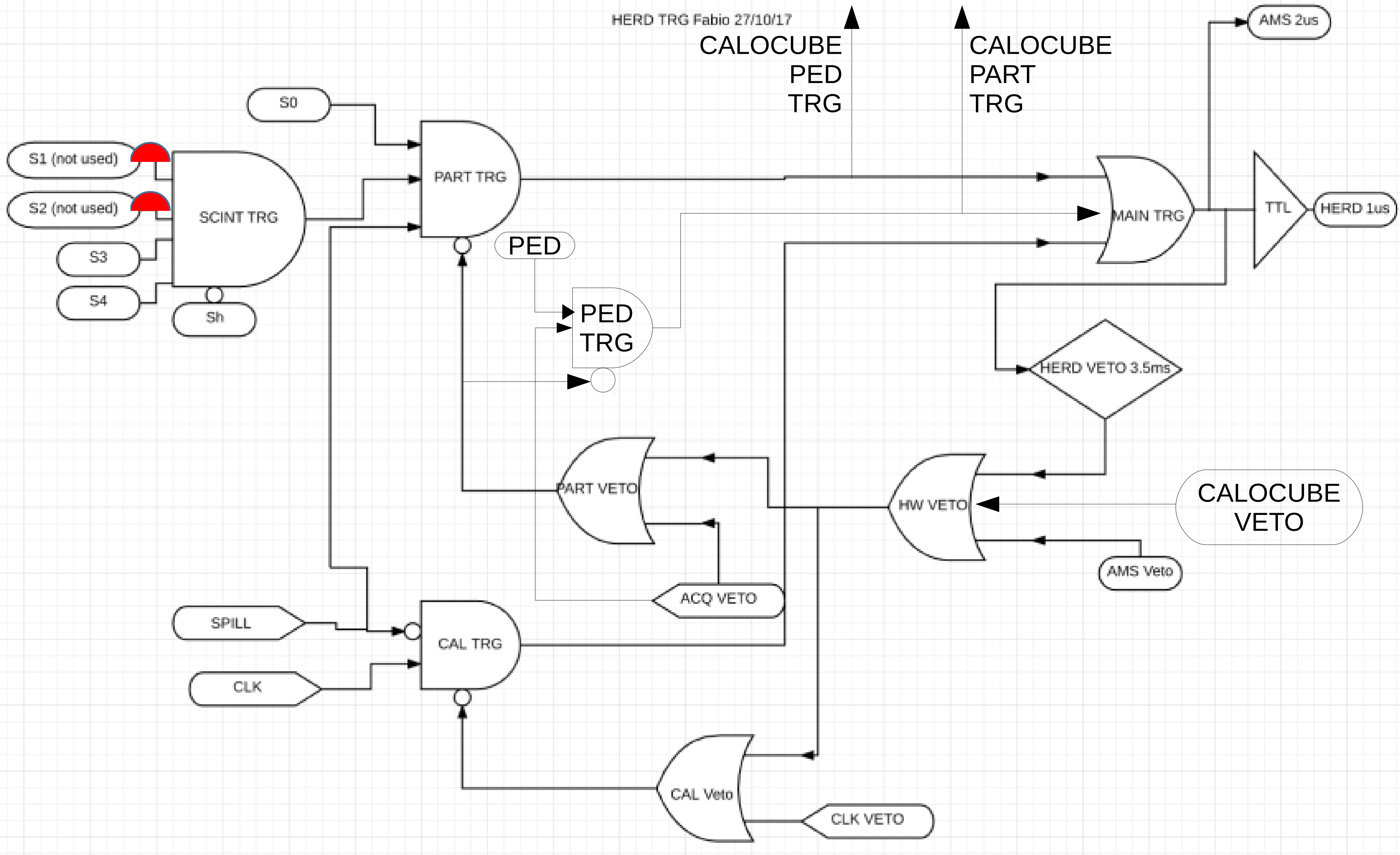
The main question about TIC DAQ is actually:
How to integrate the read-out of silicon ladders that will be installed inside TIC in the DAQ?

Summary

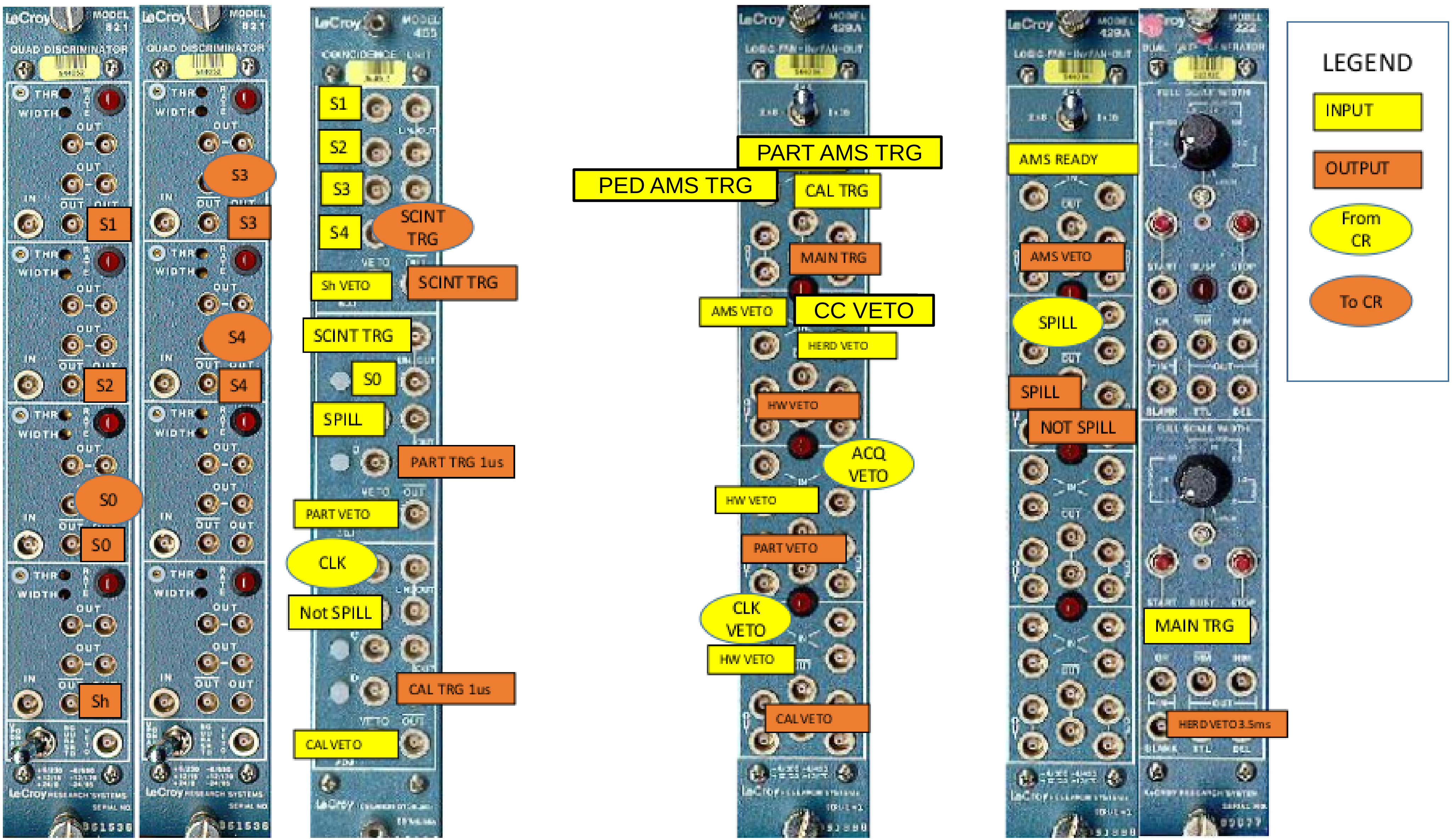
- Considering the TIC project, there is **no serious problem** in the current version of electronics and DAQ
- The main effort should be dedicated to **integrate in the DAQ the read-out of silicon ladders that will be installed inside TIC**
- If we have enough time it would be very nice to use the TIC project as a **chance to develop the Calocube read-out electronics**:
  1) Understanding which is the best solution for input capacitance discharge and electrical cross talk problems (making tests in lab)
  2) Testing the new HiDRa board together with the new ROC board (if they will be available before October 2018)

Back Up

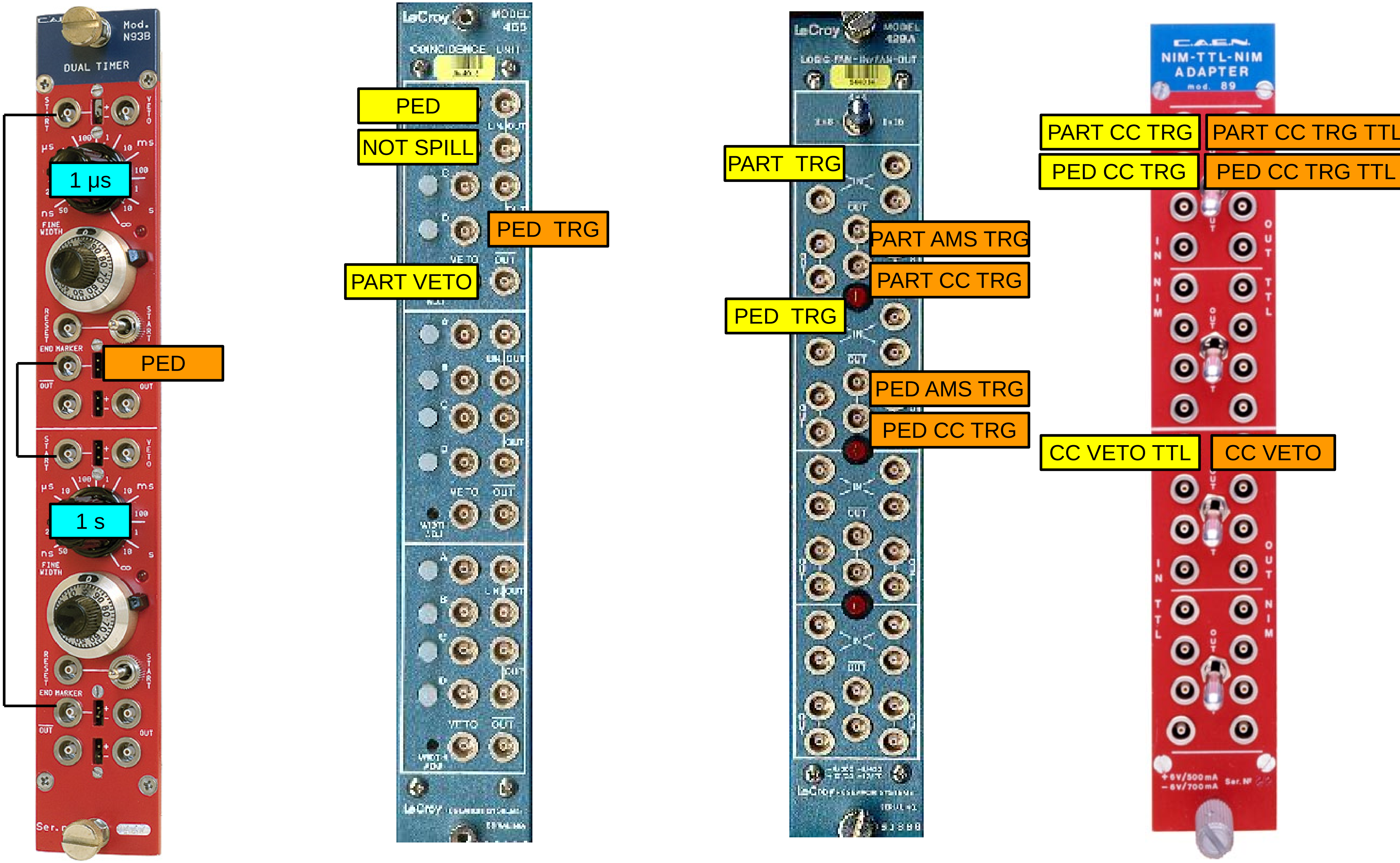
Trigger Logic (edited from Fabio)



Connections
Experimental Area (edited From Fabio)

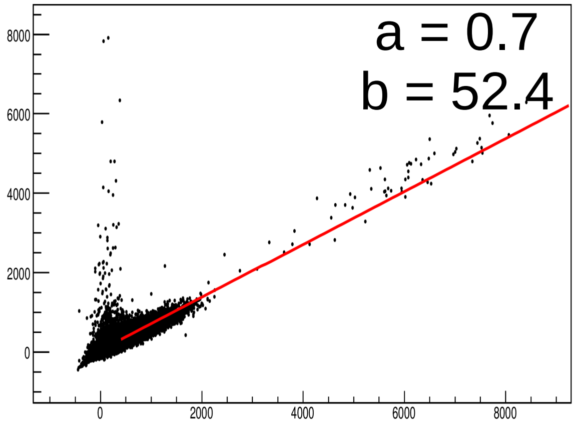


Connections
Calocube Section

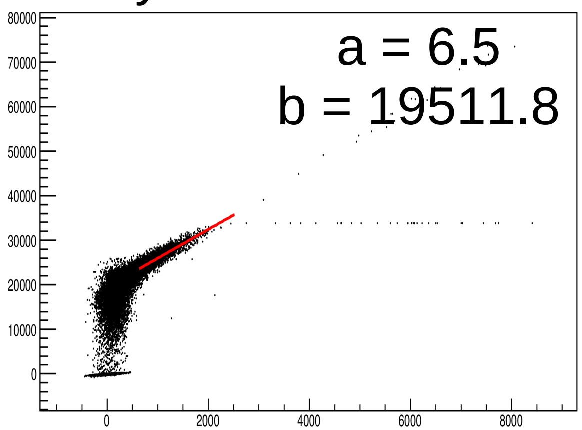


Check Correlation value in Small sensor

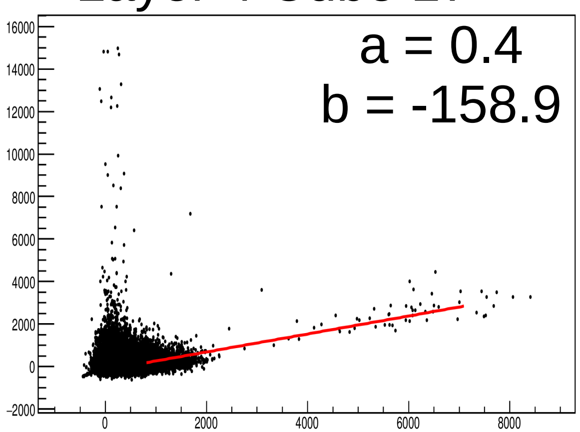
Layer 4 Cube 7



Layer 4 Cube 12



Layer 4 Cube 17



$y = ax + b$

In a simplified model we expect that the signal on a given cube is

$S[ADC] = G_S\, S[MIP] + CT[ADC]$

Making the following assumption

$CT[ADC] = \alpha\, CN[ADC]$

$CN[ADC] = \beta\, G_C\, C[MIP]$

$S_S[MIP] = \gamma_S\, C[MIP]$

leading to

$S[ADC] = [(\gamma_S/\beta) * (G_S/G_C) + \alpha\, CN[ADC]$

Even considering cube with the same energy release (7, 17) γ_S is the same, but G_S is different so that the angular coefficient is different.

Assuming α=1 we can roughly say that cross-talk on Small PD is about 3-5% for cube 12 and 50-75% for cube 7 and 17 !?