WP1: Design and test of 3D Si sensors for fast timing

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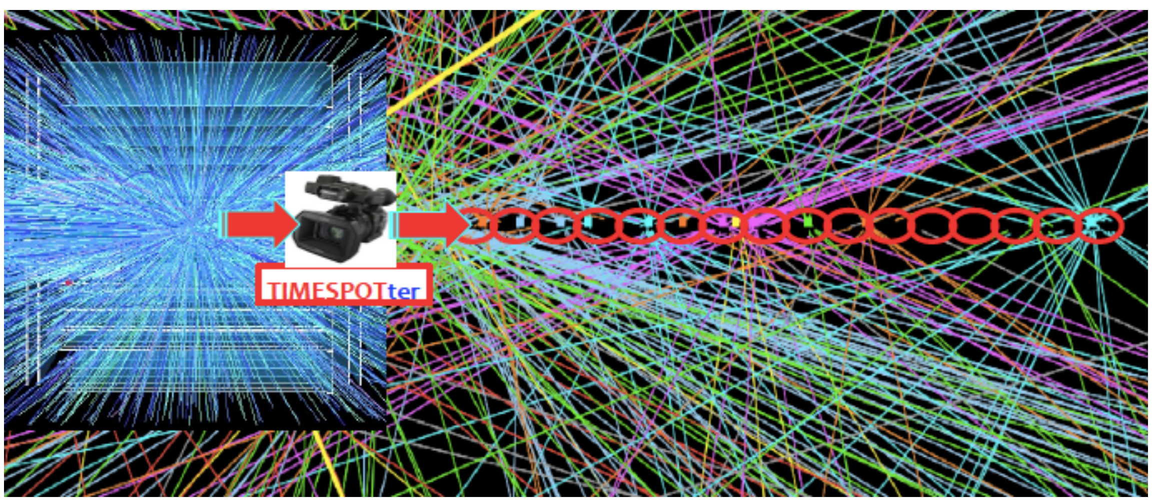

Kickoff Meeting
TIMESPOT
Cagliari
December 1, 2017

Outline

- Introduction to 3D Si sensors
    - Technology
    - Intrinsic features
- Where are we now ?
- How to address timing issues ?
- Workplan for 2018

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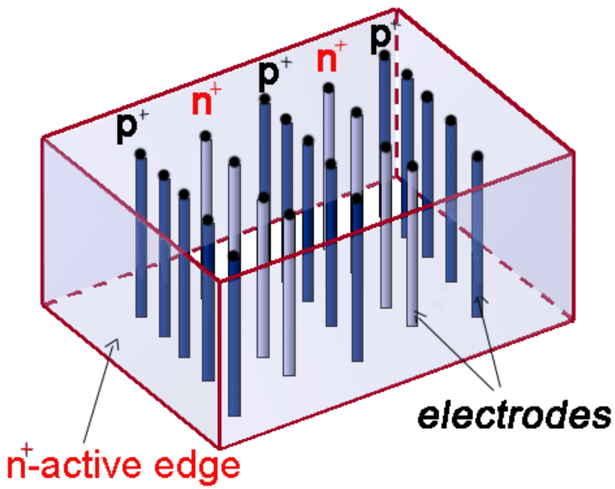
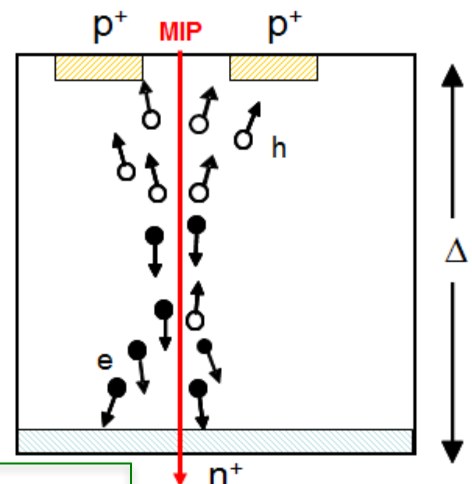
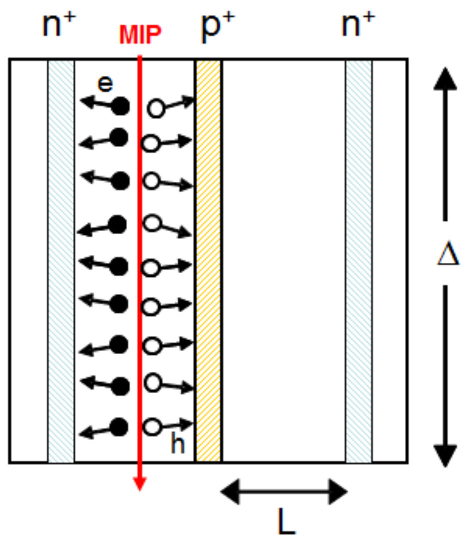
3D sensors

S. Parker et. Al. NIMA 395 (1997) 328

Electrode distance (L) and active substrate thickness (Δ) are decoupled → L<<Δ by layout







ADVANTAGES:

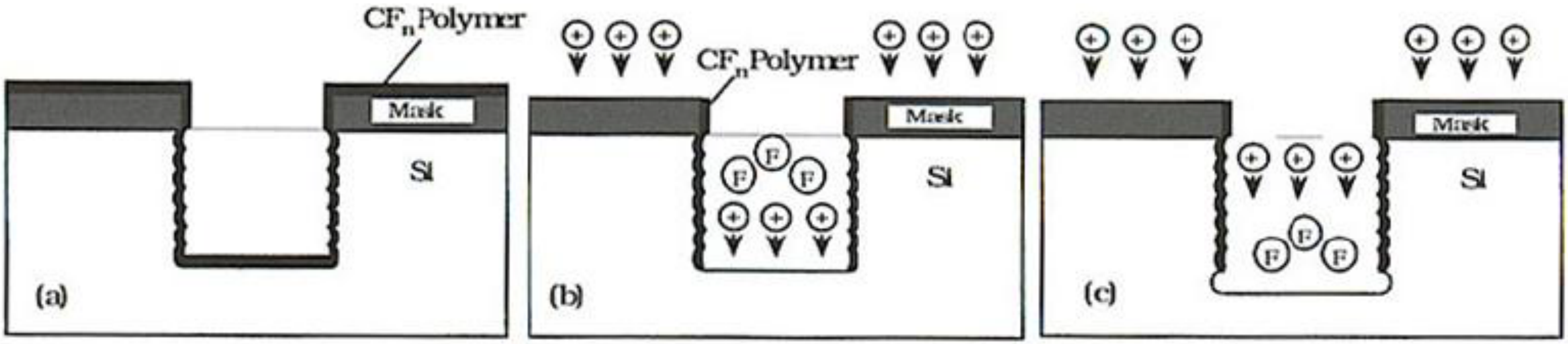
- Low depletion voltage (low power diss.)
- Short charge collection distance:
  - Fast response rise
  - Less trapping probability after irr.
- Lateral drift → cell "shielding" effect:
  - Lower charge sharing
  - Low sensitivity to magnetic field
- Active edges

→ **HIGH RADIATION HARDNESS**

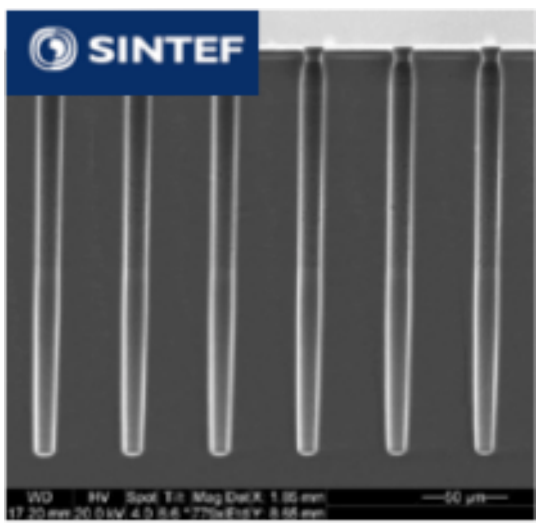
DISADVANTAGES:

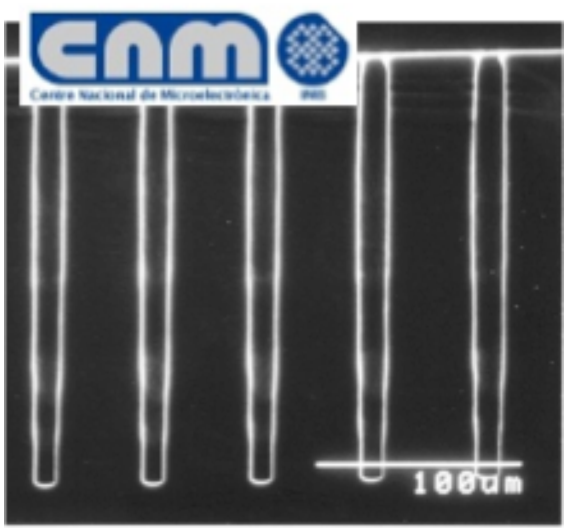
- Non uniform spatial response (electrodes and low field regions)
- Higher capacitance with respect to planar (~3-5x for ~ 200 μm thickness)
- Complicated technology (cost, yield)

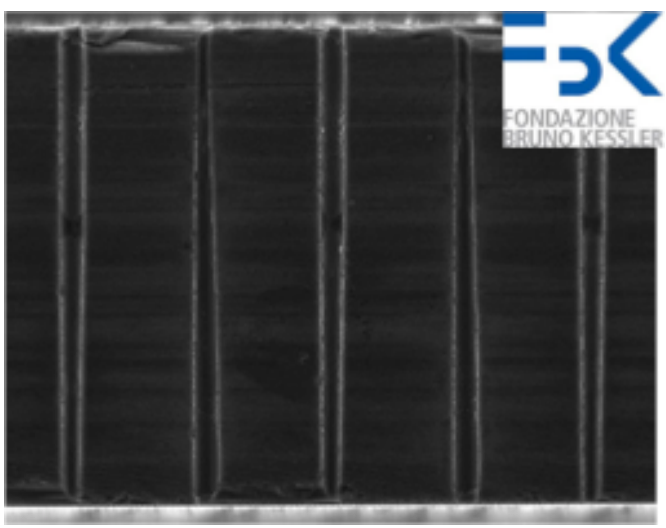
Key technology: DRIE by the Bosch process



- Alternating etch cycles (SF_6) and passivation cycles (C_4F_8)
- High aspect ratio (>20:1 or better for trenches) and good uniformity



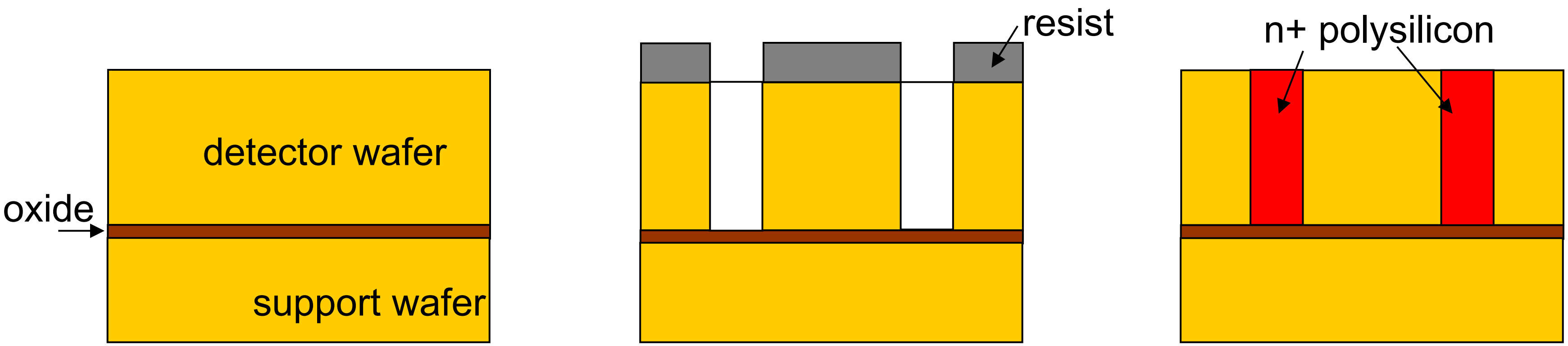




Full 3D with active edge

3D Consortium
The Stanford Nanofabrication Facility
SINTEF

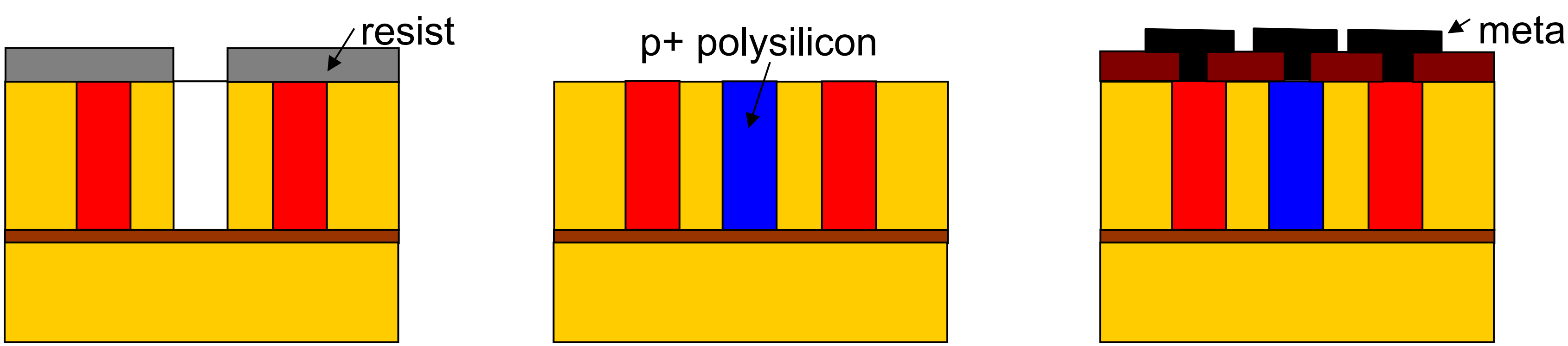
C. Kenney et al., IEEE TNS, vol. 46, n. 4 (1999) 1224
T.E. Hansen et al., JINST 4 (2009) P03010



1) wafer bonding

2) n+ hole definition and etching

3) hole doping and filling



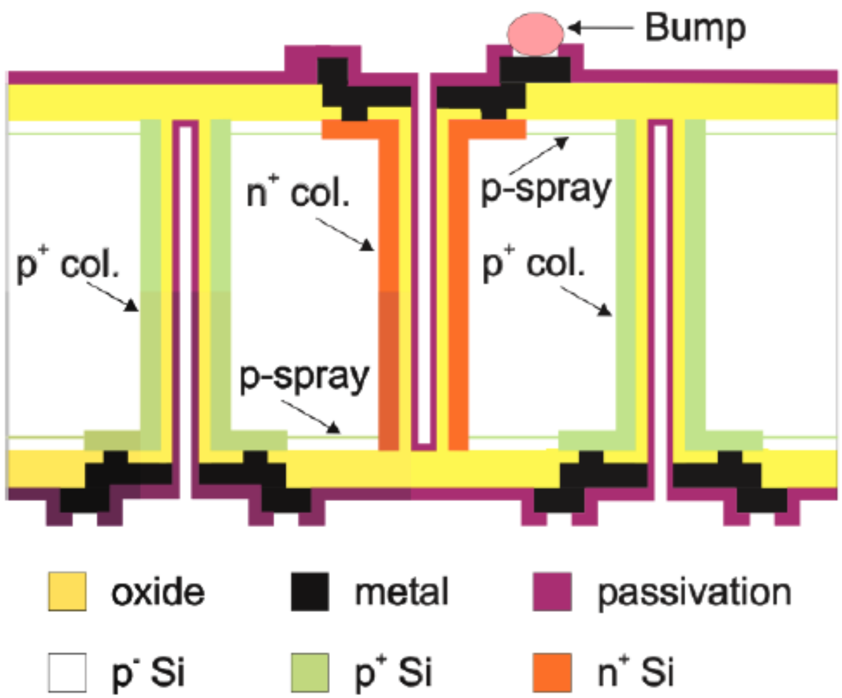
4) p+ hole definition and etching

5) hole doping and filling

6) Metal deposition and definition

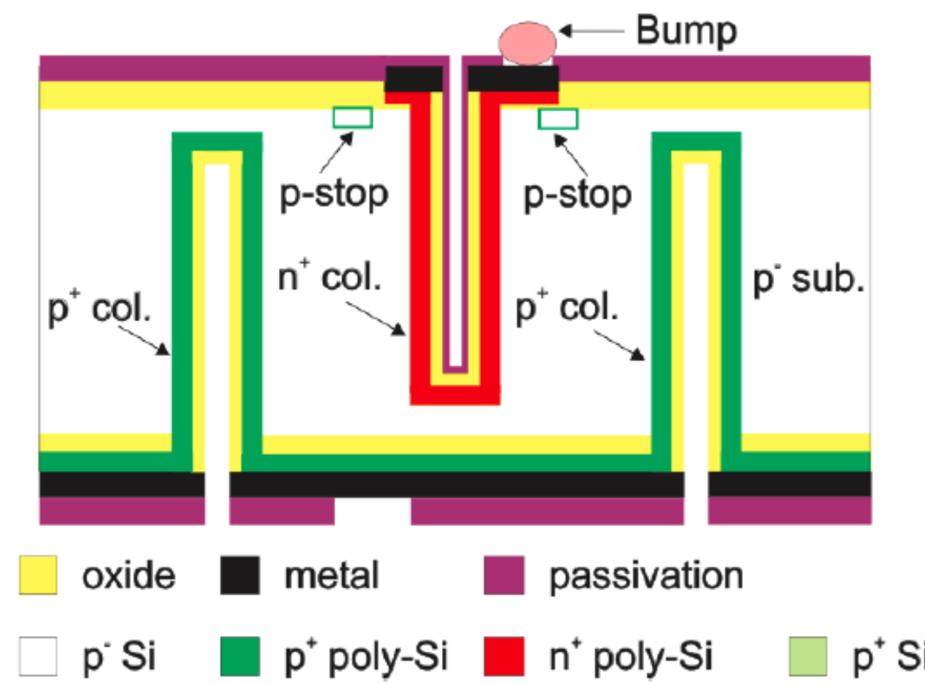
Double-sided 3D sensors

FBK (Trento, Italy)



A. Zoboli et. al., IEEE TNS 55(5) (2008), 2775
G. Giacomini, et al., IEEE TNS 60(3) (2013) 2357

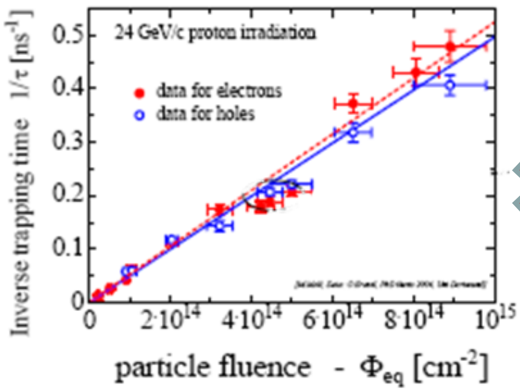
CNM (Barcelona, Spain)

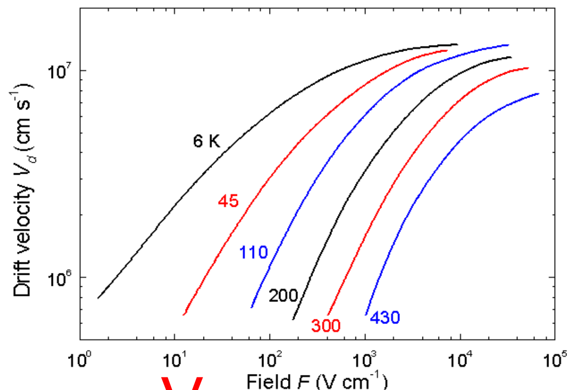


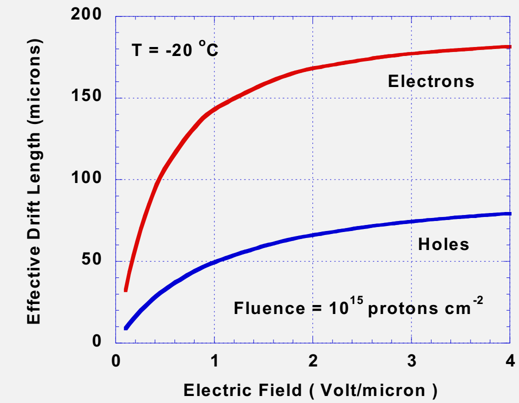
G. Pellegrini et. al. NIMA 592(2008), 38
G. Pellegrini et. al. NIMA 699(2013), 27

- Do not use support wafer → reduced process complexity
- Back-side accessible → Easier assembly within a detector system
- Active edge not feasible → Slim edge

Charge trapping and inter-electrode spacing







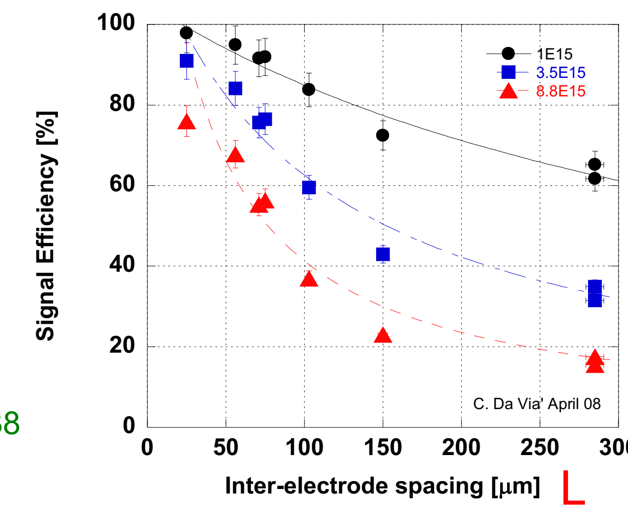
τ_{tr} Trapping Times × V_n Drift Velocity = λ Effective drift length

$$\frac{dS}{dt} = q\frac{dV_W}{dx}\frac{dx}{dt}\exp(-\frac{x}{\lambda})$$

$$S = \frac{\lambda}{L}\left[1-\exp(-\frac{L}{\lambda})\right]$$

Expected signal efficiency after irradiation (without multiplication) depends on λ/L

$$SE = \frac{1}{1+0.6L\dfrac{K_\tau}{v_D}\Phi}$$

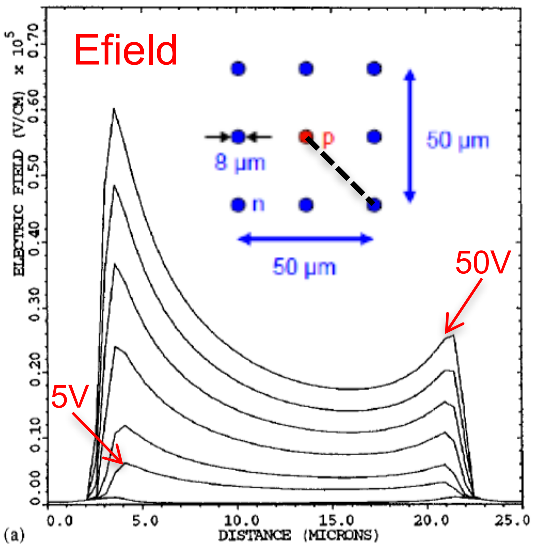


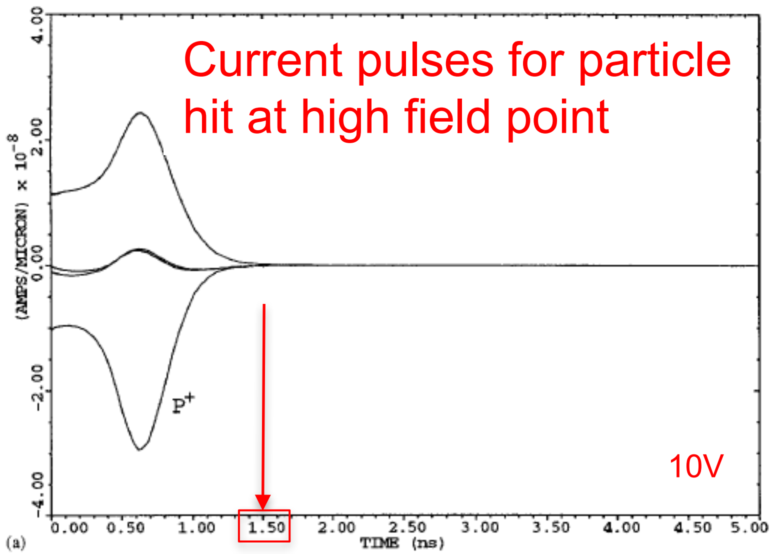
L

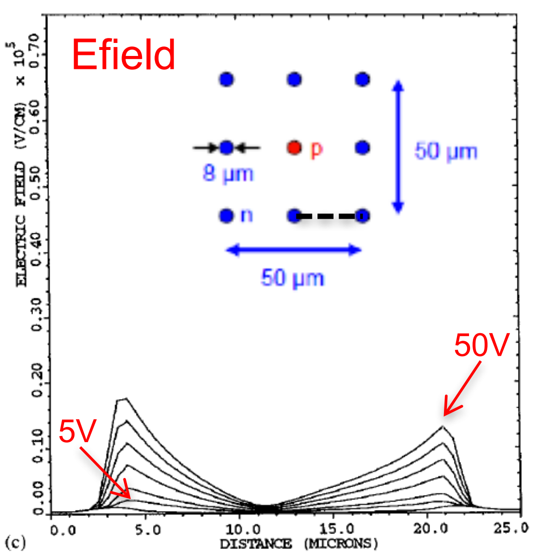
Trapping times from G. Kramberger et al, NIMA 481 (2002) 100, NIMA 501 (2003) 138

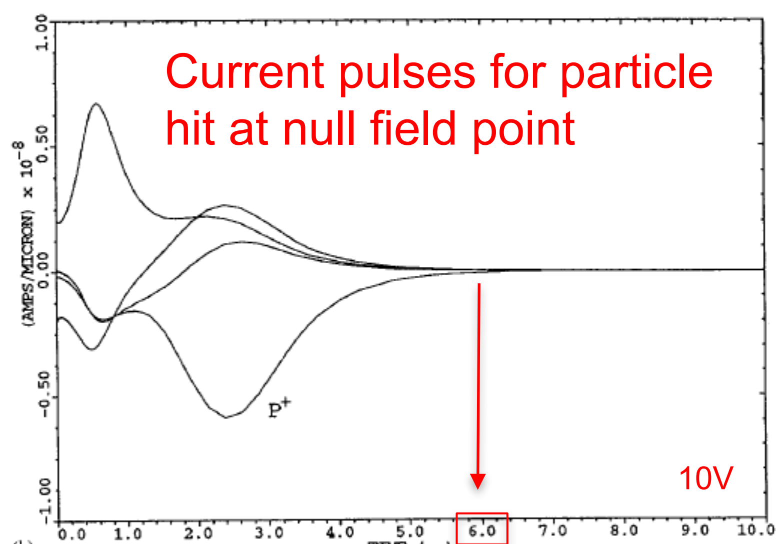
Calculations from C. Da Via, NIMA 603 (2009) 319

Null field points and delayed signals





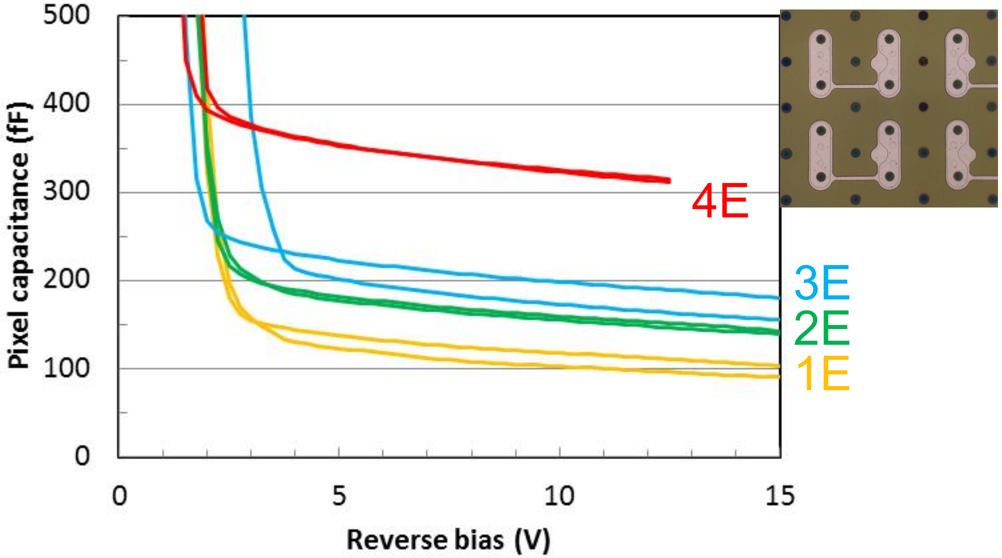




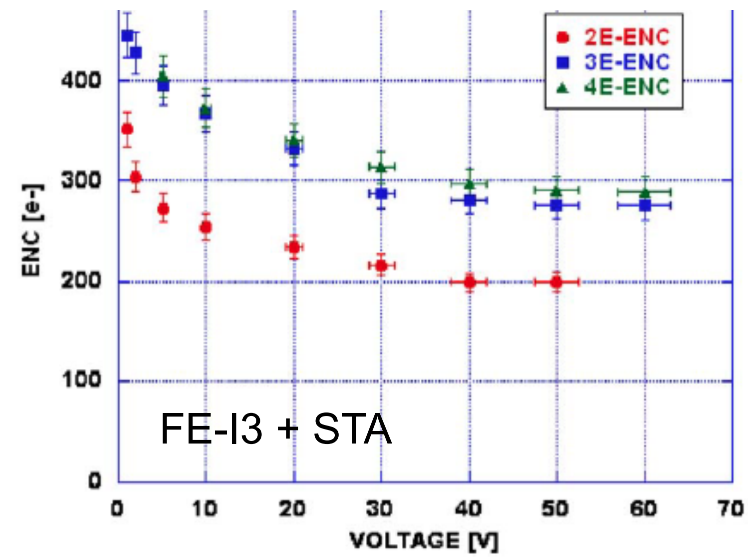
S. Parker et al. NIMA395 (1997) 328

- 3D structure can potentially yield very fast signals of the order of 1 ns
- But electric field is not uniform, and null field points are present: signals are delayed due to initial diffusion
- Moreover, electrodes are (almost) dead regions
- These aspects can be improved with dedicated designs

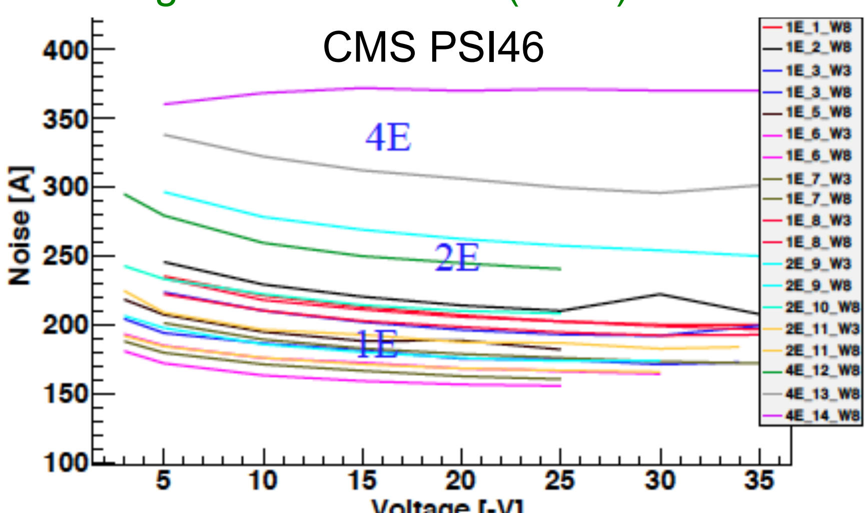
Capacitance and noise

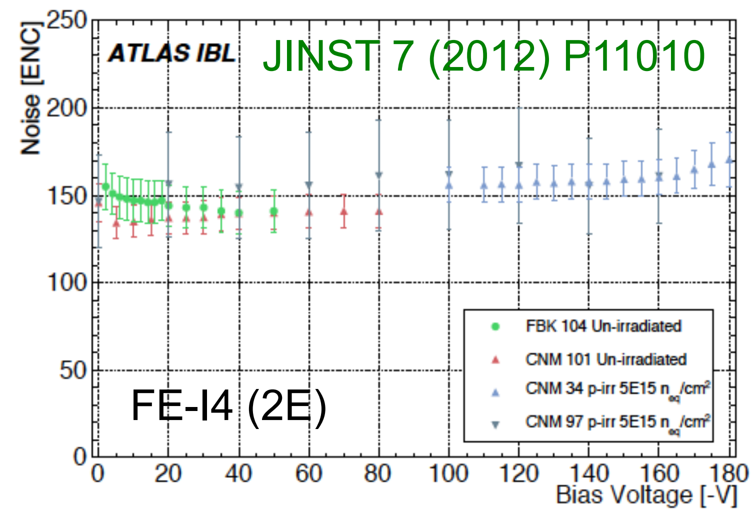


C. Da Via et al. NIMA 604 (2009) 505



E. Alagoz et al. JINST 7 (2012) P08023

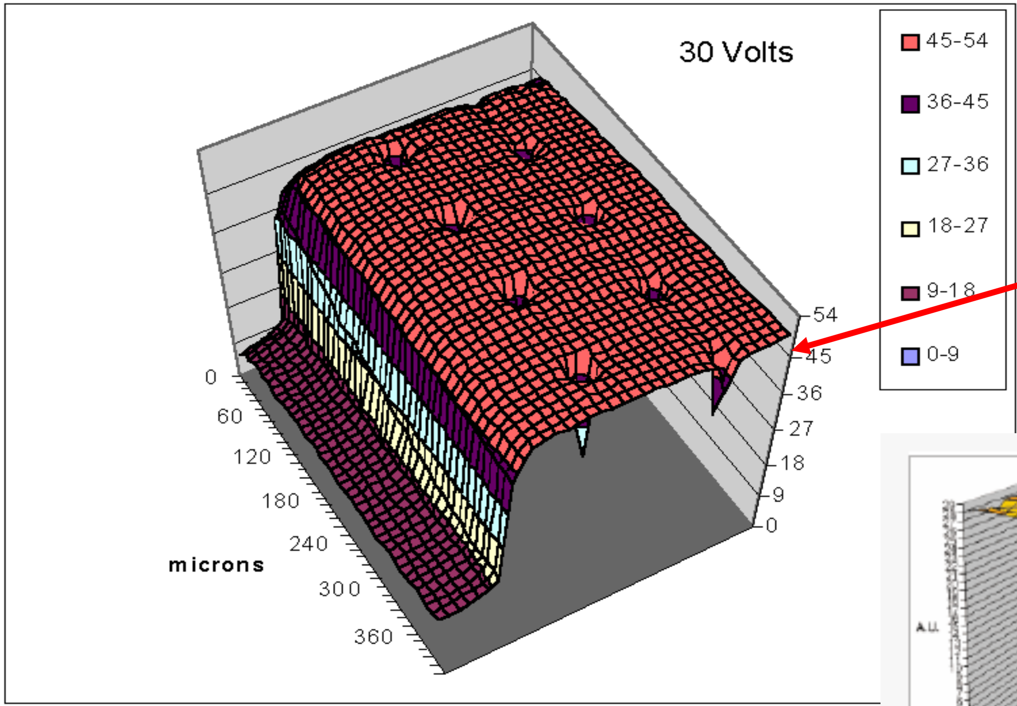


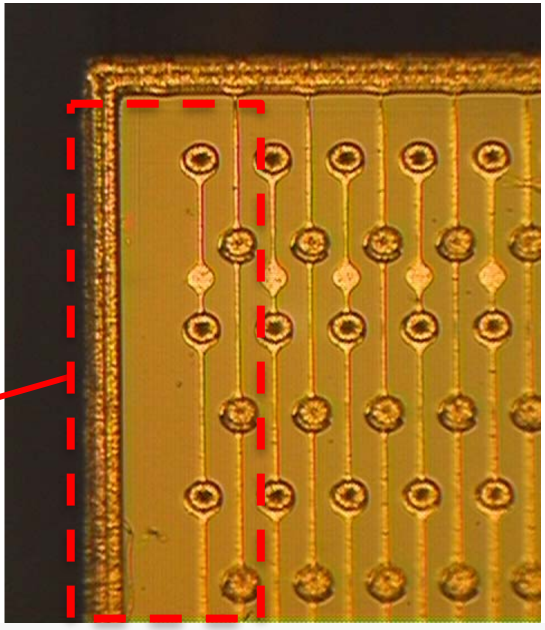


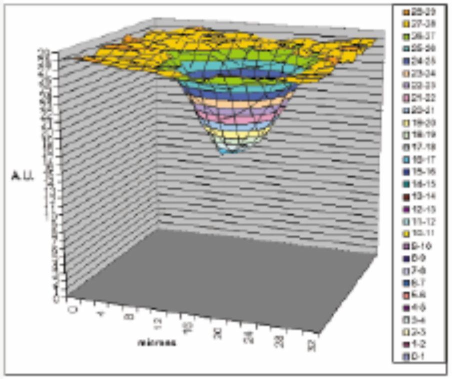
Poly-Si electrode inefficiency

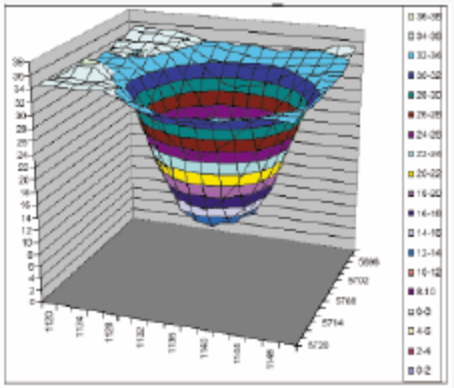
J. Hasi, PhD thesis, Brunel, 2004

Electrode response using 12 keV X-ray beam (ALS at LBNL), beam size ~ 2µm









- Diffusion, lifetimes (poly-Si grain sizes)
- Oxide barrier effect at the interfaces …
  - → Replace $POCl_3$ with PH_3
  - → Replace BBr_3/O_2 with B_2H_6

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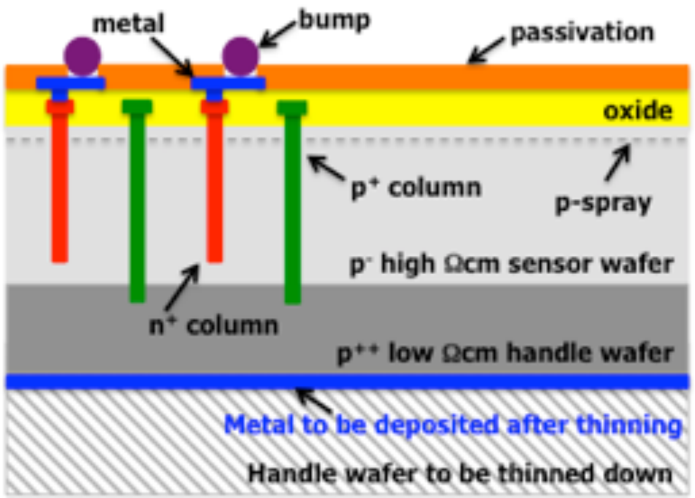
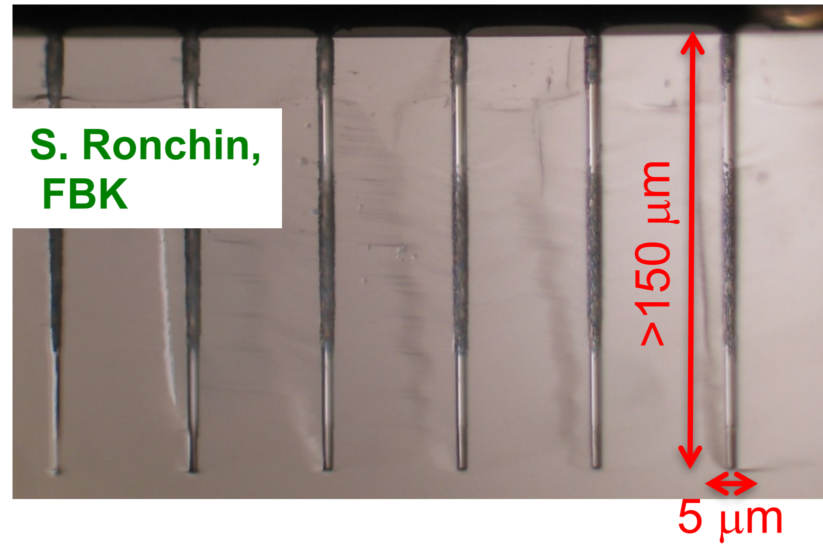
3D technology at FBK

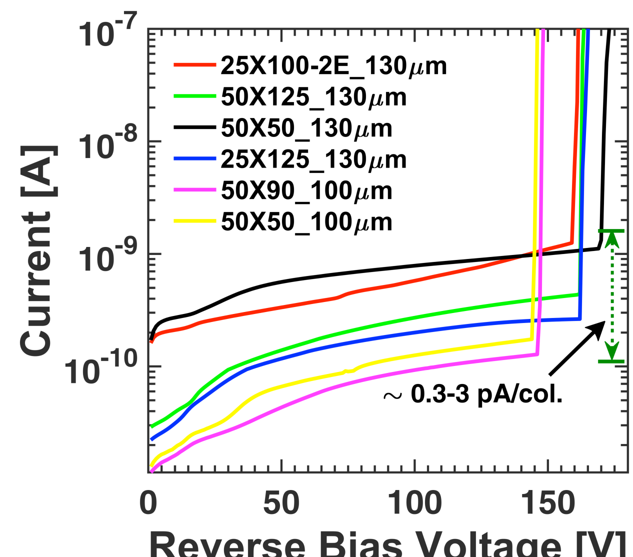
Project INFN-FBK "RD_FASE2"



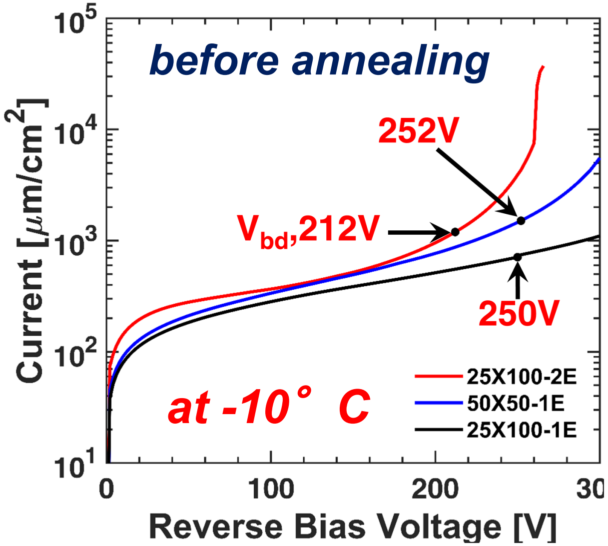


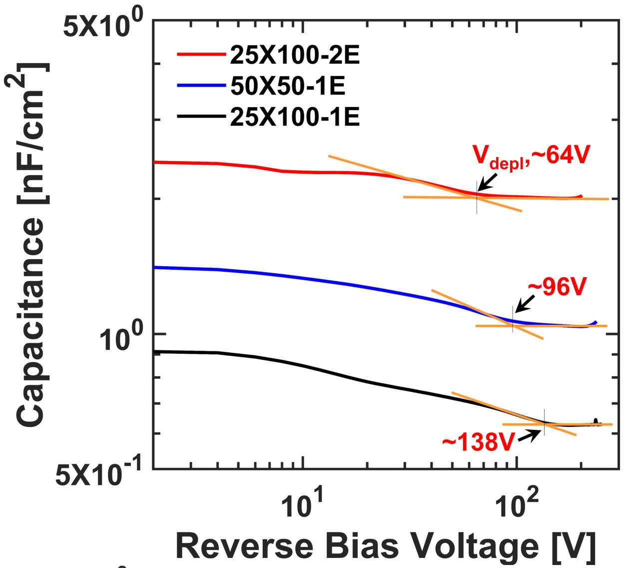
- Very impressive progress made in the past few years for small pitch 3D sensors oriented to HL-LHC
- Back to single-sided process with back-side bias
- Flexibility in the choice of active thickness and inter-electrode distance
- High breakdown voltage can be achieved also before irradiation, allowing for large V_{bias} range

(in good agreement with TCAD simulations)



3D diode proton irradiation





Fluence $1.3x10^{16}$ n_{eq}/cm^2

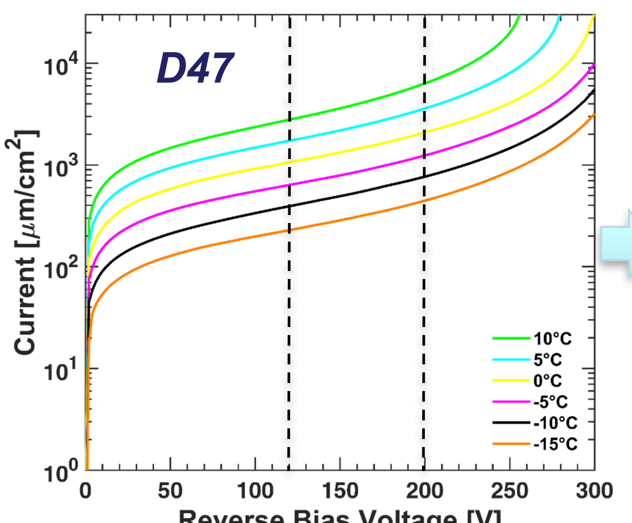
ITk target …)

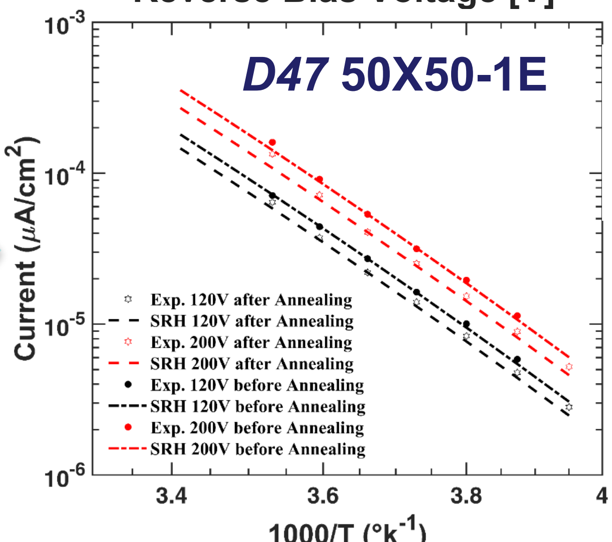
V_{bd} and V_{depl} increase

V_{bd} >> V_{depl})

Current increase as exp.

α close to std values)

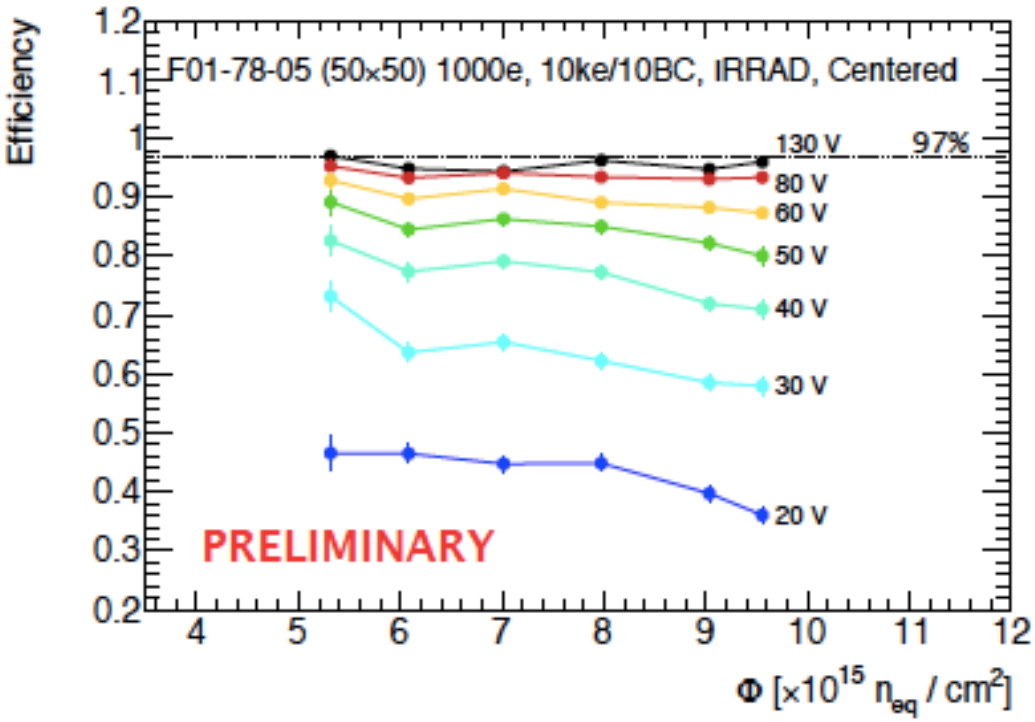


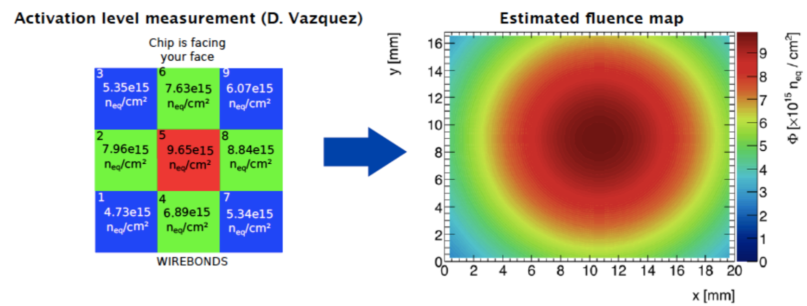


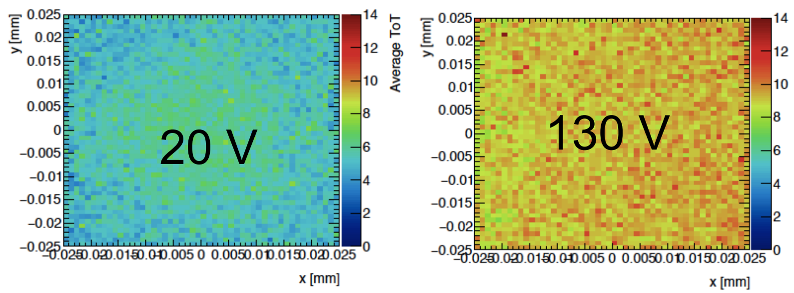
$$I(T) = I(T_R)\cdot\left(\frac{T}{T_R}\right)^2\cdot\exp\left[\frac{E}{2k_B}\cdot\left(\frac{1}{T_R}-\frac{1}{T}\right)\right]$$

- I(T) follows SRH trend
- Current decrease (1.5x) after annealing

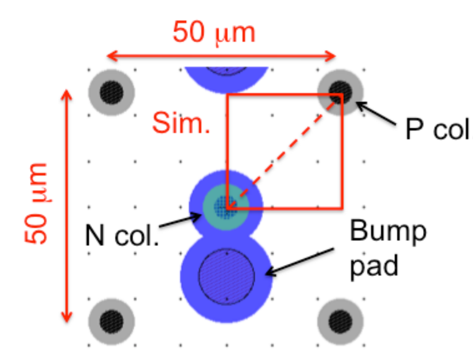
Test beam results on irradiated pixels







- 50x50 μm^2 pixels with FEI4 read-out
- Non uniform proton irradiation at CERN IRRAD
- Low threshold (1000 e^-) operation feasible
- At 130 V high efficiency (~97%) at all fluences, close to the geometrical limit for un-tilted particles
- The average efficiency saturates at ~97 % below 100 V bias
- The collected charge is uniform within the pixel



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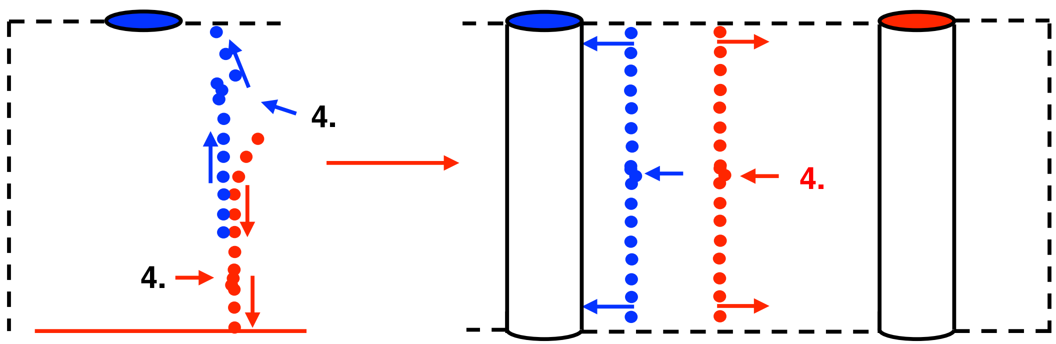
Timing: planar vs 3D



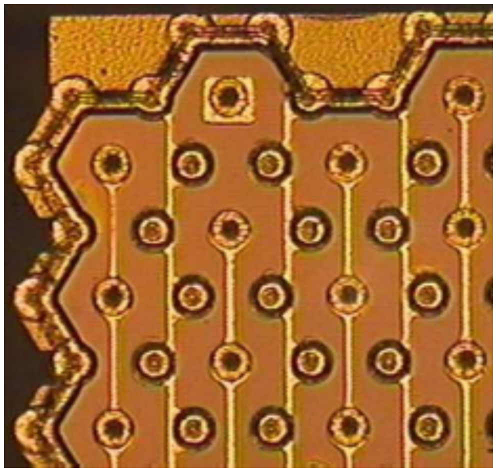
1. 3D lateral cell size can be smaller than wafer thickness, so
2. in 3D, field lines end on electrodes of larger area, so
3. most of the signal is induced when the charge is close to the electrode, where the electrode solid angle is large, so planar signals are spread out in time as the charge arrives, and
4. Landau fluctuations along track arrive sequentially and may cause secondary peaks

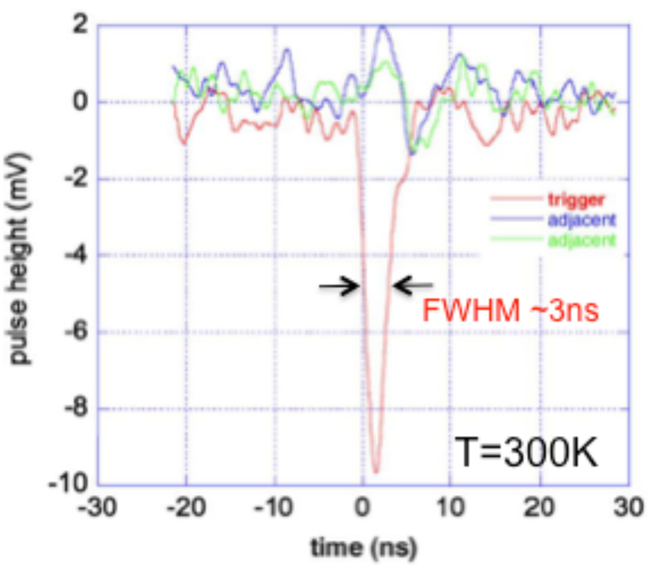
1. shorter collection distance
2. higher average fields for any given maximum field (price: larger electrode capacitance)
3. 3D signals are concentrated in time as the track arrives
4. Landau fluctuations (delta ray ionization) arrive nearly simultaneously

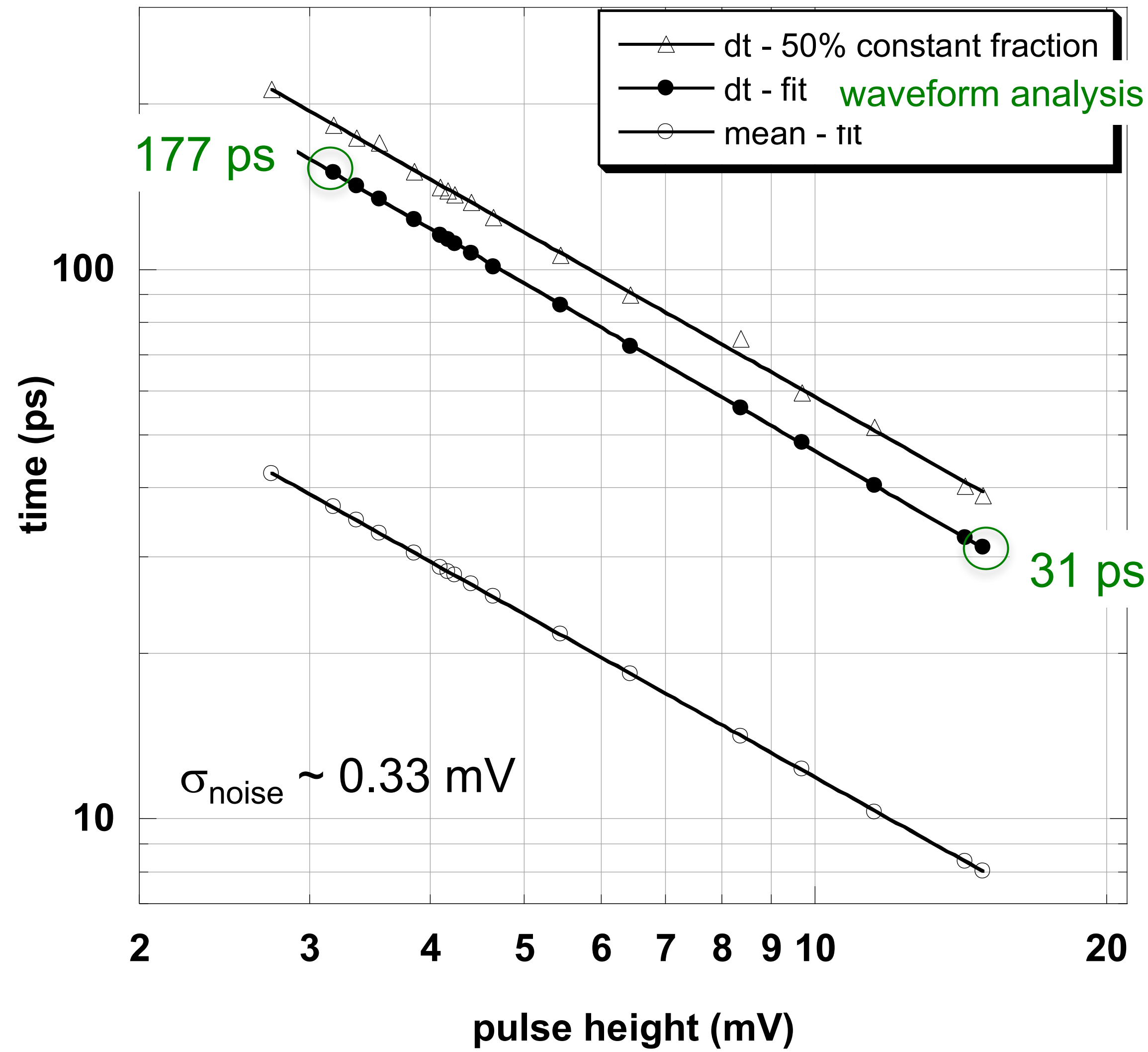
Timing with 3D

S. Parker et al. IEEE TNS 58(2) (2011) 404

So far tested with hex-cell 3D's (L=50μm) & fast current amplifier

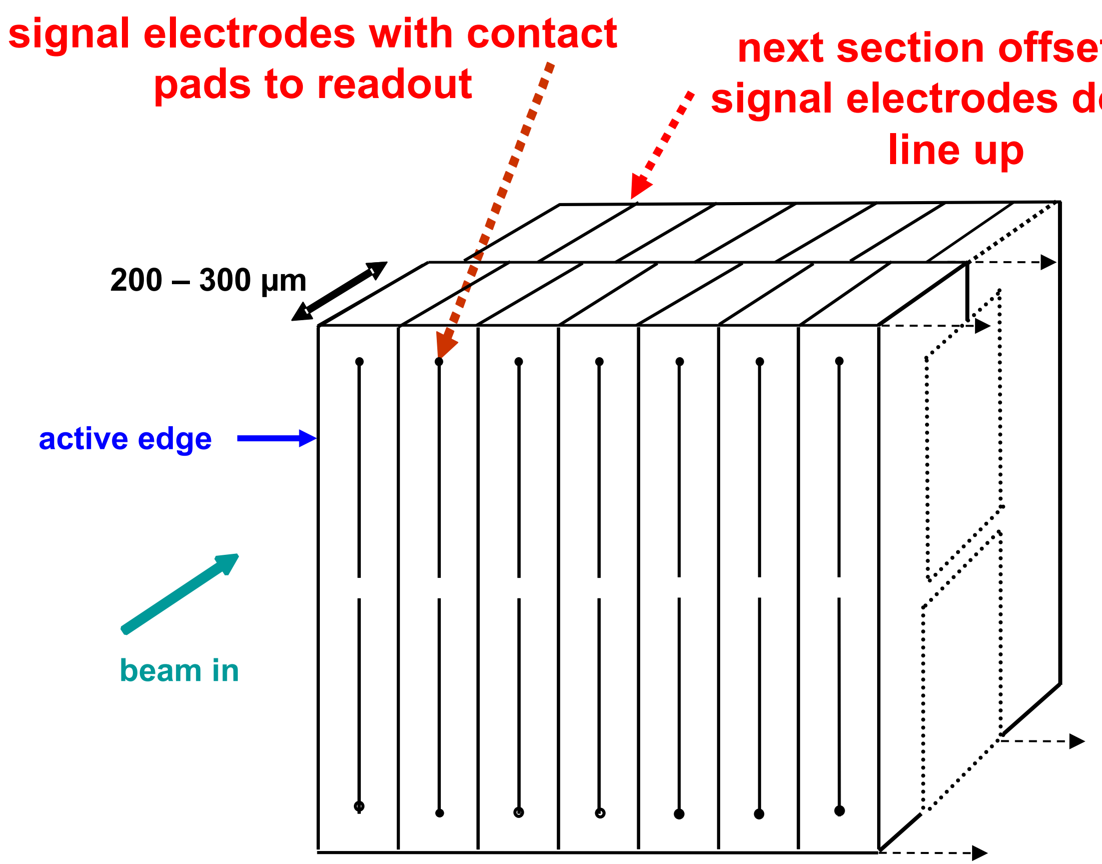




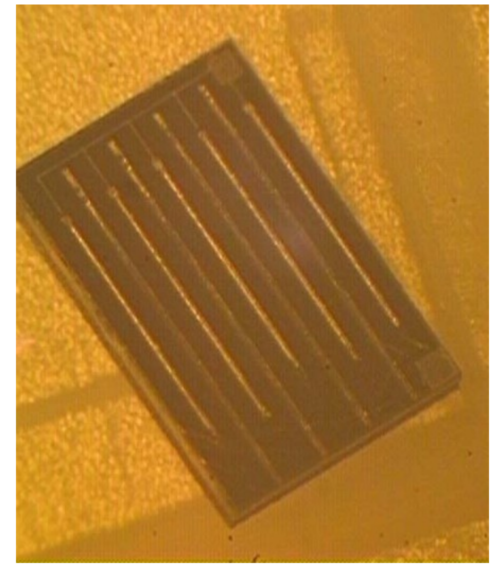


Trench-electrode sensors

S. Parker et al. IEEE TNS 58(2) (2011) 404



Schematic diagram of multiple plane arrangement in an active-edge 3D trench-electrode detector. Other offsets (⅓, ⅔, 0, ⅓, ⅔ ..etc.) may also be used.



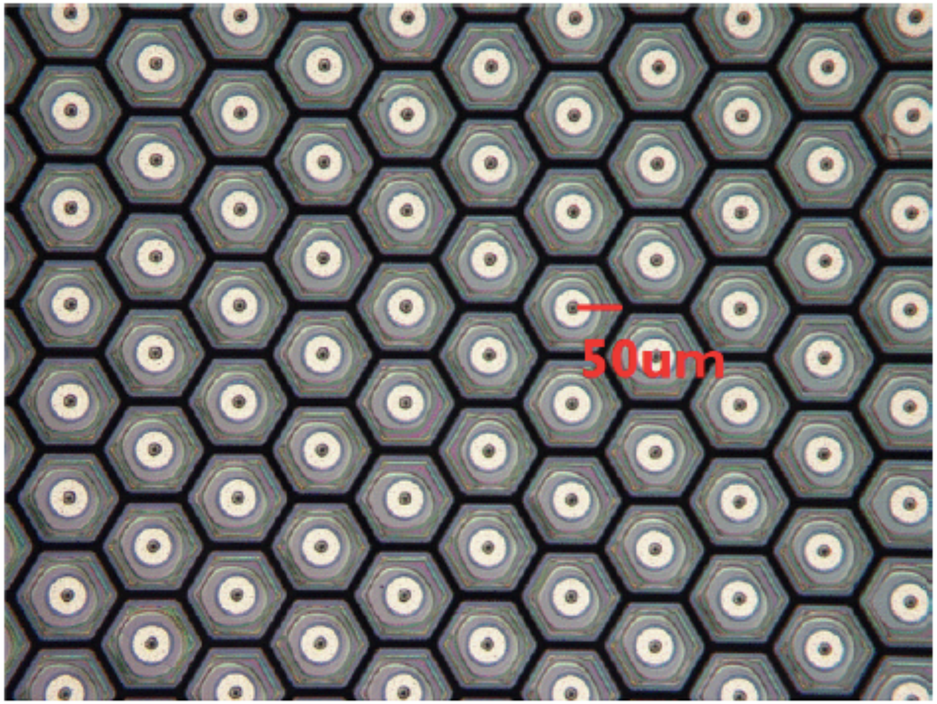
Benefits from trench electrodes

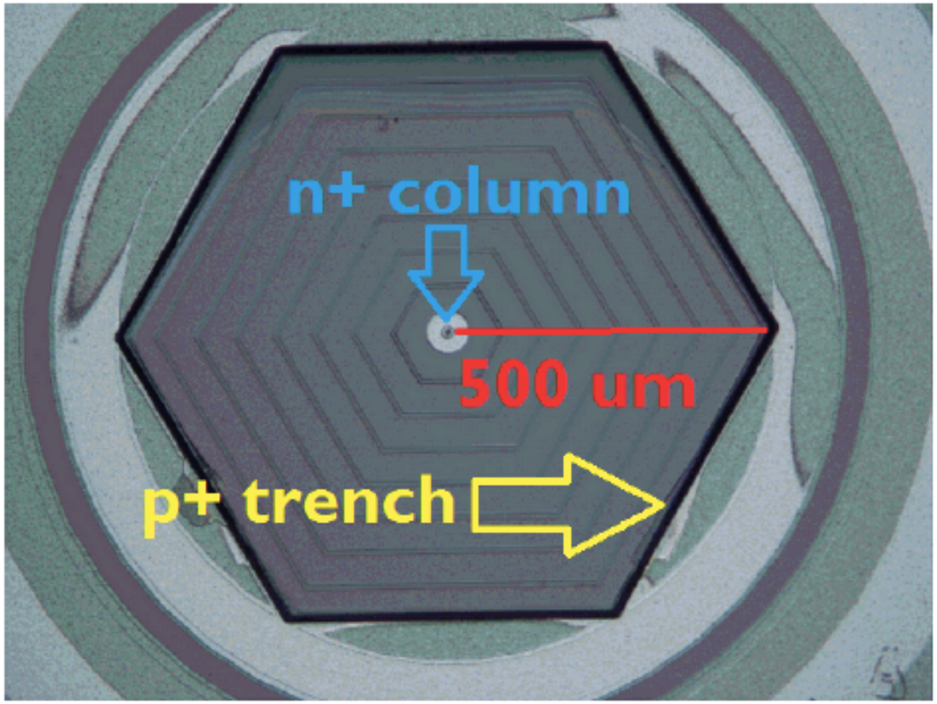
- High average field / peak field
- Uniform Ramo weighting field
- Initial pulse time independent of the track position

Possible issues

- Fabrication complexity
- Capacitance

Trench-electrode pixels at BNL-CNM



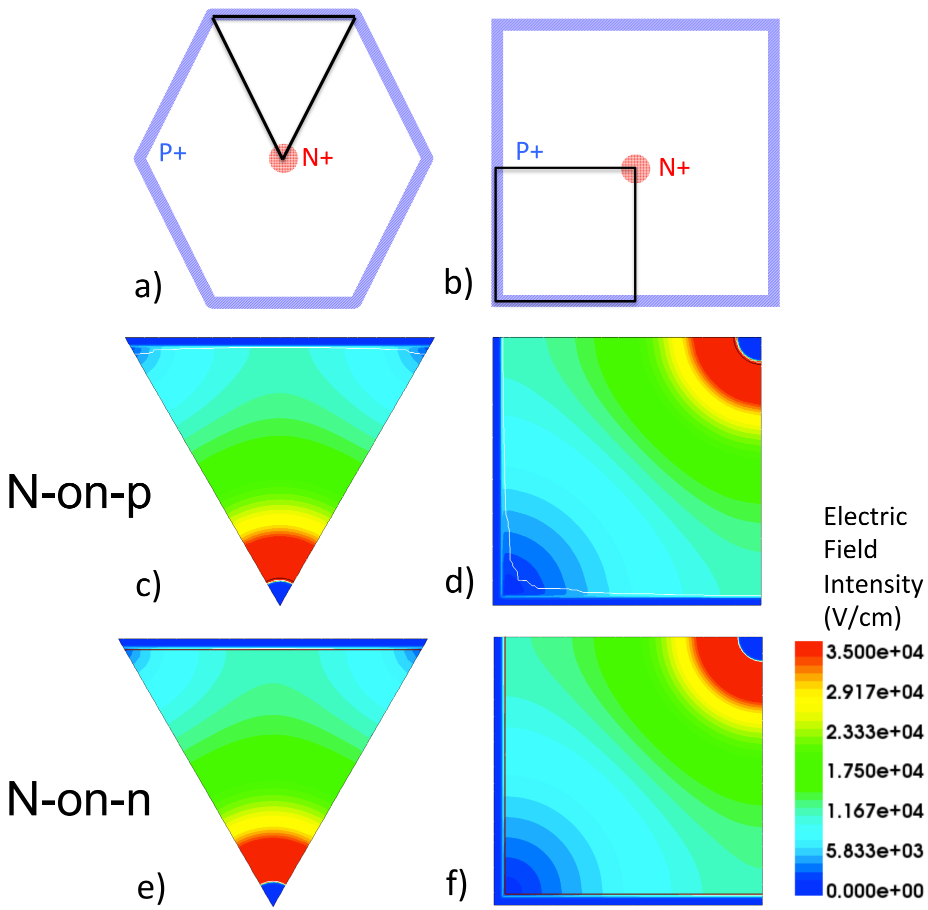


- Designed and simulated by BNL and Stony Brook University
- 1st batch fabricated at CNM Barcelona in 2013
- High leakage currents
- Charge collection tests performed on large pixels only
- 2nd batch announced in 2014 …

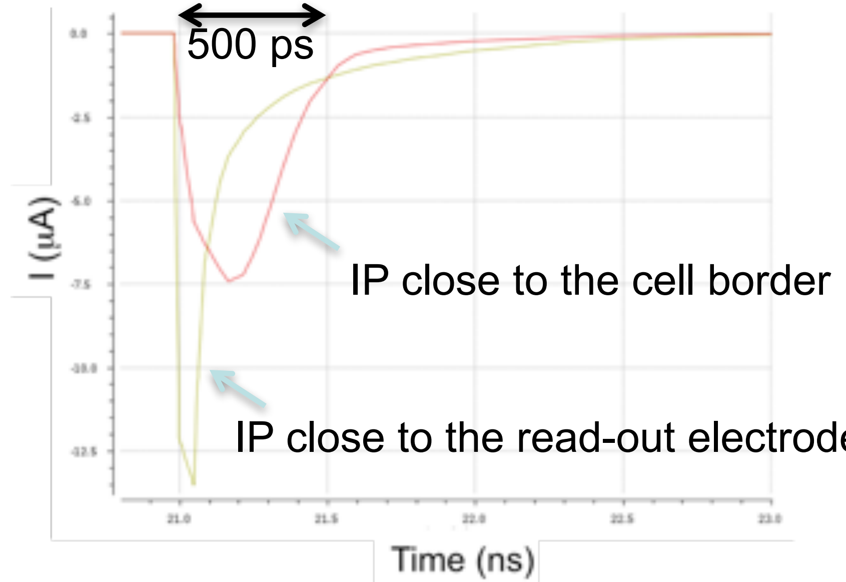
A. Montalbano et. al. NIMA 765 (2014), 23

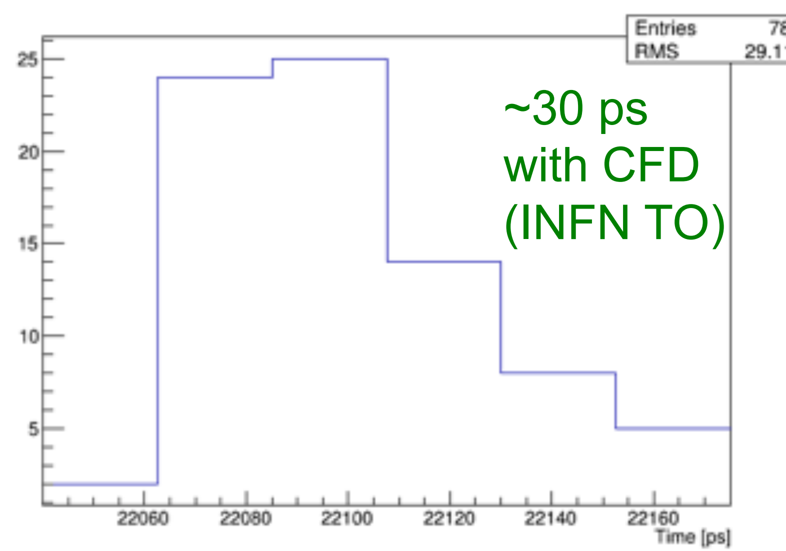
Trench-electrode simulations (1)

Considered layouts



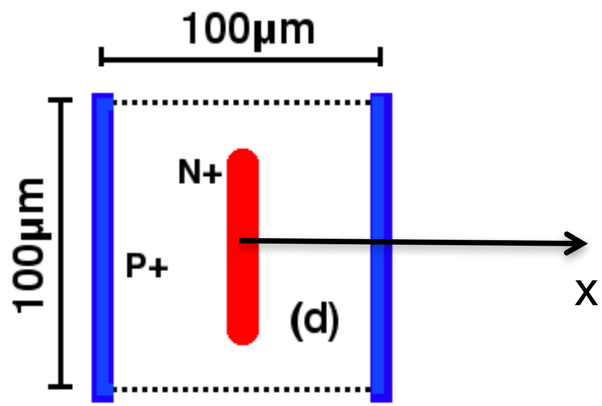
Simulated Efield at V_{bias} = 100 V

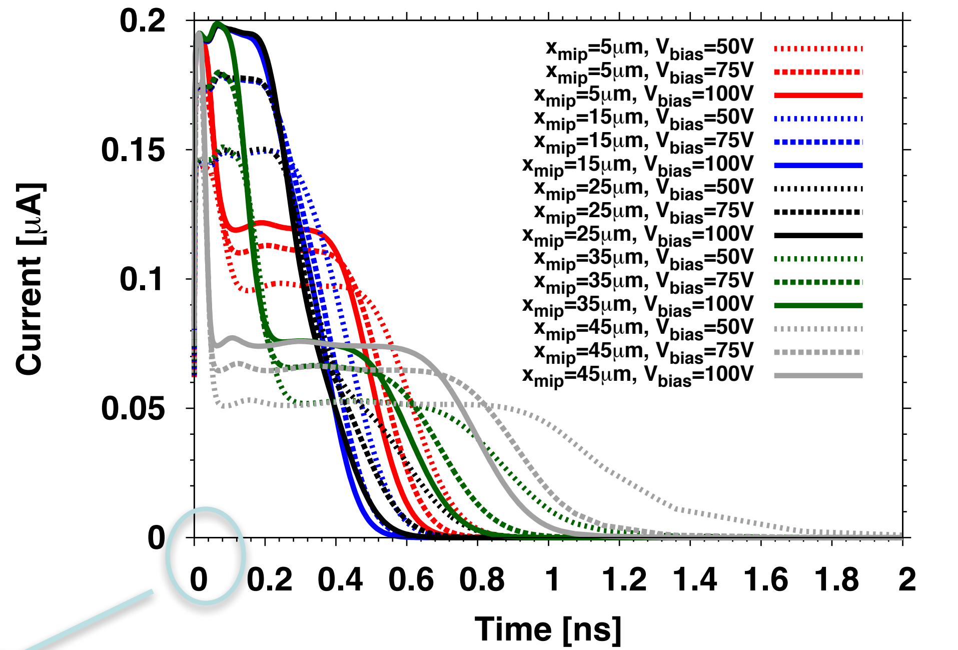


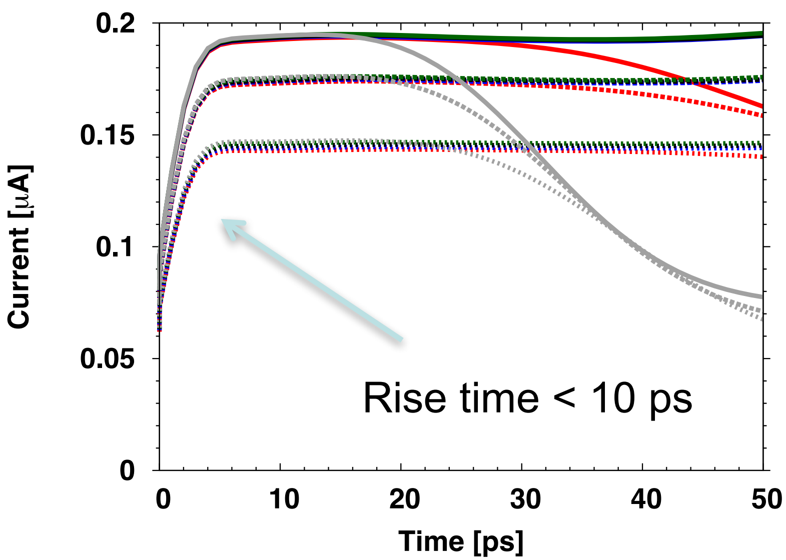


Trench-electrode simulations (2)

Another possible 3D pixel layout



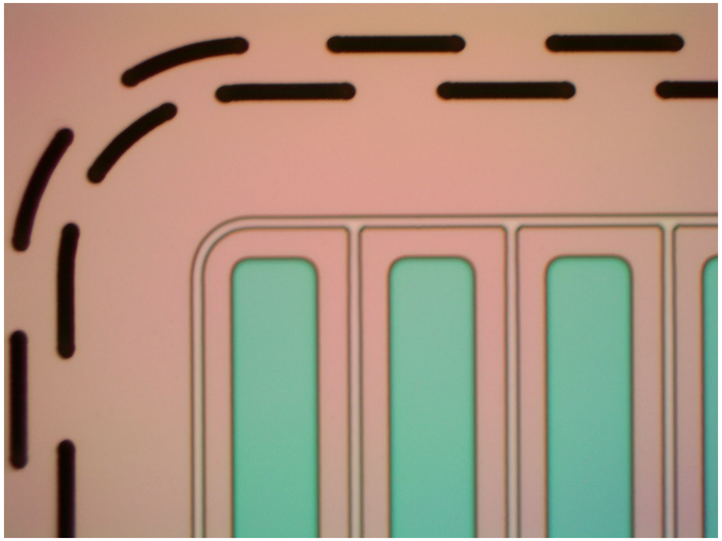


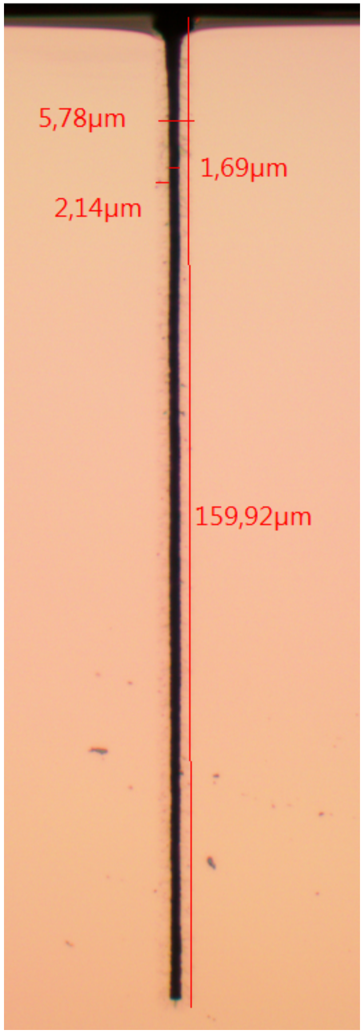


READOUT ELECTRODE CURRENT IN RESPONSE TO A MIP CROSSING THE PIXEL AT DIFFERENT POINTS

More in the next talk from Angelo Loi

Trenches at FBK

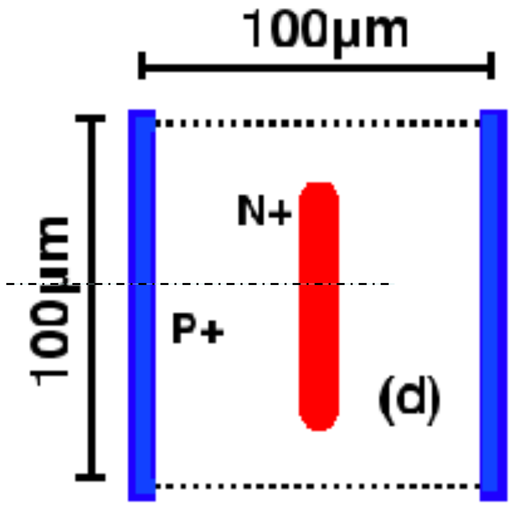


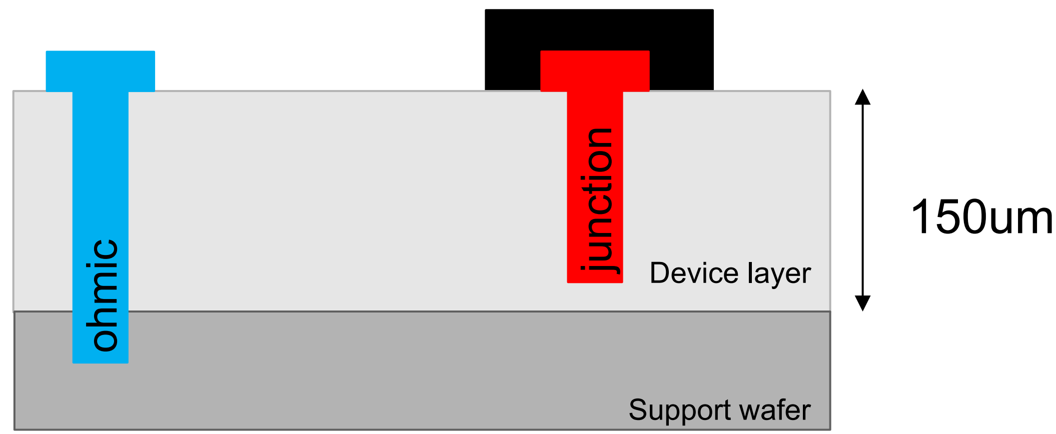


- Layout based on "staggered" trench
- 5 µm width and 40 µm length "small" trenches
- Trench depth ~20 µm larger than Active Thickness
- Trench partially filled with un-doped poly
- Trench doped via BBr_3 gas source
- Etching rate depends on area !

Project INFN-FBK "RD_FASE2"

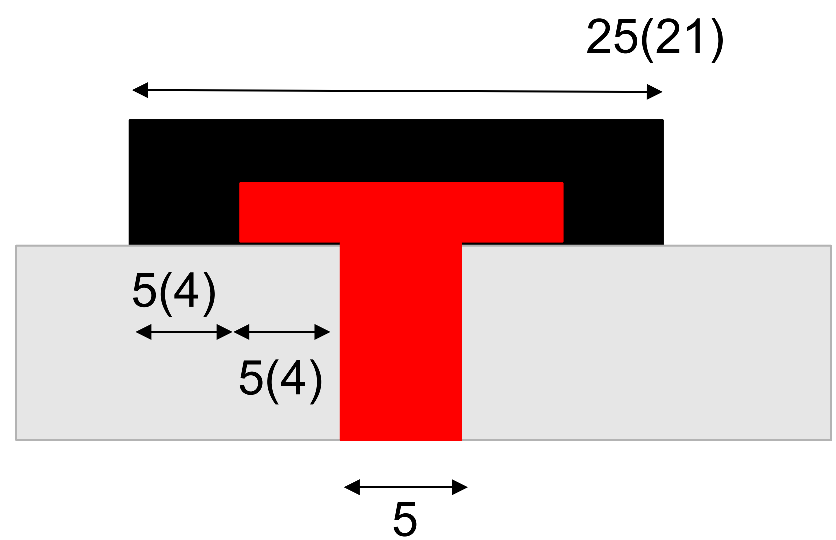
Timespot pixel geometry (1)





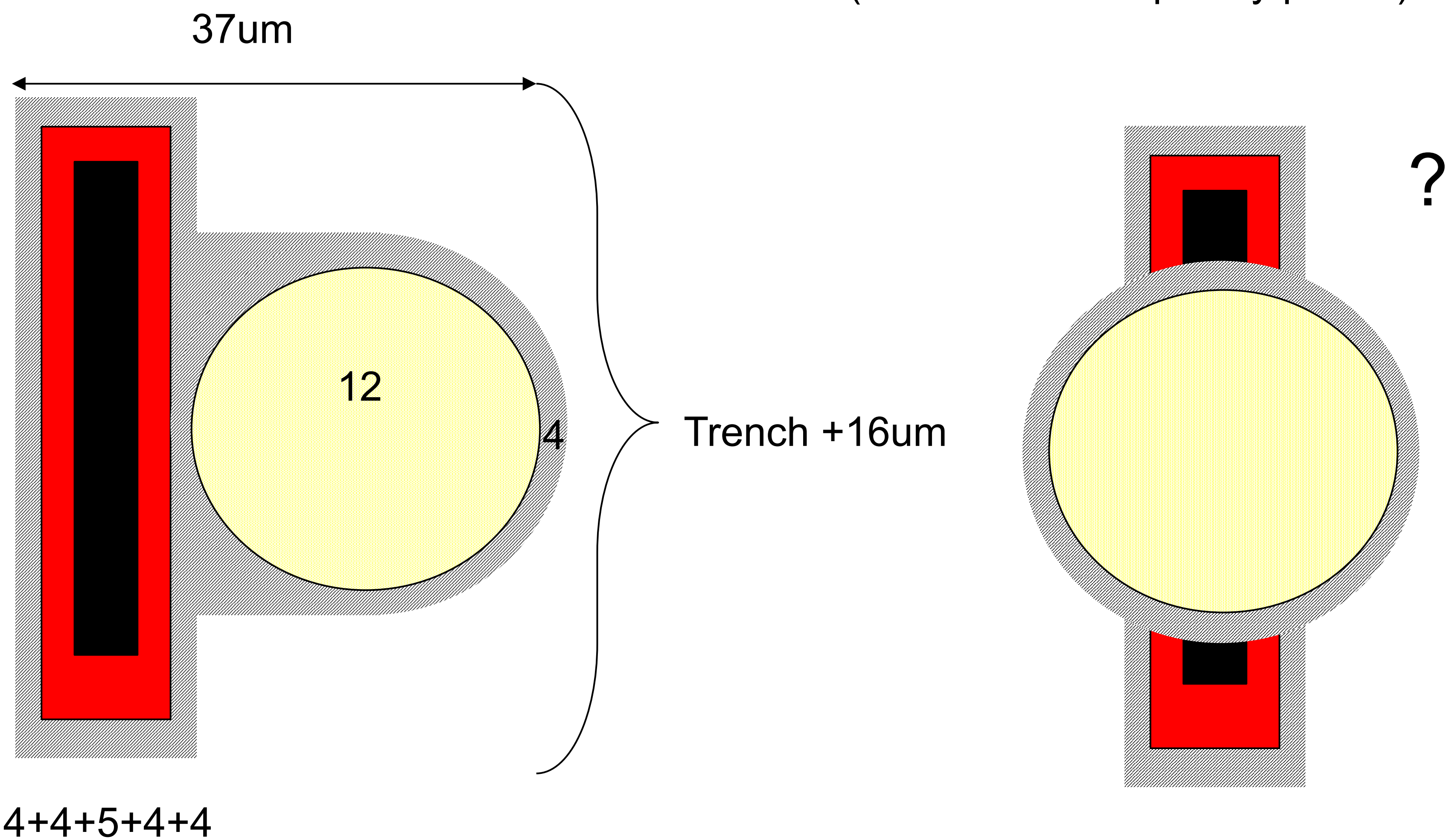
Realistic dimensions

- Trench width ~5 µm
- Min overlaps between layers 5(4) µm
- Min distance between trenches to be defined (metal mask)
- Min bonding pad opening size at IZM 12 µm (yielding metal pad 20 µm)

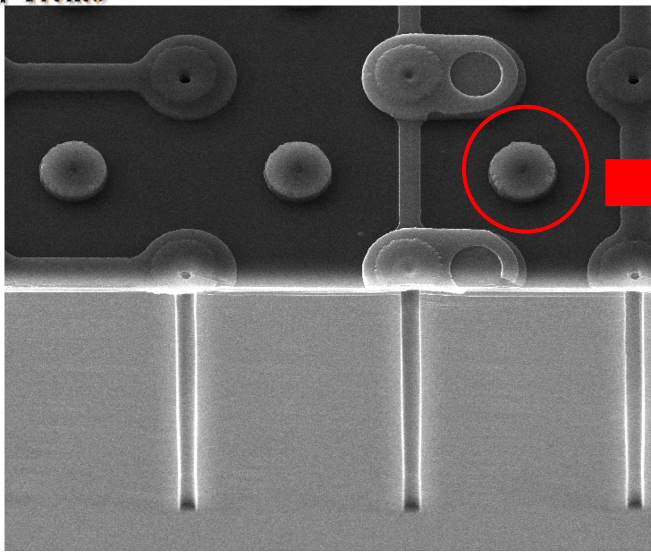


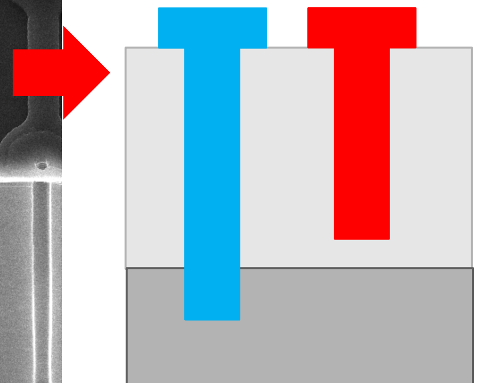
Timespot pixel geometry (2)

BUMP on TRENCH could be evaluated for pixel size reduction (surface not completely planar)



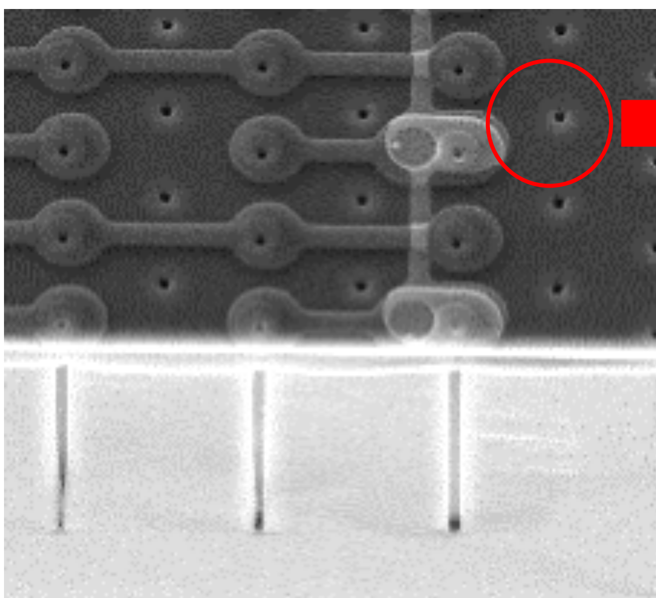
p-Poly-Si definition

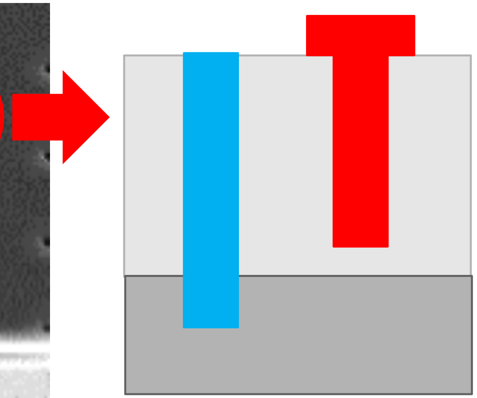




<u>With POLY CAP</u>

- Better control of the process





<u>W/o POLY CAP</u>

- Increases distance between n-metal and p electrode
- Reduces number of lithographies
- Lower control of the process

Mask aligner vs stepper

• Mask Aligner

- One single shot per wafer
- Minimum feature size and mask alignments of about 4um
- Proximity → defects …
- Max area = all the wafer

Wide varietes of structures possible
Lower geometrical accuracy

• Stepper

- Step and repeat (auto focus at every shot) n- shots per wafer
- Minimum feature size 350nm and alignment at **80nm**
- Projection = Low defect level
- Max exposure area : Square ~2x2 cm^2

Only one block of 2x2cm2 possible, repeated n times on wafer
High geometrical accuracy

So far all 3D productions at FBK used mask aligner, but two batches with stepper are planned for 2018.

Outline

- Introduction to 3D Si sensors
  - Technology
  - Intrinsic features
- Where are we now ?
- How to address timing issues ?
- Workplan for 2018

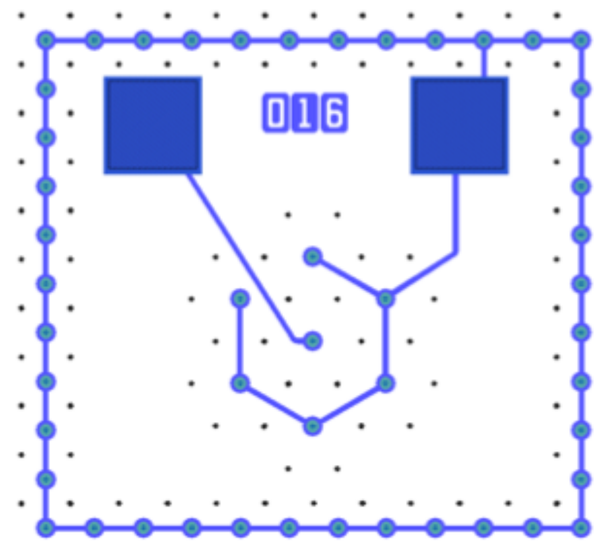
Workplan for 2018

1. Technological tests at FBK
2. Simulation and design of trench-electrode pixels
   - TCAD + Geant 4: Trento, Cagliari, Ferrara ? Others ?
   - Impact on timing via front-end: Torino, others ?
   - Choice of substrate thickness and wafer purchase (in due time)
   - Milestone M1: submission of first wafer layout to FBK by Month 6
3. Fabrication of first prototypes at FBK (months 7-11)
4. Preparation of experimental setups (all groups involved)
5. Start with testing by the end of 2018
   - Electrical tests (I-V, C-V): Trento, Cagliari, Padova ? Others ?
   - Functional tests: Trento, Cagliari, Torino, Padova
   - Deliverable D4: characterization of 1st prototypes by February 2019

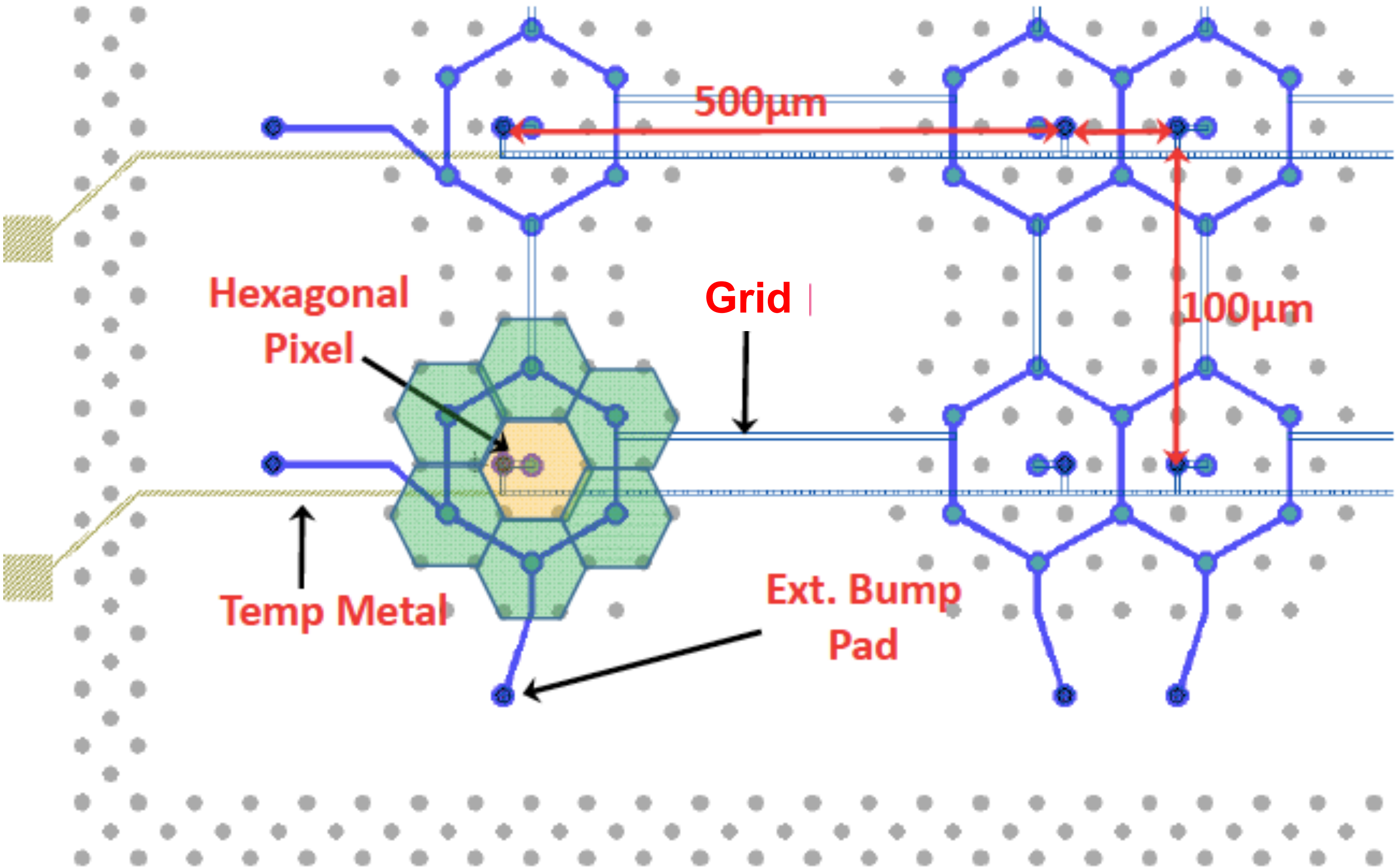
Tests on existing samples ?

- FBK has just completed the fabrication of a new 3D pixel batch within the INFN-FBK Phase2 R&D
- We had designed hexagonal-cell test structures (diodes) and ”pseudo-pixels” compatible with NA62 ROC (pixel clusters using all bumps – L = 30, 40, and 50 μm, and empty regions for geometrical matching)
- Very good electrical characteristics
- We could test their time response with:
  - Fast commercial single-channel amplifiers
  - NA62 assemblies

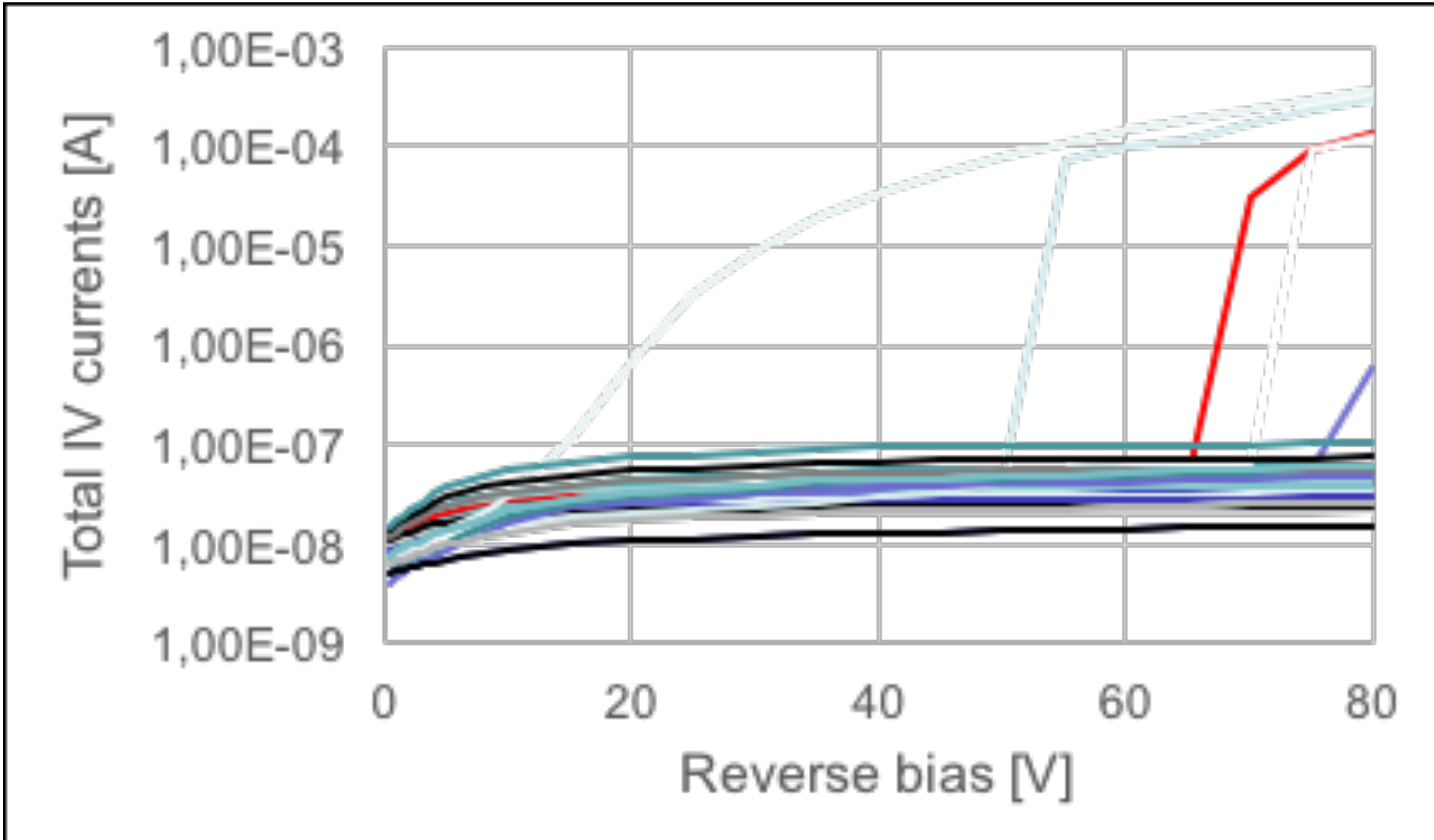
Hex-cell 3D diode



NA62 compatible pixels



NA62 pixel total I-V curves



Back-Up Slide

From Manuel Rolo (Torino)

”Siamo arrivati alla conclusione che il modo migliore di affrontare il problema presuppone che le simulazioni vengano fatte, in una prima fase, con un modello ideale di VFE+CFD.In questo modo, si possono isolare più facilmente i parametri legati alla forma del segnale prodotto dal sensore che contribuiscono alla performance in tempo.

In questa prima fase, quindi, l'analisi (C o C++) non è vincolata ad una architettura specifica del CFD. Successivamente, possiamo implementare modelli comportamentali di architetture possibili per fare una scelta della tipologia più adatta per il CFD. A questo punto, le simulazioni di risoluzione temporale possono essere fatte con routine Ocean su Cadence.”