Pixel_ROD board
From ATLAS to TIMESPOT

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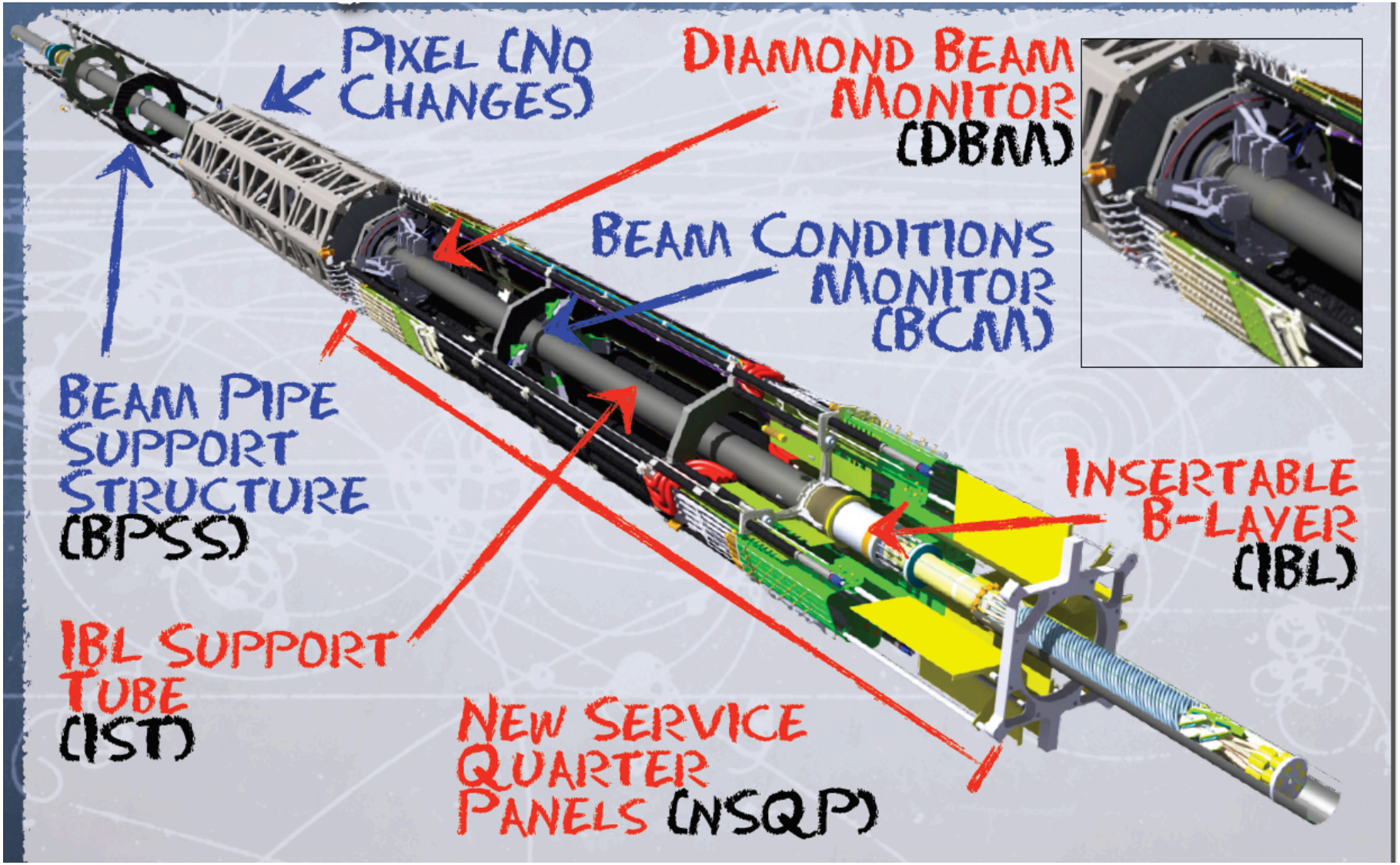
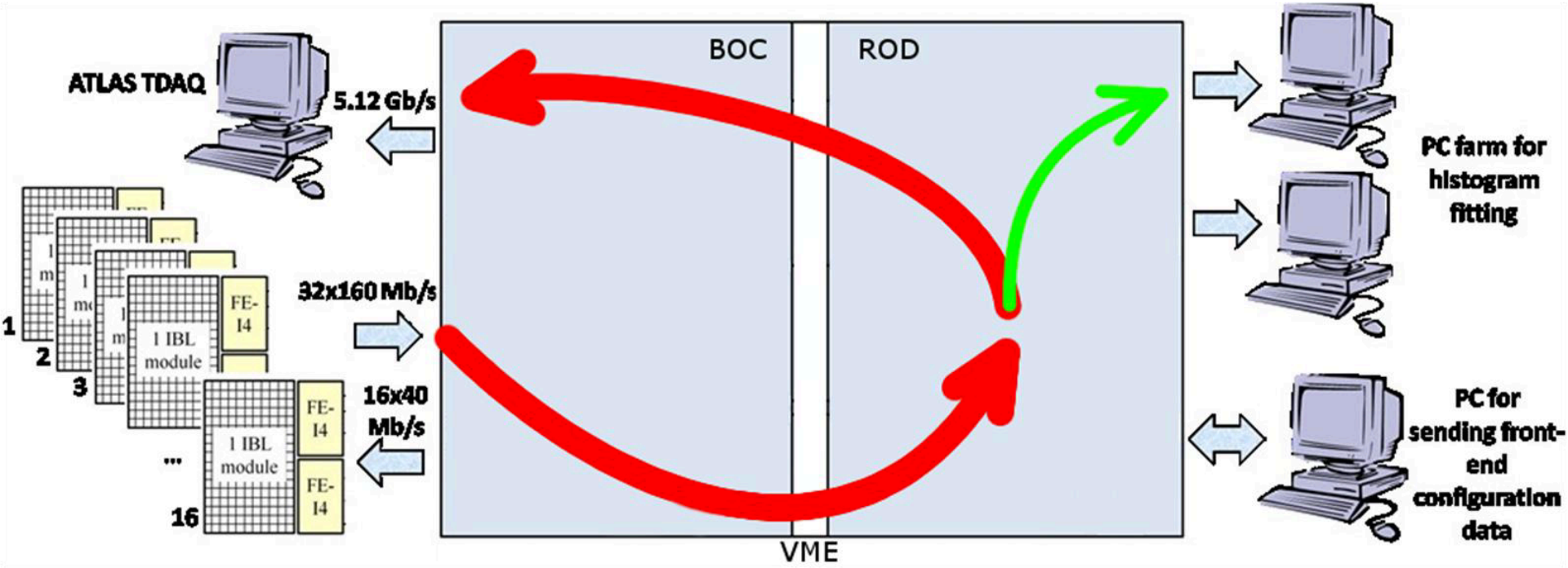
IBL plan

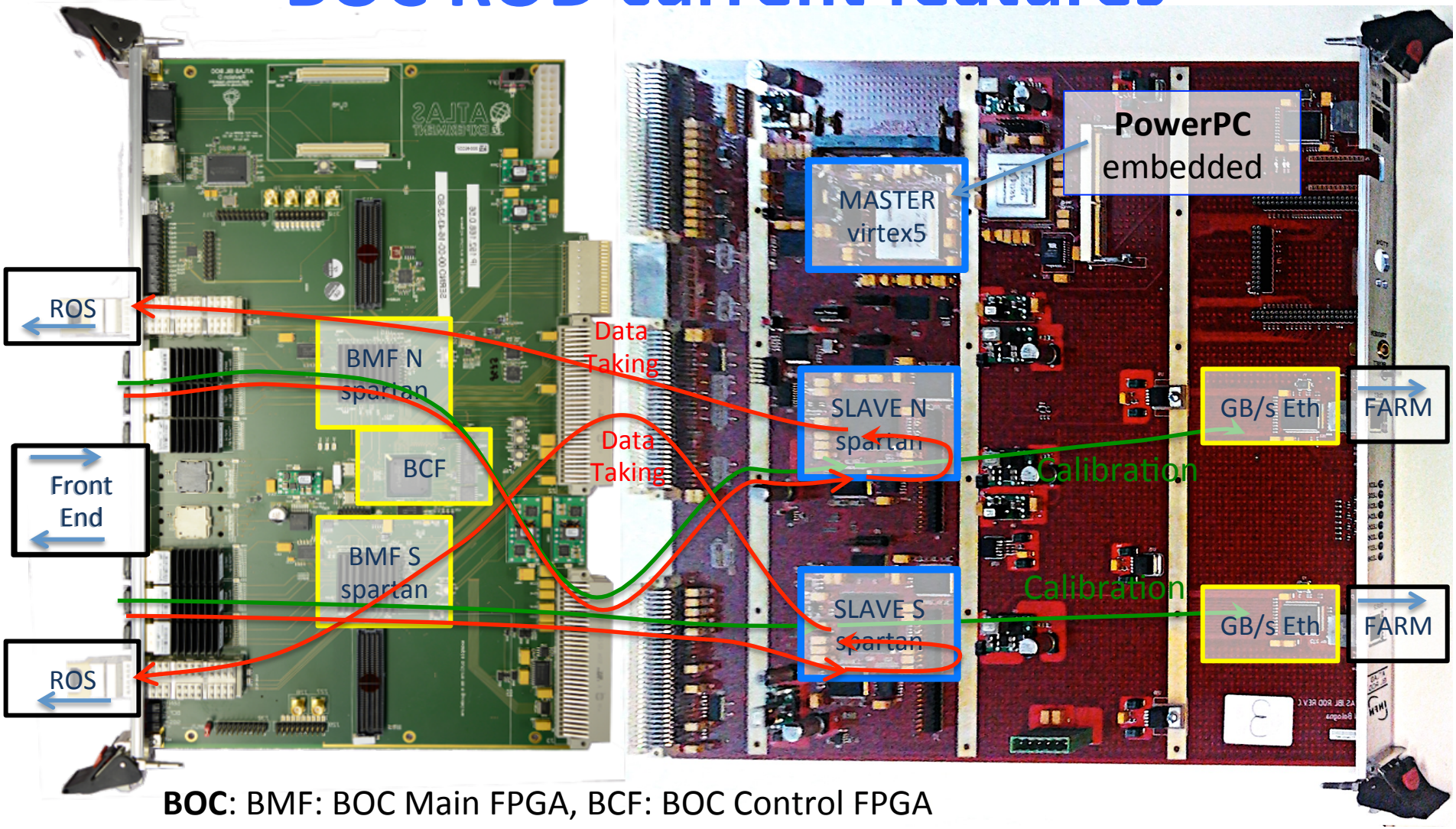
2009



IBL: BOC + ROD in the DAQ



IBL/L2/L1/B-Layer/Disks
BOC ROD current features



BOC: BMF: BOC Main FPGA, BCF: BOC Control FPGA

ROD: PRM: Program Reset Manager, Master and 2 x Slaves

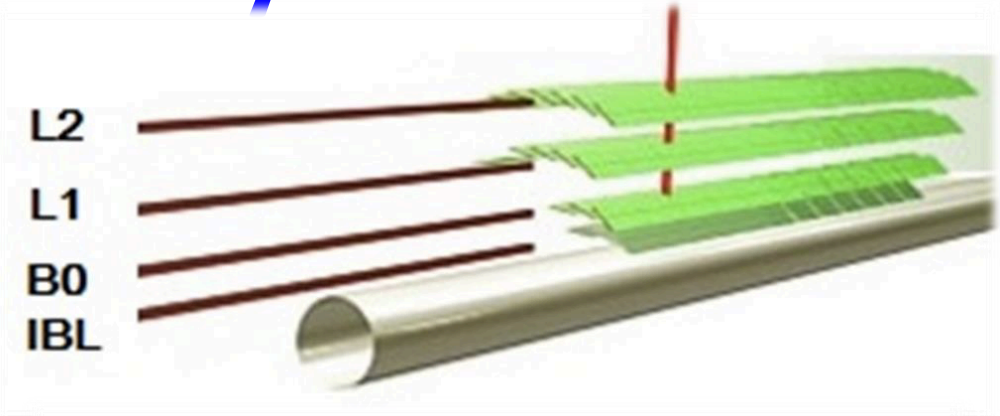
Bologna activity 2013-2017

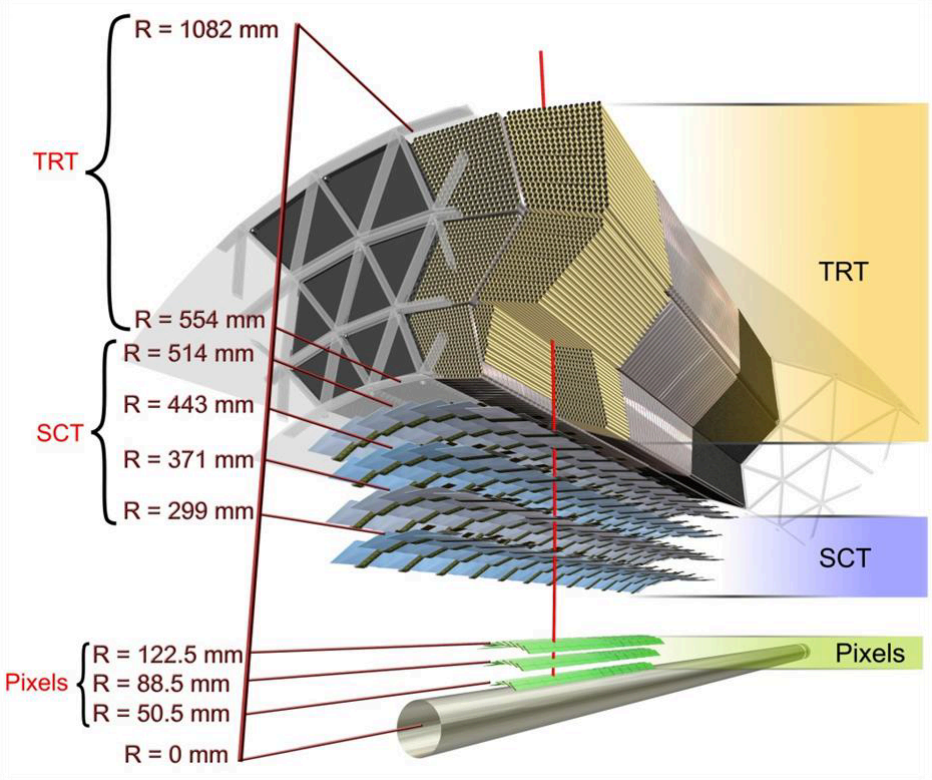
Now Taking Data

- ✓ **14+1** RODs for IBL (FEi4)
- ✓ **26** RODs for L2
- ✓ **38** RODs for L1

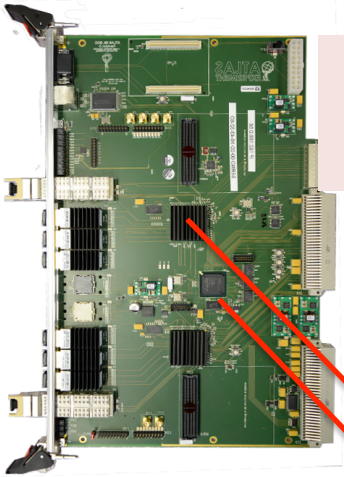
Under Commissioning
Already Produced

- ✓ 12 RODs for Disks
- ✓ 22 RODs for B0





Pixel_ROD Design

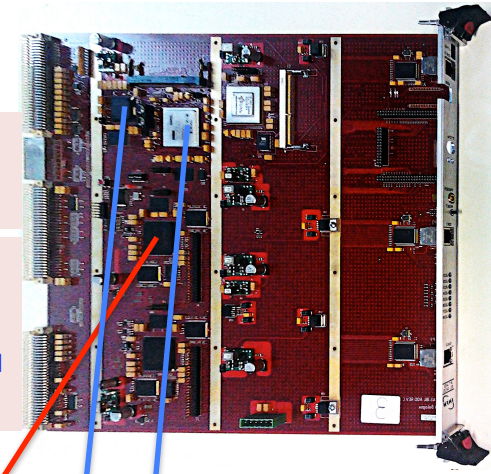


BOC
1 x BMF out of 2
1 x BCF

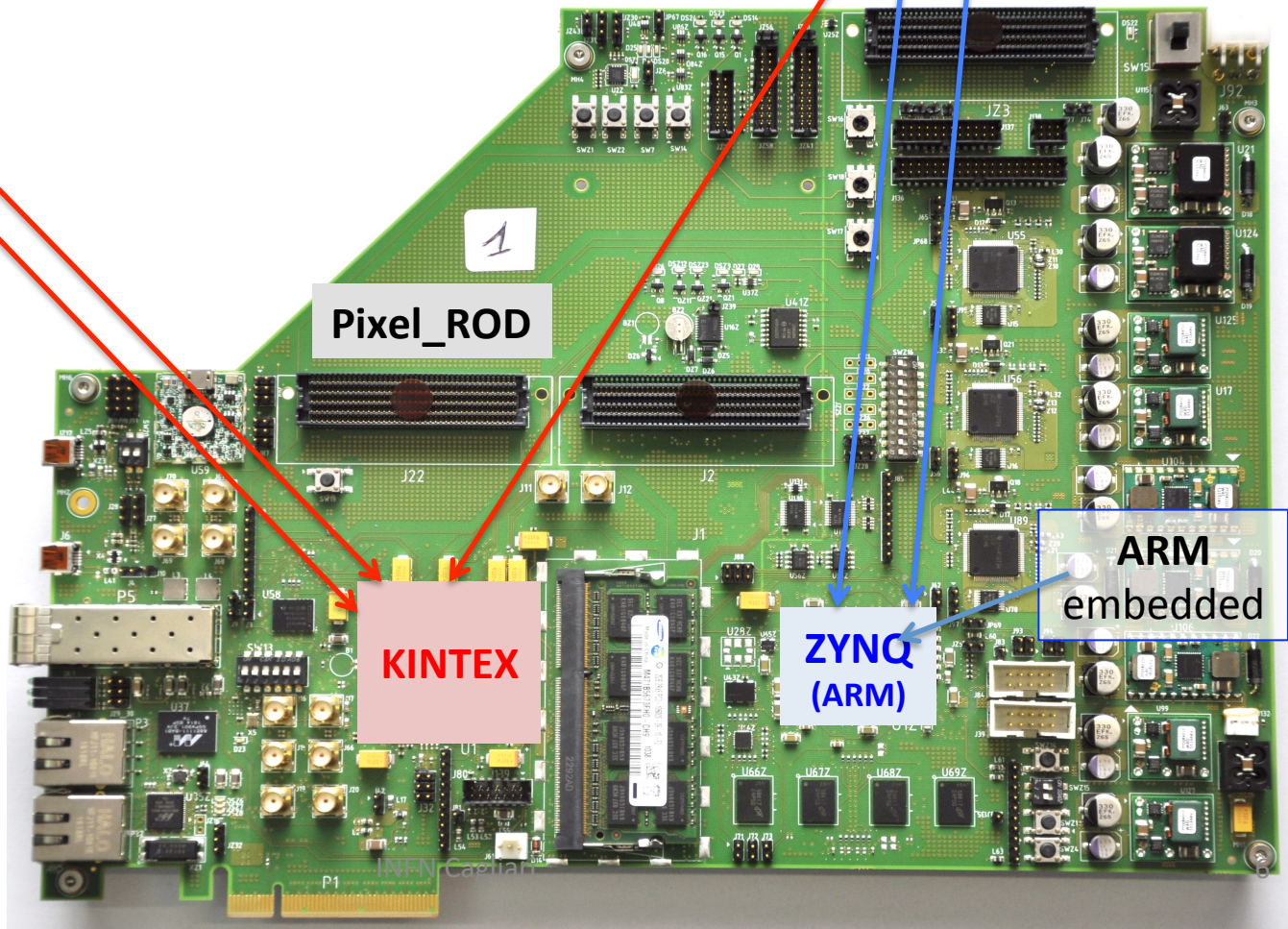
115 board pairs installed in the ATLAS Pixel Detector

ROD
1 x SLAVE out of 2

ROD
1 x MASTER
PPC → ARM
1 x PRM



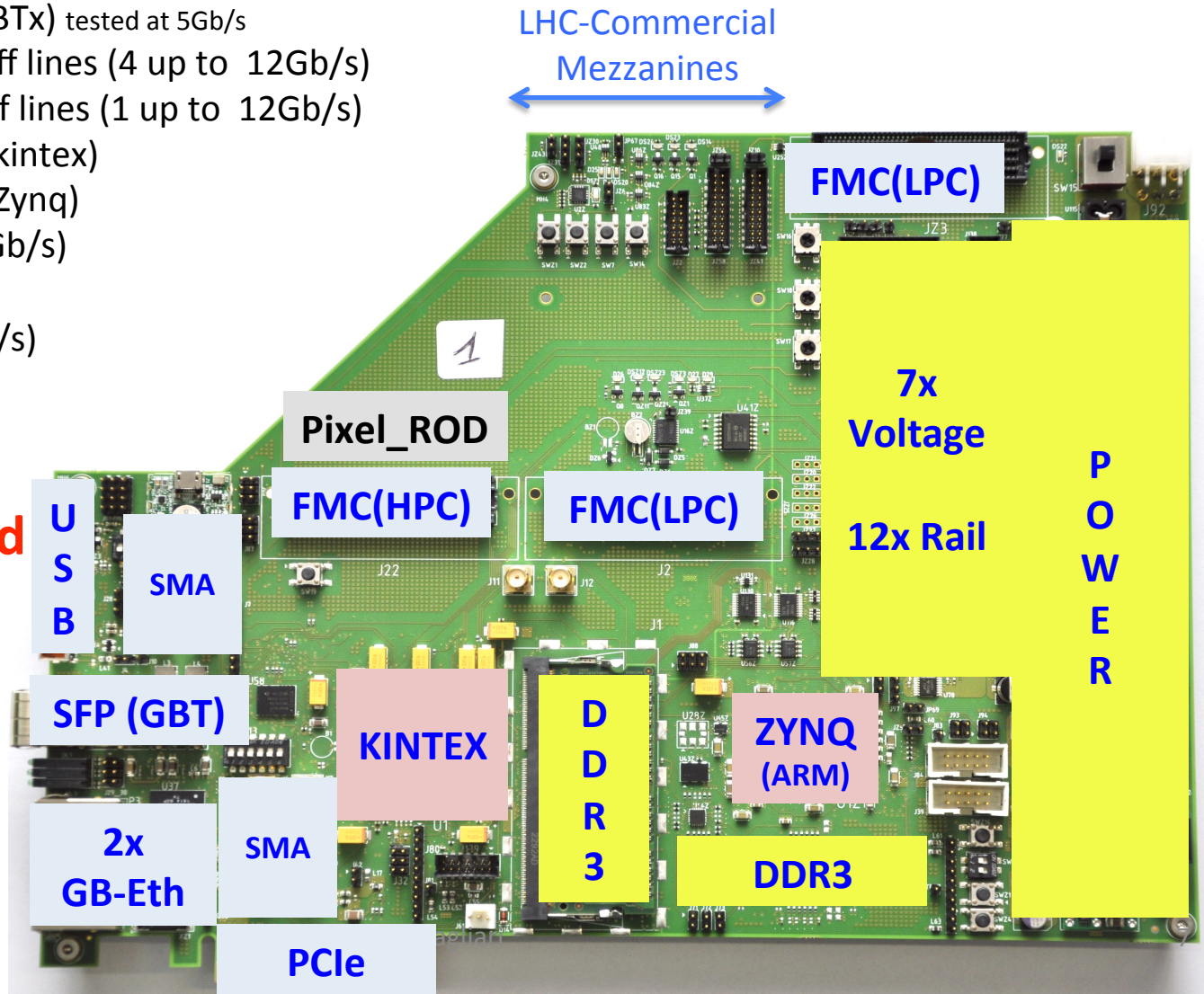
1 Pixel_ROD can interface up to 16 equivalent FEI4 channels as half of the 32 channels of the BOC-ROD pair



Pixel_ROD IO-Features

- 7-series Xilinx® FPGAs
  - ✓ Kintex7 XC7K325T-2FFG900C;for trigger and data processing
  - ✓ Zynq XC7Z020-1CLG484C with physical dual-core ARM Cortex-A9
- 1 x PCIe Express Gen2 8x-lane (2Gb/s min to the PC memory, up to 10Gb/s)
- 16 x GTX@ 12.5Gb/s on PCIe, SFP, SMA, FMC, Eth
  - ✓ 1 x SFP 10-Gb/s link (GBTx) tested at 5Gb/s
  - ✓ 1 x HPC (400-pin) HS diff lines (4 up to 12Gb/s)
  - ✓ 2 x LPC (160-pin) HS diff lines (1 up to 12Gb/s)
  - ✓ DDR3 2GB x 667 MHz (kintex)
  - ✓ DDR3 1GB x 667 MHz (Zynq)
  - ✓ 2 x GB/Eth (1 up to 12Gb/s)
  - ✓ 2 x USB JTAG
  - ✓ 2 x SMA (1 up to 12Gb/s)

- **2 Boards Fabricated**



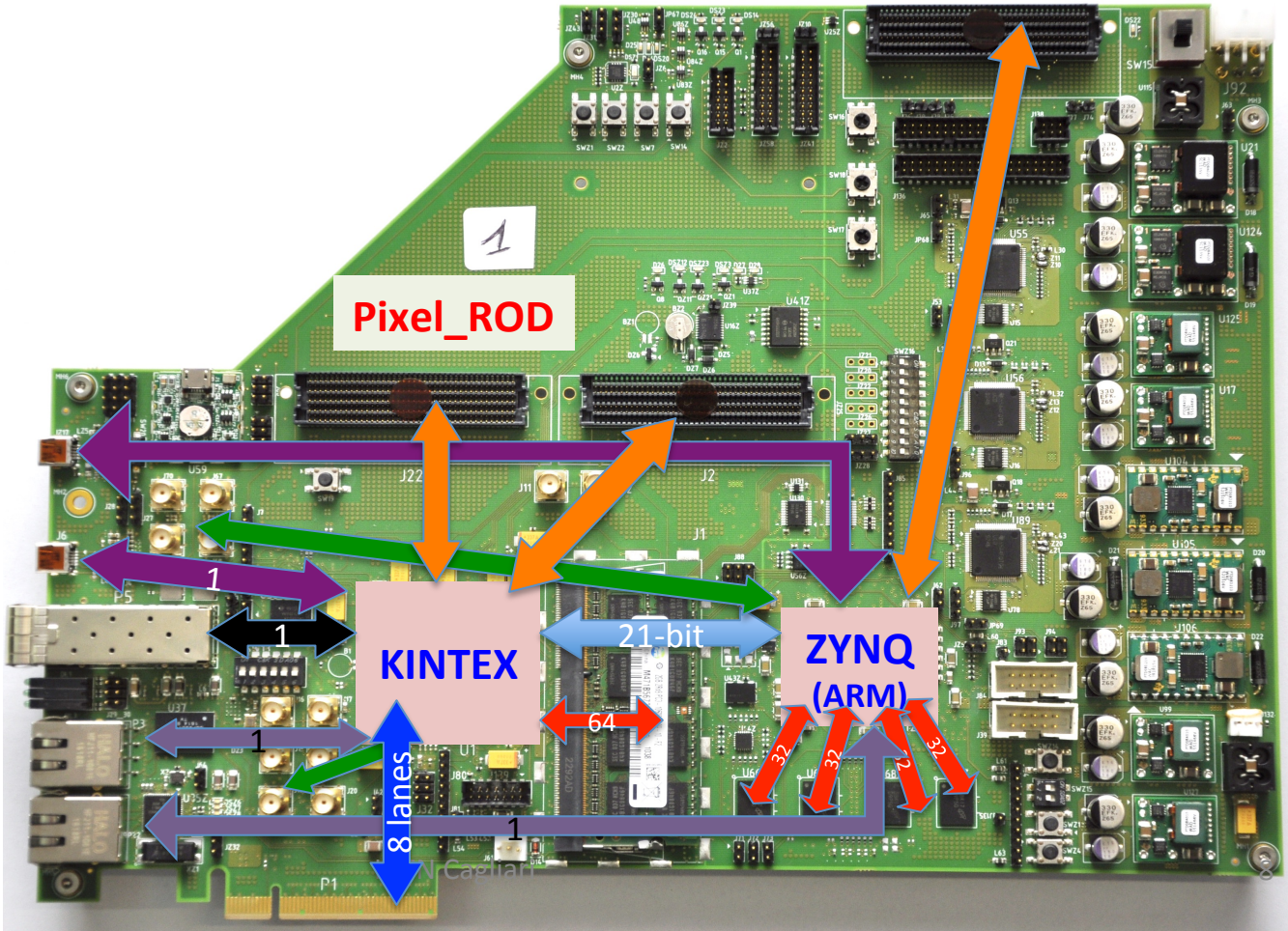
Low Pin Count (LPC)
High Pin Count (HPC)
FPGA Mezzanine Card (FMC)
small form-factor pluggable (SFP)
SubMiniature version A (SMA)

Pixel_ROD Buses

7-series Xilinx FPGAs

- ✓ Kintex7 to Zynq bus 21-bit differential bus
- ✓ 32-bit / 64-bit DDR3 differential buses
- ✓ SFP diff bus (1 Transceiver)
- ✓ 2x ETH diff buses (1 Transceiver)
- ✓ FMC (HPC) diff buses (4 Transceivers)
- ✓ FMC (LPC) diff bus (1 Transceiver)
- ✓ 2 x UART buses
- ✓ 2 x SMA (1 Transceiver)
- ✓ PCIe (8 Transceivers)

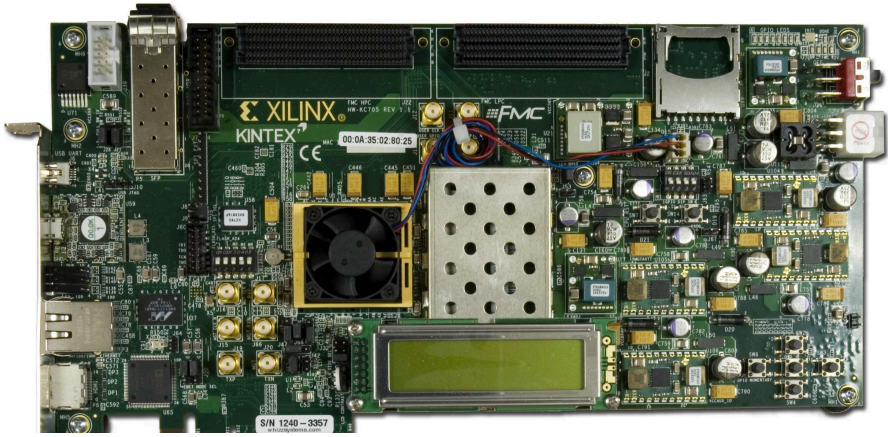
ALREADY TESTED !!



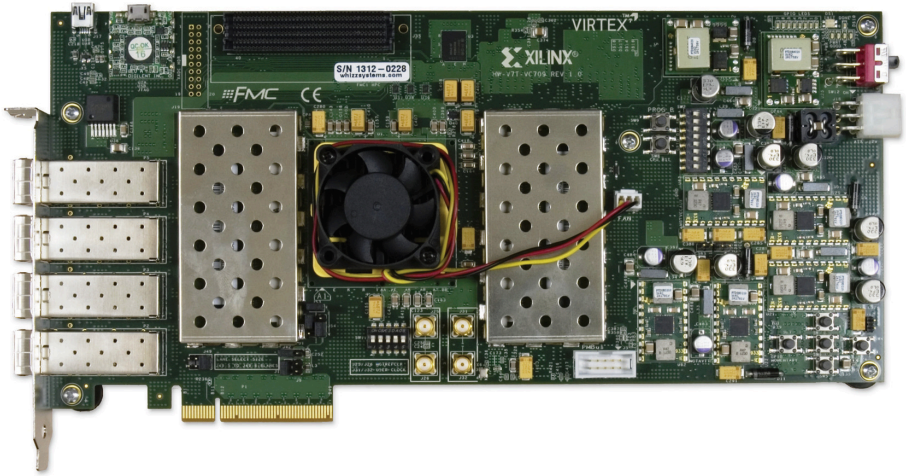
Low Pin Count (LPC)
High Pin Count (HPC)
FPGA Mezzanine Card (FMC)
small form-factor pluggable (SFP)
SubMiniature version A (SMA)

Basic summary of available *"low-cost"* cards Within the ATLAS TDAQ table

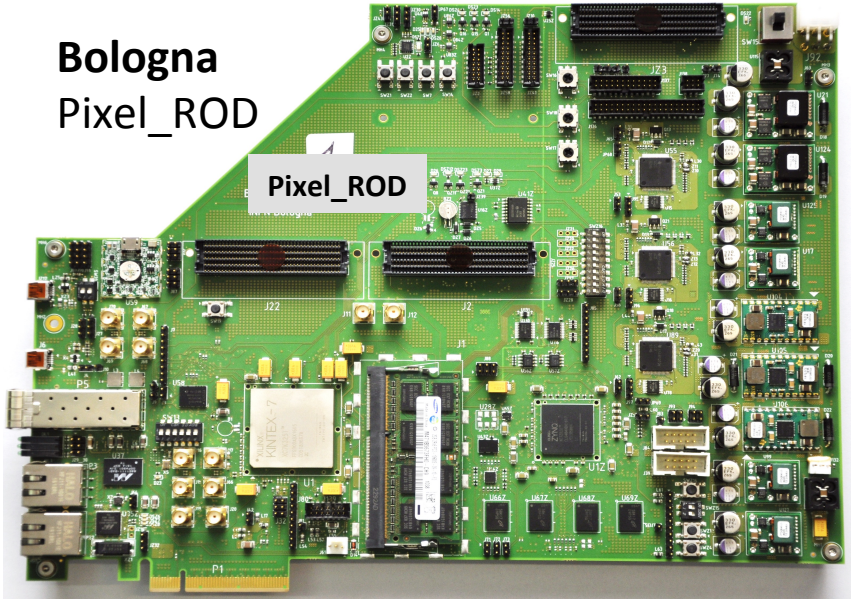
Demo KC-705



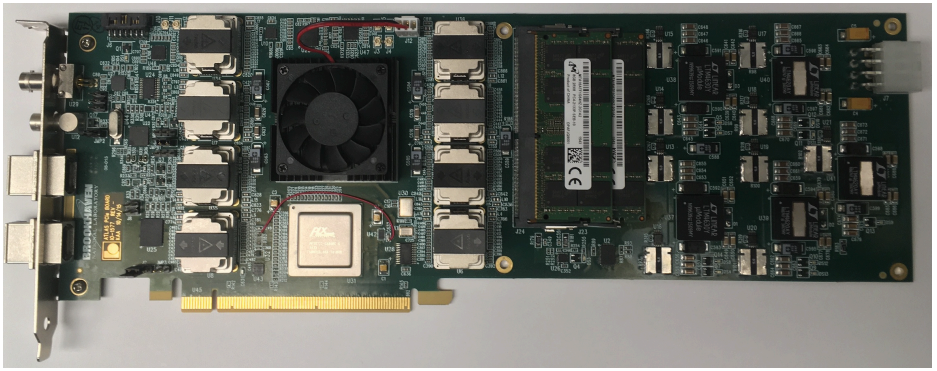
Demo Mini-Felix VC-709



Bologna
Pixel_ROD



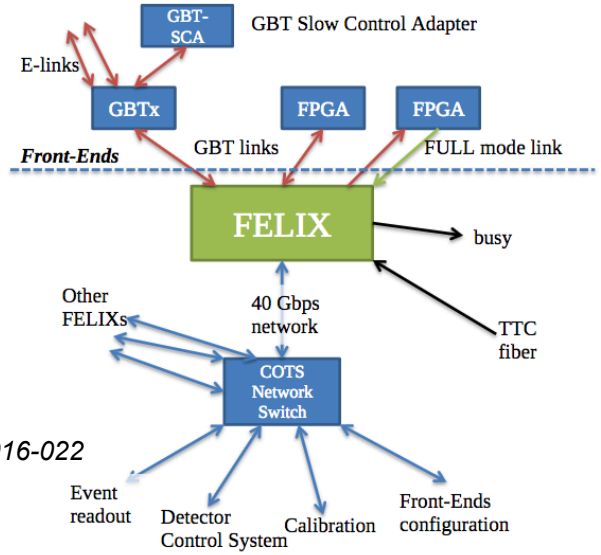
FELIX FLX-711



Basic summary of available *"low-cost"* cards

Board FPGA	Debug	Family Cost k€	Embedded Processor	PCI Ex Rate	Type Transc	Speed Gb/s	MiniPOD Links	≈ Cost k€
KC705 (Demo) XC7K325T_2FFG900C	NO	Kintex7 1.5	NO	8 x Gen2 32 Gb/s	GTx 16	12.5	0 / 1+1+5	> 1.7
Pixel_ROD XC7K325T_2FFG900C	YES	Kintex7/Zynq 1.5+0.3	Dual-Core ARM Cortex-A9	8 x Gen2 32 Gb/s	GTx 16	12.5	0 / 1+1+1+1+4	> 3
mini-FELIX **VC-709 (Demo)** XC7VX690T_2FFG1761C	NO	Virtex7 3.5	NO	**8 x** Gen3 50 Gb/s	GTH 22	13.1	0 / 4+10	> 5
FELIX FLX-711 XCKU115 FLVF1924	YES	UltraScale 7.5	NO	16 x Gen3 100 Gb/s	GTH 64	16.3	4 in + 4 out / 48	> 10

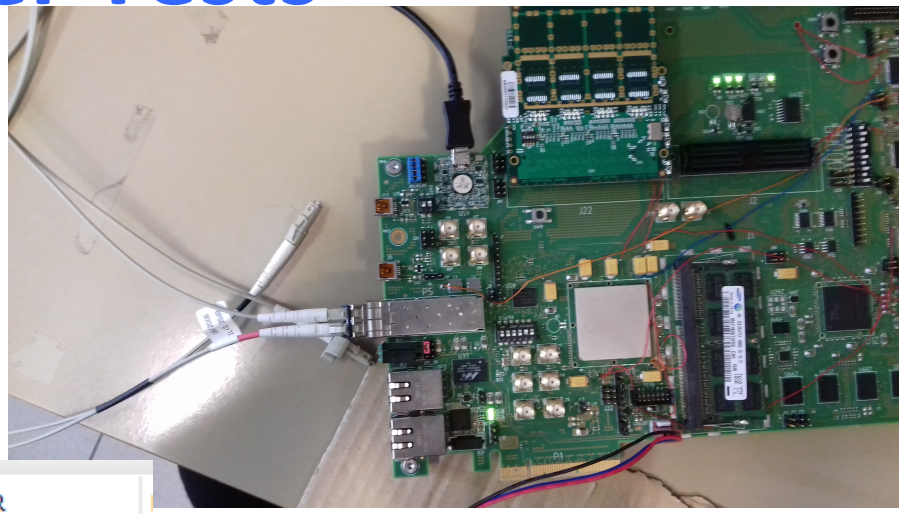
- FELIX is a PC based DAQ system designed for bridging custom links (GBT) to a COTS computer network
- *Bologna is interested in joining the FELIX project to:*



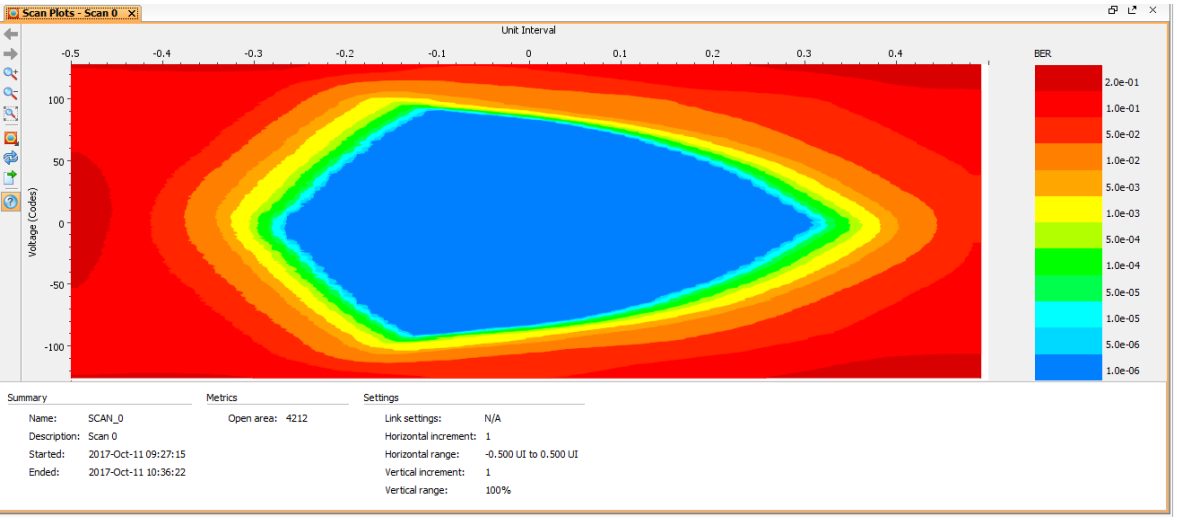
ATL-DAQ-PROC-2016-022

Transceiver Tests

SFP connector at 10 Gb/s with **BER ≈ 10^{-12}**



Name	TX	RX	Status	Bits	Errors	BER
Ungrouped Links (0)						
Link Group 0 (1)						
Link 0	MGT_X0Y15/TX	MGT_X0Y10/RX	10.000 Gbps	2.421E13	0E0	4.13E-14



Eye diagram in loopback test on (HDC) **FMC** connector at:

- **10 Gb/s, BER ≈ 10^{-14}**

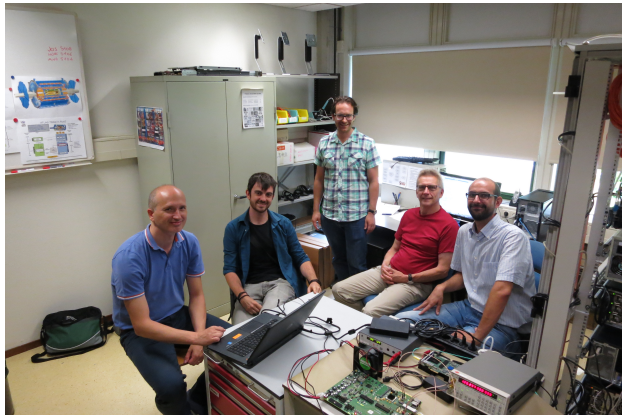
Low Pin Count (LPC)
High Pin Count (HPC)
FPGA Mezzanine Card (FMC)
small form-factor pluggable (SFP)
SubMiniature version A (SMA)

Pixel_ROD integration test with Mini-Felix at NIKHEF, July 2017

We already join the FELIX developers meetings

- **Current status (NIKHEF July 2017)**
  - Bologna is able to run the:
    - **Aurora** (64b/66b) protocol in **Duplex** mode: (4 lanes at 1.28 Gbps) in loopback only
    - **Aurora** (64b/66b) protocol in **Simplex** and **Duplex** mode: (1 lane at 5.12 Gbps)
    - Communication to FELIX in **GBT** mode: (4.8 Gbps)
    - Communication to FELIX in **Duplex mode** (custom protocol): (9.6 Gbps): ≈ 100 GByte of data transmitted in 100 s at NIKHEF on July 2017

Pixel_ROD integration test with Mini-Felix at NIKHEF, July 2017



Presentation of a Poster at TWEPP-17 in Santa Cruz

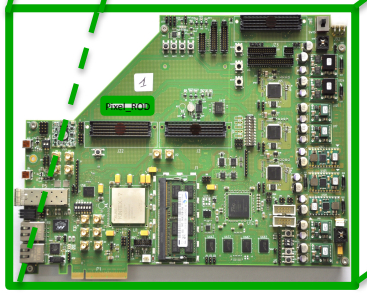
Stand-Alone Pixel_ROD running:

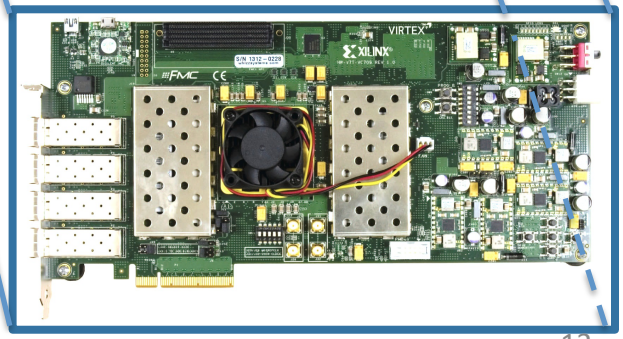
- GBT-FPGA protocol
- FELIX FULL-mode

Full Mode @ 9.6 Gbps
GBT Mode @ 4.8 Gbps

Mini-FELIX
Xilinx VC-709 kit

FELIX PC





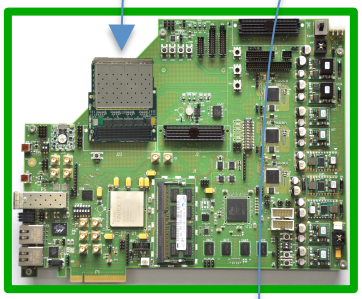
Possible Case Study for TIMESPOT
120 Gb/s 10-channel Data Generator

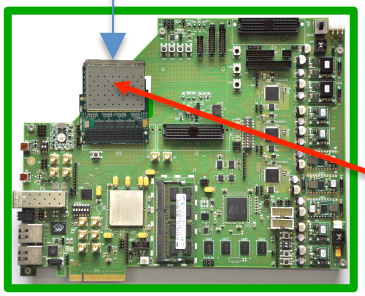
(1+1) x 12 Gb/s bidirectional optical links

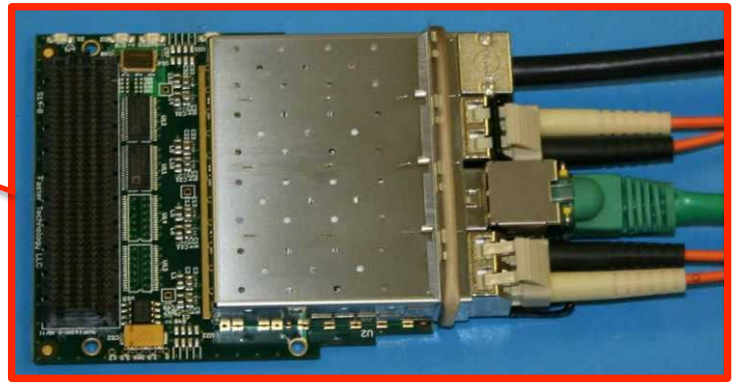
(4+4) x 12 Gb/s bidirectional optical links

Total of 120 Gb/s bidirectional optical links

gFEX board
RETINA-based Trigger/Tracker

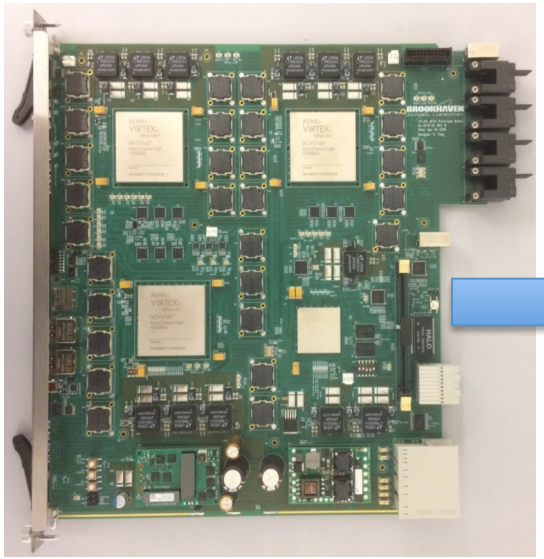






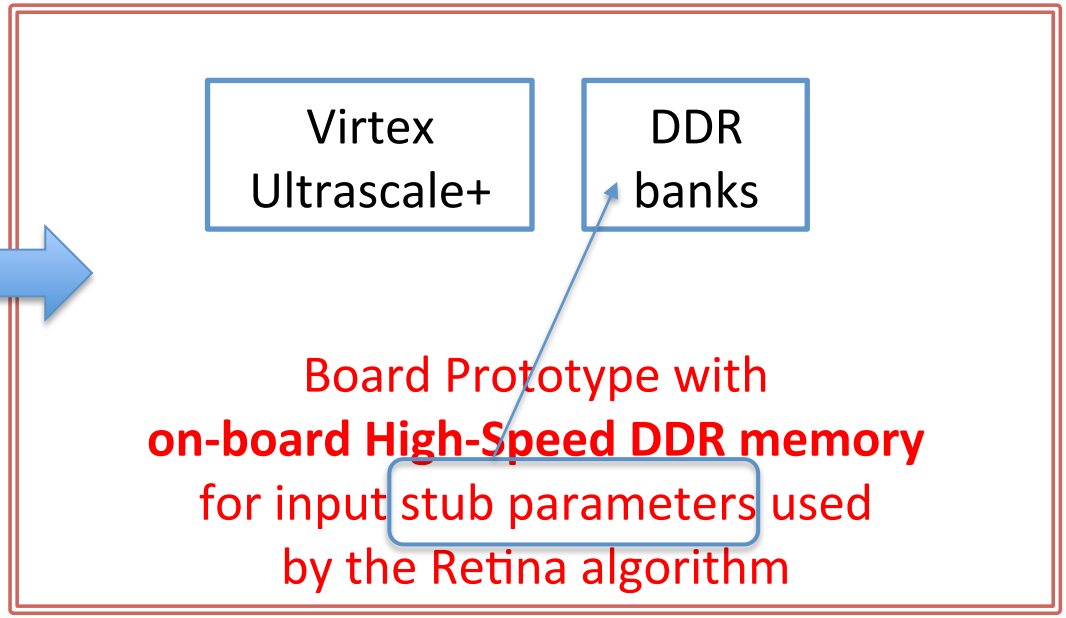
Two Bologna board available and
usable for free very soon in 2018

Doable board design for TIMESPOT ….
……. in two-years



The ATLAS gFEX v2 board with three ultrascale FPGA, one ZYNQ Soc and 28 MiniPODs
ATL-DAQ-PROC-2017-035 16 October 2017

- **No DDR memory on-board**
- **No PCI-e bus**



Ultrascale+ …. DDRs: not trivial PCB!!