TimeSPOT WP3: Design and test of pixel front-end

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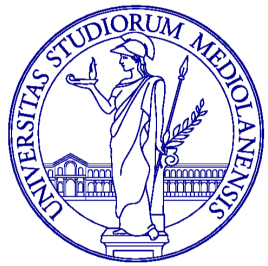


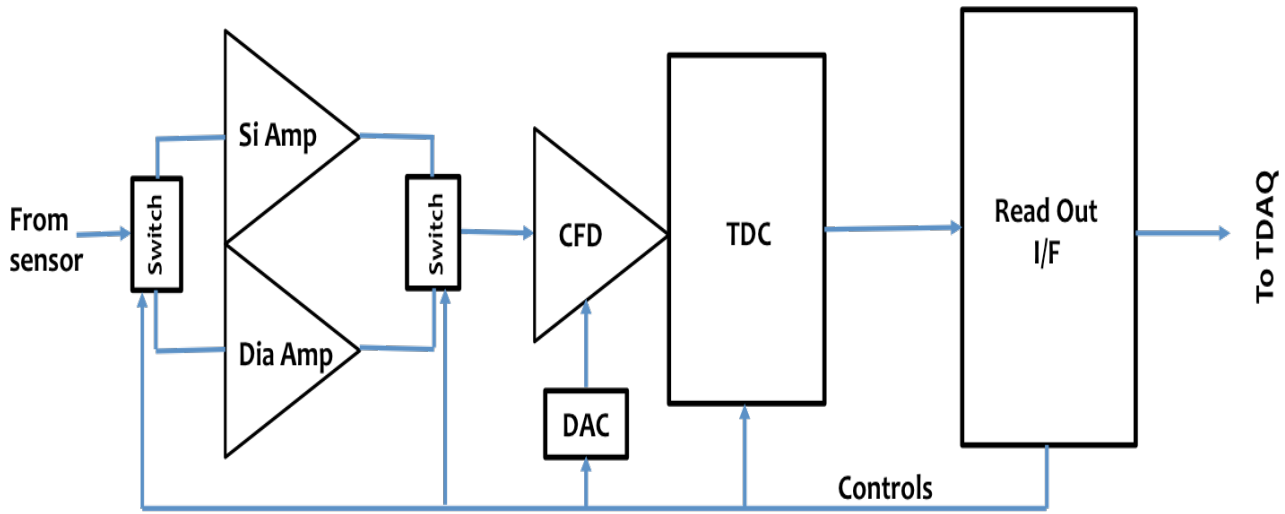
UNIVERSITÀ
DEGLI STUDI
DI MILANO

Cagliari, Dec. 2017

TIMESPOT

TIME & SPace real-time Operating Tracker

Work Package 3: Front-end Electronics



Human resources

Cagliari	Adriano Lai, Sandro Cadeddu, Massimo Barbaro
Milano	Valentino Liberali, Alberto Stabile, Luca Frontini, Stefano Riboldi, Carlo Fiorini - PoliMI (?)
Torino	Angelo Rivetti, Gianni Mazza, Giulio Dellacasa, Margherita Obertino, Luca Pacher, Manuel da Rocha Rolo, Lorenzo Piccolo

Preliminary meeting held in Milano on Nov. 23, 2017

Somebody missing? Please, let me know!

Target: MiniASIC

We plan to use the **mini@asic** fabrication service, provided by Europractice/IMEC.

Advantage:

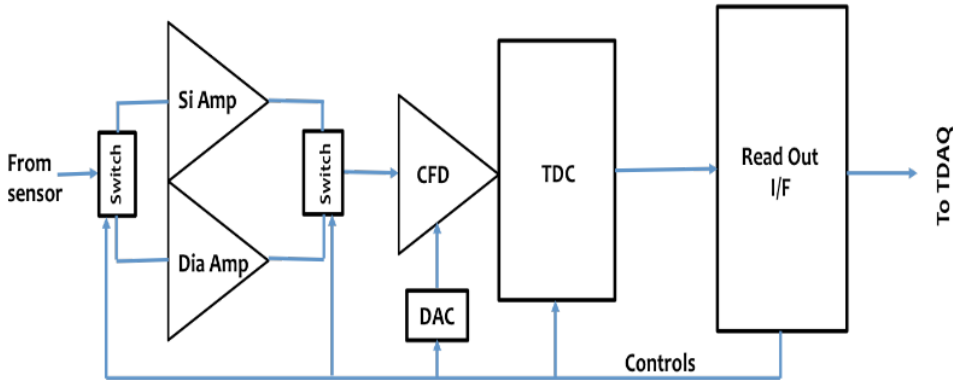
- LOW COST: 2017 Price 23 kEUR per block of 1570x1570 microns

Disadvantage:

- Fixed area; pad-limited chip
- Few submission dates (2 possible dates in 2017 - Apr./Oct.)

Our target: **First submission in Oct. 2018** (submission dates not available yet)

Activities



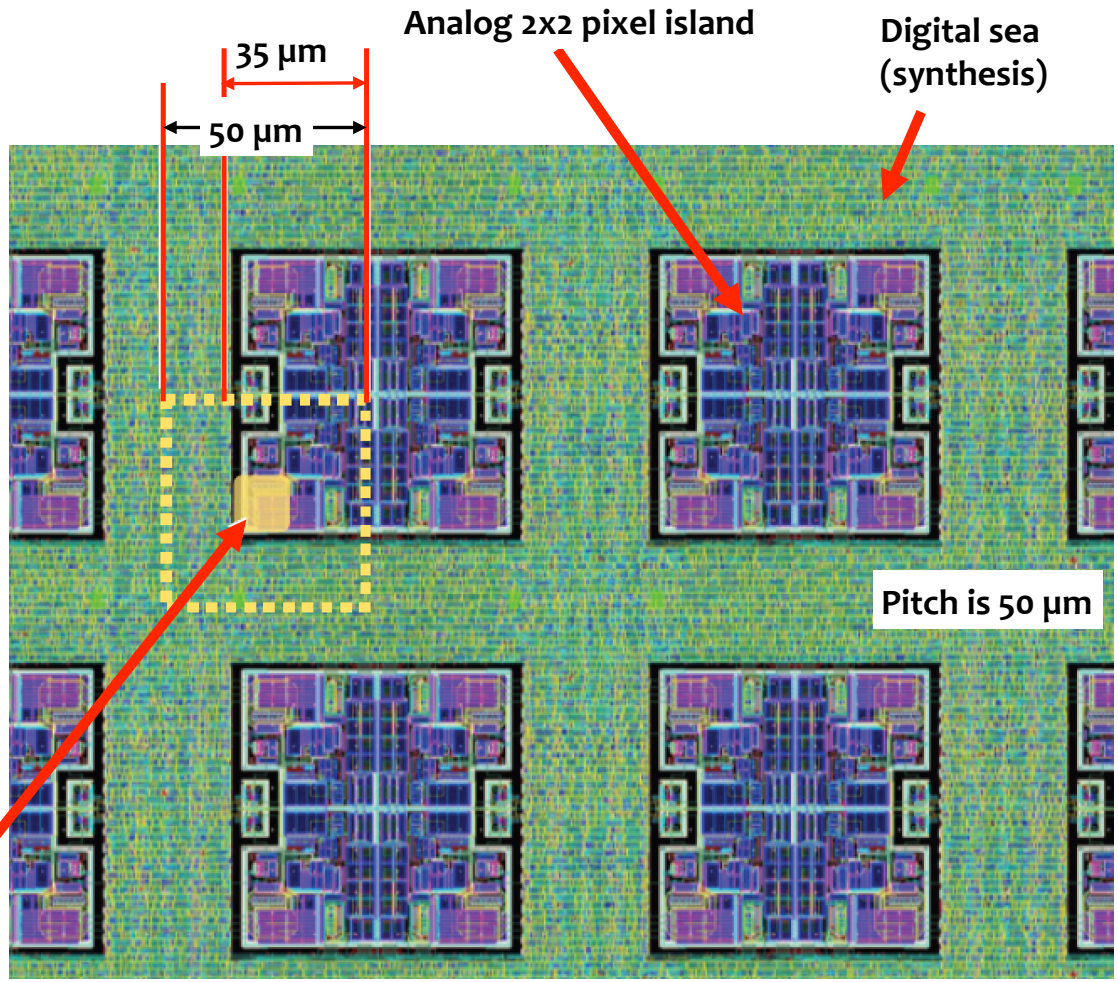
	Cagliari	Milano	Torino
CSA			×
Discriminator			×
TDC	×		
DAC	×	×	
BandGap		×(+BG)	
LVDS		×(+BG)	
OpAmp (Voltage Buffer)	×	×	
Standard cells		×	
[Digital I/F]			

Preliminary meeting held in Milano on Nov. 23, 2017

State of the art of pixel ROCs

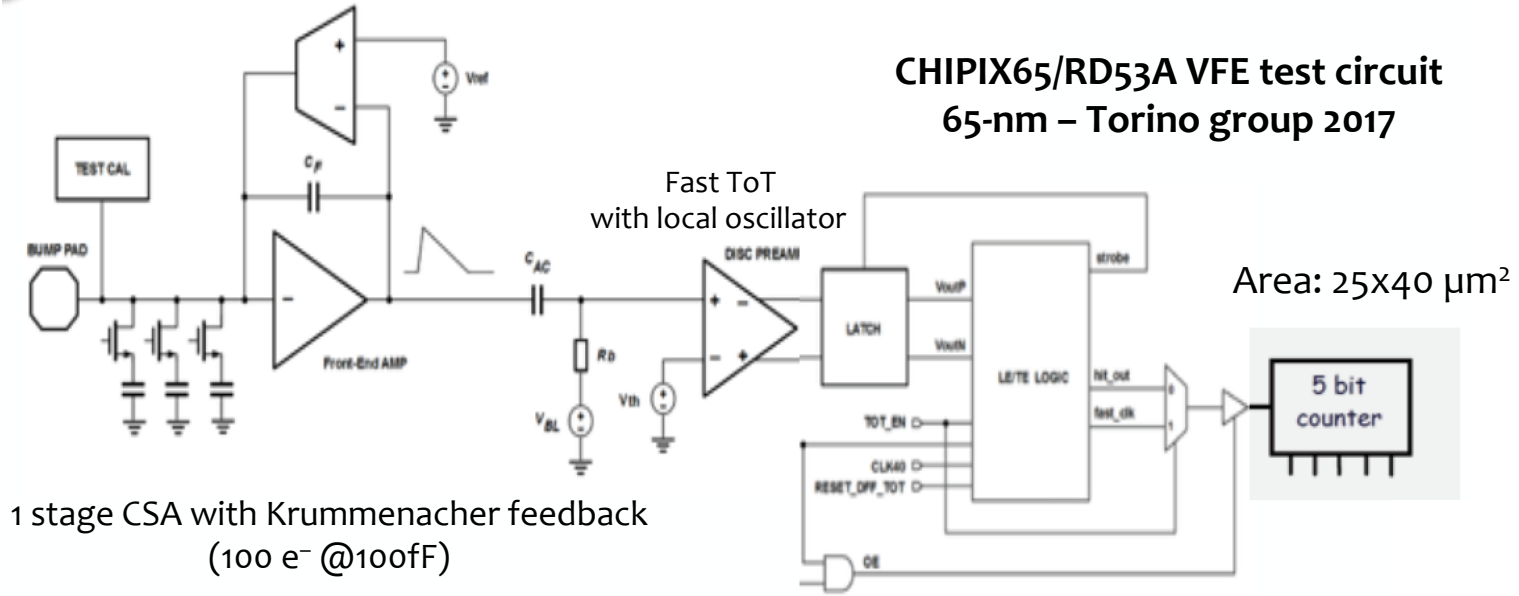
The present frontier in high energy experiments ROCs is at 65 nm. But...
will it be adequate to the requirements of the next generation of trackers ?

RD53A pixel circuit does not integrate a TDC



RD53A (ATLAS-CMS Phase2 prototype)

Ultra-scale front-end for pixels with timing



How about adding a TDC per pixel?

TIMESPOT Approach: probe 28-nm CMOS technology

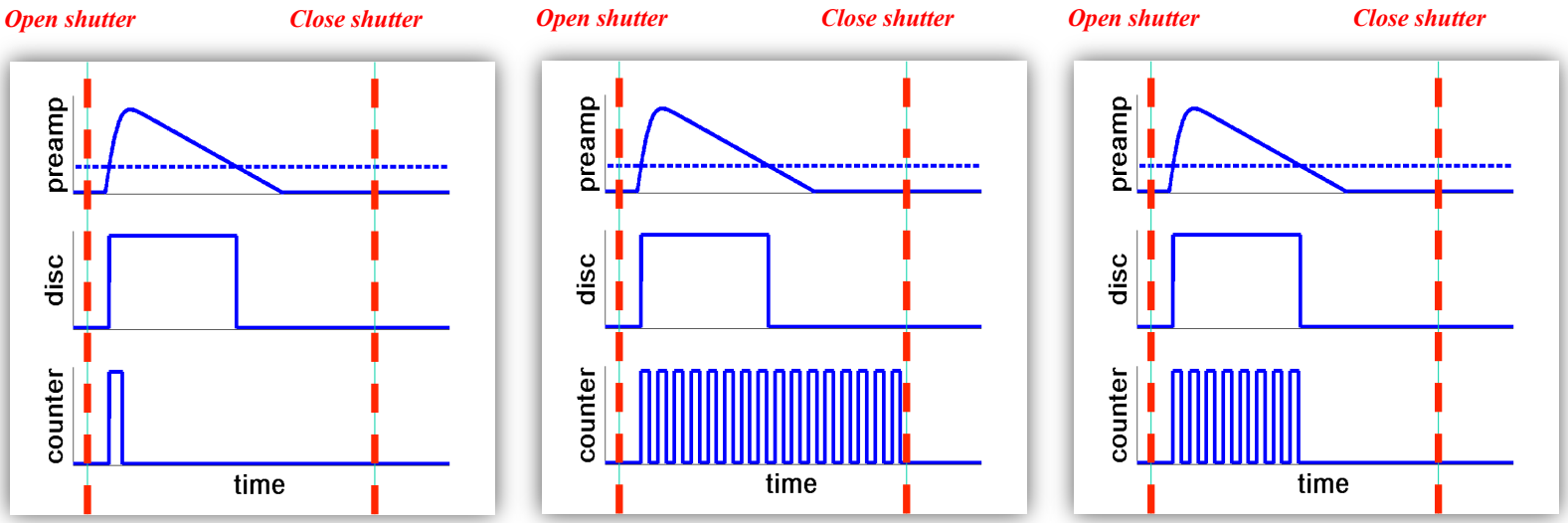
1st step: Design and characterization of single elementary cells (CSA, Discriminator, TDC, R/O I/F etc…

2nd step: Implementation and test of a demonstrator/rescalable ROC (reduced size)

Timepix reading scheme

Timepix Operation Modes

- Particle counting
- Arrival Time
- Time over threshold



- **TOT mode was added during the design phase:**
  - **Linear response up to ~300 Ke$^-$/pixel**

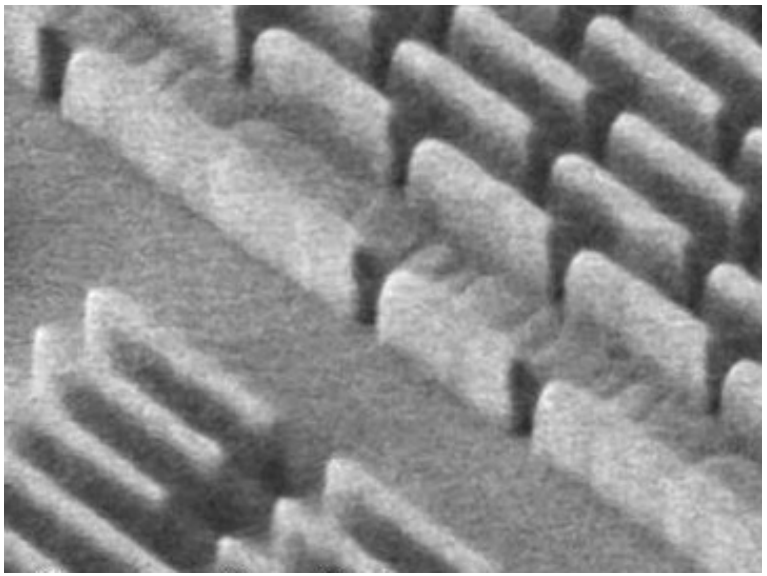
Technology choice: 28 nm

28 nm is a common and mature technology
(Xilinx Kintex-7, Nvidia 600-700-900 series)

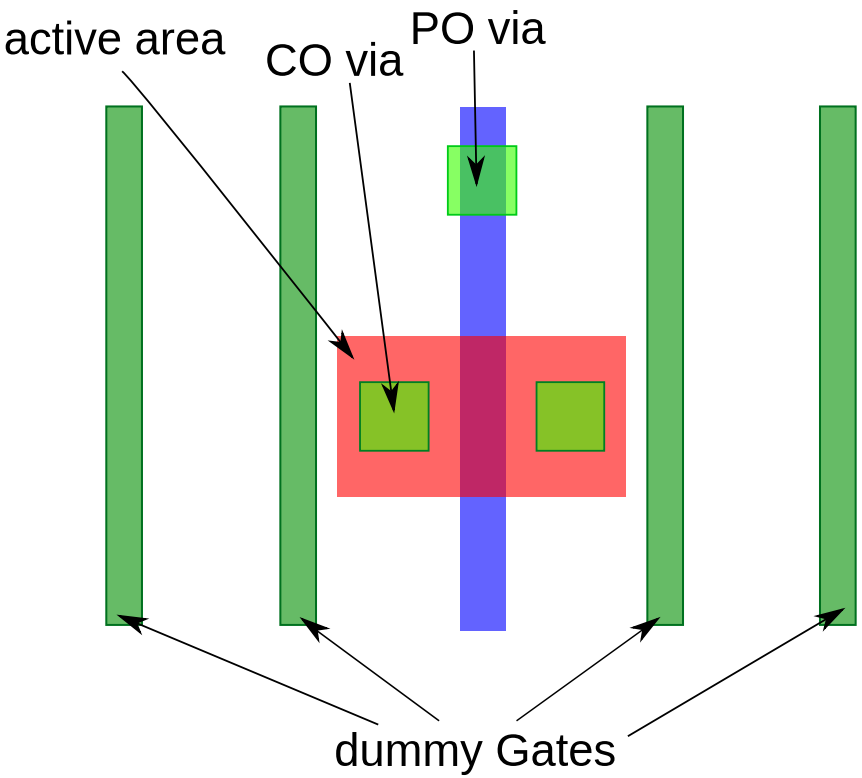
- Minimum gate length 28 nm
- Minimum gate pitch 120 nm

- UV $\lambda >$ gate length

- Interference figure needed to fabricate transistors
- "REGULAR FABRICS"
- More (and complex) design rules

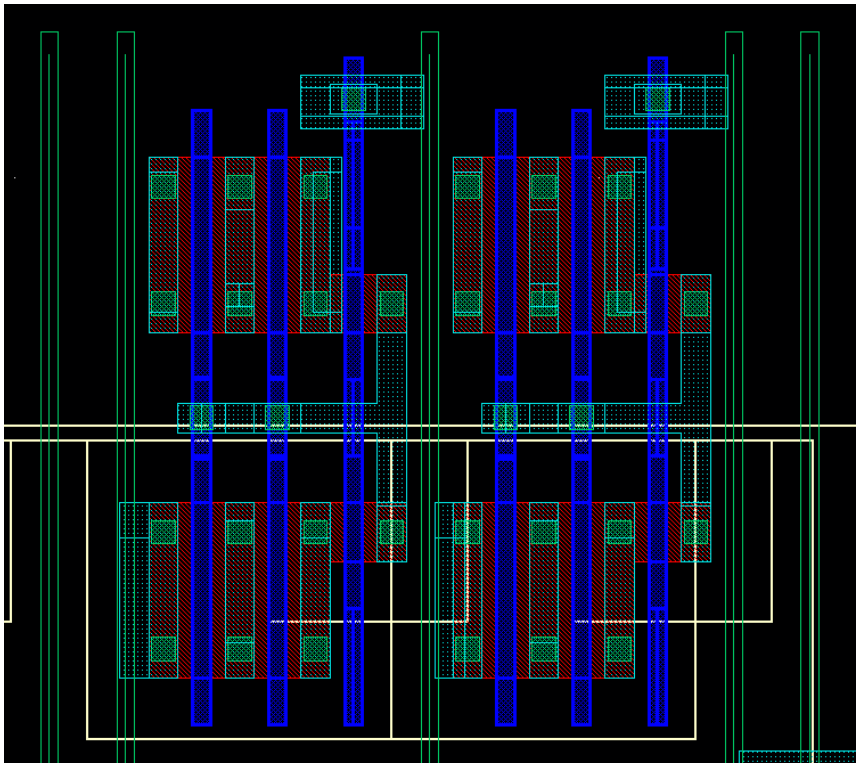


28 nm technology: MOSFET and dummy gates



- Two dummy gates per side
- Fixed space between gates
- No L-, T-, U-shaped gates
- Contact larger than min. gate

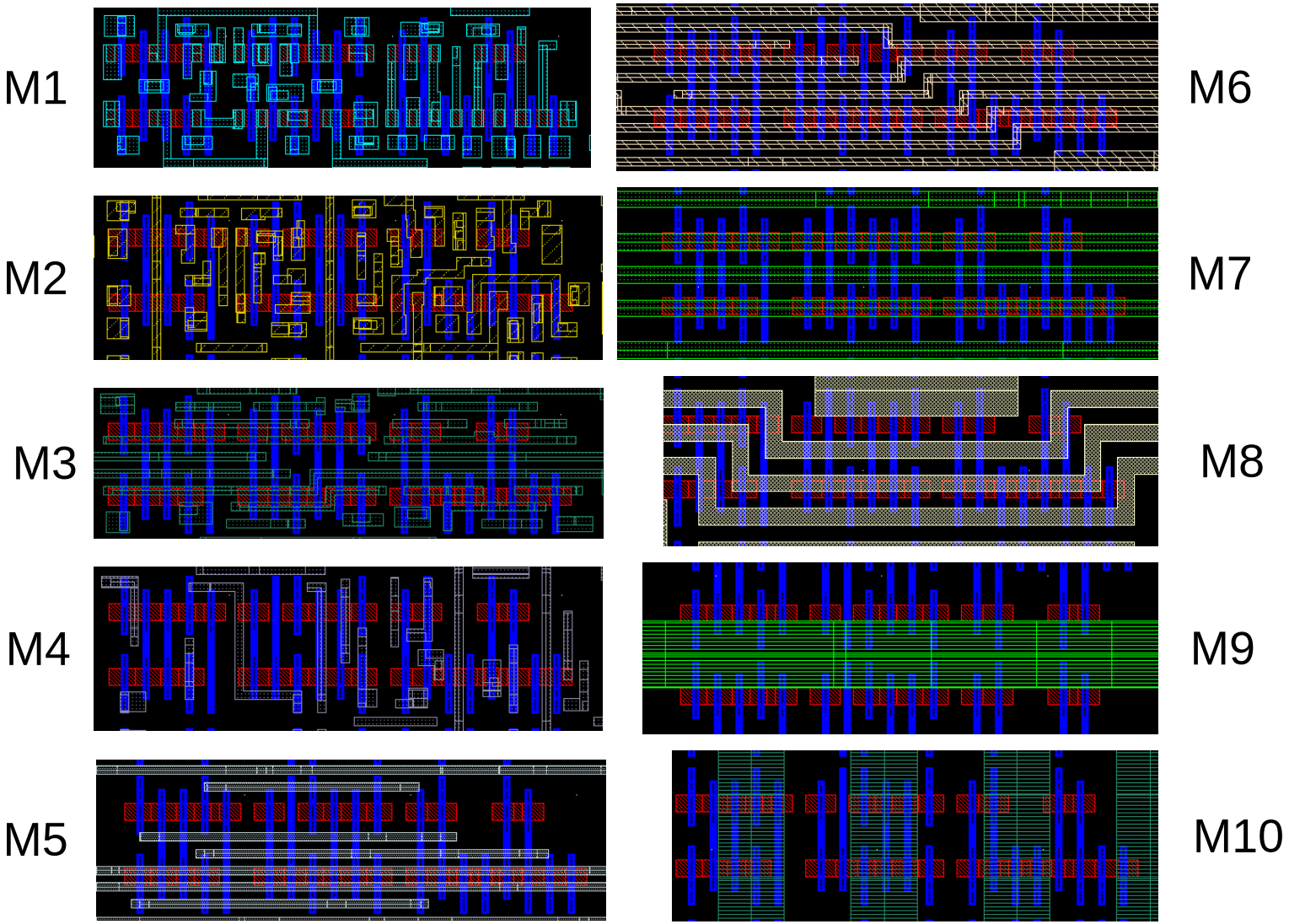
Example: multi-finger transistors



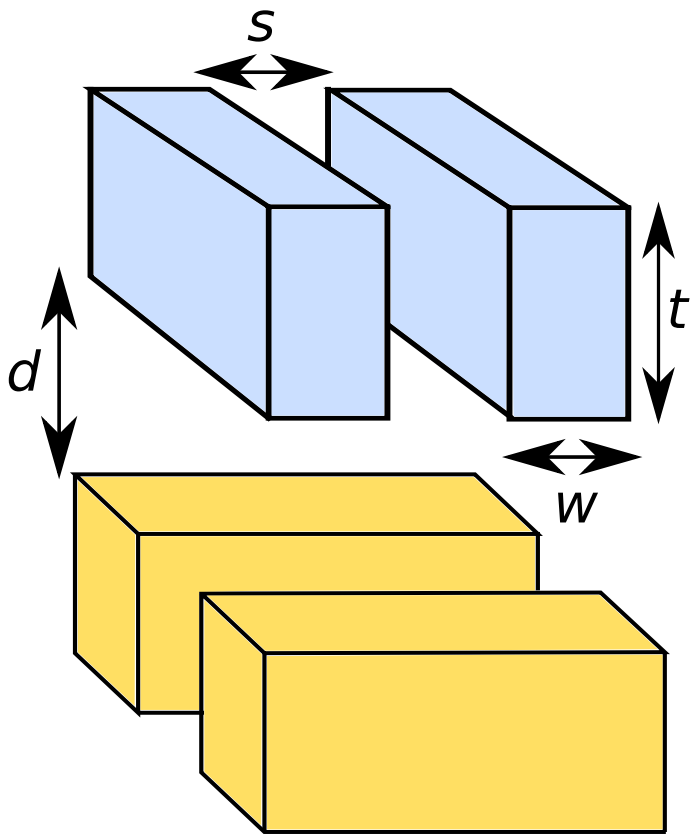
- Different width is possible

Metals (10 layers)

M1: local; M2-6: thin; M7-8: medium; M9-10: large (VDD and VSS)



28 nm technology: interconnection capacitances



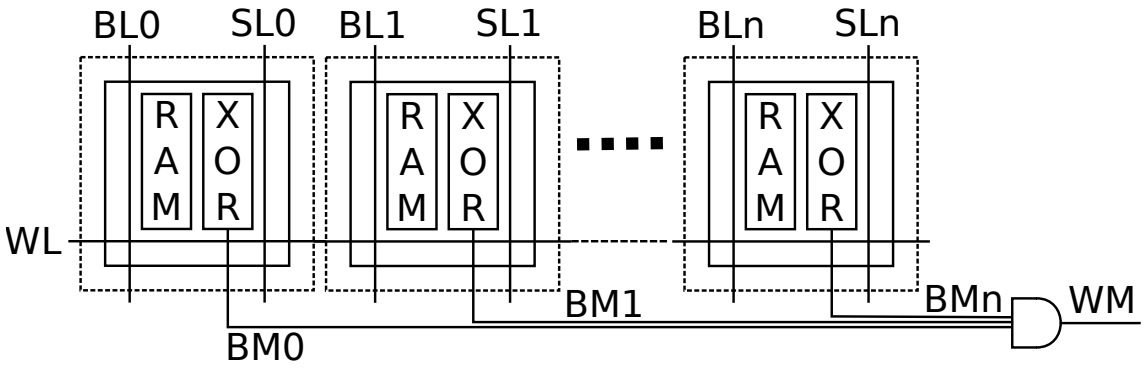
- $s < d$
- $t \approx 2 \cdot w$

Frequency performance and power consumption are affected by the capacitance of interconnections

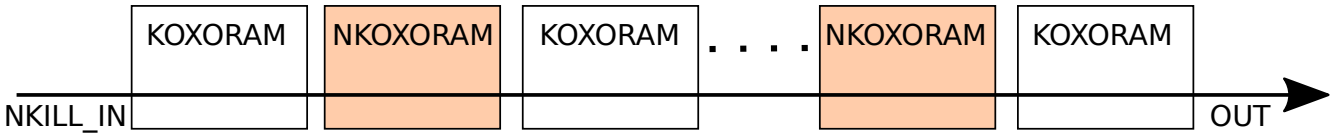
Lateral capacitance is dominant

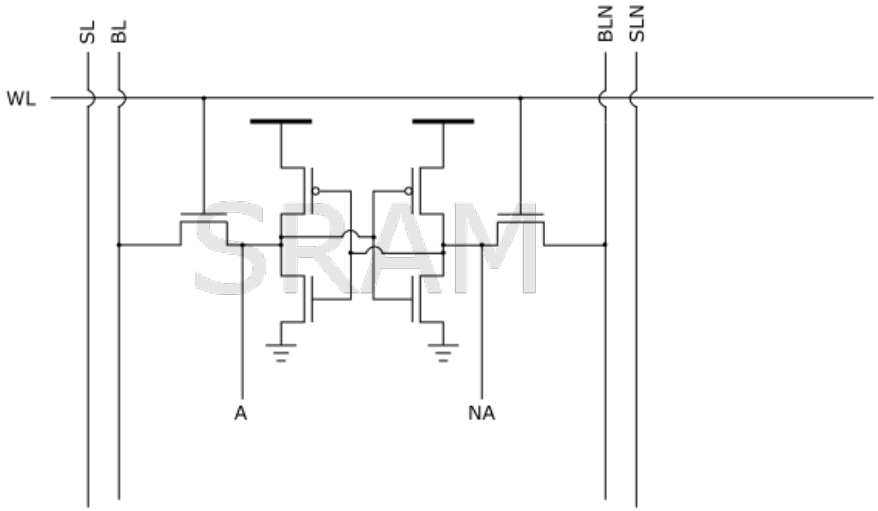
Example: Associative memory for TrackTrigger

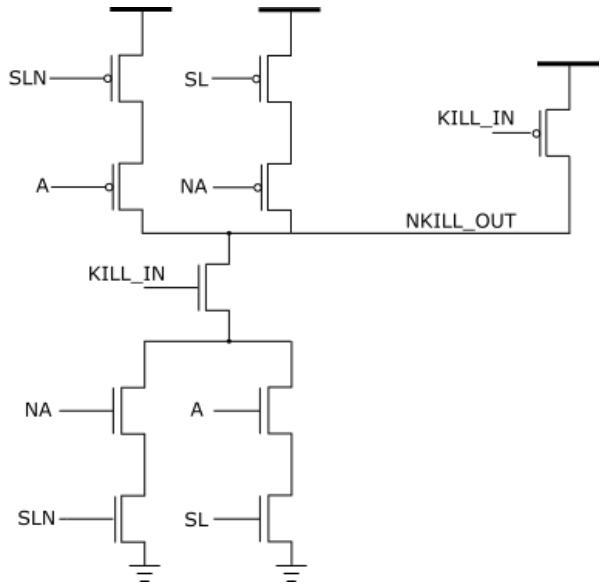
conventional:



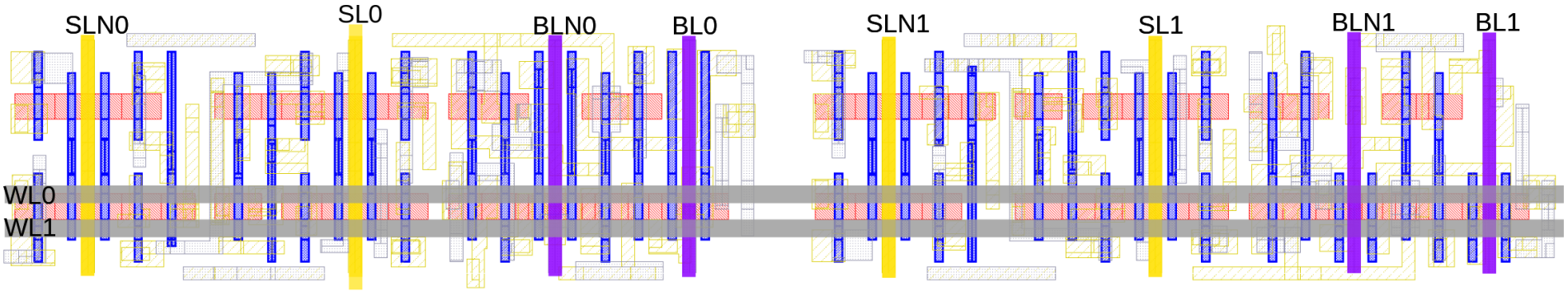
NEW:







KOXORAM cell



M2 SL and SLN, M4 BL and BLN, M5 WLs

Design goals:

- Reduce as much as possible the capacitance on SLs without increasing the cell area
- Reduce the switching activity of the transistors during comparison

Results

- The capacitance associated to the search lines is 0.27 fF for two cells (0.20 fF due to gate capacitances, and 0.07 fF due to metal-metal capacitances)
- The average energy per comparison is 0.3 fJ/bit

Analog design: DCO

- In the previous AMchip (AM06) power consumption can raise from 0.1 A to 2.2 A in 0.1 ns when it changes state from 'idle' to 'compare'
- Current peaks are synchronous with the 100 MHz CLK
- This power consumption generates a ripple on supply voltage

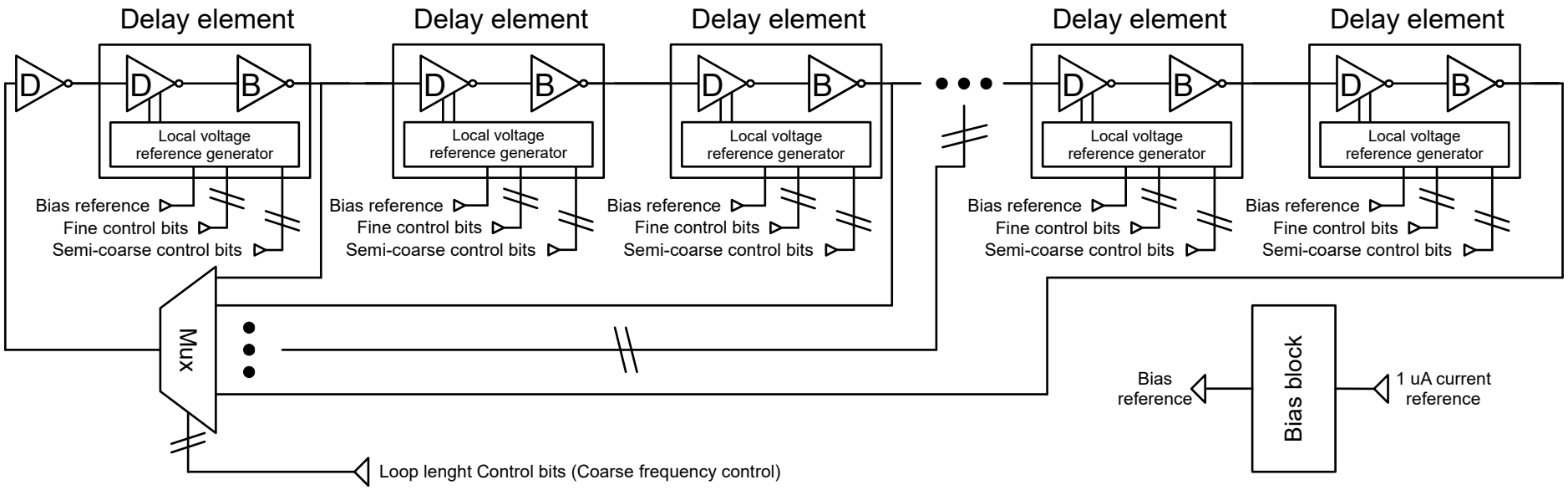
- Divide the total number of memory cells into eight groups
- Spread the power consumption of these groups along the reference clock cycle with eight phase-shifted replicas of the original clock
- Use a digital PLL produce a clock signal locked in phase with the incoming one, but with a frequency that is 8 times higher.

Oscillation frequency:

- Typical and FastFast 1 GHz up to 3.2 GHz
- Slow Slow at least 1 GHz up to 2 GHz

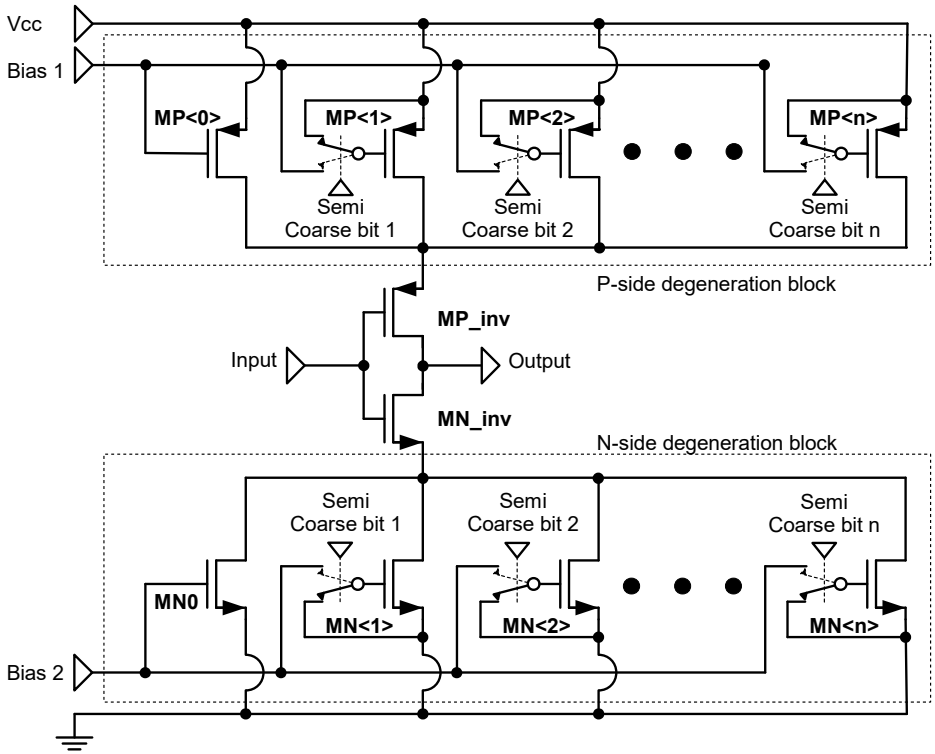
DCO Schematic

Resistors and capacitors in 28 nm technology have a variability of $> 30\%$, we decide to design a delay element only with MOS.



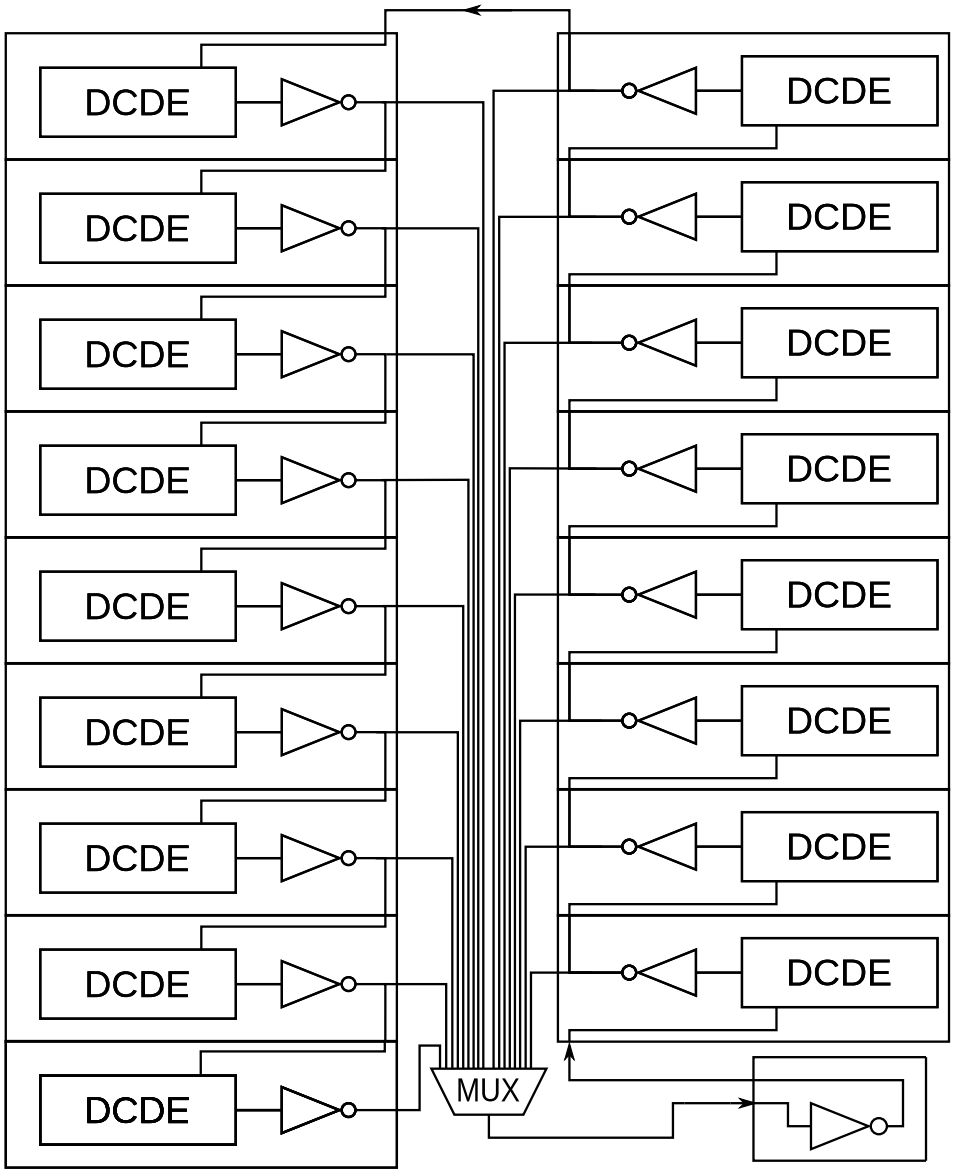
- All controls are thermometric
  - 12bit broad controls
  - 7bit medium controls
  - 64bit fine controls
- 1 µA current reference
- Delay element interleaved with Buffers
- Local and global polarization

DCO Delay element



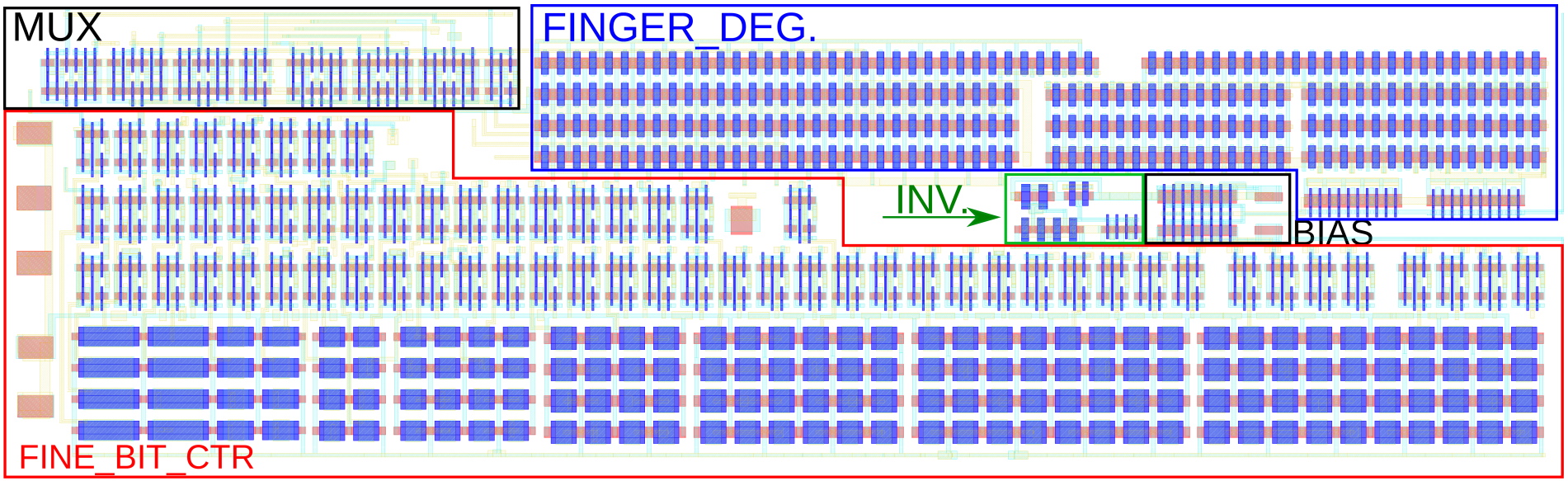
- Based on a current starved inverter
- Each mos of MP<7:1> and MN<7:1> is controlled by control bits
- MN and MP are the output of a current mirror

DCO Layout – top block



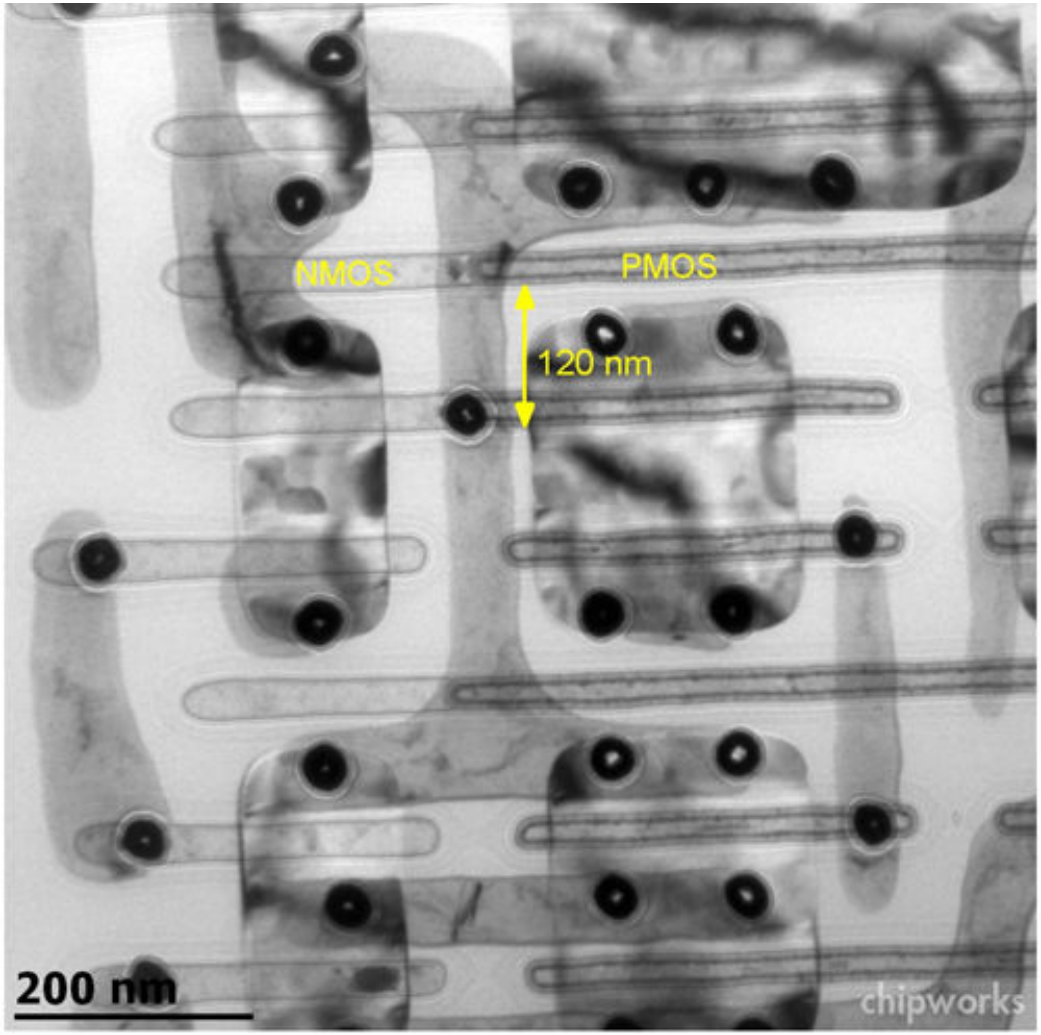
- dimensions: 44 $\times$ 83 µm
- composed by 17 delay blocks
- the returning path is design to reduce parasitic capacitances

Delay element layout



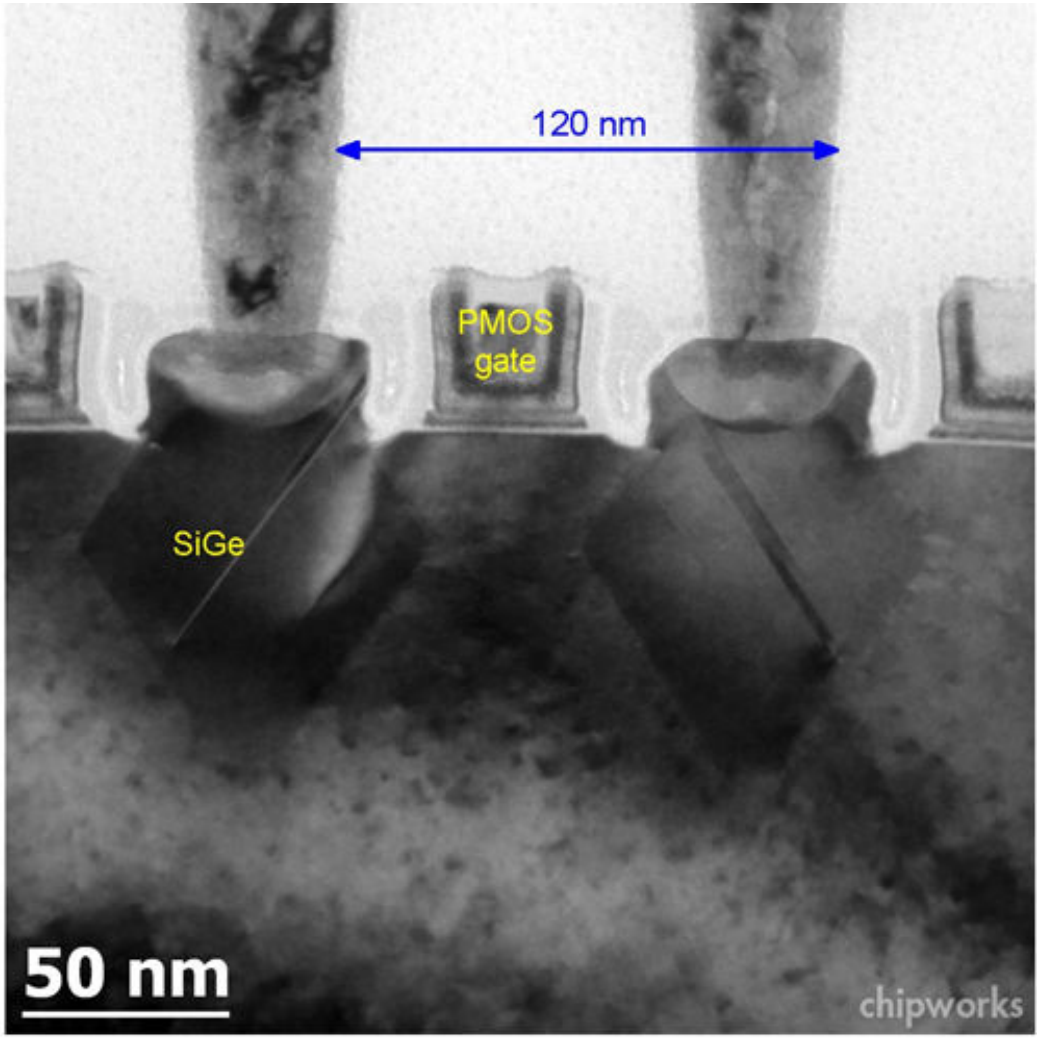
- We made a start-up simulation an the DCO starts
- Performing a post-layout simulation we discover a great dependency from fabrication corners, with the same control set(12/6/32):
  - tt = 2.2 GHz
  - ss = 1.8 GHz
  - ff = 3.3 GHz

Images (1)



Xilinx XC7K325T Kintex-7 TSMC 28 nm HPL - Plan View TEM
(from `https://www.chipworks.com/about-chipworks/overview/blog/review-tsmc-28-nm-process-technology`)

Images (2)



Altera 5SGXEA7K2F40C2 Stratix V 28 nm HP PMOS - TEM
(from https://www.chipworks.com/about-chipworks/overview/blog/
/review-tsmc-28-nm-process-technology)

Example: TSMC 28 nm 'flavors'

(from `https://www.semiwiki.com/forum/content/4530-tsmc-unleashes-aggressive-28nm-strategy-e.html`)

28 nm technologies from TSMC

HP	(high performance)
HPM	(high performance mobile)
HPC	(high performance computing)
HPC+	(faster version of HPC)
HPL	(high performance low power)
LP	(low power)
ULP	(ultra-low power for IoT and other battery powered applications)

Big differences in 28 nm 'flavors'

Low power versions use conventional **poly gate with ONO dielectric**
$\longrightarrow$ low gate capacitance, low on-current, low leakage

High performance versions use **high-k metal gate (HKMG) transistors**
$\longrightarrow$ high gate capacitance, high on-current, high leakage

28 nm HPC with 10 metal layers could be a good choice ...
We are investigating!

THANK YOU !

Next activity in WP3:
Chip design workshop, Milano, 21-22 Jan. 2018