TIMESPOT

TIME and SPace real-time Operating Tracker

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Activity plans of the six Work Packages. Long Version

Support Document to Project Proposal

The present document is added to the requested documentation for this CSN5 call as a more detailed explanation about project activities.
Our revisors will decide if its partial or complete reading is useful or not.

WP1: Design and test of 3D Si sensors for fast timing

WP1 coordinator: Gian-Franco Dalla Betta (INFN TIFPA Trento)

WP1 is concerned with the development of 3D pixel sensors optimized for timing while retaining their usual good features of low depletion voltage, and extreme radiation hardness. The work will leverage the significant experience so far gained within the INFN-FBK collaboration for the 3D pixel sensors oriented to Phase 2 Upgrades of ATLAS and CMS at the High-Luminosity LHC. In particular, the fabrication will still be based on the FBK single-sided approach using Si-Si Direct Wafer Bonded (DWB) substrates [1]. This process has already been shown to be feasible, yielding devices with good electrical figures, among them low leakage current (~1 pA per electrode) and high breakdown voltage (~150 V), thus offering a wide range for operation bias.

The main effort in both the design and the technology will be devoted to the optimization of the pixel geometries in terms of size, electrode configuration, and shapes to ensure the most uniform electric field distribution necessary to improve the timing properties. Following recommendations from the only work so far devoted to timing with 3D sensors [3], the benefits attainable by using trench electrodes will be explored, while keeping into account some relevant constraints for manufacturability. In fact, it should be mentioned that 3D sensors normally come only with cylindrical electrodes. Besides the early attempts at Stanford oriented to wall electrodes at the sensor periphery [3], trench electrodes were fabricated once at BNL/CNM [4], but they had a very wide inter-electrode spacing (~500 mm) that is not really significant. At FBK, segmented-trench edge terminations have been successfully made [5], which constitute a useful starting point for the proposed activity. Among other parameters, the sensor active (high-resistivity) layer thickness should be chosen, aiming at the best trade-off between signal amplitude and capacitance (noise), both of which increase with thickness. Of course the choice will have to take into account the properties of the read-out chip and the electrode aspect ratio (ratio of vertical and lateral dimensions of the vertical electrodes) achievable on the fabrication side, that is currently ~30:1 for cylindrical electrodes at FBK [1].

The specific activities to be carried out in WP1 are outlined in the following:

1) Initial technological tests will be carried out at FBK to check the critical process step of etching by DRIE trench electrodes of different shapes and geometries compatible with the envisioned pixel features, and their overall compatibility with the full process sequence.

2) In parallel with (1), the design and TCAD simulation of the sensors will be carried out, addressing all relevant aspects and leading to the definition of the main design parameters (sensor thickness, pixel size, electrode configuration, …). The sensor thickness should be chosen in due time to procure the Si-Si DWB substrates, whereas the layout will be finalized by the end of Q2-2018. It will contain pixel sensors with different geometrical options, but also several test structures aimed at process monitoring and also allowing the electrical and functional device characterization without the need for bump bonding. Among them, short strips and diodes are the most useful and lend themselves to be easily wire bonded to read-out circuits.

3) While the fabrication of the first batch of 3D sensors will be carried out at FBK, with completion expected for Q4-2018, the activity will focus on the preparation of the measurement setups for the automatic tests of bare 3D sensors on wafer and on the design of special PCB's for the functional characterization of prototypes.

4) Following the delivery of the first batch from FBK, the activity will be devoted to the characterization of the sensors. Electrical measurements, i.e., Current-Voltage (I-V) and Capacitance-Voltage (C-V), will be performed on test structures and sensors at the wafer level with probe-stations. These tests will allow for extracting some relevant information about the fabrication process and the design, also allowing to finely tune the TCAD simulations, as well as for selecting the best devices to be later used for functional and radiation hardness tests.

5) Test structures will be used to proceed with functional testing in the laboratory. To this purpose, devices (diodes and strips) will be mounted on PCBs and wire bonded to read-out electronics, i.e., either discrete fast amplifiers or read-out circuits developed in the first phase of WP3. These tests will include functional measurements with position resolved IR laser setups, radioactive sources, and particle beams, in order to study the charge collection efficiency, the spatial uniformity of the signals, and the signal dynamics (response speed).

6) Selected samples will be irradiated with neutrons and protons up to large fluences, and re-tested after irradiation.

7) In case the quality of pixel sensors from the first batch will be high enough, the best wafer will be used to proceed with bump bonding to ROC's. Most probably TIMESPOT WP3 ROC will be ready not before Q4-2019. In fact, among existing ROC's, the NA62 ones feature the best timing performance (~100 ps) but have a pitch of 300 μm that is far too large to be suitable for 3D sensors. The TIMEPIX3, although not optimized for timing (~1ns), has a pitch of 55 μm and would allow a first evaluation of the proposed pixels, both in the laboratory and in a beam test.

8) While the characterization of the devices from the first batch is still in progress, TCAD simulation and design activities will restart in view of the submission of the second batch of 3D sensors, that will be optimized both in terms of the sensor layout and of the fabrication technology.

9) The same test procedures adopted for the first batch will be applied also to the second one. The pixel sensors will finally be bump-bonded to the final ROC from WP3.

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WP2: Design and test of 3D Diamond sensors for fast timing

WP2 coordinator: Silvio Sciortino (INFN Firenze)

The main goal of the Workpackage WP2 is the development, fabrication and characterization of 3D diamond sensor for timing application. This will be mainly pursued by:

- performing TCAD simulations aiming at evaluating the effect of different electrode configurations and biasing schemes on charge collection/timing performance;
- improving the laser fabrication technology of 3D sensors by modification induced by radiation of CVD diamond material.

TCAD simulations

Standard design and verification tools should be adopted following the conventional Technology Computer Aided Design (TCAD) flow. However, diamond is not included in the material's library of commercial TCAD simulation tools. A suitable modeling scheme is being developed within a previous INFN CSN5 experiment (3DOSE 2017-2018) [1, 2]. Comparison between simulation results and measured data of charge collection in terms of charge collection efficiency (CCE) as a function of the applied voltages have been carried out on simple test structures fabricated by different vendors (Element Six, II-VI, Audiatec -University of Augsburg, see Fig. 1).
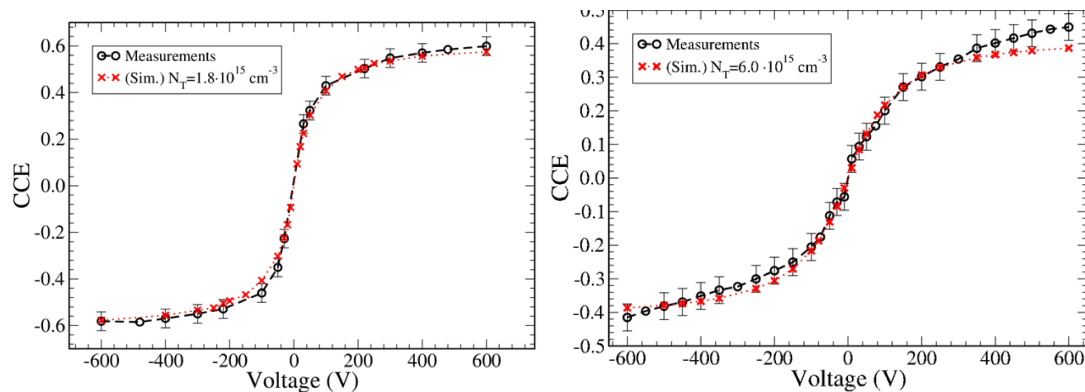

Figure 1 CCE as a function of the applied voltages – Left: Element 6 sample (5×5×0.5 mm3), planar contacts (2D). Right: Sample of diamond heteroepitaxially grown on iridium at the University of Augsburg (5×5×0.5 mm3), planar contacts (2D).

The good agreement between simulation findings and experimental measurements foster the application of this tool for the predictive analysis and the design optimization of more advanced diamond device, sensors with 3D architectures fabricated with different diamond materials. In particular, the effect of different electrode configuration and biasing on the electric field profiles can be simulated, aiming at avoiding low electric field regions in diamond detectors (Fig. 2). Radiation damage effects can be evaluated as well within the TCAD simulation framework.
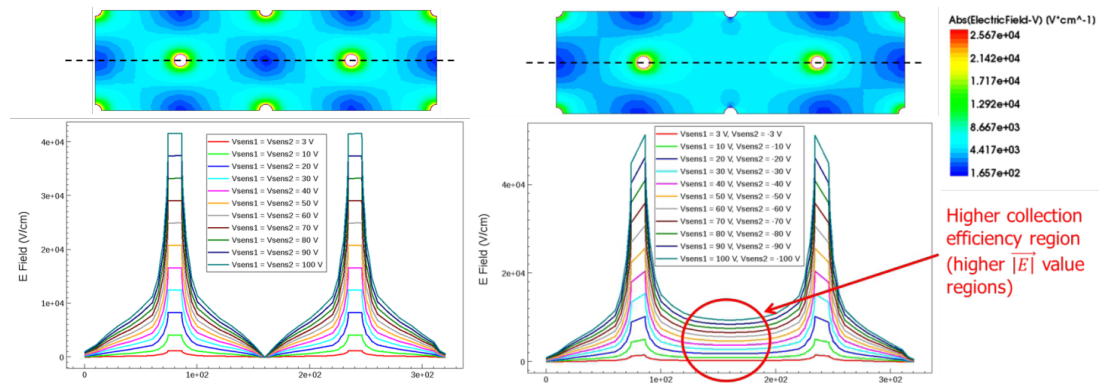
Figure 2 Effect of sense node biasing at same polarity (left) and opposite polarity (right) on inter-electrode electric field distribution.

3D fabrication technology

Another critical milestone of WP2 is the improvement of the technology of laser fabrication of 3D electrodes. Figure 3 shows the present state-of -the-art of our radiation hardness study [3,4]. The static collected charge response (number of electrons) of a 3D sensor on monocrystalline 5x5x0.5 mm^3 plate is plotted as a function of equivalent fluences of irradiations of 1 MeV neutrons.
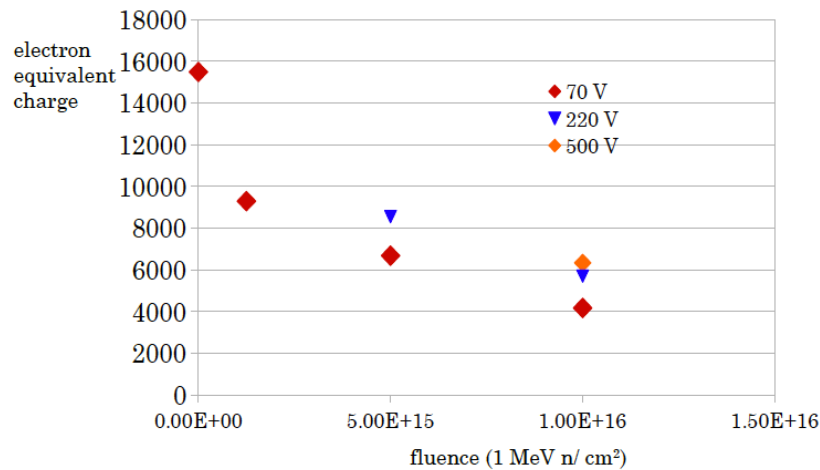

Figure 3.

We note an inefficiency at zero fluence (100 % collection correspond to 36 e/um that is 18000 electrons for a thickness of 500 um), due to the process of fabrication when the pitch is as low as 50 um. We also note that the 3D sensors are operative after a fluence of 1 10^{16} n/cm^2 at 40% of the unirradiated signal level. We intend to explore further the 10^{16} n/cm^2 fluence level to assess the ultimate radiation hardness of our sensors.

The first batch of our samples yielded a time resolution of 280 ps [5]. We ascribe this unsatisfactory result to the high resistivity of the modified material which is a mixed sp^2-sp^3 phase [6]. In fact the measured capacitance of our sensors is about 25 fF per each electrode pair which multiplied by a column resistance of the order of 10 k Ω, gives a rationale for the observed resolution. Nonetheless, it has been demonstrated that the resistivity can be strongly diminished (1 Ω cm to 0.022 Ω cm) by removing the optical aberrations [7]. This can greatly increase the sensor's time response, which will be limited, after this optimization by the drift time between electrodes.

Moreover a better definition of the laser focus will allow to use a lower pulse intensity

and minimize the local damage to the surrounding diamond lattice and the related inefficiency of the as-fabricated sensor.

High temperature annealing in vacuum (up to 1100 °C) will also be attempted in order to improve the connection between conductive domains inside the modified material of the electrode. The optimization of the electrodes geometry resulting from the TCAD simulations, will finally lead to the required resolution range of tens of ps.
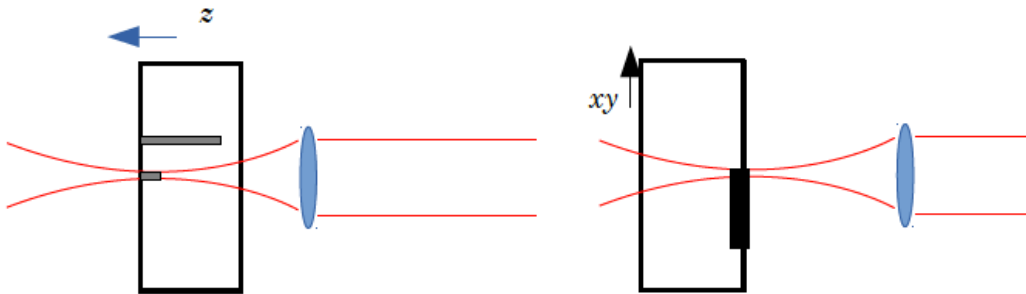

Figure 4

Figure 4 shows the principle of laser fabrication of columnar bulk electrodes (on the left, obtained by a fs laser) and surface graphitization (on the right, obtained by a ns laser) [8]. As the focus of the laser is moved inside the bulk to write the columnar electrode (actually the sample is moved with a controlled *xyz* system), the penetration depth of the laser beam is changed. An adaptive optics is required to correct in real time for spherical aberration.
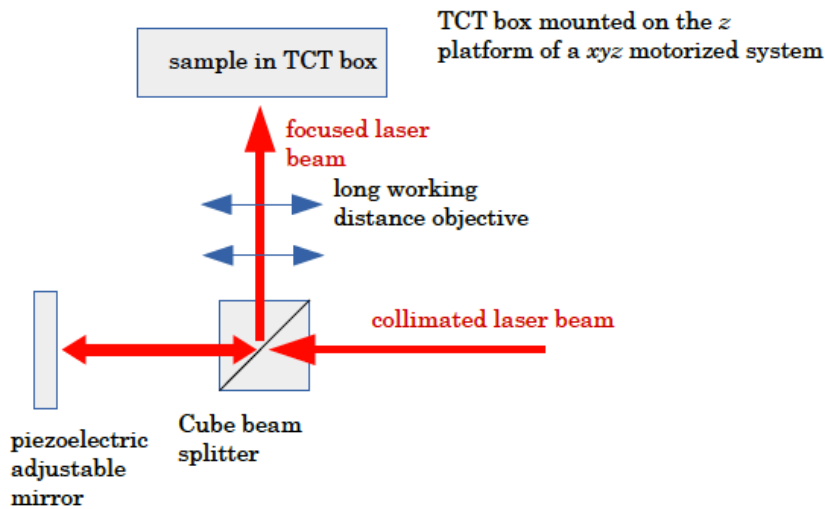

Figure 5

Figure 5 is a schematic of the procedure we intend to follow to correct for aberration. The piezoelectric mirror is adjusted at a given position of the focus inside diamond to correct the laser wavefront. The laser excites carriers in a planar diamond sensor well below the graphitization intensity. The correction of the wavefront is given by optimizing the transient current intensity recorded. As the correction is determined once for all at any penetration depth inside the diamond material, the TCT system can be replaced by a virgin diamond plate in a dedicated sample holder, in order to fabricate the 3D sensors.

This is in our opinion an effective way to solve the problem far less expensive than

correcting the wavefront with a real time adaptive system as in ref [7]. The Transient Current Technique system is sketched in Fig. 6.
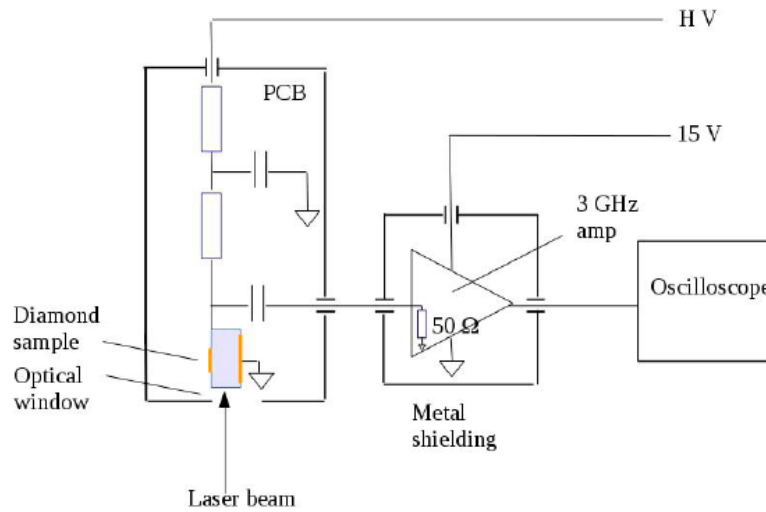

Figure 6 TCT setup (modified from Fink et al. [9])

In Fig. 6 the laser probe is entering the sample through a polished face perpendicular to the ohmic contacts connected to the readout setup.

For the uniformity of the response of the pixel detectors we intend to fabricate we need motorized *xyz* stages of repeatability of less about 1 um which will ensure that the uniformity of the unit cell sizes will not be affected by faults in positioning the laser beam inside the sample. The range of the *xyz* linear stages is 26 mm which is necessary to adapt a 20x20 mm^2 sample in the last phase of our fabrication activity.

Interconnection with readout electronics

The interconnection between the columns is carried out by surface graphitization with no need of masking and metalization. As shown schematically in Fig. 4 (on the right) the laser irradiation at the sample's surface can turn the *sp*^{3} diamond bonds directly to *sp*^{2} graphitic ones. However interconnection with the readout electronics is the second main step of 3D sensor fabrication. Different strategies will be employed as local metalization of the surface graphitic paths and wire-bonding or even direct wire-bonding on graphite contacts which has been reported by other group of research, more focused in laser fabrication of surface contacts [10].

A bonding technique developed in a previous experiment (GR5, RAPSODIA 2007-2009) can be possibly used: laser enhanced direct bonding of diamond to metal. In this technique UV laser pulses are transmitted through the transparent diamond and absorbed by an opaque material which melts locally and melt a nano-layer of diamond, resulting in a mechanically robust connection. This has been proposed by us for silicon-diamond integrated chips [11,12] but has been also demonstrated for diamond Al bonding (experiment GR5,3D_SOD).

Spectroscopy of the modified materials and other characterizations

Raman spectroscopy [6] of the modified material is of paramount importance for two

aspects: (i) monitoring the chemical bond of the modified material; (ii) measuring the stress state of the diamond material around the electrodes. This will serve to give a rationale for the measured resistivity and possible local damage of the crystal lattice and complement any electrical characterization. Timing measurement can be envisaged using a MIP radiation source or the graphitization laser itself, which far below graphitization threshold can be used a source of photons with pulse width as low as 25 fs.

Characterization of the base CVD material

A very important issue is the choice of the diamond material. Polycrystalline diamond (pCVD) is believed to be highly inhomogeneous due to grain boundary, although progress in the CVD technology has allowed to strongly increase the grain size and reduce the defect density. Monocrystalline ("single-crystal", sCVD) diamond is quite expensive because it requires homoepitaxial growth of (electronic/quantum grade) pure material on a less pure synthetic diamond substrate. For this reason the highly homogeneous scCVD material is limited in area to below about 1 cm^2. Our choice of testing heteroepitaxially grown diamond on iridium (DOI), through a collaboration with the University of Augsburg, can be a viable solution because DOI is a highly homogeneous material. DOI defects are dislocations which are present also in monocrystalline diamond. Hence the heteroepitaxial grown material is also technically referred to as "single crystal" also if its electronic quality is not yet the same of the monocrystalline best samples (synthesized by Element Six or IIa). The cost is similar to that of polycrystalline material and the homogeneity and quality is close to that of the sCVD material and is continuously improving. In addition to that DOI is not limited in area. Very recent progress in fabrication have resulted in a 9 cm diameter wafer (see Fig. 7 below and ref. [13]).
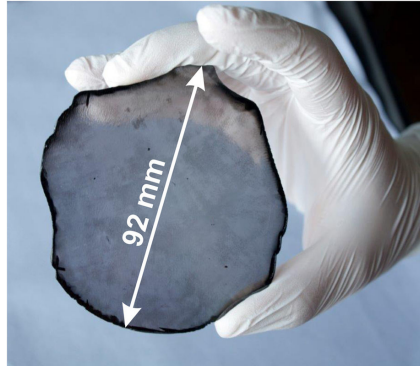

Figure 7 Single crystal of diamond (free from the substrate 1.6 mm thick) grown heteroepitaxially on an iridium substrate (DOI) by the University of Augsburg. From ref [13]

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WP3: Design and test of front-end IC for pixel read-out (ROC)

WP3 coordinator: Valentino Liberali (INFN Milano)

The front-end electronic interface will be designed in ultra-scaled CMOS technology (28 nm CMOS provided by TSMC through Europractice).

The research unit in Milano has already used the 28 nm CMOS technology for the design of an associative memory chip for the ATLAS trigger [1]; the chip includes a low-voltage differential signal interface (LVDS) for serial input/output communication at 1 Gbit/s, supplied with 1.8 V [2]. The research unit in Cagliari developed a custom TDC for the muon system of the LHCb experiment [3] and the LHCb muon system upgrade, where a fully synthesizable digital circuit has been implemented [4]. The research unit in Torino has recently partecipated to the CHIPIX65 CSN5 initiative, where several cells for the ATLAS and CMS pixel readout have been developed in 65-nm CMOS technology.

The suitability of the 28 nm CMOS for analog design and its radiation tolerance are currently being assessed by other projects, including the Scaltech28 project funded by INFN [3].

To take advantage of the scaled technology, the analog part of the front-end must be very simple, and the information extracted from the pixel will be converted in digital format after the amplifier and shaper stage. As the two sensor arrays have different characteristics (silicon and diamond), two different versions of the preamplifier are foreseen. The two circuit designs will be both the result of an accurate optimization study between a transimpedance amplifier (faster) scheme and a charge integrating amplifier scheme (slower but less noisy).

The design of the analog front-end must account for process variations (in particular, the "Slow" corner is known to be the most difficult one for high-speed analog circuits), for component mismatch, and for noise. A suitable trade-off between area, speed, mismatch and noise is crucial for a successful design.

The workpackage includes the design, fabrication, packaging/assembling and test of four mini-ASICs, each of them having an area of 2 mm x 2 mm:

1) Analog front end and test structures: different preamplifier architectures, shaper, analog buffer, analog multiplexer, and single transistors with different W/L ratio. All the circuits in the mini-ASIC will be controllable and observable from external pins, to characterize the component and to validate separately each circuit.

2) Time-to-digital converter and digital read-out. This mini-ASIC will be designed through synthesis from VHDL (or Verilog) description. The characterization will demonstrate the functionality and the speed of the digital part. A preliminary demonstrator could be built by assembling together the chip #1 and the chip #2. Radiation tests will be performed on both the analog and the digital mini-ASIC (in WP 6).

3) First pixel demonstrator, consisting of a small array of processing chains made with the blocks included in chips #1 and #2, improved according to the outcome of tests. The demonstrator will be tested alone; then it will be assembled with the detector (in WP6), and tested again.

4) Second pixel demonstrator, consisting of a larger array, with minor design modifications (if needed). The system made by assembling the second demonstrator with the sensor is the final demonstrator of the project.

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WP4: Design and implementation of fast tracking devices

WP4 coordinator: Nicola Neri (INFN Milano)

The reconstruction of charged particle trajectories in high energy physics experiments is a complicated task that requires the identification of possible trajectories from a large number of detector hit combinations. Fast track finding systems are based on custom processors that allow track pattern recognition without combinatorics by means of parallel matching of hits to pre-calculated track patterns stored in pattern banks. Track parameters can be extracted subsequently from linearised fits using constraints obtained from pattern matching. Existing fast track finders are based on Associative Memory chips (AM): devices that rely on the general concept of content-addressable memory where to retrieve data, one provides the data and obtains the address at which that data is stored.

The first use of such a device was in the CDF experiment [1] and provided good quality tracks with a latency of about 10 µs at an event rate of 30 kHz. Recently the ATLAS experiment developed a device [2] based on a similar concept and capable to operate at 100 kHz event rate.

The full exploitation of the high luminosity LHC requires new detectors and trigger systems. Level 1 trigger decisions based on tracking information are crucial for reducing data rate to sustainable level and maintaining good efficiency and purity for signal events. However real-time tracking at LHC is extremely challenging due to the 40 MHz event rate, the large flow of data from tracking detectors exceeding Tbit/s, and the requested short latency of the response at the level of a few µs. In order to achieve this goal it is necessary to explore different approaches and possibly find innovative solutions.

Recently, a fast track finding system based on the artificial retina algorithm [3] has been proposed for the upgrade of the LHCb experiment [4]. The algorithm allows massively parallelisation of the calculations and it is implemented in commercial FPGAs that are capable of processing high data rates, in excess of Tb/sec per chip. This approach features different characteristics with respect to the AM approach since only relevant data reach the processing units (engines), and the data processing starts already in the switch while data is transmitted. Ultimately, the retina algorithm provides an analog response for the track matching contrarily to the AM that returns a "yes/no" pattern matching response.

The INFN-CSN5 Retina experiment (2015-2017) developed a fast track finding prototype implemented in commercial FPGA. A real-time tracking prototype based on artificial retina algorithm was constructed and tested demonstrating the feasibility of the approach [5]. Studies are still ongoing to evaluate the performance at high event rates, e.g. up to 40 MHz and with hundreds of tracks per event, using latest generation FPGAs and realistic simulated data in input.

Here, we intend to make an additional step forward. We propose to develop an innovative detector, based on accurate time and position measurements, coupled to a dedicated processor for real-time reconstruction for a 4D real-time tracking system [6, 7], as depicted in (right) Fig. 1 and Fig. 2. This device would provide in real time the parameters and the time of the track for fast trigger decisions based on 4D pixel hit information. In order to achieve this goal, we rely on two levels of processing of the hit information. In the first level, the system will reconstruct track segments, "stubs", based on hits on adjacent pixel layers within space and time acceptance of real tracks. In a second step, the reconstructed stubs will be sent to the fast track finding processor for the reconstruction of the track parameters.

In order to test the ultimate performance of the fast track finding processor, a board with latest generation FPGA (e.g. Xilinx Virtex7 Ultrascale), featuring high-speed serial links (>10 Gb/s) for high band data transfer (>1 Tb/s), will be developed in the project. High speed

tests will be based on simulated data generated by a detector emulator board and sent in output through SerDes modules and optical transceivers to the fast track finding board. Such a board will be a first prototype for a building block of a system of large dimensions, capable to process a large tracking detector of a LHC experiment. The performance measured on the prototype board will be eventually scaled to a complete system.

The main tasks of WP4 are:

- Optimisation of the 4D fast tracking algorithm and tracking detector layout based on high-level simulations ;
- Design of fast track finding device architecture based on a realistic tracking detector and running conditions of the HL-LHC ;
- Study of the performance of the device based on low-level simulations ;
- Implementation of the firmware in fast track finding boards based on Bologna (ATLAS) and Milano (Retina) boards. Four boards developed in Bologna will emulate hits of the detector and perform stub reconstruction. The Retina board will receive the stubs and perform the track reconstruction ;
- Emulation of a realist tracking detector at HL-LHC and study of the performance of the device based on simulated data on optimise board to be designed and constructed in Timespot ;
- Study the performance of the fast track finding device using a multilayer pixel prototype in a test beam.

Its main Milestones are:

- Dec. 2018: document with the specifications for the fast track finding device for a realistic tracking detector for the HL-LHC phase
- Sept. 2019: Test of the performance of the device using emulated tracks on existing boards developed in ATLAS and Retina experiments
- June 2020: Test of the performance of the device using a emulated data using an optimised board to be developed in Timespot
- Dec. 2020: Test of the performance of the device on beam using a multilayer pixel detector prototype
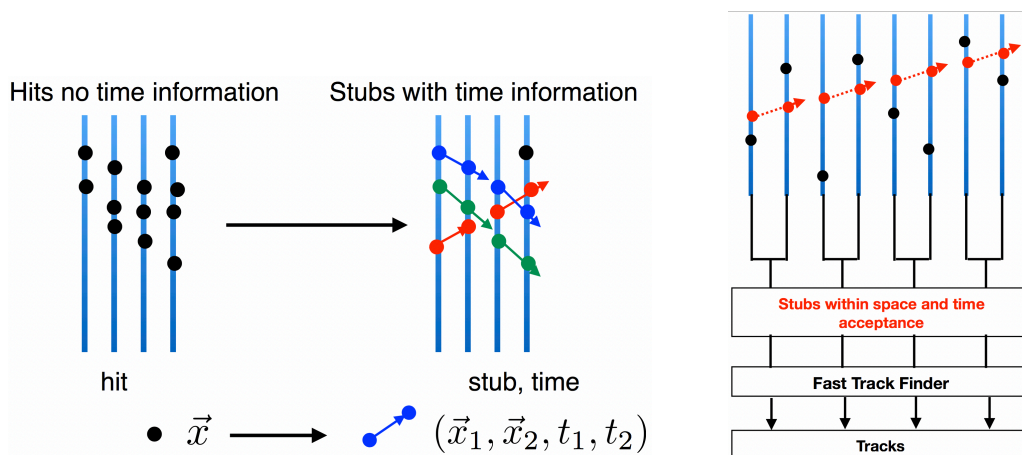

Figure 1. (left) Track pattern recognition based on hits with no time information compared to track segments "stubs" with time information; (right) sketch of a conceptual design for a detector with embedded tracking capabilities based on stub information.
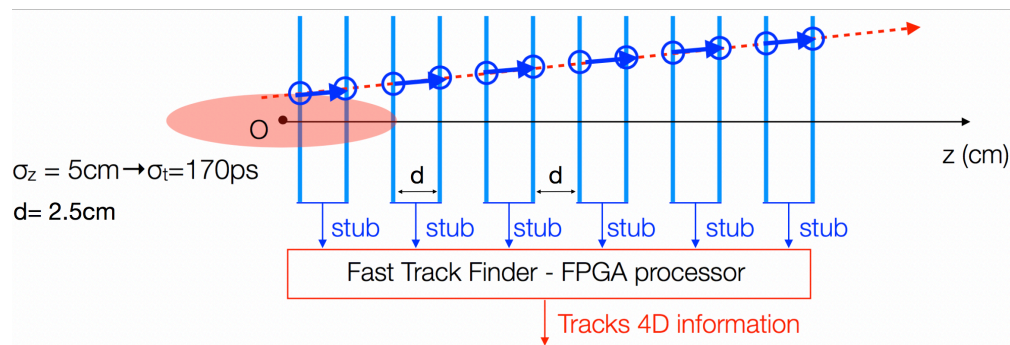
Figure 2. Sketch of a possible 4D tracking device for the high luminosity phase of the LHCb experiment. The distance between the pixel layers is d=2.5 cm and the luminous region is Gaussian distributed with σ=5 cm.

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WP5: Design and implementation of high speed read-out boards

WP5 coordinator: Alessandro Gabrielli (INFN Bologna)

WP5 exploits firstly the know-how and skills developed recently for having commissioned the readout upgrade of the current ATLAS Pixel Detector (the entire set of layers), and for being involved into the Phase II TDAQ ATLAS upgrade [1]. Secondly, the project can benefit from the long experience acquired by the Bologna group in the analysis of the LHCb data (on-line and off-line). This competence will become crucial for the study, test and the implementation of the fast tracking algorithms (FTA) at the front-end and readout level for fast pre-processing tracking/triggering. For this specific task, the Bologna group will be also involved in the activities of the WP 4.

High Speed Trigger investigation

WP5 will join the effort to develop a neural-network based reconstruction algorithm (RETINA-like) to be implemented on to-date high-speed multichannel FPGA devices. In addition, we want to fit the current software version of RETINA used in Milano into the below custom Pixel-ROD board that features two Xilinx devices: one Kintex7 XC7K325T-2FFG900C and one Zynq XC7Z020-1CLG484C with physical dual-core ARM Cortex-A9. The second FPGA can run directly part of the RETINA software, currently used within the Milano group, to generate emulated data. These data can be sent to the second FPGA on the same Pixel-ROD board that is dedicated to run the first layer of stubs of the RETINA algorithm. The Pixel-ROD board features 16 x 10 Gb/s electro-optical transceivers that can be used to run several channels in parallel, for example 8 input lanes to reach 80Gb/s data rate and 8 output lanes to out the data towards the PCIe channel. Another possibility id to send the output data, after the stub layer implemented on the Pixel-ROD, to a second custom board (gFEX in use in Milano) that features hundreds of 10 Gb/s lanes to fit the full RETINA algorithm. In conclusion, this activity is aimed at studying, analyzing and validating a hardware-based algorithm to data reconstruction for application in future triggers.

Data Taking application

The Pixel-ROD board in use in Bologna (two prototypes only) already features a sufficient number of I/O channels to be immediately used as readout board to interface with new front-end devices. The only restriction is that the inputs to the board must be digital. Any other specification can be adapted via firmware on the two FPGAs. This approach can be used in the test beams that will be built at CERN within the TIMESPOT collaboration. In particular, the PCIe (express PCI gen. 2 8 lanes), will be plugged into a PC mother board with free PCIe slots. For this reason Bologna has a secondary goal to set up a test stand for this application using a "PCIe-base crate" to mount eventually more than one board at a time, with or without a gFEX board.

Figure 1 shows the Pixel-ROD board with a list of the main technical features. Again, this board was designed and is currently oriented to ATLAS upgrade applications for data readout or interface to other boards of the TDAQ collaboration (Felix cards). In Bologna we can handle the necessary firmware.

✓ Kintex7 to Zynq bus 21-bit differential bus
✓ 32-bit / 64-bit DDR3 differential buses
✓ SFP diff bus (1 Transceiver)

- ✓ 2x ETH diff buses (1 Transceiver)
- ✓ FMC (HPC) diff buses (4 Transceivers)
- ✓ FMC (LPC) diff bus (1 Transceiver)
- ✓ 2 x UART buses
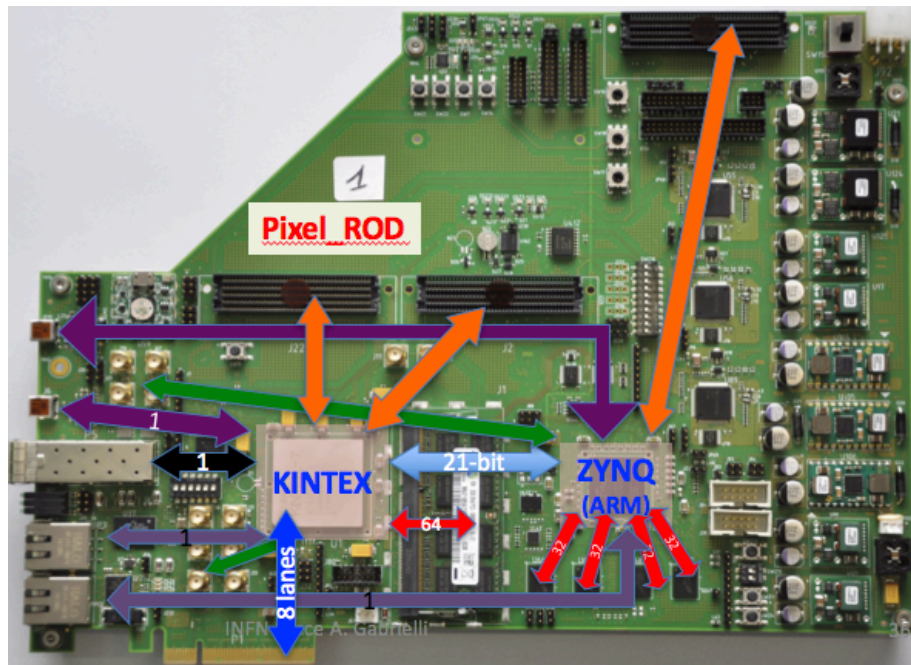- ✓ 2 x SMA (1 Transceiver)
- ✓ PCIe (8 Transceivers)

Figure 1. ATLAS Pixel-ROD board

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WP6: System integration and test

WP6 coordinator: Alessandro Cardini (INFN Cagliari)

WP6 addresses the sensors and electronics radiation-hardness qualification, their assembly and system level tests both in the laboratory and on dedicated beam tests and the construction and test of the final demonstrator.

Initial component qualification

Both the sensors and the FEE chip will be initially tested in our clean rooms using probe stations. 3D sensors will be at first qualified in DC and some pixels will also be bonded to a single-channel preamplifier for preliminary measurements of the sensor, fully aware of all the limits due to the non-optimal connection between the pixel and the preamplifier. The readout chip will also be tested on the probe station by injecting a know charge at the input. In these initial tests the general functionality of both the sensors and the readout chips will be assessed, but likely not much will be learned from the point of view of their timing performances. Subsequently the 3D sensors will be bump-bonded to FEE. The bonding will be done using available techniques at well-known firms as Selex [1] and/or IZM [2]. After this the assembly will be mounted on a test board and will be tested in laboratory. A 1064nm 5ps pulse width laser will be used to illuminate, by means of an appropriate focusing optics and an automated XY scanner, a specific area of a single pixel, allowing performing charge-collection efficiency and time resolution measurements. Radioactive sources will also be used at this stage, in particular electron (^{90}Sr and ^{106}Ru) and low-energy photon sources (^{55}Fe).

Radiation-hardness qualification

The qualification of the individual components is the first step of the radiation-hardness qualification procedure of the final detector. Our sensors and their readout chips need to be able to operate after 2E+16 1 MeV neutron equivalent per cm^2, the fluence expected at 3cm from the LHC beam line after 3000fb^{-1}, as show in Fig. 1. In this region the total ionizing dose (TID) will be about 10MGy [3].
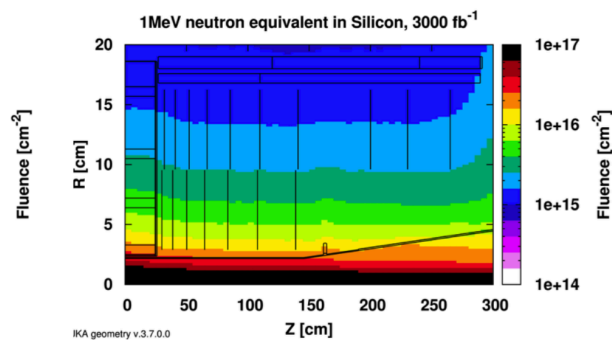

Fig. 1: Map of the expected particle fluence in the CMS Inner Pixel volume at an integrated luminosity of 3000 fb^{-1}, expressed in terms of 1 MeV neutron equivalent fluence [3].

The sensors and the readout chip will be initially characterized using X-Ray tubes, as this is the easiest way to integrate an equivalent TID in a test environment. Our group has already used the CERN facility available from the CERN/MIC group [4], able to provide dose rates in excess of 10MRad/h (100kGy/h), allowing reaching the expected TID in a few days. The CERN/MIC facility also includes a semi-automatic probe-station with a thermal chunk able to operate down to -50C, allowing powering both sensors and electronics during the irradiation procedure. Similar facility also exist at the Cagliari and Genova Research Units, so many tests could also be performed in our laboratories. The sensor bonded to the readout chip will be tested for radiation hardness by exposing it to a charged hadron beam. For these tests the CERN IRRAD [5] facility is among the possible options that our group is considering. In IRRAD the sensor and the chip are directly exposed to the CERN PS 24

GeV/c proton beam, allowing to reach very high proton fluences in a short time, thanks to the 5E11 protons per spill and a standard beam spot of 12mm x 12mm (and as small as 7mm x 7mm with a special beam tuning). Similar fluences could also be obtained in other facilities as the PSI Irradiation Facility (PIF) [5] and at Louvain la Neuve [6], but also in Italian INFN laboratories (TIFPA, LNS and LNL). The access to these facilities will be planned at the beginning of 2018, to allow irradiation tests to be performed when sensors and chips will be available. We foresee a minimum of two irradiation campaigns, one in 2019 and one in 2020. We plan to use three reference doses for the first irradiation campaign: 1e+15, 5E+15 and 1E+16 1MeV neutron equivalent per cm^2, to get a full picture of the evolution of the radiation damage and assess the viability of these 3D technologies at higher doses; in a second irradiation campaign we are planning to push the irradiation up to 2E+16 1MeV neutron equivalent per cm^2.

Detector qualification with beam

The sensor bonded to the readout chip will be fully qualified on a charged hadron beam line. The LHCb Collaboration has a permanent test facility on the SPS H8 beamline at the CERN North area, and the Collaboration has granted us the use of their experimental area and all the common facilities. A pixel telescope with micrometric resolution developed by the VELO group is available and will be used to measure particles with precision independently of the detectors under test. A XY moving table is also available and will be used to align the detectors on the beam line. More facilities, as a cold-water cooling system, are available and could be used if needed. While the SPS H8 beam line would be the preferred location for our beam tests, other facilities are also considered. The πM1 beam line at the Paul Scherrer Institute (PSI) has been successfully used in the past years by many of us, and PSI support to detector test activities has always been extremely effective. The detectors to be tested will be mounted on an optical rail located inside a thermally-insulated box, allowing also shielding from ambient light. A patch-panel on the outside of the box will expose all the cable and optical fiber connections, allowing an easy installation of the system on the test beam area and the system debugging in our home laboratories. We are also considering the possibility of cooling the detectors by means of thermoelectric cooler or by an evaporative CO2-based cooling [7]: in this case the box will be continuously flushed with dry nitrogen to avoid water vapor condensation. A triggerable silicon strip telescope, consisting of 8 planes of sensors with 180 μm pitch and 512 channels per plane [8,9], is owned by our Milano colleagues and is available for use.

Final demonstrator assembly and testing

The final demonstrator will be engineered and will be integrated at the RU of Cagliari. It will be installed in the same box used for detector testing. A few days long preliminary dry run will be performed before moving the demonstrator to the beam line for the final testing. A big effort will be devoted to the preparation of the data taking software and the real-time monitoring software, to allow performing most of the important measurements (efficiency, time resolution) in real time.

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