The Upgrade of the ALICE Inner Tracking System at the CERN LHC

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Outline

1. Present and future of ALICE
2. Inner Tracking System upgrade
3. Features of the new tracker: detectors, modules and staves
4. Expected physics performance

ALICE is an experiment at the Large Hadron Collider (LHC) at CERN, Geneva.

ALICE was specifically designed to study the nuclear matter at high densities and temperatures: Quark Gluon Plasma (QGP).

Present setup (LHC Run 2):
- Central Barrel ($|\eta| < 1$):
  - vertexing, tracking, particle identification.
- Muon spectrometer: $2.5 < \eta < 4.0$.
- Detectors for timing and centrality determination

**Key Components**

- ITS (Inner Tracking System)
- TPC (Time-Projection Chamber)
- TOF (Time of Flight)
- TRD (Transition Radiation Detector)
- EMCal
- Muon
- TRD

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6 layers:
- Silicon Pixel Detectors (SPD)
- Silicon Drift Detectors (SDD)
- Silicon Strip Detectors (SSD)
ALICE – Run 3 (2021-2023)

**Physics goals**
- High-precision measurements of rare signals with main focus on the low $p_T$ region.
- High-precision measurements of QGP properties.
- Target luminosity (Pb-Pb $\sqrt{s_{NN}} = 5.5$ TeV): $10^{nb^{-1}}$.
- Heavy-flavour and quarkonia at very low $p_T$.
- Improve vertexing and tracking capabilities.

**Upgrade strategy (2019-2020 during LS2)**
- New high-resolution, low-material thickness ITS
- Upgrade of the TPC with Gas Electron Multipliers (GEM)
- Upgrade of the readout electronics of TRD, TOF, PHOS, and Muon spectrometer.
- Upgrade of the forward trigger detectors and trigger system for high-rate operations
- Upgrade of the Online and Offline Systems: HLT, DAQ, trigger system, software
ITS Upgrade: design objectives

**Limits**
- **SDD max readout speed:** 1 kHz
- **Material budget:** 1.1% $X_0$
- **Spatial resolution** for secondary vertex reconstruction (e.g. $\Lambda_c$ $c\tau \approx 60 \mu m$)

**Design objectives: present vs new ITS**
- **Readout rate:** 1 kHz $\rightarrow$ up to 400 kHz (pp), 50 kHz (Pb-Pb)
- **Improve impact parameter resolution** by a factor $\sim 5$ in $z$ and $\sim 3$ in $r\varphi$ at $p_T = 500 MeV/c$
  - **Material budget:** $1.1\% X_0 \rightarrow 0.3\% X_0$ (inner layers)
  - **Pixel size:** $50x425 \mu m^2 \rightarrow \sim 30x30 \mu m^2$
  - **Closer to the vertex** (first layer radius): $39 \text{ mm} \rightarrow 22 \text{ mm}$
- **Improve tracking efficiency and $p_T$ resolution** at low $p_T$:
  - **Increase granularity:** 6 layers $\rightarrow$ 7 layers
New ITS layout

7 layers of Monolithic Active Pixel Sensors (MAPS)
- 3 Inner Layers (Inner Barrel)
- 2 Middle + 2 Outer layers (Outer Barrel)

Total area: \( \sim 10 \, m^2 \)
\(|\eta|\) coverage: \(|\eta| < 1.22\)
\(r\) coverage: 22 – 400 mm
ALPIDE chip

− TowerJazz 0.18 μm CMOS imaging process
  − High resistivity \((1 \div 6 \text{ kΩ} \cdot \text{cm})\) p-type epitaxial layer (25 μm) on p-type substrate.
  − Small n-well diode (2 μm diameter), ~100 times smaller than pixel \(\rightarrow\) small capacitance (\(~fF\))
  − Reverse bias voltage to substrate: \(-6V < V_{\text{BB}} < 0V\)
  − Deep PWELL shields NWELL of PMOS transistor (full CMOS circuitry within active area)
  − Fast (~2μs) data driven encoder for pixel matrix readout
  − Pixel signal amplified and digitized at a pixel level \(\rightarrow\) low power consumption (< 40 mW/cm²)
  − Data sent towards periphery to the Data Transmission Unit (Serializer + PLL + LVDS driver)
ALPIDE chip

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- 400 Mb/s (OB), 1.2 Gb/s (IB) data output
- Triggered or continuous acquisition
- 50 μm (IB), 100 μm (OB) thick

Pixel size | \(~27\times29 \mu\text{m}^2\)
---|---
Matrix size | 512x1024 pixels

Cern-INFN-China collaboration
Inner barrel – first 3 layers

Inner barrel Hybrid Integrated Circuit (HIC)

- 9 ALPIDE chips
- 1 Flex circuit for data, clock, control signal transmission and chip powering
- Chip – Flex connection with wire bonds
- Good performance after 1 year operation (aging test)

Chip threshold correlation: After vs before aging test
Inner barrel – first 3 layers

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  - 9 ALPIDE chips
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- **Inner barrel stave**
  - One HIC is glued on the space frame incorporating a cold plate for chip cooling (water cooling)
  - Three cylindrical layers
  - 48 Staves in total
Inner barrel – first 3 layers

- **Half-Layer 0**
- **Half-Layer 1**
- **Half-Layer 2**
- **Cooling pipes**
- **Sensitive area**
- **Third half-layer from the beam pipe**
- **~38 mm**
- **17 cm**

**Inner barrel HIC**
- **9 ALPIDE chips**
- **1 Flex circuit for data, clock, control signal transmission and chip powering**
- **Chip–Flex connection with wire bonds**

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**A Large Ion Collider Experiment**

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Outer Barrel – HIC assembly

- **Outer barrel HIC**
  - 14 (7x2) ALPIDE chips
  - 1 Flex circuit for data, clock, control signal transmission and chip powering
  - **Master-slave** architecture
  - Chip – Flex connection with glue + wire bonds (line connections, ~70 pads per chip)

- Bari
- Pusan/Inha
- Wuhan
- Strasbourg
- Liverpool
Outer Barrel – Half-Stave/Stave assembly

Outer barrel Half-Stave (HS)
- OL-HS: 7 HICs, ML-HS: 4 HICs.
- HICs are aligned and glued onto a Cold Plate with 10-20 µm precision
- 98 (OL), 56 (ML) ALPIDE chips on HSs
- \(\sim 5.1 \times 10^7\) 30x30 µm\(^2\) pixels on 1 OL-HS

- LBNL, Berkeley
- INFN, Torino
- LNF, Frascati
- STFC, Daresbury
- Nikhef, Amsterdam

HIC alignment station

OL

ML

Cross-cables

150 cm

80 cm

LBNL, Berkeley
INFN, Torino
LNF, Frascati
STFC, Daresbury
Nikhef, Amsterdam
Outer Barrel – Half-Stave/Stave assembly

➤ Outer barrel Stave (90 OL + 54 ML)
  - 2 HSs aligned and glued onto a carbon fiber Space Frame (support structure) with about 100 µm precision
  - Soldering of Power-Bus to cross-cables for chip powering
  - Flipping of the Power Bus

➤ LBNL, Berkeley
➤ INFN, Torino
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  - Flipping of the Power Bus
  - Electrical test

Example for HS-3-Upper in Torino
- Average noise is uniform for chips on the same and different HICs
- Same conclusion for the average threshold

- LBNL, Berkeley
- INFN, Torino
- LNF, Frascati
- STFC, Daresbury
- Nikhef, Amsterdam
New ITS simulated physics performances
(examples)
Heavy-flavour: B mesons

Access to beauty at low $p_T$ will be achieved via:

- **Inclusive channels**: displaced $J/\psi$ and D mesons, muons/electrons from B semi-leptonic decays

- **Exclusive channels**
  - $B \rightarrow D^0 + X$ (BR $\approx 60\%$) $\rightarrow$ reconstruction down to $p_T = 0$
  - $B^\pm \rightarrow J/\psi(\rightarrow ee) + K^\pm$ (BR $\approx 0.1\%$) $\rightarrow$ reconstruction down to $p_T = 0$
  - $B^+ \rightarrow \bar{D}^0 + \pi^+$ (BR $\approx 0.48\%$) with $\bar{D}^0 \rightarrow K^+\pi^-$ (BR $\approx 3.88\%$) $\rightarrow$ full kinematic reconstruction down to $p_T = 2 - 3$ GeV/$c$

**Not measured with present setup!**
Conclusions

- 7 layers of the new ITS will be equipped with monolithic pixels (~ 30x30 µm² each)
- ALPIDE showed an efficiency > 99 % even after 10X lifetime Non-Ionizing Energy Loss (NIEL) dose
- Inner Barrel
  - 3 half-layers assembled
- Outer Barrel
  - Mechanical tools developed and fully working for 5 sites
  - Stave production is proceeding within the schedule (end: April 2019)
  - Stave tests are showing a good performance of the HICs
- All activities are registered in a database with results and, functional and physical statuses of the components
- Heavy-quark baryons and mesons (Λ_c, Λ_b, B) will become measurable with the new setup
Backup slides
## Pixel-chip requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Inner Barrel</th>
<th>Outer Barrel</th>
<th>ALPIDE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon thickness</td>
<td>50 $\mu m$</td>
<td>100 $\mu m$</td>
<td></td>
</tr>
<tr>
<td>Spatial resolution</td>
<td>5 $\mu m$</td>
<td>10 $\mu m$</td>
<td>$\sim 5 \mu m$</td>
</tr>
<tr>
<td>Chip dimension</td>
<td>$15 \times 30 \text{mm}^2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power density</td>
<td>$&lt; 300 \text{mW/cm}^2$</td>
<td>$&lt; 100 \text{mW/cm}^2$</td>
<td>$&lt; 40 \text{mW/cm}^2$</td>
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<tr>
<td>Event-time resolution</td>
<td>$&lt; 30 \mu s$</td>
<td></td>
<td>$\sim 2 \mu s$</td>
</tr>
<tr>
<td>Detection efficiency</td>
<td>$&gt; 99%$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fake-hit rate$^a$</td>
<td>$&lt; 10^{-6}$ /event/pixel</td>
<td></td>
<td>$&lt;&lt;&lt; 10^{-6}$ /event/pixel</td>
</tr>
<tr>
<td>NIEL radiation tolerance$^b$</td>
<td>$1.7 \times 10^{13}$ $\text{1MeV n}_{eq}/\text{cm}^2$</td>
<td>$10^{12}$ $\text{1MeV n}_{eq}/\text{cm}^2$</td>
<td></td>
</tr>
<tr>
<td>TID radiation tolerance$^b$</td>
<td>2.7 Mrad</td>
<td>100 krad</td>
<td>Tested at 350 krad</td>
</tr>
</tbody>
</table>

$^a$ number revised w.r.t TDR

$^b$ with a safety factor of 10 (load integrated over the approved program = 6 years of operation), number revised w.r.t TDR
From prototype to final ALPIDE

May 2014
pALPIDE-1
• Full-scale prototype (512x1024 pixels)
• 4 sectors with different pixel geometries/characteristics
• No final interface

May 2015
pALPIDE-2
• 4 sectors with different pixel geometries/characteristics
• Final interface: allows integration into ITS modules
• No high-speed output link (1.2 Gbit/sec replaced by 40 Mbit/s)

Oct 2015
pALPIDE-3
• 8 sectors with different pixel geometries/characteristics
• Final interface including 1.2 Gbit/s high-speed output

Aug 2016
ALPIDE
• Final chip version. Full matrix with same pixel type (pALPIDE-3 sector 5)
• High-speed serial output: 400Mb/s (OB) – 600Mb/s or 1.2Gb/s (IB)
• Pixel pitch: ~29 x 27 𝜇m²
• Ultra-low power consumption (<40 mW/cm²)
• Triggered or continuous acquisition

Block diagram of the ALPIDE pixel cell
ALPIDE test beam results

- **NIEL and TID effects on efficiency and fake-hit rate @Cern PS**
  - Fake-hit rate $< 10^{-10}$/pixel/event after masking 10 pixels
  - Efficiency close to 100% on a wide range of thresholds

- **NIEL and TID effects on resolution and cluster size @Cern PS**
  - Good resolution also after irradiation: $\sim 5 - 6 \, \mu m$ (for MIPs)
  - Average cluster size: $\sim 1 - 3$ pixels (using centre-of-gravity)

Performance fully satisfies the constraints on the pixel chip even after TID and NIEL irradiation!
Inner and Outer Barrel Staves

- 3 Inner Layers (Inner Barrel)
- 2 Middle + 2 Outer layers (Outer Barrel)

Half-Stave to Half-Stave:
\[ i = 1744 \, \mu m \]
\[ o = 834 \, \mu m \]

Stave to stave:
\[ i = 1906 \, \mu m \]
\[ o = 1264 \, \mu m \]
OB Module & FPC: data, clock and control lines

- Two independent rows of 7 chips: 1 master and 6 slave per row
- Data (@400 Mb/s) are sent out only from the master (master-slave internal communication)
- 40 MHz clock arrives at the master and it is regenerated and sent to the slaves
- Control line is bidirectional and serves to:
  - provide write and read access to internal registers, commands, configuration and memories
  - distribute trigger commands or other broadcast synchronous signals

Data, Control and Clock lines are routed on the FPC (Cu lines 18 μm thick) that is wire-bonded to chip pads
IB Module & FPC: data, clock and control lines

- One rows of 9 chips: all masters
- Data (@1.2 Gb/s) are sent out from each master
- 40 MHz clock arrives at all the masters
- Control line is bidirectional and all masters share it.

→ Data, Control and Clock lines are routed on the FPC (Al lines 25 μm thick) that is wire-bonded to chip pads.
Readout electronics

1 Readout Unit per Stave

Inner layers
1.2 Gb/s data
40 MHz clock

Outer layers (3,4,5,6)
400 Mb/s data
40 MHz clock

Central Trigger Processor

One way, passive optical splitting, no busy back

GBT optical

Identical Readout Units (RU) cover the full ITS

Common Readout Unit & O2

× 192

Rad levels
TID: 1 Mrad
Fluency: $\sim 10^{13} \ M_{eV} n_{eq}/cm^2$

Rad levels
TID: <10 krad
Fluency: $< 10^{12} \ M_{eV} n_{eq}/cm^2$

Position of the RUs
330 cm from interaction point

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PID with pixel cluster shapes

- **Present ITS**: PID is performed via dE/dx in the four outermost layers (SDD + SSD)
- **New ITS**: digital readout adopted → Tagging of heavily ionizing particles (e.g. $^3He$ and $^4He$) thanks to the analysis of the cluster sizes/shapes associated to their track:
  - Study performed assuming $20 \times 20 \mu m^2$ pixels with an effective thickness of $18 \mu m$
  - PID algorithm: arithmetic mean of the cluster size values associated to the track
  - PID algorithm calibration: distribution of the mean cluster size values for each hadron specie in a given momentum interval → fit with a Gaussian function $(\mu, \sigma)$ → $\mu$ vs. momentum curve fitted with 2nd-degree polynomial function.

- $\mu$ and $\sigma$ for $^3He$ and $^4He$ are different from those of pions → light nuclei PID

- $\mu$ vs. $p$
  - Pions, protons and deuterons are not distinguishable
  - A cut of $2\sigma$ is sufficient to tag nuclei

### Graphs and Data

- PID efficiency for $^3He$ and $^4He$ vs. pion
- Mean cluster size distribution for different particle types
- $\mu$ vs. momentum curve for pions and hadrons

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A Large Ion Collider Experiment

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Hypernuclei: $^{3}_ΛH$, $^{4}_ΛH$, $^{4}_ΛHe$ via mesonic weak decays

- Nuclei that contain at least a strange baryon (hyperon) in addition to protons and neutrons: the hyperon-nucleon interaction plays a role in understanding the structure of neutron stars.

- **Present detector**: only allows the detection of $^{3}_ΛH$ and $^{3}_ΛH$ with poor significance. The detection of heavier (anti)-hypernuclei is precluded with the present statistics.

- **New ITS detector**
  - Very large statistics of minimum-bias Pb-Pb events will be collected after LS2.
  - Improved tracking resolution will allow a better separation of the reconstructed signal decays from the combinatorial background → significance improvement.
Heavy-flavour baryon: $\Lambda_c \rightarrow p K^- \pi^+$

- $ct \approx 60\mu m$ – $BR \approx 5\%$: challenging! High tracking precision needed to separate the secondary vertex.

- Present detector:
  - Not observed in Pb-Pb because of the very large combinatorial background

- New detector:
  - In Pb-Pb most-central collisions: $S/B$ improves by a factor 400 ($2 < p_T < 4$ GeV/$c$), significance improves by a factor 5-10 ($p_T > 2$ GeV/$c$)
  - Reconstruction of the $\Lambda_c$ down to $p_T = 2$ GeV/$c$