Simone Valdré

INFN – Sezione di Firenze

for the **FAZIA collaboration**

Time of flight identification with FAZIA

EuNPC 2018

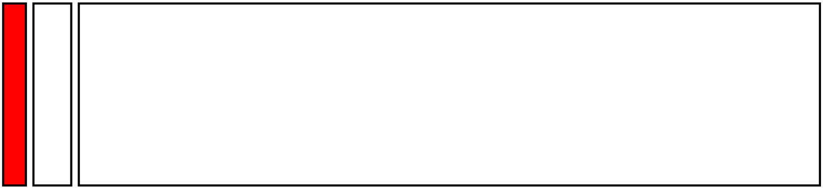
Bologna, September 2nd – 7th, 2018

The FAZIA telescope

The telescope stages

1. 300 μm reverse-mounted Si detector;
2. 500 μm reverse-mounted Si detector;
3. 10 cm CsI(Tl) cristal read by a photodiode.

To achieve the best possible energy resolution and A and Z identification Si detectors come from a nTD ingot cut at random angle to avoid channeling effects.



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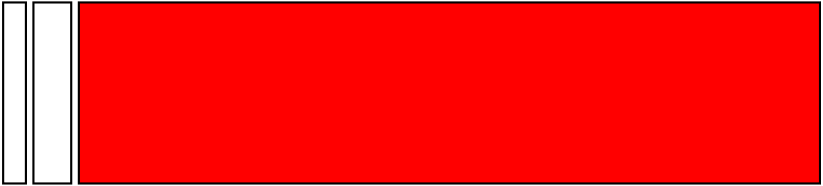
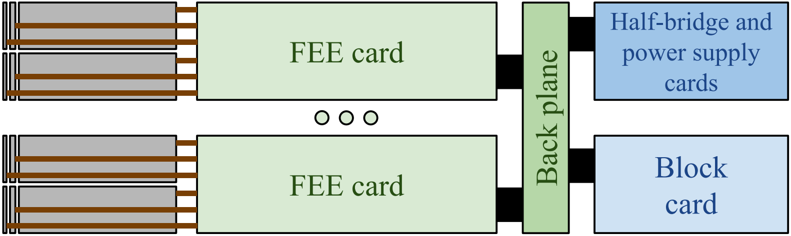


The FAZIA block

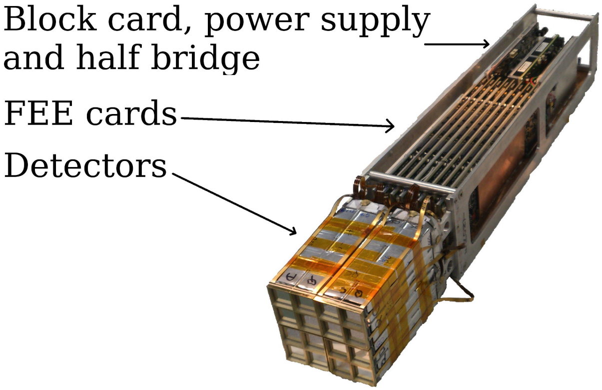
2 telescopes are connected to a FEE card.

The FAZIA block



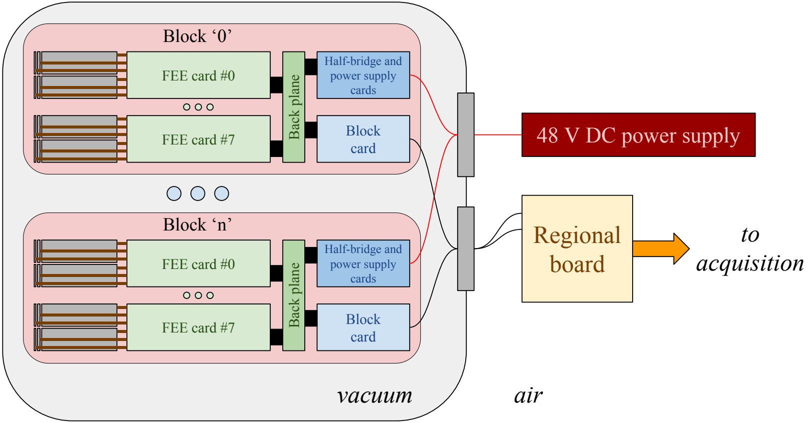
8 FEE cards are connected to a block card via a back plane.

The FAZIA block



Block is mounted on a copper base in which water flows to provide cooling

The FAZIA block



up to 36 block cards are connected to a regional board via a full duplex 3 Gb/s *optical link*

FAZIA electronics

Front-end

- Analogue chain: charge preamplifiers and anti-aliasing filters

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Pros and cons

- Compactness and modularity
- Very good isotopic discrimination capabilities
- High identification thresholds (2–10 MeV/u)

Identification methods

$\Delta E - E$ correlation

- exploits the Bethe-Bloch energy loss relation
- identification threshold due to first layer thickness

Pulse Shape Discrimination[a]

- charge collection depending on the impinging nuclei
- identification threshold corresponding to $\sim 50\,\mu\mathrm{m}$ penetration

[a] N. Le Neindre *et al*, Nucl. Instr. and Meth. A 701 (145), 2013

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Pulse Shape Discrimination[a]

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- identification threshold corresponding to $\sim 50\,\mu m$ penetration

$E - ToF$ correlation

- FAZIA implementation proposed here
- lowest identification threshold
- FURBO project

[a] N. Le Neindre *et al*, Nucl. Instr. and Meth. A 701 (145), 2013

FURBO project

FAZIA **U**pgrade for **R**adioactive **B**eam **O**peration

(INFN grant for new staff researchers)

FURBO project

FAZIA **U**pgrade for **R**adioactive **B**eam **O**peration
(INFN grant for new staff researchers)

Reduction of identification thresholds

- Funtamental task to measure in future ISOL facilities (SPES, Spiral2,. . .)
- Different possible solutions:
  - **time of flight** implementation (discussed here)
  - use of **thin** Si detectors as first stage
  - use of **alternative** detectors

Time of Flight measurement

Time of flight	ToF	$\equiv$	$t - t_0$
Flight base	d	$=$	$\lvert\vec{x}(t) - \vec{x}(t_0)\rvert$
Kinetic energy	E	$=$	$\frac{1}{2}m\left(\frac{d}{ToF}\right)^2$

A **start** time mark is needed to measure ToF

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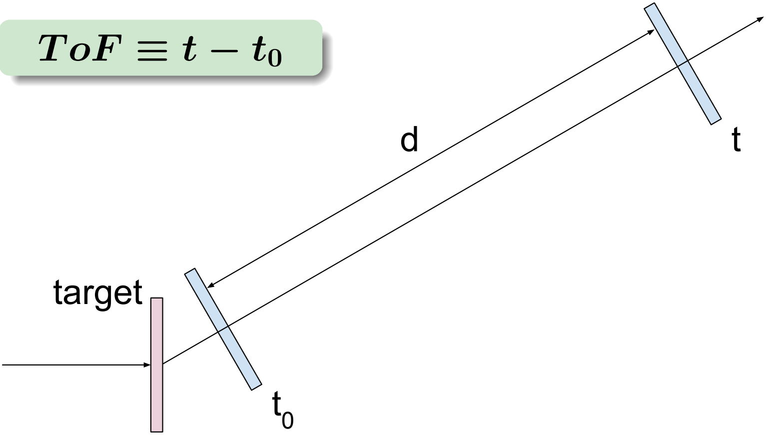
Time reference in FAZIA

- all acquired waveforms are referred to the **validation** time t_V
- applying a digital CFD algorithm to waveforms
  gives a time mark $t_{CFD} = t - t_V + t_{off}$
- t_V is **the same** for all detectors

A **start** time mark is needed to measure ToF

Time of flight in heavy-ion collisions

$$ToF \equiv t - t_0$$



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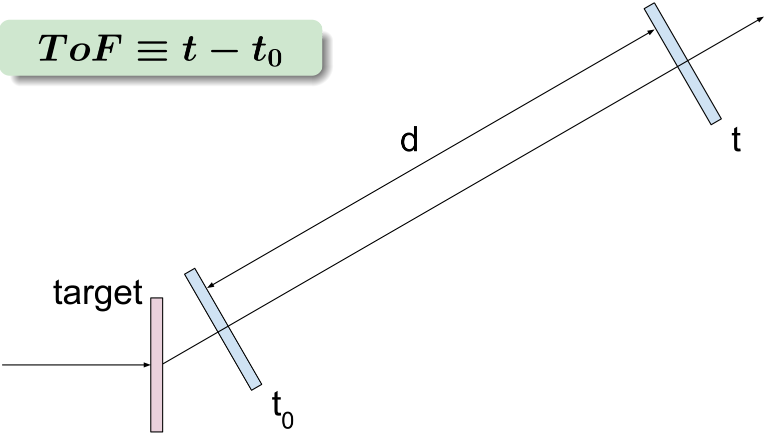

Start detector needed

Time of flight in heavy-ion collisions

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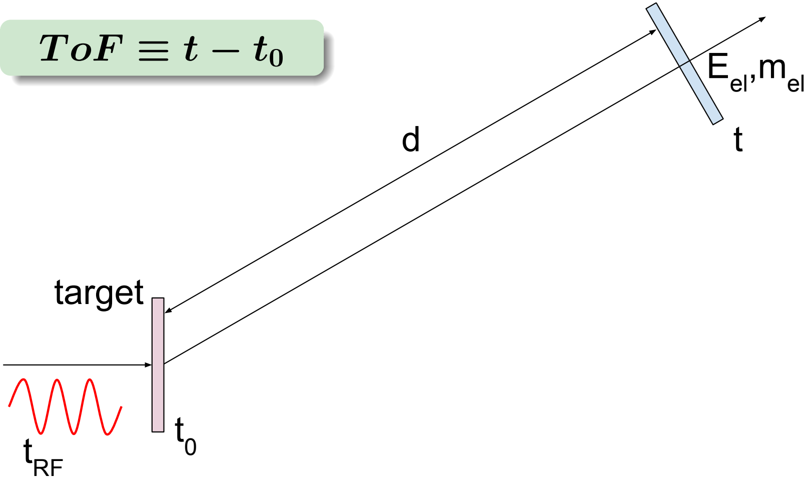


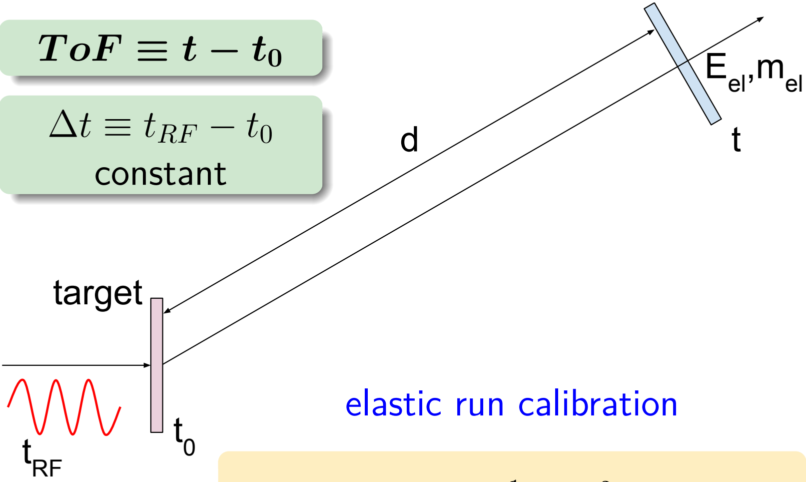
Start time mark from accelerator RF

Time of flight in heavy-ion collisions

$$\boldsymbol{ToF \equiv t - t_0}$$

$$\Delta t \equiv t_{RF} - t_0$$

constant



elastic run calibration

$$E_{el} = \frac{1}{2} m_{el} v_{el}^2$$

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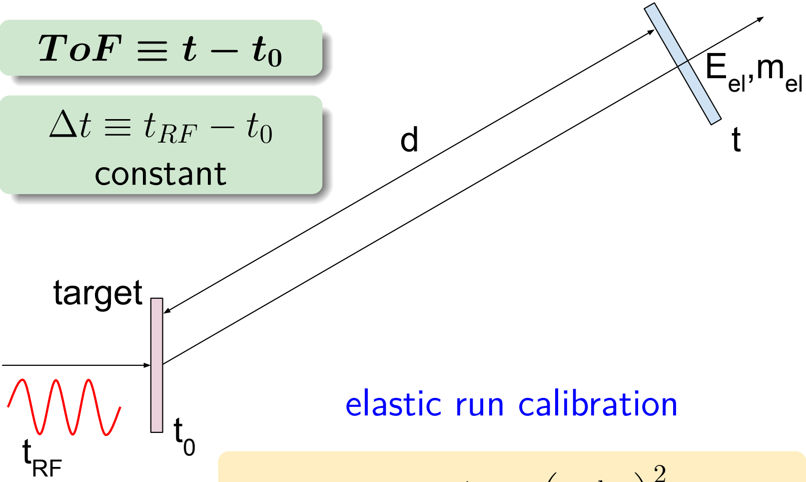

elastic run calibration

$$E_{el} = \frac{1}{2} m_{el} \left(\frac{d}{t_{el} - t_0} \right)^2$$

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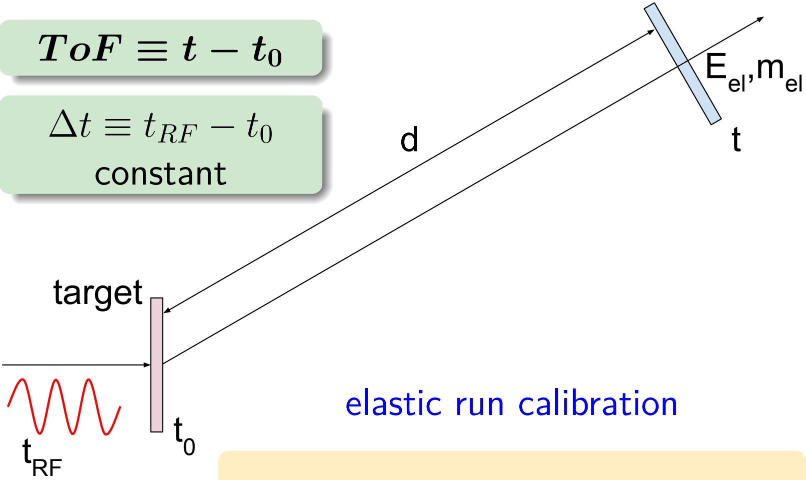

elastic run calibration

$$t_0 = t_{el} - d_{el}\sqrt{\frac{m_{el}}{2E_{el}}}$$

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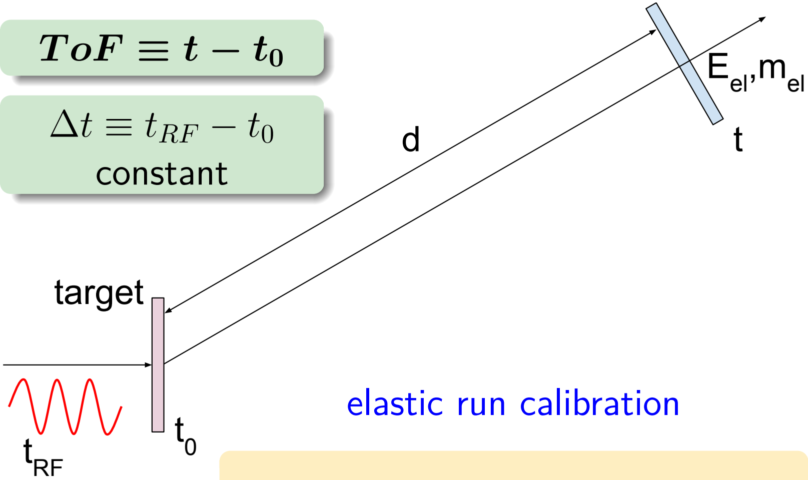

elastic run calibration

$$\Delta t = t_{RF} - t_{el} + d_{el}\sqrt{\frac{m_{el}}{2E_{el}}}$$

Time of flight in heavy-ion collisions

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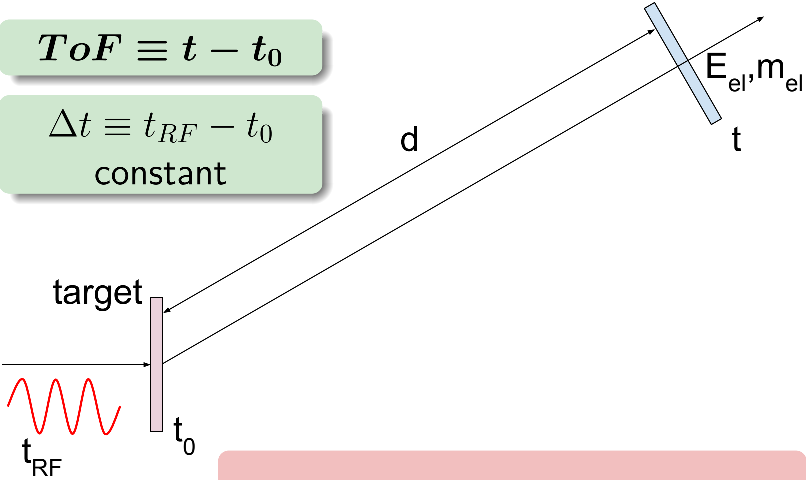

$$\boldsymbol{ToF = t - t_{RF} + \Delta t}$$

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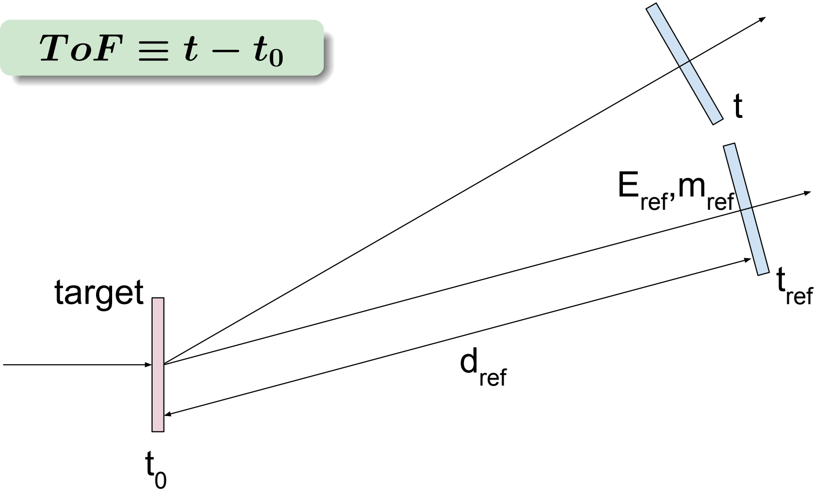
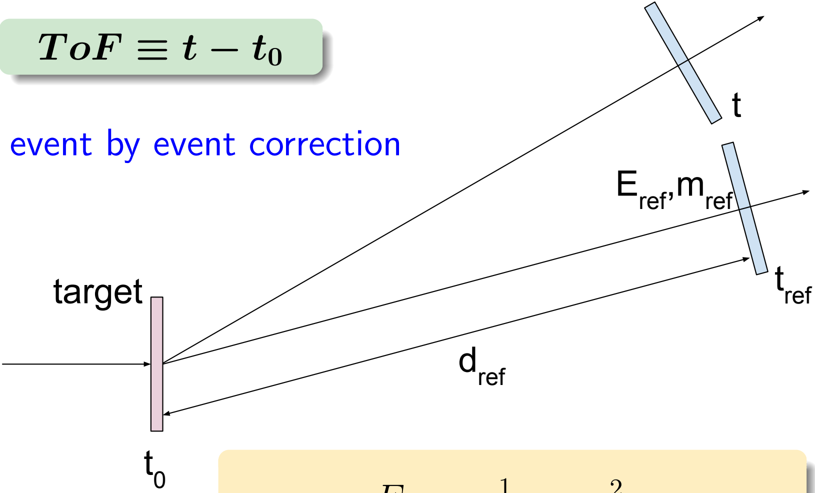


Proposed solution without a start detector or RF

Time of flight in heavy-ion collisions

$$ToF \equiv t - t_0$$

event by event correction



$$E_{ref} = \frac{1}{2} m_{ref} v_{ref}^2$$

Time of flight in heavy-ion collisions

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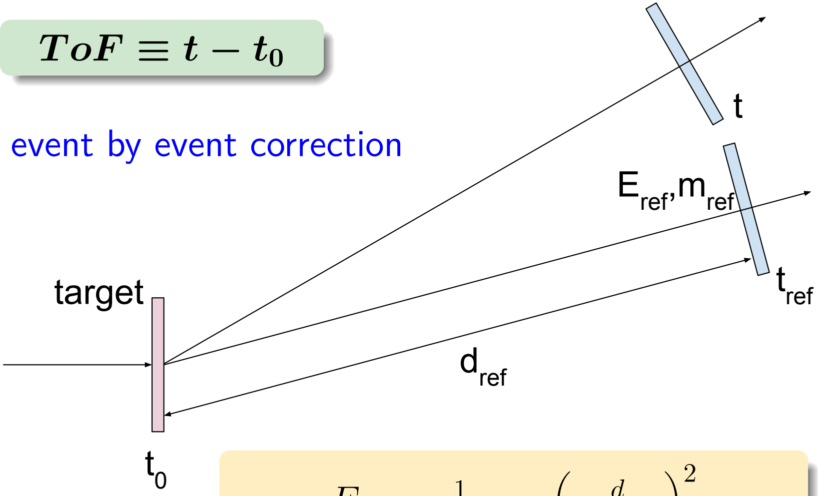

$$E_{ref} = \frac{1}{2} m_{ref} \left(\frac{d}{t_{ref} - t_0} \right)^2$$

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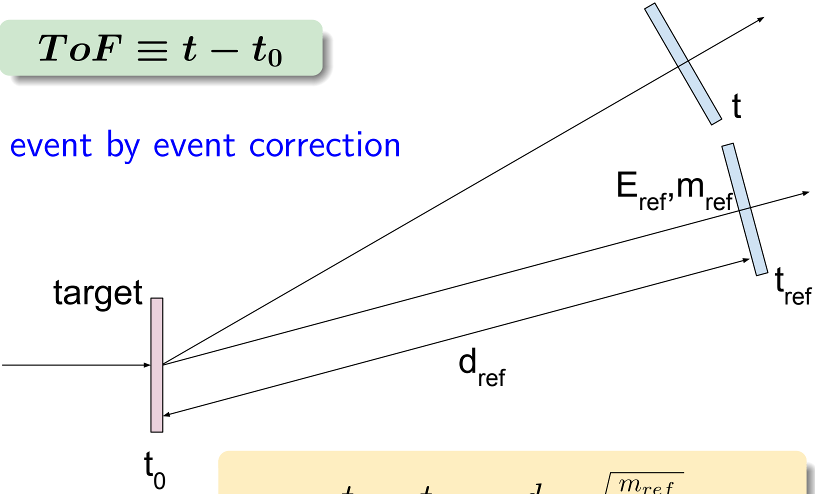

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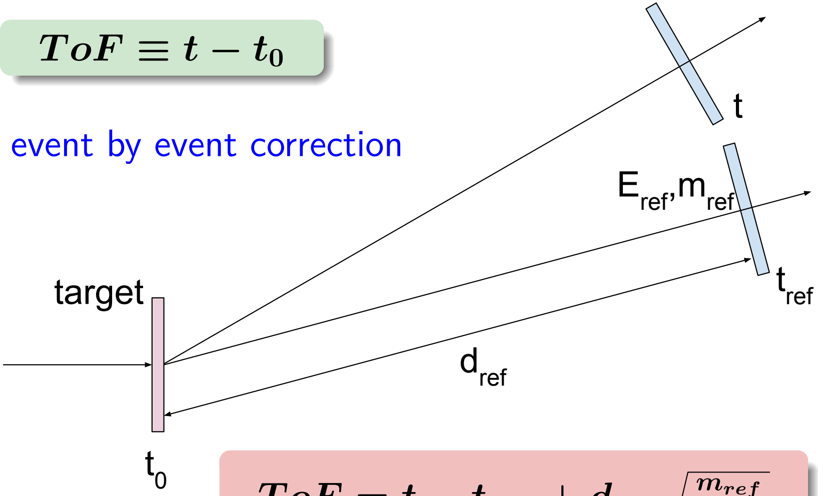

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Expected identification capabilities

^{12}C – ^{13}C discrimination

FAZIA flight base: 1 m

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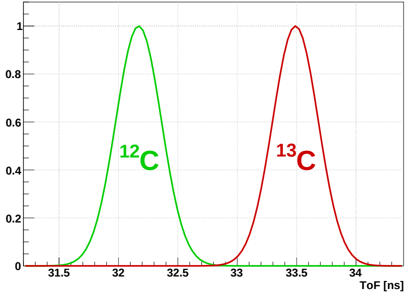
PSD mass discrimination:

60 MeV



$$\sigma_{ToF} = 0.19\,\text{ns}$$

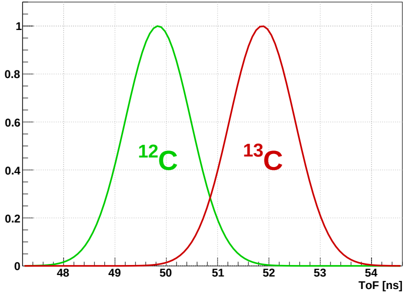
Expected identification capabilities

^{12}C – ^{13}C discrimination

FAZIA flight base: 1 m

PSD identification threshold:

25 MeV



$$\sigma_{ToF} = 0.64\,\mathrm{ns}$$

PSD mass discrimination:

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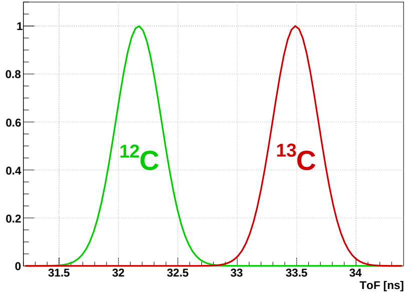

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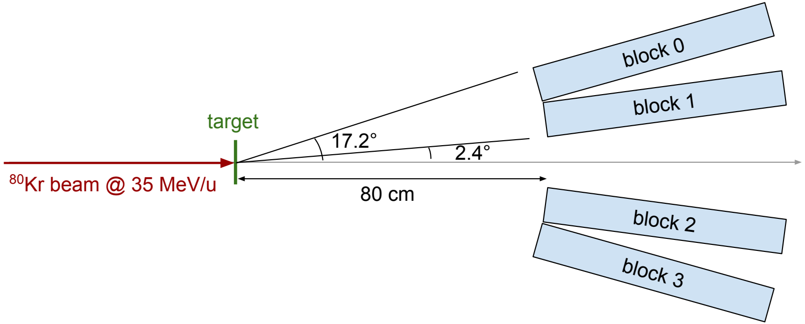
ISOFAZIA experiment at LNS



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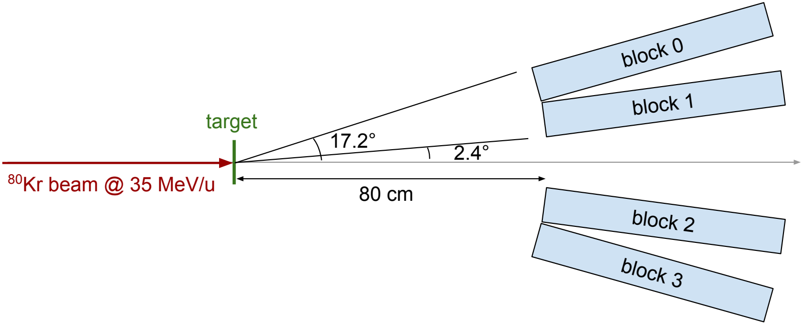

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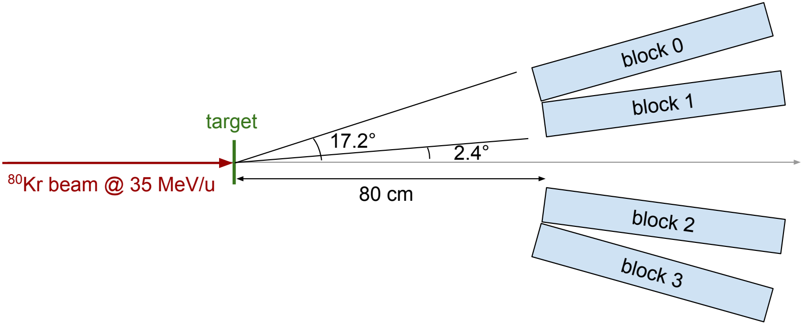

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- Fully calibrated with mass ID up to $Z \sim 24$

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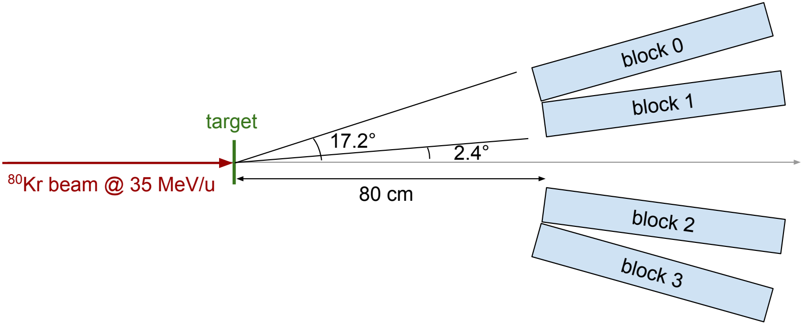

- First physics oriented experiment with FAZIA
- Fully calibrated with mass ID up to $Z \sim 24$
- In many events we have at least a fully identified particle which permits to recover t_0

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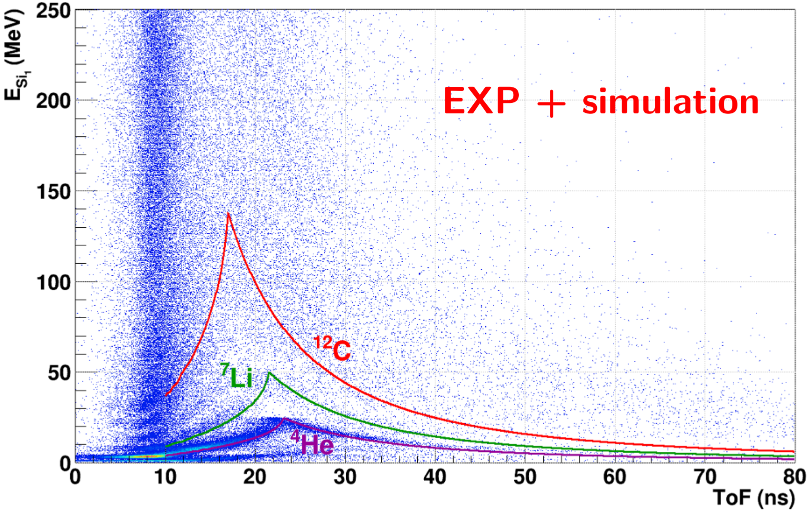

courtesy of A. Buccola, Università di Firenze

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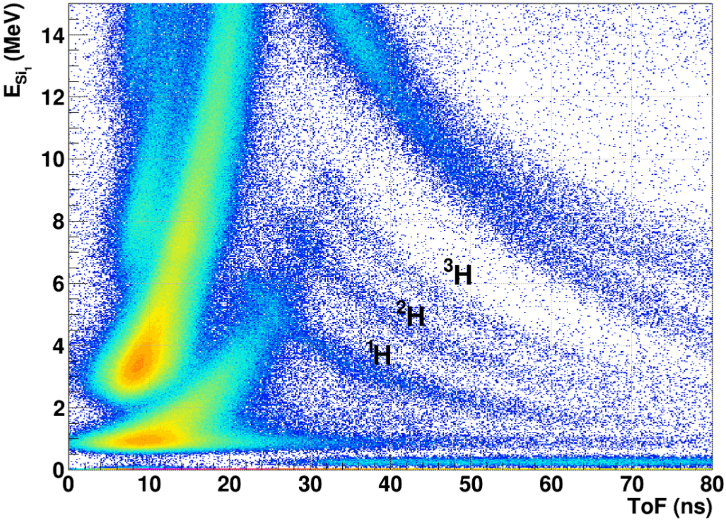

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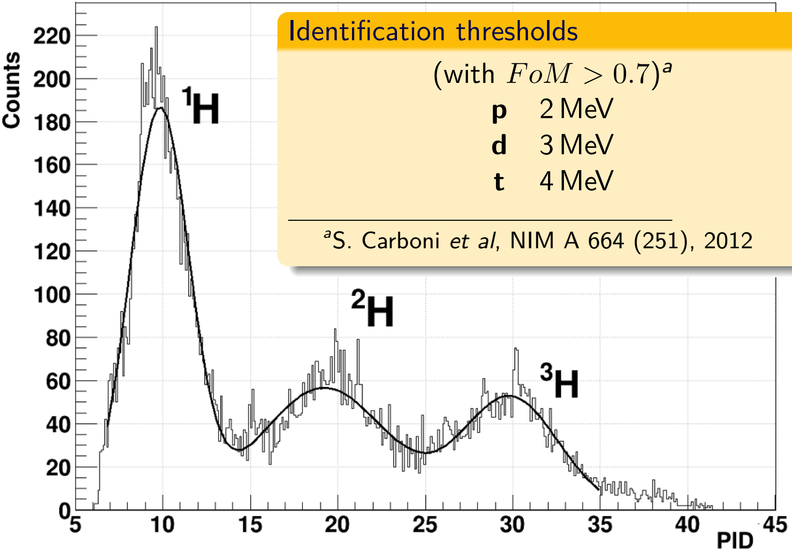

Identification thresholds

(with $FoM > 0.7$)[a]

p	2 MeV
d	3 MeV
t	4 MeV

[a] S. Carboni *et al*, NIM A 664 (251), 2012

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ISOFAZIA experiment at LNS

p,d,t stopped in the first Si layer

- PSD doesn't resolve $Z < 3$ isotopes
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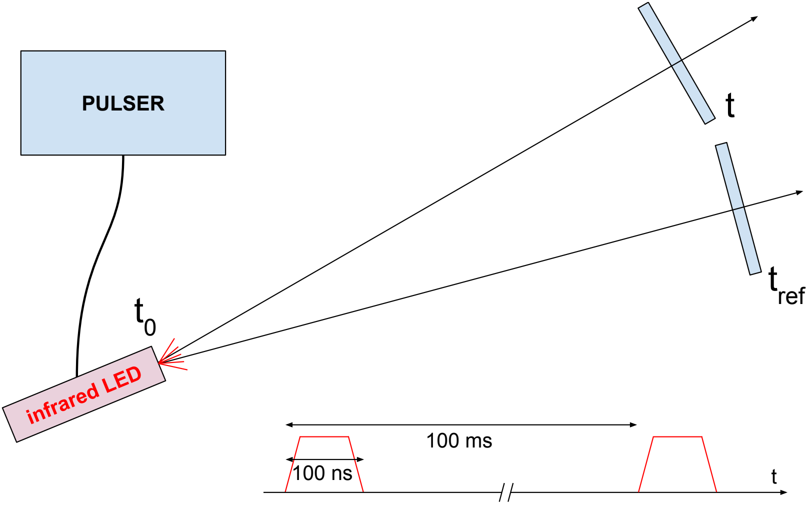
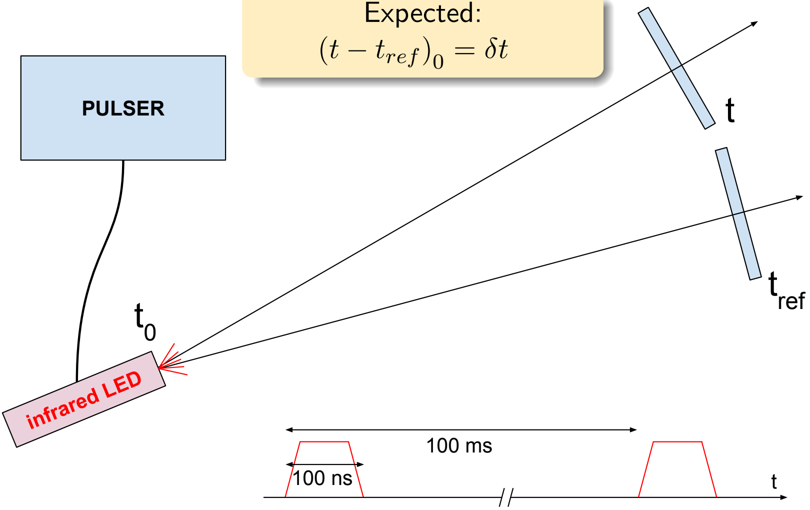
Illuminate all Si1 detectors with the same
fast infrared pulse

Timing accuracy test in Florence



Timing accuracy test in Florence

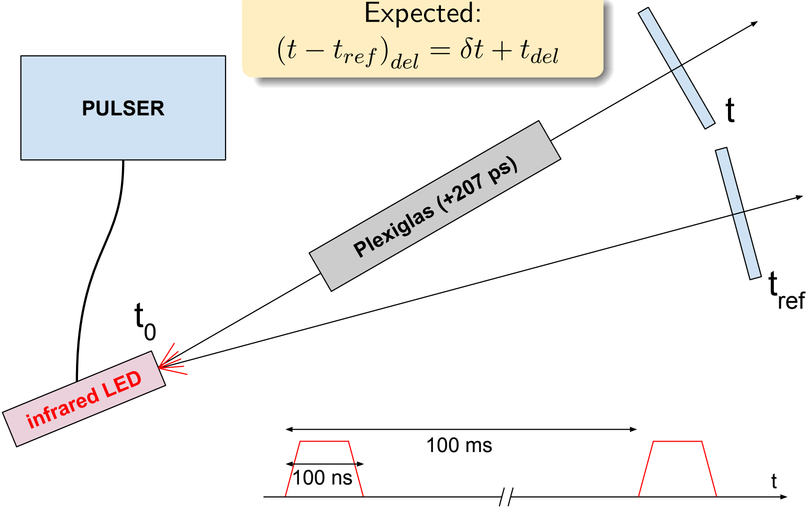
Expected:
$$(t - t_{ref})_0 = \delta t$$



Timing accuracy test in Florence

Expected:

$$(t - t_{ref})_{del} = \delta t + t_{del}$$



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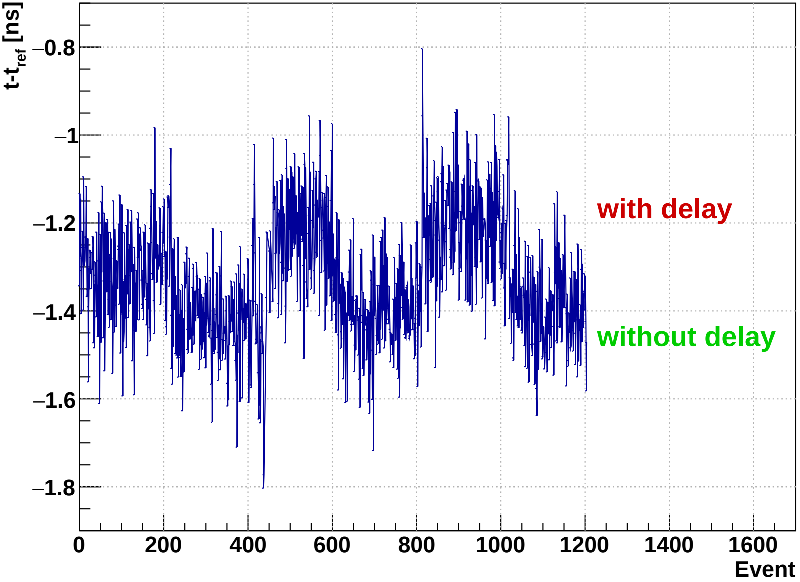

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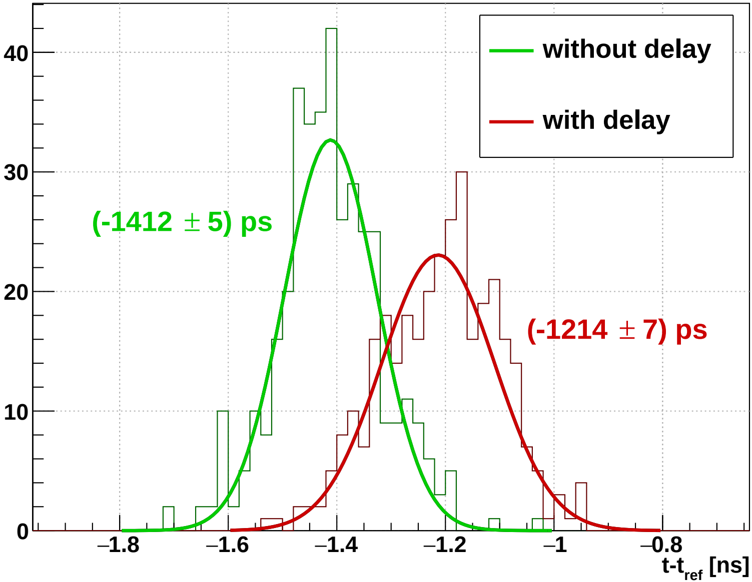

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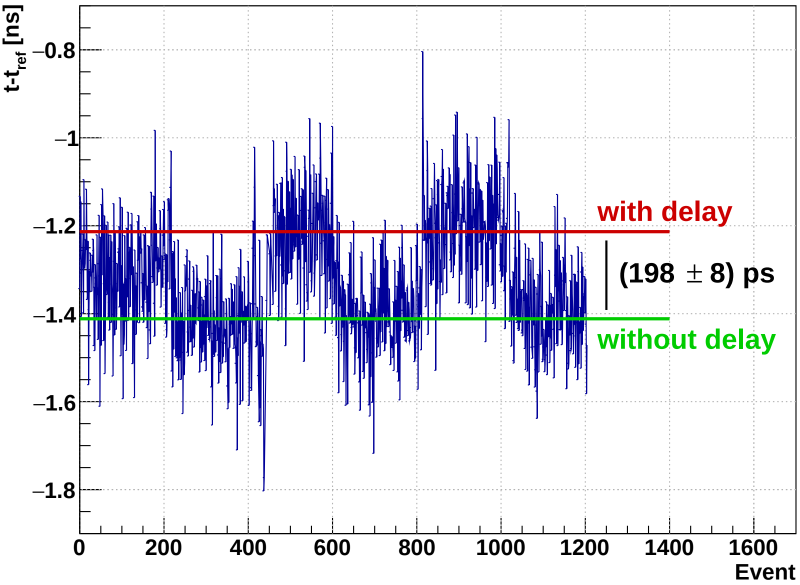

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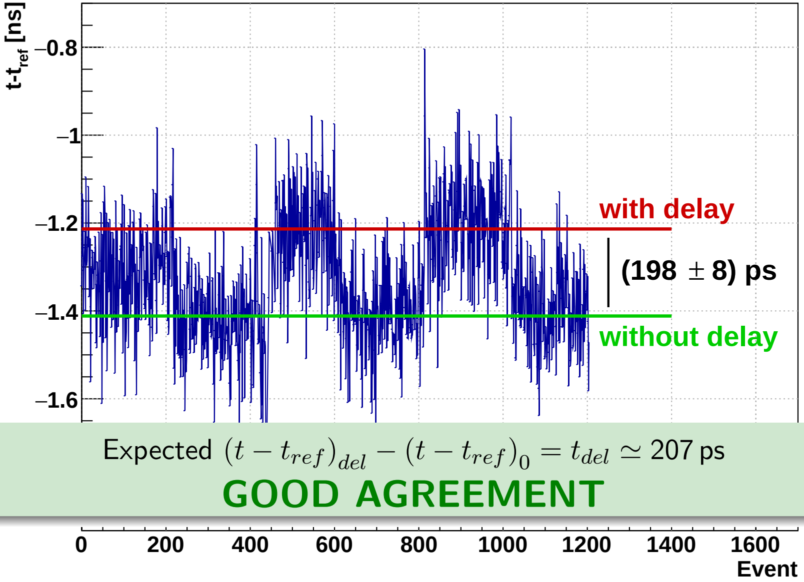

Expected $(t - t_{ref})_{del} - (t - t_{ref})_0 = t_{del} \simeq 207$ ps

GOOD AGREEMENT

FAZIAPRE experiment at LNS

Timing test

The same timing test performed on the test bench was repeated during the mounting of FAZIAPRE experiment at LNS giving a measured delay of (203 ± 13) ps *(added delay was nominally* 207 ps*)*

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During the FAZIAPRE experiment, the infrared LED was mounted inside the scattering chamber and was kept on during all the shift (at a 0.1 Hz *rate) to trace channel delays*

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Calibration and identification still in progress. . .

Summary and conclusions

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  - common clock doesn't guarantee a perfect synchronization
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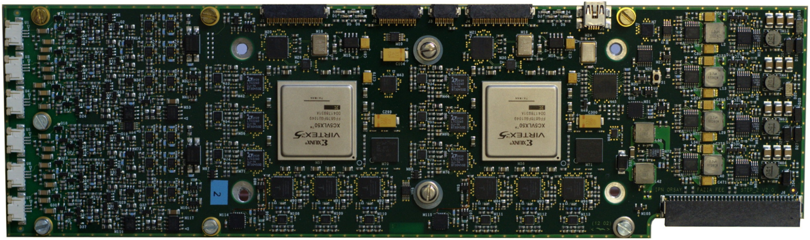
  - expected precision on time measurements: ∼500 ps after delay corrections
- LED pulses tested during FAZIAPRE experiment
  - we need particle identification and calibration to produce $E - ToF$ correlations (work in progress. . .)

FAZIA collaboration

Thanks for your attention

Backup slides

Front-end electronics



FEE card

- Designed at IPN, Orsay[a]
- 2 FAZIA telescopes per card
- Programmable logic performs on-line analysis of sampled data
  - VHDL code has been mainly written by P. Edelbruck
- FEE supplies also the bias voltages of Si detectors

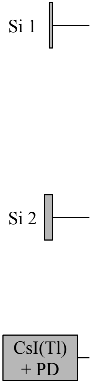
[a] F. Salomon *et al*, J. Instrum. 11 (C01064), 2016

Front-end electronics

Detector connectors

- Detectors are connected using kapton cables
- Silicon side kapton connection:
  - **ultra-sonic μbonding**
  - **conductive glue**

Front-end electronics



Front-end electronics

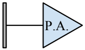
Analog chain (for each telescope)

- 3 fixed gain charge pre-amplifiers
- High range signals are **attenuated** by a factor 4
- Low range signals are **amplified** by a factor 4
- Current signal by **analog differentiation** of charge signals

Front-end electronics

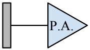
analog chains

Si 1

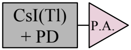


8 V, 4 GeV range

Si 2

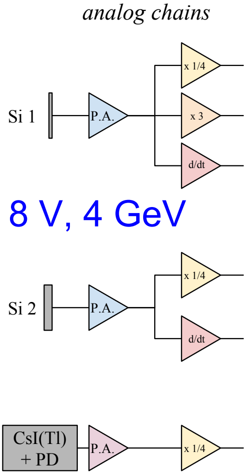


8 V, 4 GeV range



8 V, 300 MeV Si-equivalent range

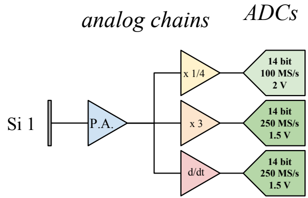
Front-end electronics



8 V, 4 GeV

8 V, 300 MeV

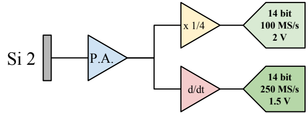
Front-end electronics



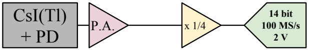
4 GeV full-scale

250 MeV full-scale

8 V, 4 GeV



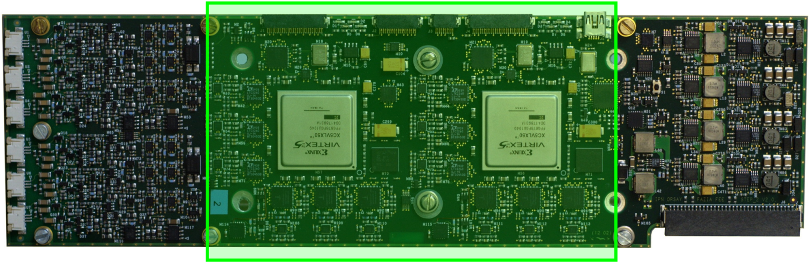
4 GeV full-scale



300 MeV Si-equivalent full-scale

8 V, 300 MeV

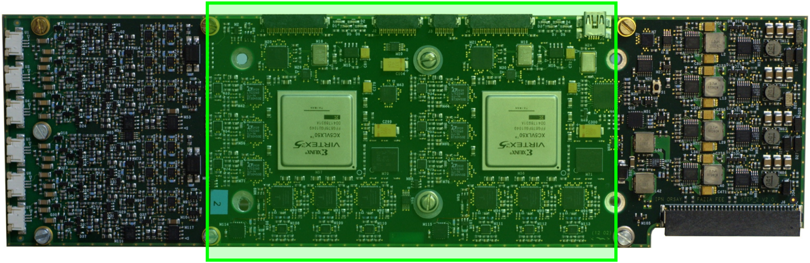
Front-end electronics



6 sampling ADCs per telescope

Si 1	14 bit, 100 MHz	4 GeV full-scale charge signal	**QH1**
	14 bit, 250 MHz	250 MeV full-scale charge signal	**QL1**
	14 bit, 250 MHz	current signal	**I1**
Si 2	14 bit, 100 MHz	4 GeV full-scale charge signal	**Q2**
	14 bit, 250 MHz	current signal	**I2**
CsI(Tl)	14 bit, 100 MHz	300 MeV Si-eq. f.s. charge signal	**Q3**

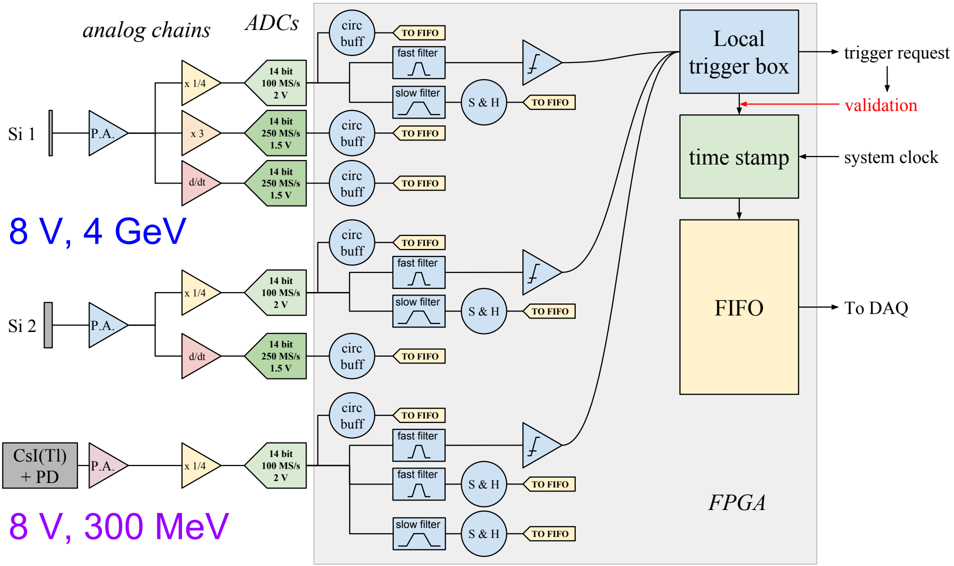
Front-end electronics



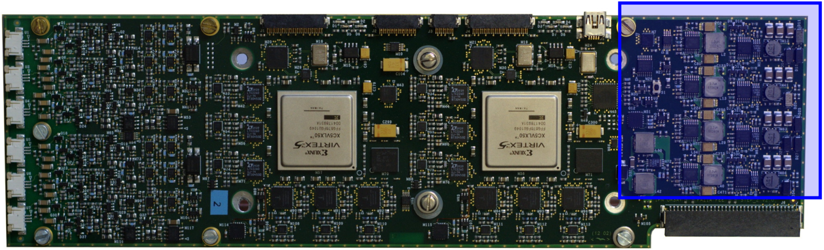
Xilinx Virtex-5 FPGAs

- Each FPGA processes signals from one telescope
  - signals stored in **FIFO memories** (up to **8192 samples**)
- On-board **real-time** trapezoidal shaping
  - fast shaped signals to leading-edge discriminators
  - maximum of slow shaped signals to acquisition
  - no pole-zero correction

Front-end electronics



Front-end electronics



HV generation

- DC/DC converters produce the Si detectors **bias voltages**:
  - 0–300 V for Si1 (140 V depletion voltage)
  - 0–400 V for Si2 (290 V depletion voltage)
- CsI(Tl) photodiode bias voltage from the Power Supply card:
  - **optocoupler switch** on FEE card.

Front-end electronics

Back plane connector

- Power supply and CsI(TI) HV from power supply card
- Equalized 25 MHz **clock distribution** between FEE cards
- Star connection between FEE cards and block card:
  - FEE to BC: 2x400 Mb/s links (⇒ **800 Mb/s**)
  - BC to FEE: 1x400 Mb/s link
- Slow control communication

Block Card

Block card

- Designed at INFN – Napoli
- Takes data from FEE cards via the back plane and builds up part of the event record
- Features a **3 Gb/s** optical link to regional board
  - 16-bit 8b/10b GTX transceiver
- **Fixed latency** transmission[a]:
  - all ADC clocks have the same phase ($\sim$ 20 ps skew)
  - digitized signals don't have the 1 clock indetermination typical of asynchronous systems
- 25 MHz from fibre-recovered clock
  - PLL for **jitter cleaning**

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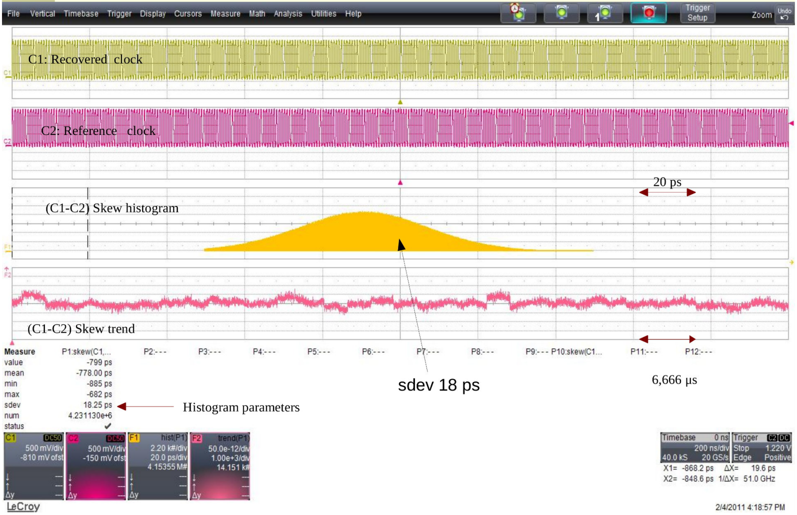
[a] R. Giordano *et al*, IEEE Trans. on Nucl. Science 58 (194), 2011

Block Card

Fixed Latency test results



courtesy of A. Boiano, INFN – Napoli

Half bridge and power supply

Half Bridge

- Designed at INFN – Napoli
- **High power** voltage conversion from 48 V DC input:
  - 22 V (14 A) DC
  - 5.5 V (70 A) DC

Power Supply

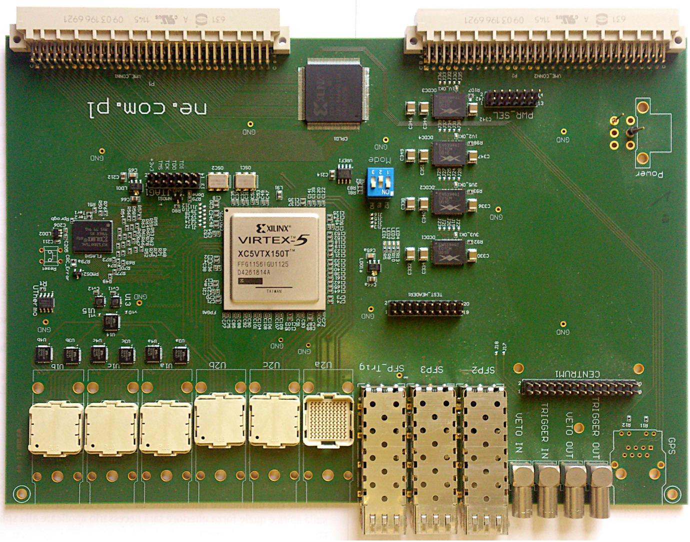
- Designed at INFN – Napoli
- Converts 22 V to 13 V, -9 V, ± 5 V and CsI(TI) HV
- PIC monitors produced voltages together with 5.5 V from HB
  - power on/power off
  - under/over voltage protection
  - voltage/current limits

Regional board

Regional Board

- Designed at Jagiellonian University, Krakow
- Features a Xilinx Virtex-5 FPGA
  - VHDL code has been written mainly at INFN – Napoli
- **36x** 3 Gb/s bi-directional optical links
  - to/from FAZIA blocks
  - fixed latency protocol
- 2x 1 Gb/s optical ethernet links (1000Base-SX)
  - now only 1 is used ⇒ room for transmission speed increase
  - **UDP protocol** for low-latency transfer
- Possibility to connect GANIL **CENTRUM** module

Regional board

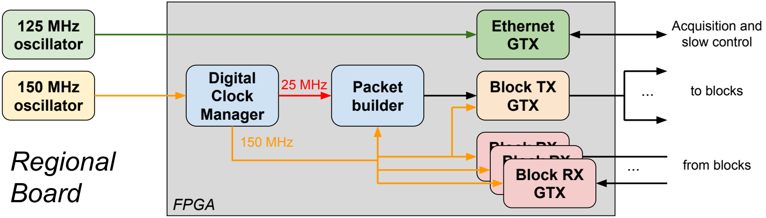


Regional board

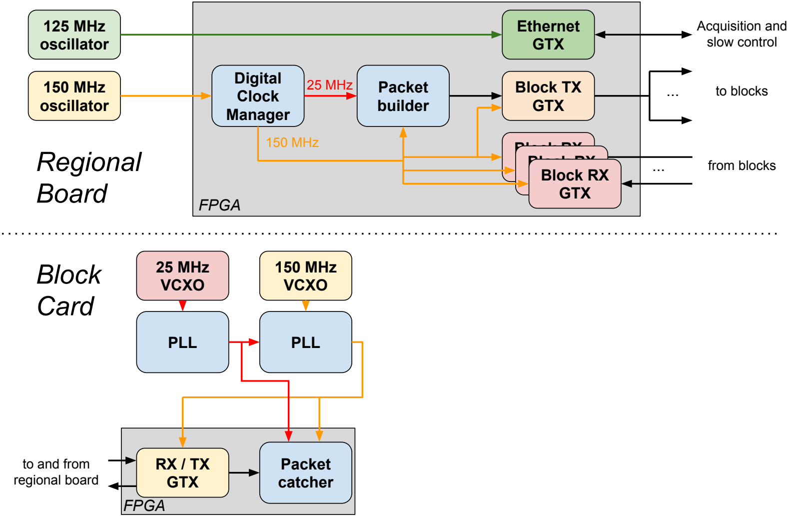
Regional Board tasks

- **Slow control** management of all the electronics
  - data transmission and slow control use the same optical fibre
- **Trigger board**:
  - multiple majority logic for trigger validation
  - trigger scaling by a settable factor
  - master/slave trigger operation (for coupling)
- **Event building** from data coming from all the blocks
  - it may add the CENTRUM timestamp to each event
- **Transmission** of acquired data to servers
  - maximum speed achieved: $\sim 80\,\mathrm{MB/s}$ ($\sim 640\,\mathrm{Mb/s}$)

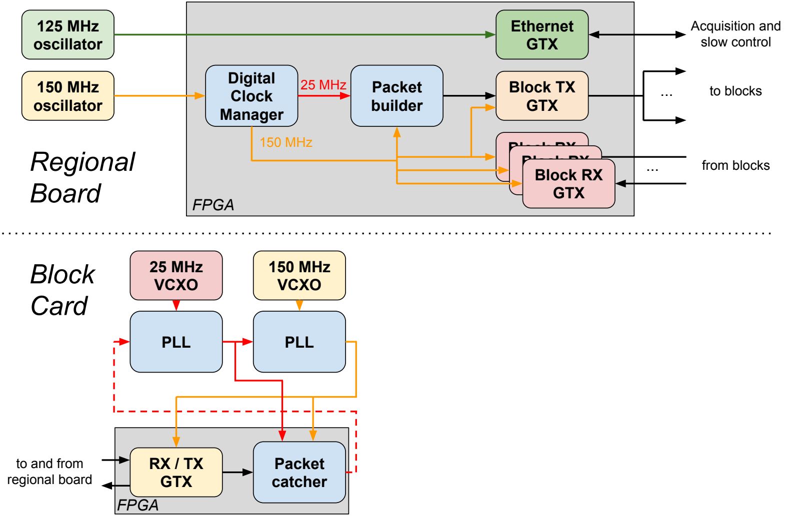
Clock tree


125 MHz oscillator
150 MHz oscillator
Regional Board
FPGA
Ethernet GTX
Digital Clock Manager
25 MHz
Packet builder
Block TX GTX
150 MHz
Block RX GTX
Acquisition and slow control
...
to blocks
...
from blocks

Clock tree


125 MHz oscillator
150 MHz oscillator
Ethernet GTX
Acquisition and slow control
Digital Clock Manager
25 MHz
Packet builder
Block TX GTX
...
to blocks
150 MHz
Block RX GTX
...
from blocks
Regional Board
FPGA
Block Card
25 MHz VCXO
150 MHz VCXO
PLL
PLL
to and from regional board
RX / TX GTX
Packet catcher
FPGA

Clock tree


125 MHz oscillator
150 MHz oscillator
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Packet builder
Ethernet GTX
Block TX GTX
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Acquisition and slow control
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Block Card
25 MHz VCXO
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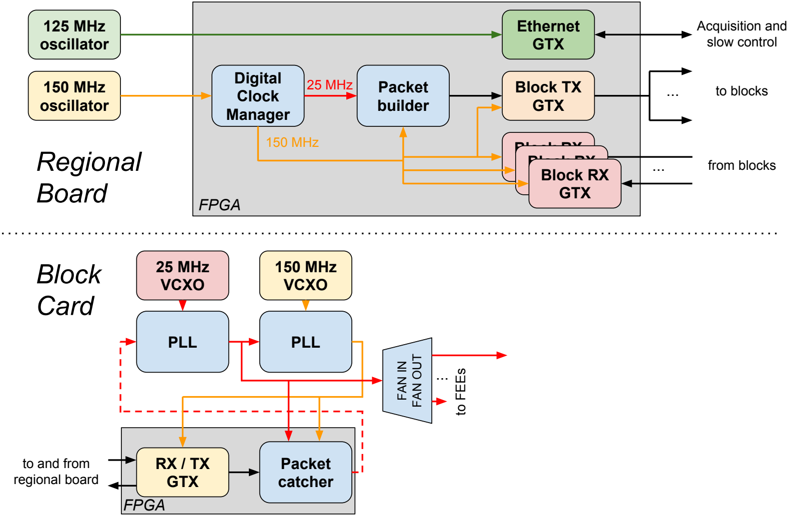
PLL
PLL
RX / TX GTX
Packet catcher
to and from regional board
FPGA

Clock tree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Acquisition and slow control
Digital Clock Manager
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Block TX GTX
...
to blocks
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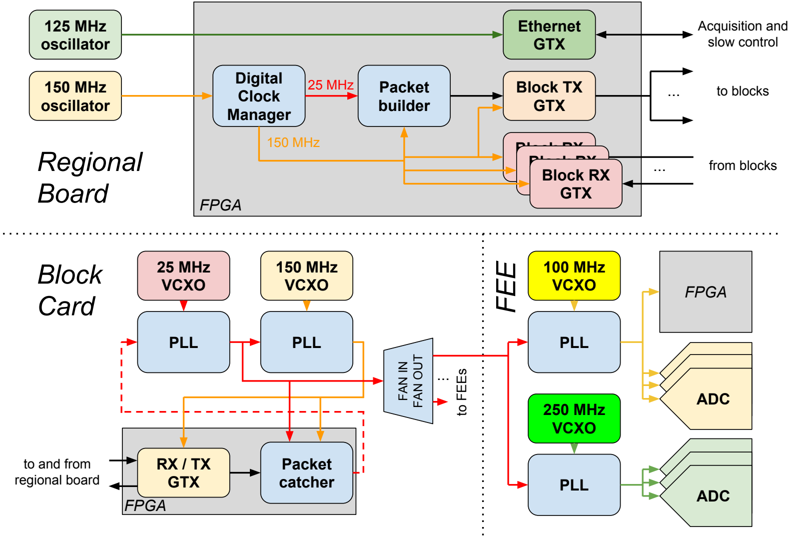
...
from blocks
Regional Board
FPGA
Block Card
25 MHz VCXO
150 MHz VCXO
PLL
PLL
FAN IN FAN OUT
...
to FEEs
to and from regional board
RX / TX GTX
Packet catcher
FPGA

Clock tree


125 MHz oscillator
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Ethernet GTX
Acquisition and slow control
Digital Clock Manager
25 MHz
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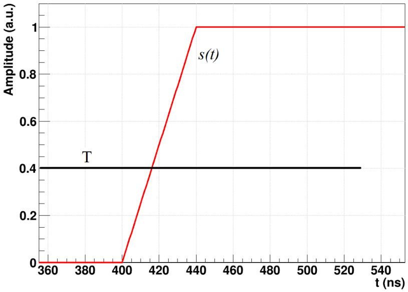
Block TX GTX
to blocks
150 MHz
Block RX GTX
from blocks
FPGA
Regional Board
Block Card
25 MHz VCXO
150 MHz VCXO
PLL
PLL
FAN IN FAN OUT
to FEEs
RX / TX GTX
Packet catcher
FPGA
to and from regional board
FEE
100 MHz VCXO
PLL
FPGA
ADC
250 MHz VCXO
PLL
ADC

Time measurement methods

Leading Edge Discriminator (**LED**)

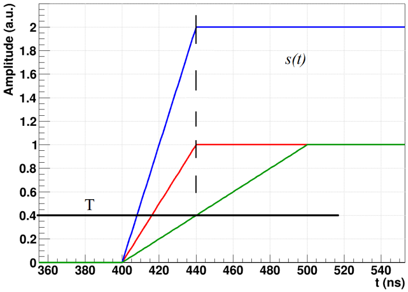


$$\sigma_{LED} = \frac{t_{rise}}{\mathrm{SNR}}$$

Intersection between a fixed threshold T and the signal $s(t)$

Time measurement methods

Leading Edge Discriminator (**LED**)



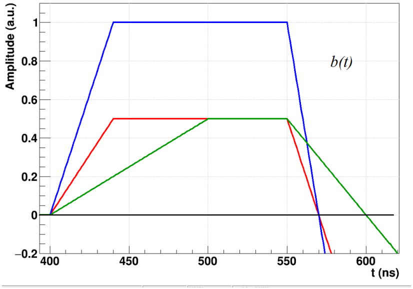
$$\sigma_{LED} = \frac{t_{rise}}{\text{SNR}}$$

Intersection between a fixed threshold T and the signal $s(t)$

Subject to amplitude and rise time walk

Time measurement methods

Constant-Fraction Discriminator (**CFD**)



$$\sigma_{CFD} = \frac{t_{rise}}{\text{SNR}}\sqrt{1+f^2}$$

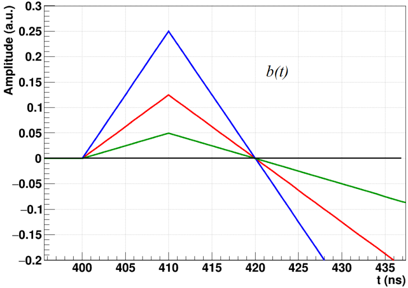
Zero crossing of the bipolar signal $b(t) = f \cdot s(t) - s(t - t_D)$

$$t_D \geq (1-f)t_{rise}$$

Subject to rise time walk

Time measurement methods

Amplitude and Rise time Compensated CFD (**ARC-CFD**)



$$\sigma_{ARC} = \frac{t_{rise}}{\mathrm{SNR}} \frac{\sqrt{1+f^2}}{1-f}$$

Zero crossing of the bipolar signal $b(t) = f \cdot s(t) - s(t - t_D)$

$$t_D < (1-f) t_{rise}$$

FAZIA collaboration

Publications

- S. Barlini *et al*, Nucl. Instr. and Meth. A 600 (644–650), 2009
- L. Bardelli *et al*, Nucl. Instr. and Meth. A 654 (272), 2011
- S. Carboni *et al*, Nucl. Instr. and Meth. A 664 (251), 2012
- N. Le Neindre *et al*, Nucl. Instr. and Meth. A 701 (145), 2013
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- R. Bougault *et al*, Eur. Phys. Jour. A 50 (47), 2014
- G. Pasquali *et al*, Eur. Phys. Jour. A 50 (86), 2014
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- F. Salomon *et al*, J. Instrum. 11 (C01064), 2016
- D. Gruyer *et al*, Nucl. Instr. and Meth. A 847 (142), 2017
- G. Pastore *et al*, Nucl. Instr. and Meth. A 860 (42), 2017