TOP STATUS

WENLONG YUAN

INFN PADOVA

8th Belle II Italian collaboration meeting
21 November 2017 - Pisa

Outline

- Firmware status
- TOP in GCR
- Calibration status
- PEEK delamination issue
- TOP Upgrade
- Summary

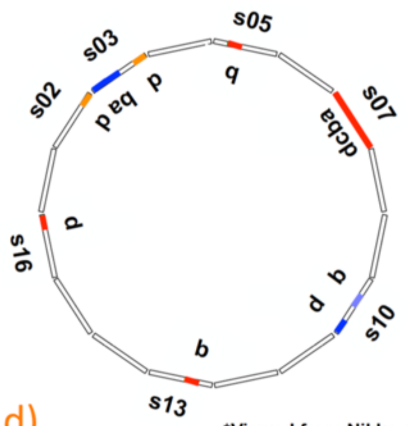
Firmware Issues

Yosuke Maeda, Hulya Atmacan, Osacar Hartbrich, Matt Andrew, Luca Macchiarulo, Kurtis Nishimura, Gary Varner

- Known Issues/Bugs:
  - **B2llost.**
  - **Carrier-level synchronization issues.**
  - **Board stack-level synchronization issues.**
  - **Apparent event skew.**
  - **Dropping matching efficiency over runs.**
- Fundamental problems:
  - **Limited event rate**

Green – Solved, deployed, verified.
Blue – Tentatively solved, waiting to be fully verified.
Red – Unsolved or unverified fix.

- 4 boardstacks are masked due to
  - Data corruption (s05-b)
  - Data taking stops (s07-c, s13-b, s16-d)
- Some more unstable boardstacks
  - Data corruption (s10-b,d, s03-a,b)
  - Data taking stops (s07-a, b, d)
  - Sudden turn off of LV power supplied off (s02-d, s03-a,d)



*Viewed from Nikko side (backward direction)

Summary of Slot Status

O = unmasked, ((O)) = mostly masked

	BS 0	BS 1	BS 2	BS 3
slot 01	o	o	o	o
slot 02	o	o	o	o
slot 03	o	o	o	o
slot 04	o	o	o	o
slot 05	o	MASKED	o	o
slot 06	o	o	o	o
slot 07	((O))	((O))	MASKED	((O))
slot 08	o	o	o	o
slot 09	o	o	o	o
slot 10	o	o	o	o
slot 11	o	o	o	o
slot 12	o	o	o	o
slot 13	o	MASKED	o	o
slot 14	o	o	o	o
slot 15	o	o	o	o
slot 16	o	o	o	MASKED

Will investigate these BS's and give feedback to firmware experts.

Firmware known bugs (fixed)

- Carrier level synchronization:
  - Last written address register should always be odd to guarantee wraparound at the correct phase.
    - Even write windows are in "**A**" phase, odd are in "**B**" phase.

Write address should transfer from **A** → **B** → **A** → … in order to match internal ASIC phases.

Example correct transition (**255**→ **0**):

0 1 2 … … 253 254 255

Example incorrect transition (**254** → **0**):

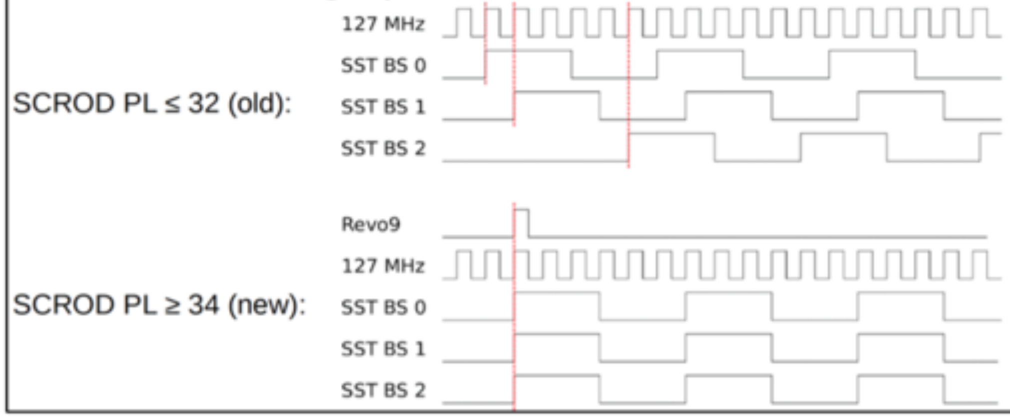
0 1 2 … … 253 254

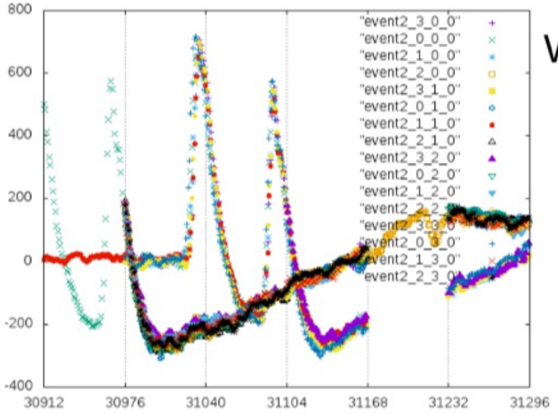
Phase is now wrong every other trip through the buffer.

➔ Fix deployed for existing firmware was a simple register change for last address. Fix is by design in production firmware.

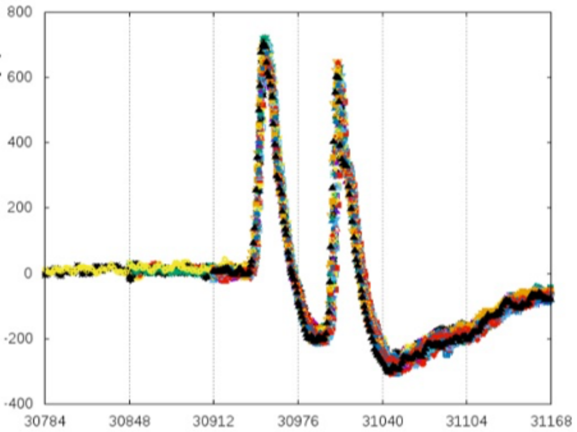
Board-stack synchronization:

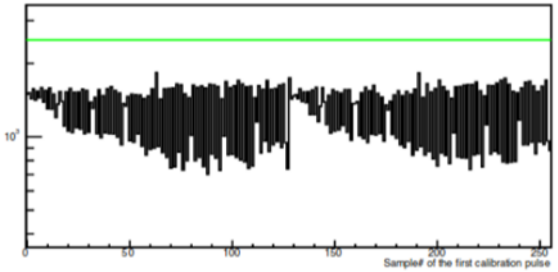
- Reset of a clock divider on the carrier was being synchronized only to 127 MHz clock
  - Fixed through sync @ Revo9



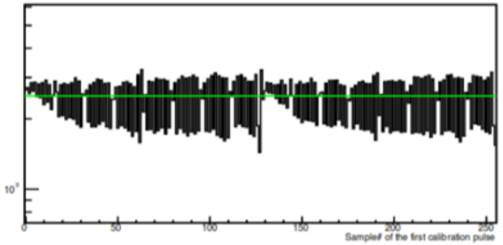


Waveform Alignment





CalPulse Efficiency

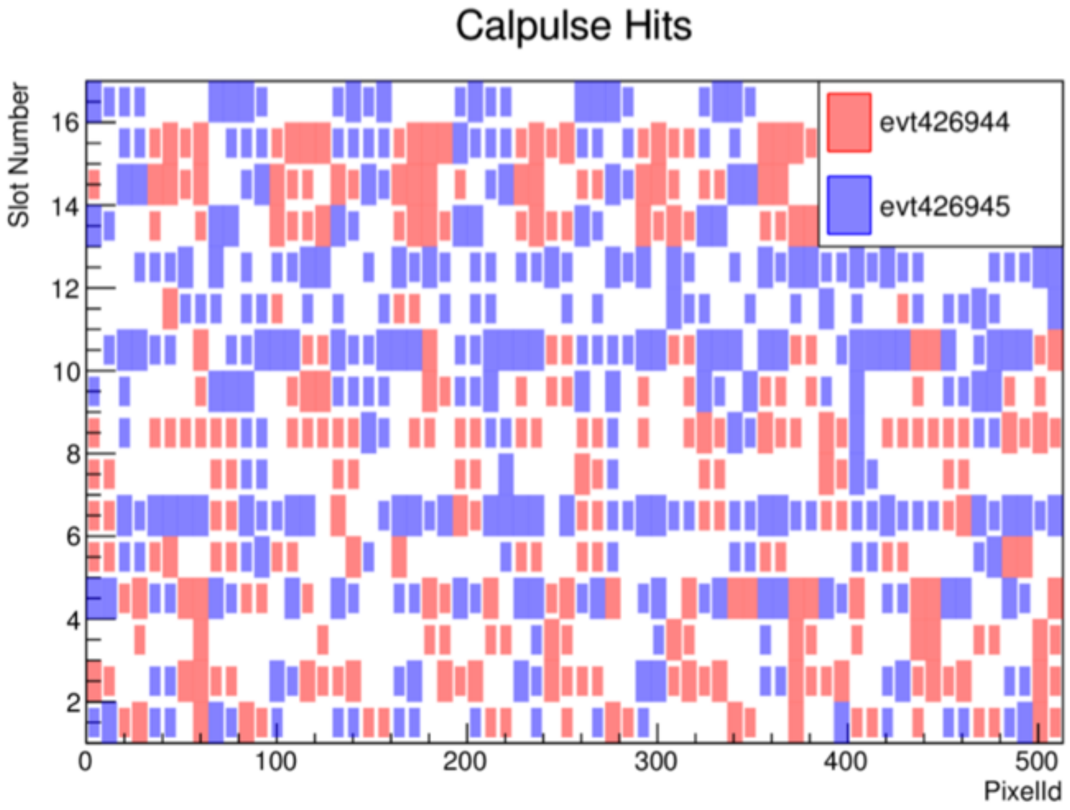


Firmware Existing bugs

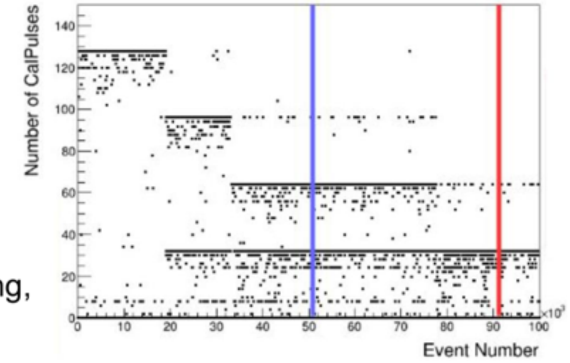
- Event number shifts/misalignments

  Data from single event is split into several events

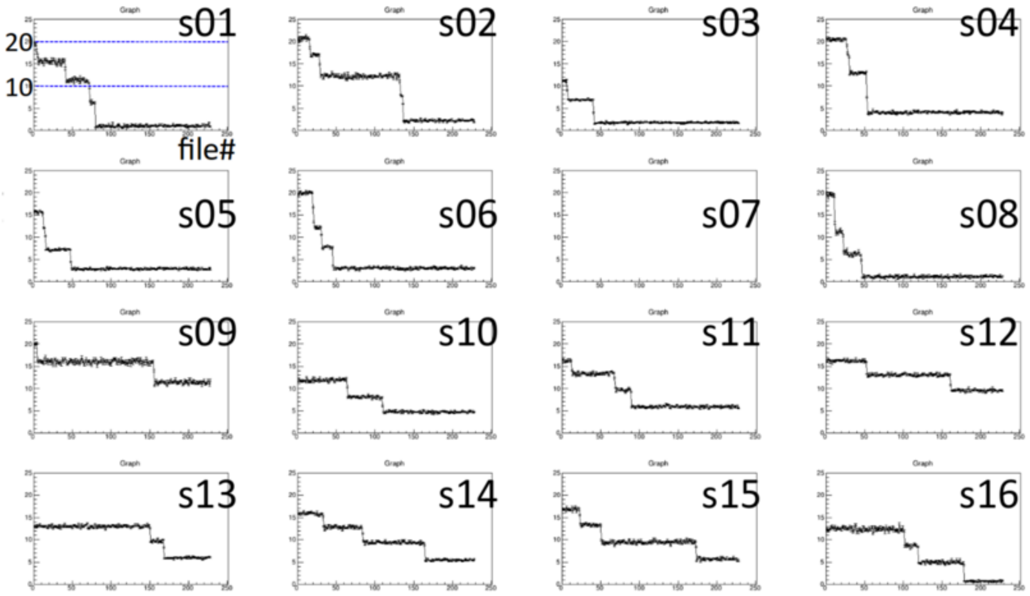
- Explains loss of matching efficiency



- Several possible causes were evaluated, shown to not be the problem
  - Appears to be dropped trigger?



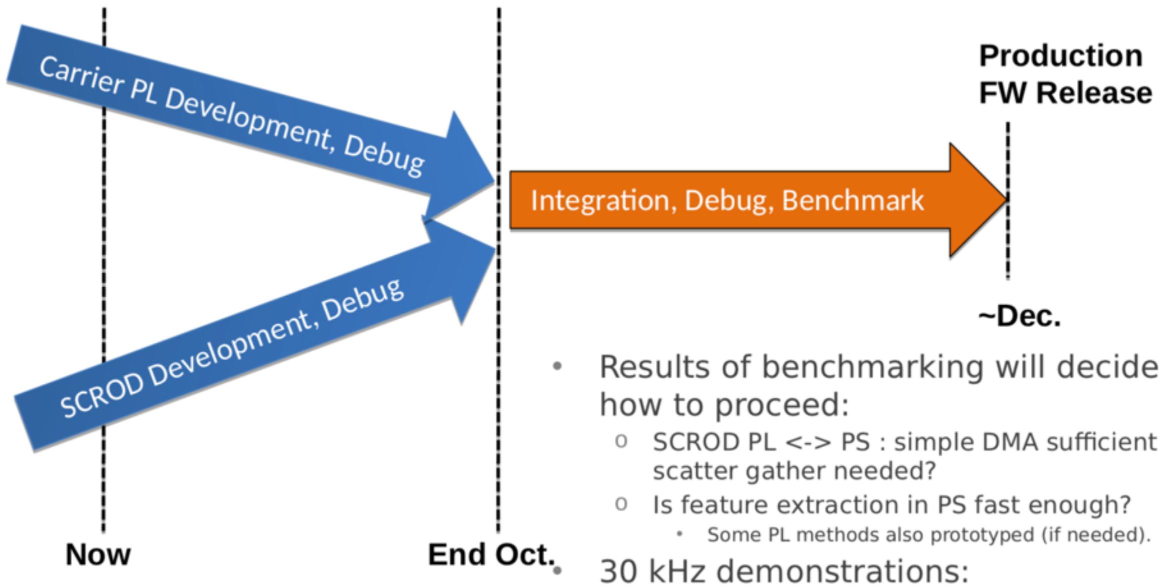
- Likely an issue in the messy PS code (interrupts, data handling, complicated call structure, etc.)
- Decision was made to focus on production firmware effort instead:
  - Person who wrote the PS code no longer working on Belle II
  - Production code is being built with all-new PS base code (may solve problem)
  - If still present, debugging will be easier in production firmware



Production Firmware

- Current FW:
  - Existing system is operating in “simple” mode.
    - Analog recording stops upon receipt of a trigger.
      - Each channel of each ASIC digitizes and reports 256 samples for every system trigger, resumes sampling only after digitization.
      - Timings not optimised
      - This is in obvious need of upgrade for high rate running.
    - Limited to ~750 Hz, as verified in local single module tests.

- Production mode:
  - Implements simultaneous sampling and digitizing/readout.
  - Only data for channels with hits. (32 samples around trigger)
  - Details available in Luca’s slides from TOP firmware bootcamp.
  - Split into two components:
    - Updated Carrier PL firmware to implement above.
    - Updated SCROD PL/PS to process new data stream.



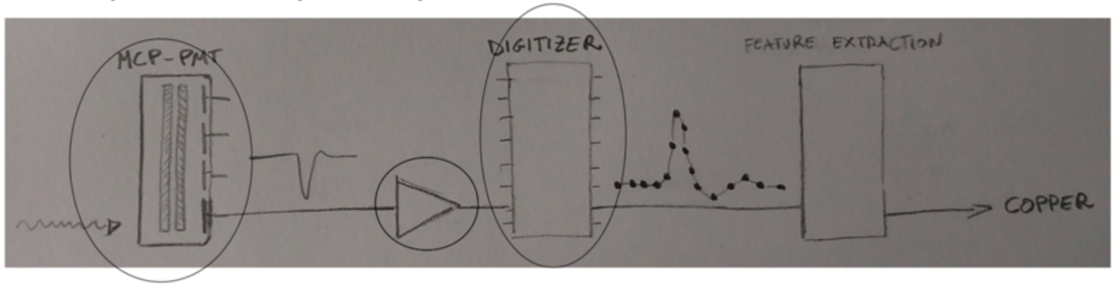
General plan here regarding benchmarking still fully relevant.

- Results of benchmarking will decide how to proceed:
  - SCROD PL <-> PS : simple DMA sufficient or scatter gather needed?
  - Is feature extraction in PS fast enough?
    - Some PL methods also prototyped (if needed).
- 30 kHz demonstrations:
  - Highly occupancy dependent.
  - Can make a simple demonstration that suppresses excess waveforms if needed.

TOP Calibration Status

Umberto Tamponi

TOP calibration is mostly about channel-by-channel synchronization



Photon detection → PMT Transient time

Fast amplifier → Transient time

Digitization of the waveform → sampling bin size

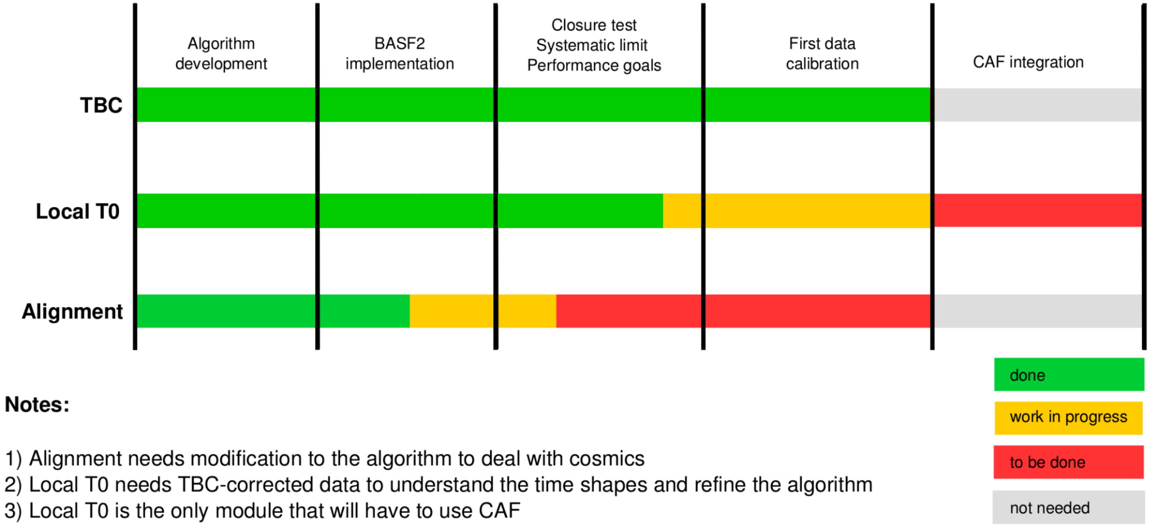
$$T_{photon} = t_{digit} + T^0_{channel} + T^0_{module}$$

Time base calibration (TBC)
Calibration of the bin size of the digitizer

Local T0
Synchronization of the channels within a single quartz bar

Module T0
Synchronization of the modules one with the others

+ Geometrical alignment !



Notes:

1) Alignment needs modification to the algorithm to deal with cosmics
2) Local T0 needs TBC-corrected data to understand the time shapes and refine the algorithm
3) Local T0 is the only module that will have to use CAF

Raw Data (TOPRawDigit) → Time Base Correction (TBC) → Local T0 (ChT0) → Module T0 (ModT0) → Calibrated Data (TOPDigit)

Time Base Correction (TBC): Corrects the sampling inhomogeneities in the FE digitizer *(< 1 ns effect)*

Local T0 (ChT0): Synchronizes the channels within a module *(few ns effect)*

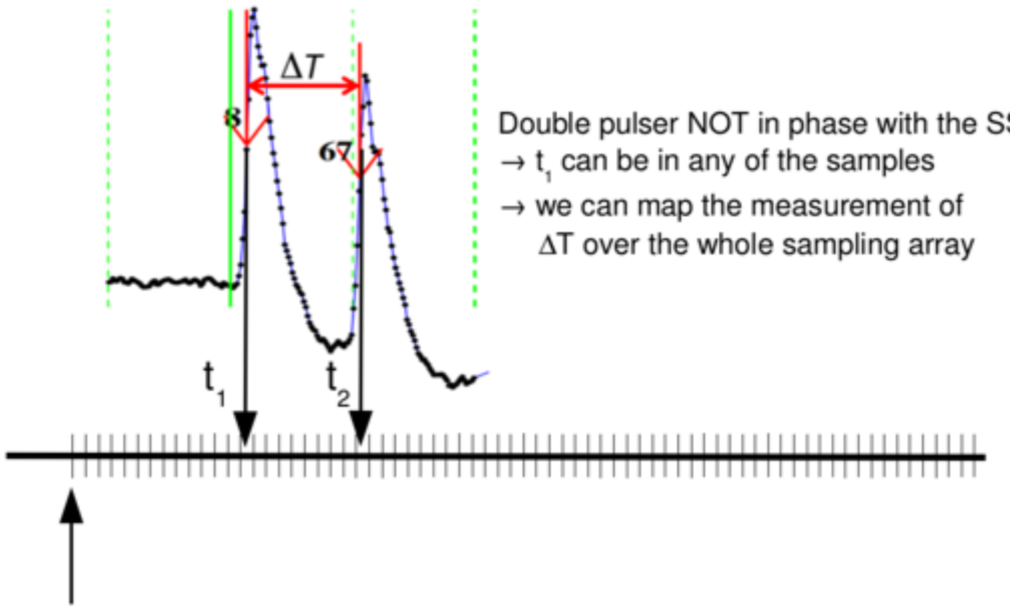
Module T0 (ModT0): Synchronizes the modules with each other *(several ns effect)*

Time base correction (TBC)

H. Kichimi, W. Xiaolong

- Each of the capacitors on the sampling array has a different time constant, and gives different time bin width.
- The trace is sampled in blocks of 64 samples ("windows"). Each ASIC has a sampling array of 4 windows, then saved in a much deeper buffer memory (Storage array)

Calibration method
→ Inject a double pulse with known delay on each asic
→ Map the delay as function of the sample number
→ Correct either iteratively or solving a linear system



SST clock (KEKB clock-based)
Sample 0

Double pulser NOT in phase with the SST
→ t_1 can be in any of the samples
→ we can map the measurement of ΔT over the whole sampling array

$$\chi^2 = \sum_i \frac{\left(\sum_{k=1}^{N} m_k^{(i)} \Delta t_k - \Delta T\right)^2}{\sigma_{t,i}^2}$$

Sum over the samples between t1 and t2

Widths of the N samples between the pulses

Sum over all the collected events

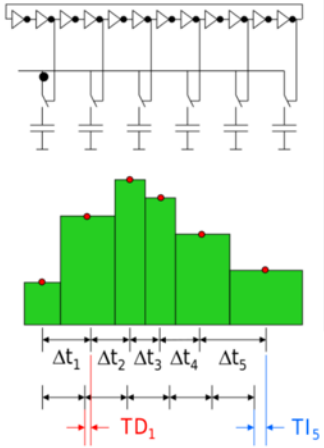
Accounts for the fraction samples (1 and N)

Two methods to minimize:

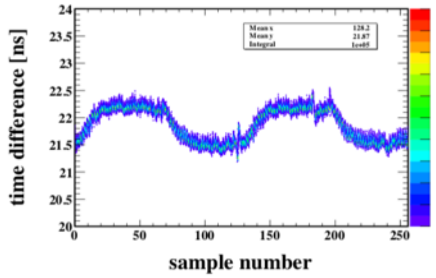
→ Iterative minimization

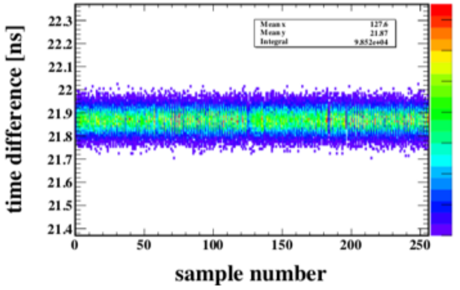
→ Matrix inversion (default one?)

1 channel → 256 time bins



- Inverter chain has transistor variations
  → Δt_i between samples differ
  → "Fixed pattern aperture jitter"
- "Differential temporal nonlinearity"
  $TD_i = \Delta t_i - \Delta t_{nominal}$
- "Integral temporal nonlinearity"
  $TI_i = \Sigma \Delta t_i - i \cdot \Delta t_{nominal}$
- "Random aperture jitter" = variation of Δt_i between measurements

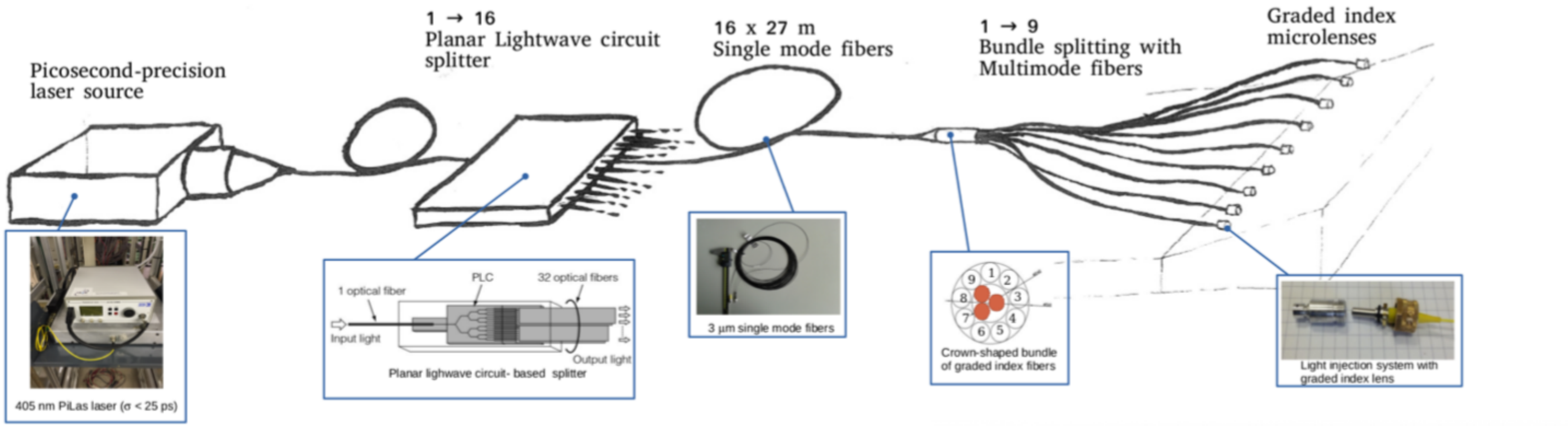




Local T0

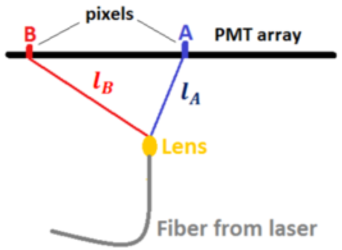
A. Morda, W. Yuan, S. Lacaprara, R. Stroili

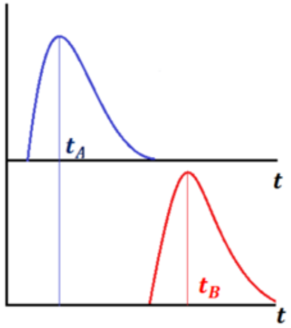
To synchronize the channels within a single module we flash them with a laser pulse



- goal of the channel time calibration is the measurement of the time offset (T^0) of each MCP-PMT pixel
- T^0 different for each pixel due to electronic & pixel properties
- a total of 512×16 channels must be calibrated

The simple case:



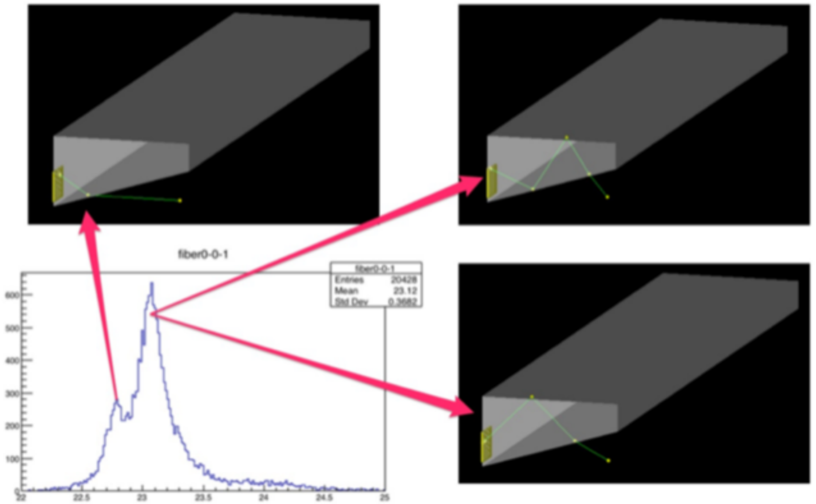


$$t_{(A,B)} = T^0_{(A,B)} + \ell_{(A,B)}/c_n$$

$$T^0 = t_{data} - t_{MC}$$

$$\delta T^0 = \delta t|_{data} + \delta t|_{MC} + \delta t|_{DATA\&MC}$$

- $T^0_{(A,B)}$: channel time cal. constant
- $\delta t|_{data\&MC}$: a large systematic error if mismatch data&MC



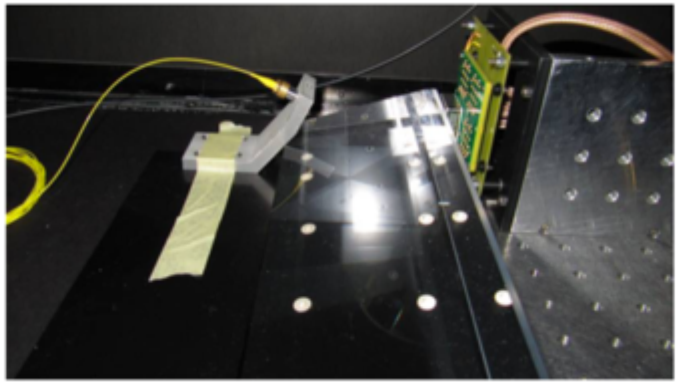
Padova test bench studies

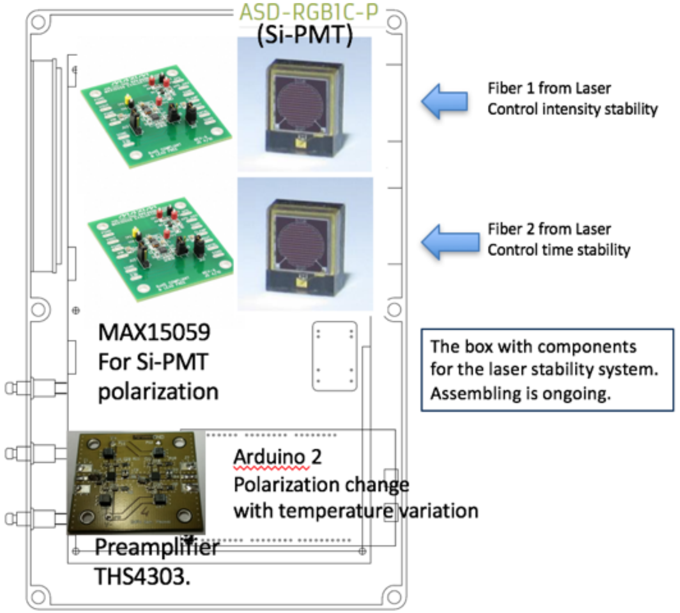
Laser stability system

- Will be installed in KEK
- A second box will be used in the Padova-Setup

Padova equipment

- 1 MCP-PMT Hamamatsu (2nd PMT is ready)
- 1 SiPM FBK
- HV = 2500 V
- digitizer CAEN V1742 @5 GHz
- fibers + final bundle
- nominal lens used in the experiment

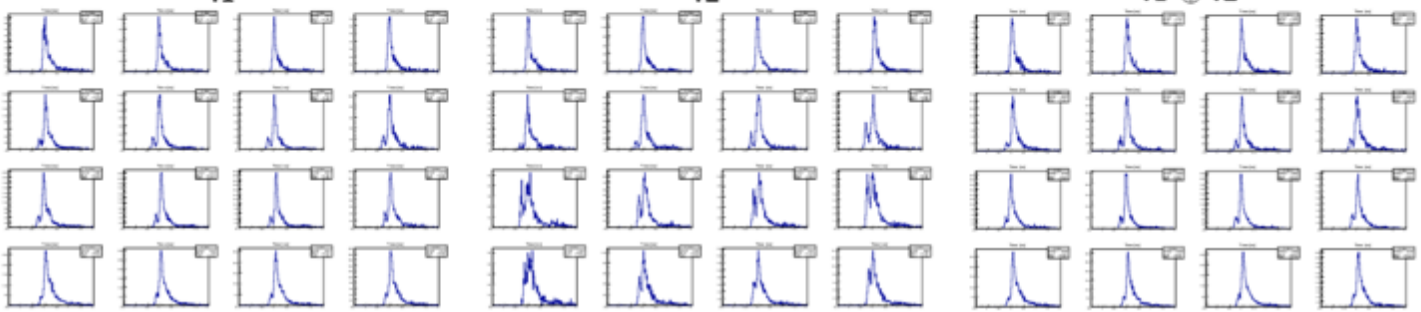




Superposition of adjacent fibers - time distribution x-axis range [-1.5,2] ns

- Laser Tune 50
- example on PMT with two separate signals

f1 f2 f1 $\oplus$ f2



- the contribution of the adjacent fiber appears to be negligible in this position
- likely two signals are enough to fit the whole spectrum with all fibers
- will check for the other positions

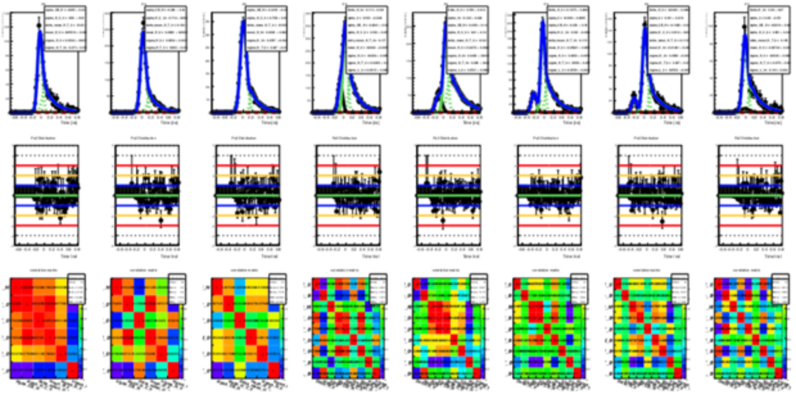
Fit of pixel column 3

PMT illuminated from two sources, laser @ T50

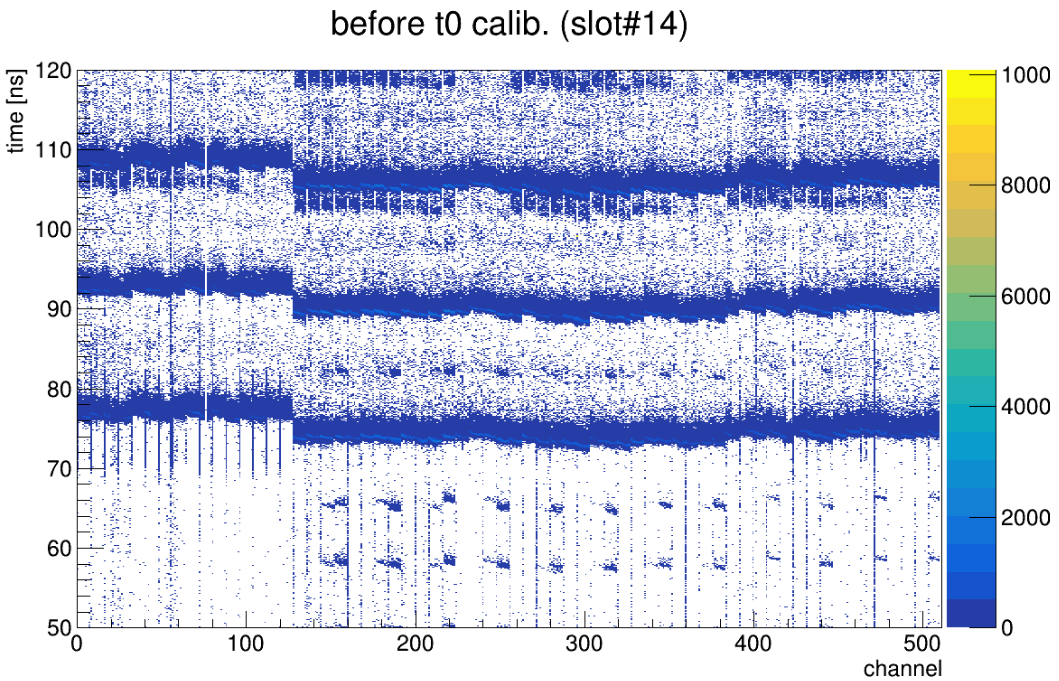
"Hybrid" model (naive compromise between data agreement & number free parameters):

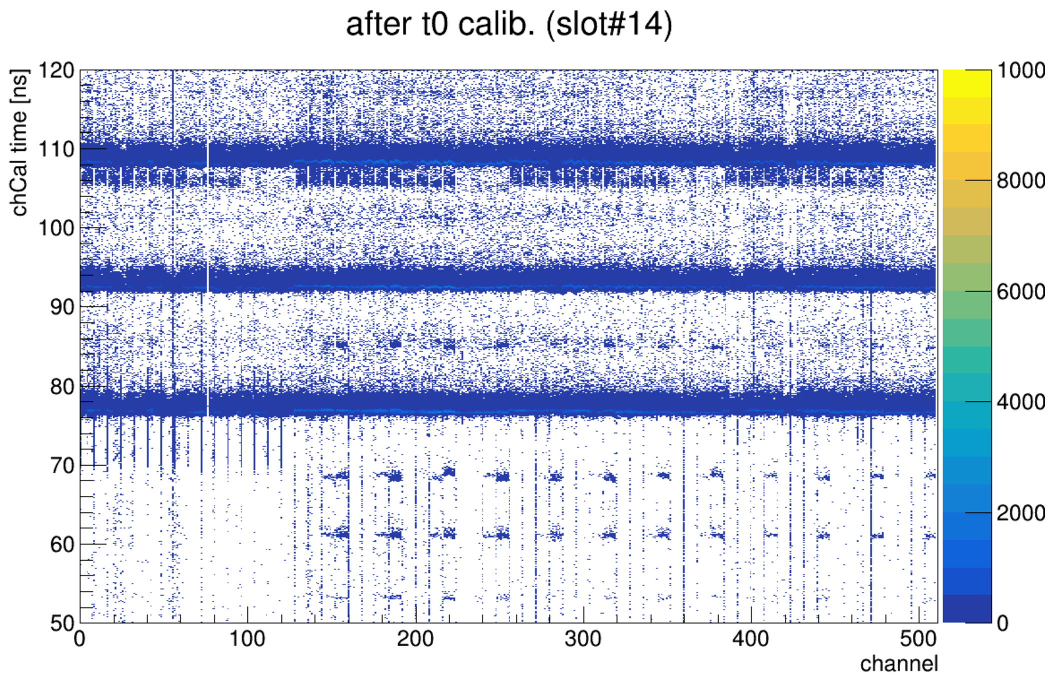
- rows 1-3 : one signal described by gaussian core $\oplus$ kinematic recoil component
- rows 4-8 : two signals. Low time described by pure gaussian, high time signal as in rows 1-3

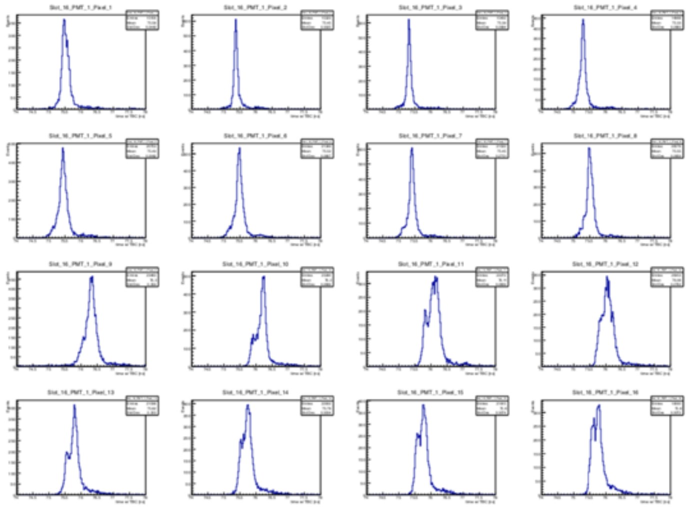
row 1 $\longrightarrow$ 8



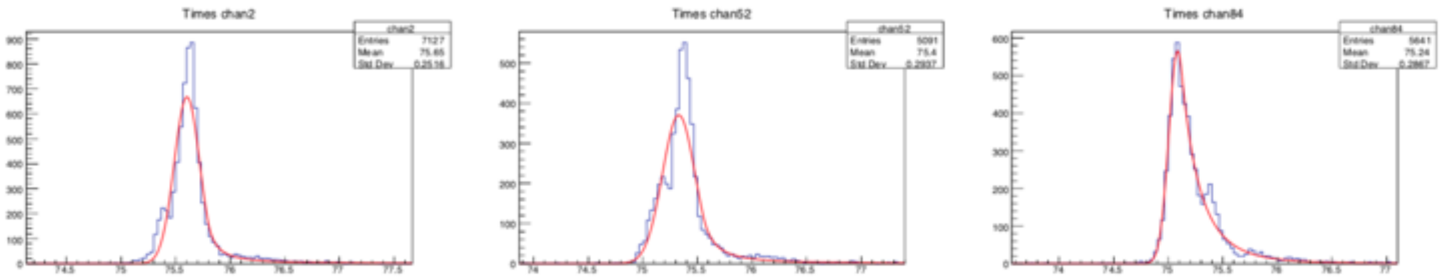
Local T0 constant implementation (preliminary)





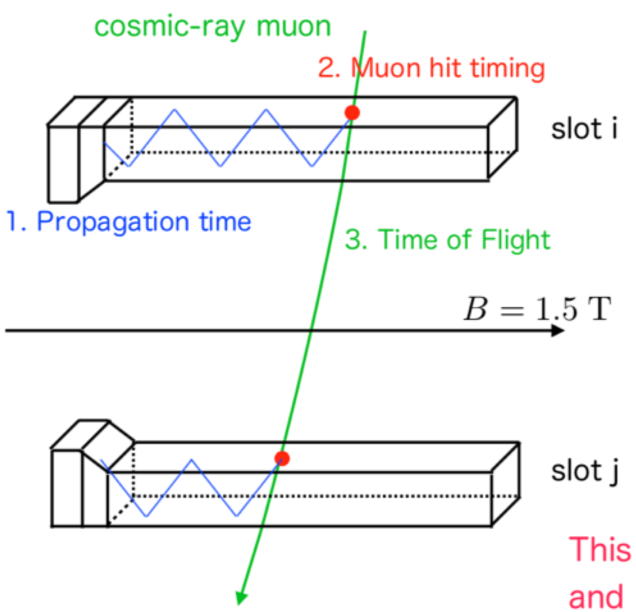


- a very rough fit using a single crystal ball function
- one single Gaussian or single crystal ball function is not an appropriate description on this data sample



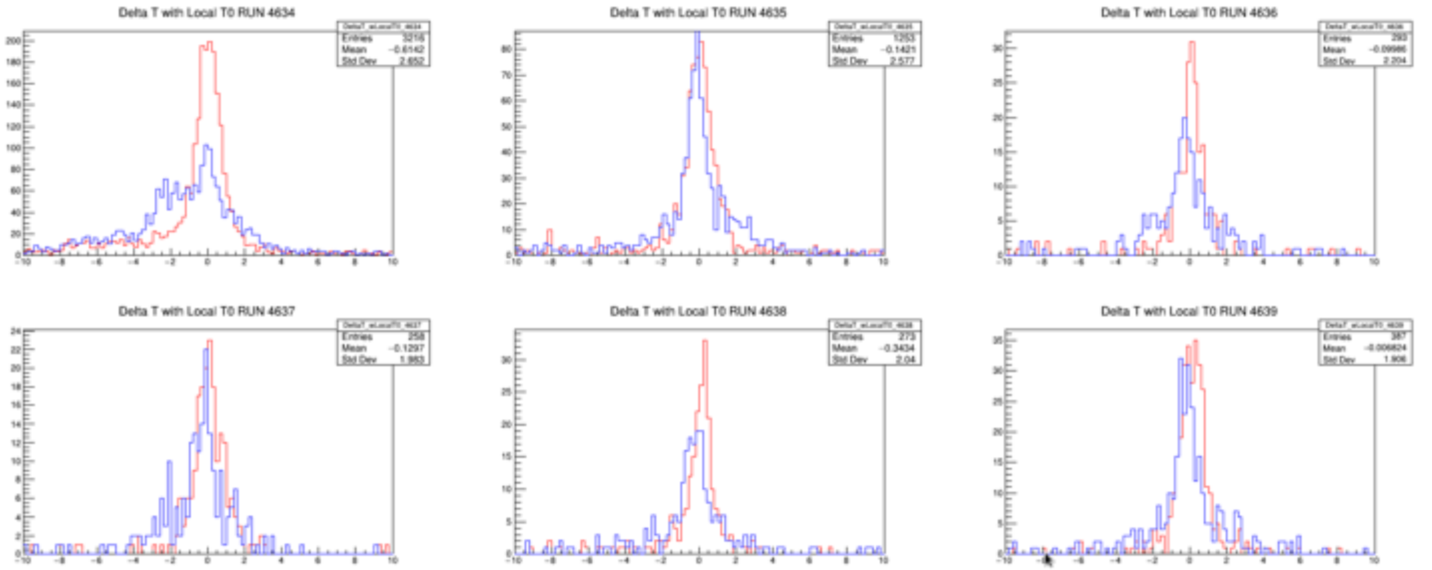
Module T0

S. Senga, A. Gaz



1. Subtract propagation time with extHit.track information, for each event.
2. Determine "muon hit timing."
3. Calculate the time difference between 2 "muon hit timing" (=TOF_{TOP}).
4. Compare that value with TOF_{trk}, computed using extHit.track information. Draw the plot $\Delta t = TOF_{TOP} - TOF_{trk}$.

This value should be zero in the simulation, and in the data if modules are correctly aligned in time.



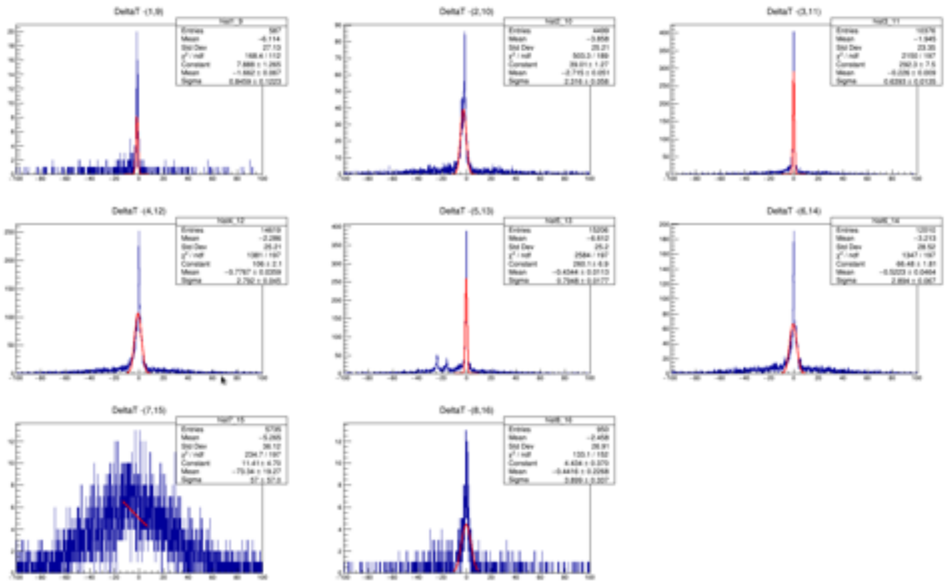
χ^2 method

$$\chi^2 = \sum_{i,j} \left[\Delta t^{ij} - \left(t_0^j - t_0^i\right)\right]^2 / \left(\sigma^{ij}\right)^2$$

Δt^{ij}: Mean(TOF_{TOP}-$TOF_{expected}$)

σ^{ij}: Mean Error

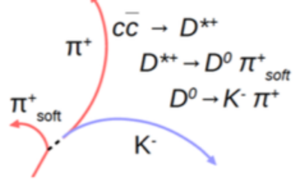
$t_0^{i(j)}$, the time origin of slot i(j), is determined so that χ^2 becomes minimum. (t_0^4 is fixed to zero.)



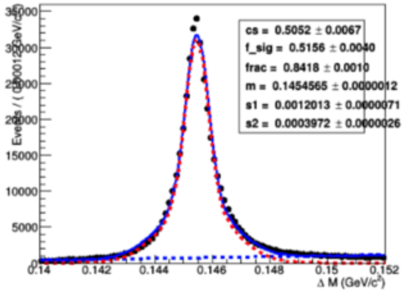
Studies in physics channels

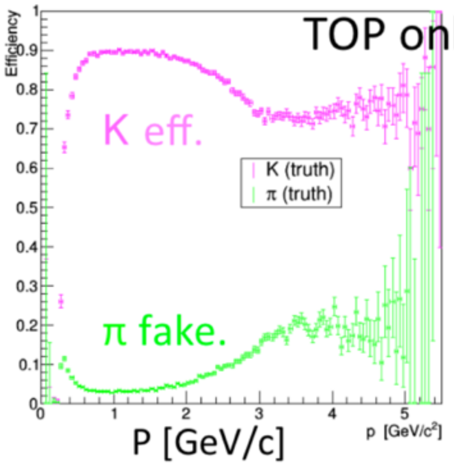
- K/p PID studies using D* decays

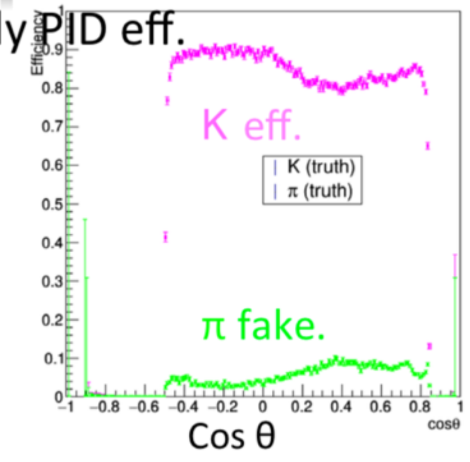
Saurabh Sandilya



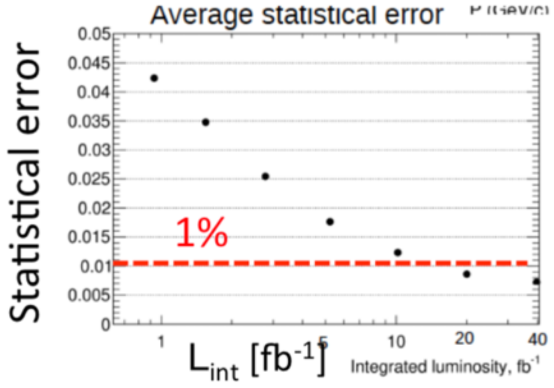
$\Delta M = M(D^*) - M(D^0)$

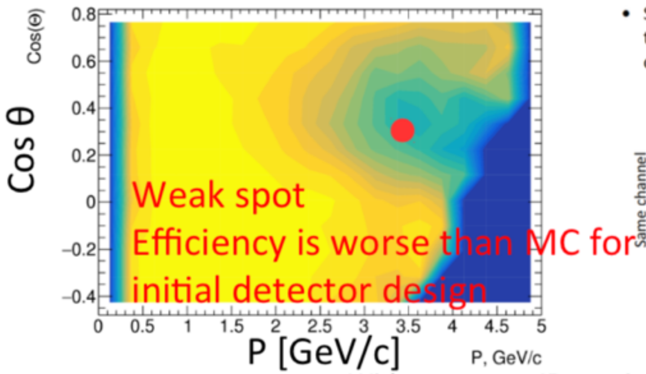






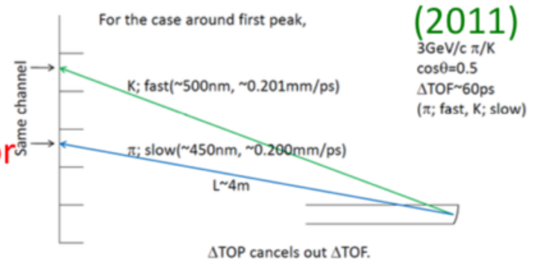
Dimitri Neverov





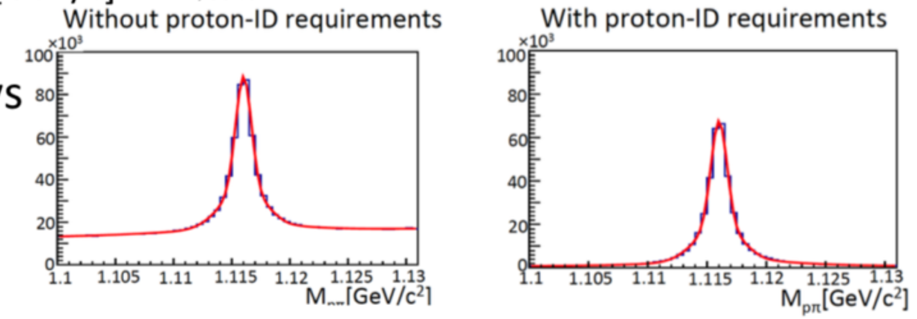
- Some of detected photons for pion and Kaon show similar timing at the same channel, accidentally, due to the difference of wavelength/group velocity.

K. Inami (2011)



Hikari Hirata

- Proton ID study using $\Lambda \to p\pi$ decays
- Proton ID eff. = 91.11 ± 0.26 %
  - +1.5 σ difference from Mctruth ?

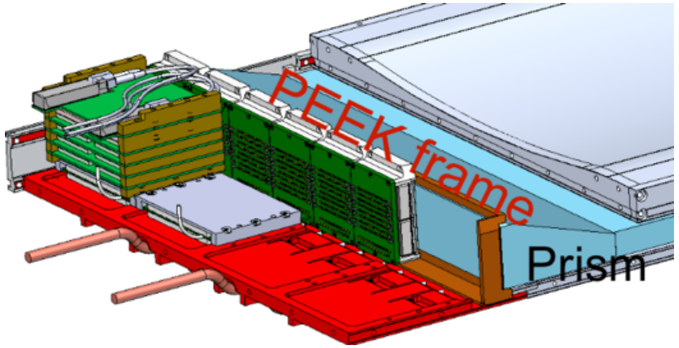


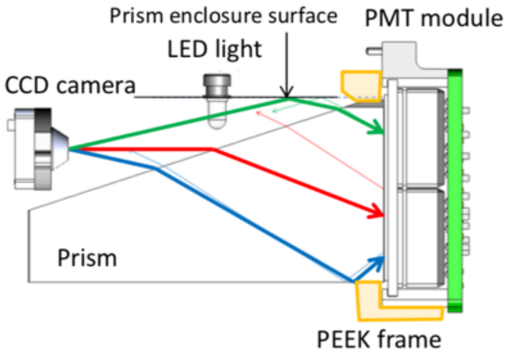
Slides from Toru Iijima, 28th B2GM

PEEK Delamination Issue

Kodai Matsuoka

- Most plausible reason is the interface stress by thermal expansion
- Confirmed that visible area of the delamination depends on whether the electronics is on or off
- Plan to measure the temperature distribution of the spare TOP module, and investigate a risk of developing delamination

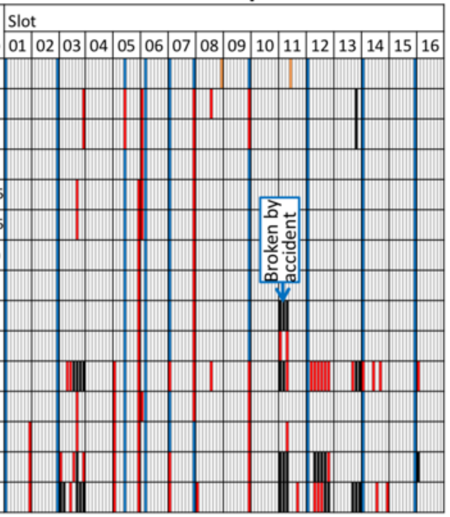




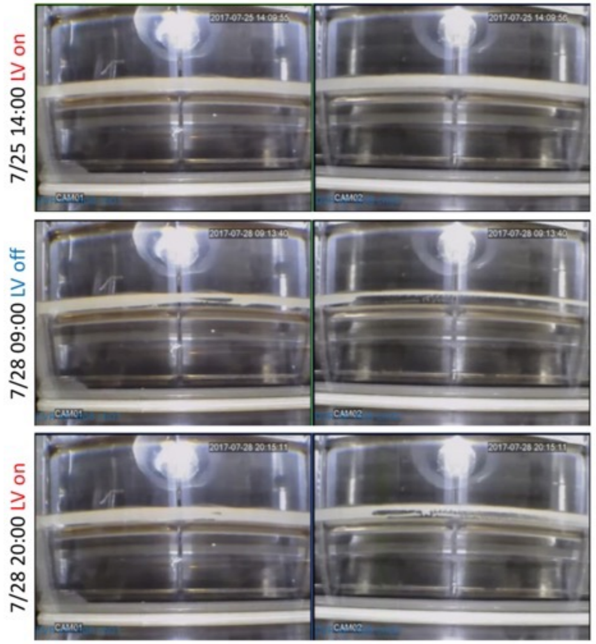
CCD view with a mockup

Delamination visible in CCD photos

Year	Shooting date	Time	LV	B-field (T)
2016	5/16 (after installation)	19:45	on	0
2016	7/26 (after B-field meas.)	10:00	on	0
2016	7/26 (after 1st repair)	11:00	on	1.5
2016	9/13 (after 2nd repair)	17:00	on	0
2016	9/16	09:15	on	0/1/1.5
2016	9/19 (start of 1 week B test)	08:45	on	0/1/1.5
2016	9/26,27 (after 1 week B test)	08:45	on	1.5/0
2016	9/27,28,29,30,10/1,2,3	18:30	on	1.5
2016	10/3 (slot11 glue broken)	17:45	on	0
2016	10/4,10	21:15 10:30	on	0
2017	4/20 (after roll-in)	14:30	off	0
2017	5/24,26	16:45 15:15	on	0/1.5
2017	7/10 (1st GCR)	14:00	on	1.5
2017	7/25 (1 h after LV off)	15:40	off	1.5
2017	7/28 (after E-hut shutdown)	09:00	off	1.5



Blue: Small delamination (apparently or in suspicion) from the beginning
Black: Large delamination can be seen (compared to 5/16)
Red: Small delamination can be seen (compared to 5/16)
Orange: Small delamination can be seen (compared to 7/26)



Thermal expansion of the PEEK frame/glue made the delamination (in)visible.

It could be a possible cause of the delamination.

Doubt if the optical oil can enter the thin gap.

TOP upgrade

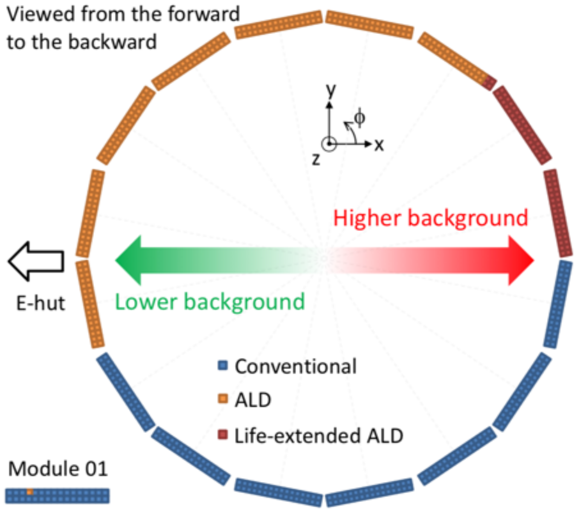
Summary of the number of MCP-PMTs

	Conventional	ALD	Life-extended ALD
Total in hand	277	231	108
To be returned	16	7	0
Installed	255	221	64
Available spares	6	3	44
To be delivered			16 + 20 (new order)

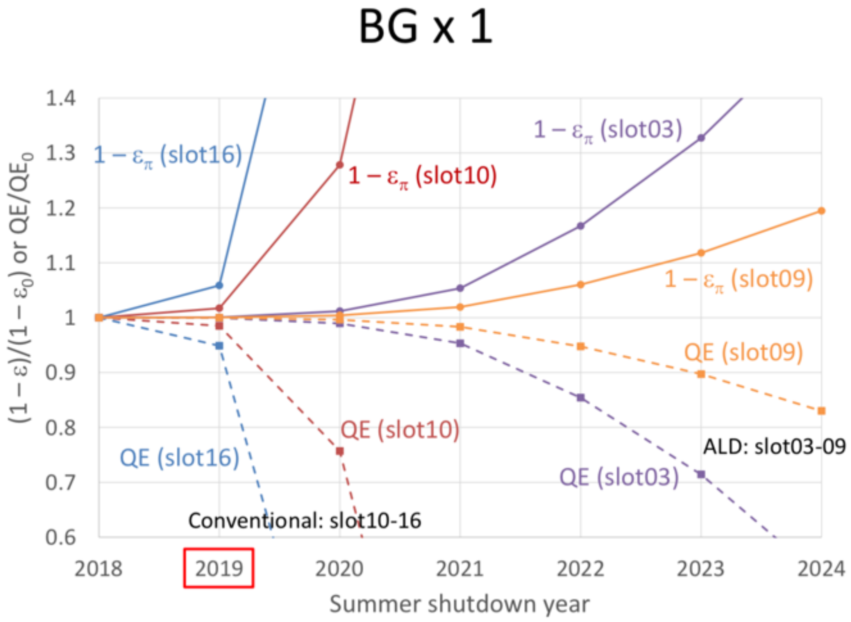
Total available for replacement of the installed conventional MCP-PMTs: 83
Conventional MCP-PMTs to be replaced: 224
Necessary additional order: 141

- The current estimation of the time of the replacement is 2020 summer shutdown, which depends on the actual level of the beam background (current assumption is 5-8 MHz/PMT) and on the PMT gain (current assumption is 2.5×10^5).
- Production rate: about 10 PMTs/month → 16 months for 161 PMTs
  - Need continuous production for stable production referring back to experience.
- Plan to continue small production until the actual beam background is understood in Phase 2 operation, but need budget.
- Decide a plan of the later production after Phase 2.

Year	2017				2018				2019				2020		
Month	1	4	7	10	1	4	7	10	1	4	7	10	1	4	7
Global schedule					Phase 2				Physics run			Physics run			
PMT production	Current production														
			Another small production (+20)												
							Mass production if necessary								
PMT test															
PMT installation													Assy		Install
Available PMTs			44	63	83	Unclear (depends on budget situation)									



- The 224 conventional MCP-PMTs in the 7 slots have to be replaced due to the QE degradation by the beam background.
- Need additional mass production of the MCP-PMTs for the replacement.
- Continue the production of the Hamamatsu 1-inch life-extended ALD MCP-PMTs.



TOP upgrade

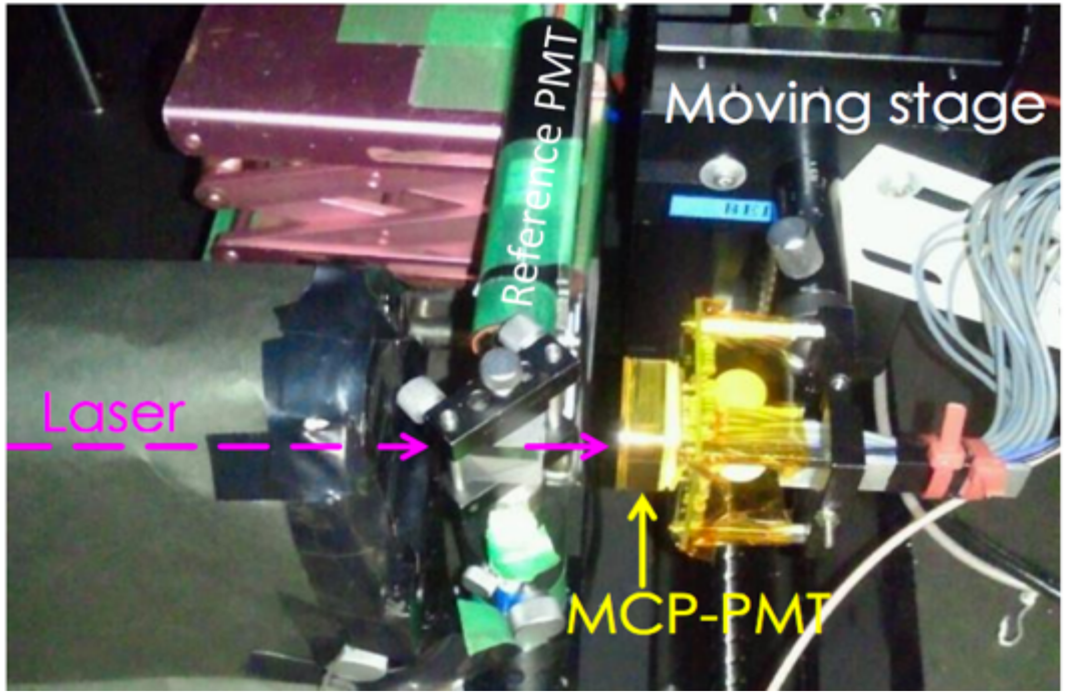
Conventional MCP-PMTs to be replaced: 224

	ALD	life-extended ALD	Ordered	TOT
Available MCP-PMTs for replacements:	3	60	20	83

60 → (tested by Nagoya) 44 / 16 (will be tested in January by PD)

20 (will be tested in spring by PD/TO)

Laser setup in Nagoya



1) **HV test**

2) **Laser test**
- Gain(HV)
- TTS(HV)
- CE(HV)

in 0 T

At Nagoya with 0 T

At KEK with 1.5 T

3) **QE measurement**
- QE(λ)

QE setup: Xe lamp

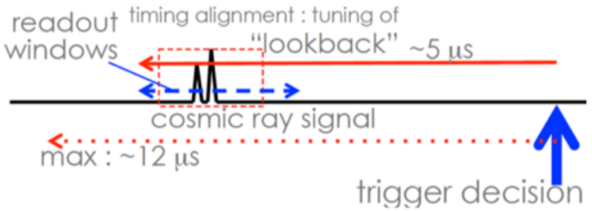
Summary

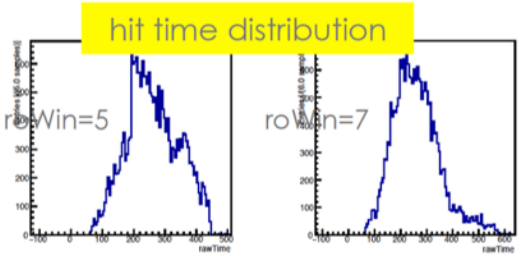
- Firmware status
  - Event skew
  - Trigger rate limitation
  - Feature extraction optimization
- Calibration tools for beam collision are becoming ready
  - ✓ Time Base Calibration
  - ✓ Local T0 (close)
  - ✓ Alignment (close)
- TOP upgrade
  - New PMTs production and test

BACKUP

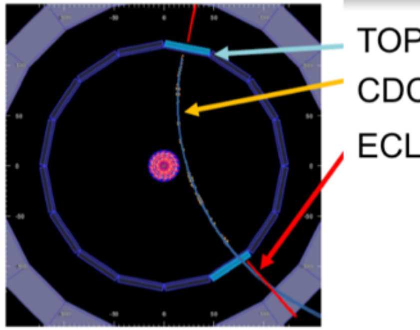
TOP in GCR

- "b2llost" problem, initially stopped DAQ frequently, was turned out to be due to frequent register access
- New firmware versions were developed
  - 32-31/3D-06: temporary fix, requires special HSLB fw, since June/end .
  - 32-31-b2llfix/3D-06: can work with normal HSLB. Was ready by the middle of Aug., but not used in Aug. GCR.
  - 33-31/3D-06, 34-31/3D-06: fix for "timing mis-alignment" problem
- Limitation
  - Single hit / channel
  - Trigger rate ≲750 Hz,
    - need 1.5ms "hold-off" time.
    - Another limitation from disk I/O
    - → ≲200 Hz in practical use
- Tuning of readout parameters carried out.
  - Readout windows
  - Lookback window
  - CFD thereshold

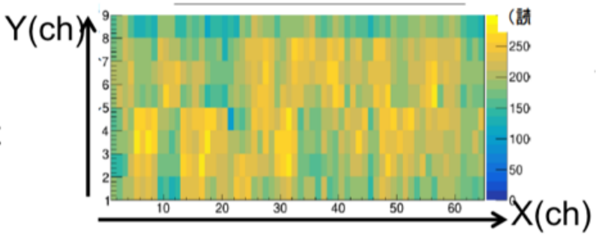




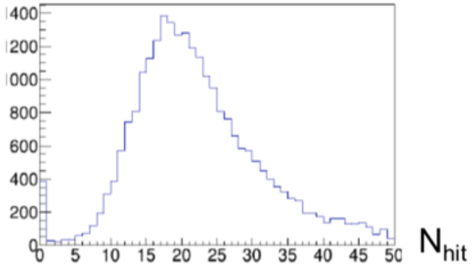
- Module N_{hit} distribution is as expected: $\langle N_{hit} \rangle$ = ~20
- Module efficiency is high with BKLMhit > 0
  - 12(7) out of 16 modules have eff. > 90%(95%)
- Still have to understand and study
  - N_{hit} stability
  - Detailed comparison between data and MC (for N_{hit} and track momentum dist.)
  - Time calibrated (x, t) ring image



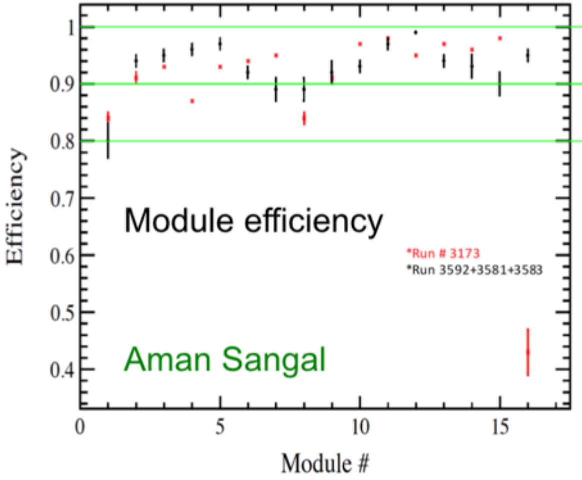
MCP-PMT hit map



Typical N_{hit} distribution



Noritsugu Tsuzuki



Slides from Toru Iijima, 28th B2GM