The ATLAS Pixel Detector for HL-LHC

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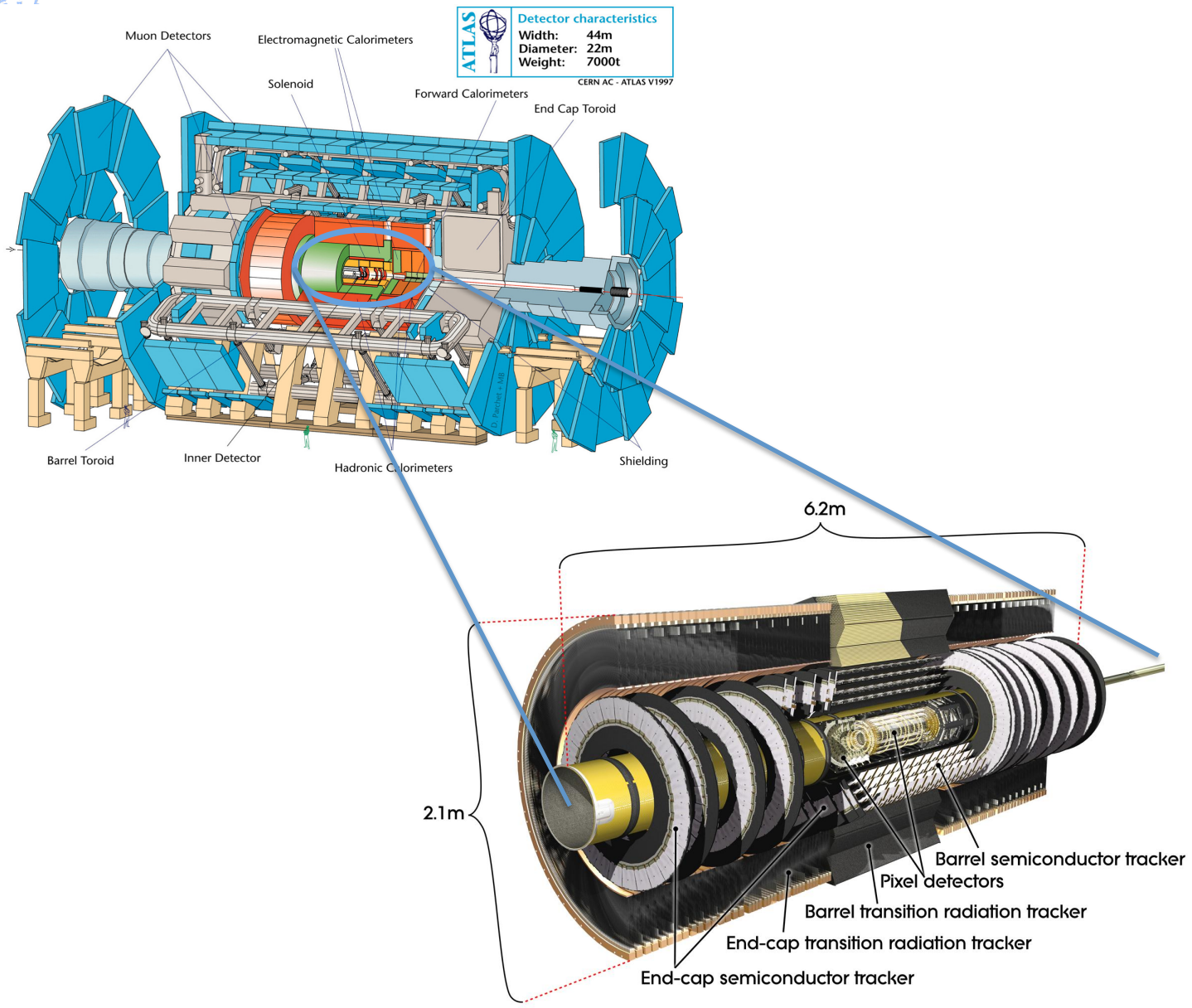
The present ATLAS pixel detector



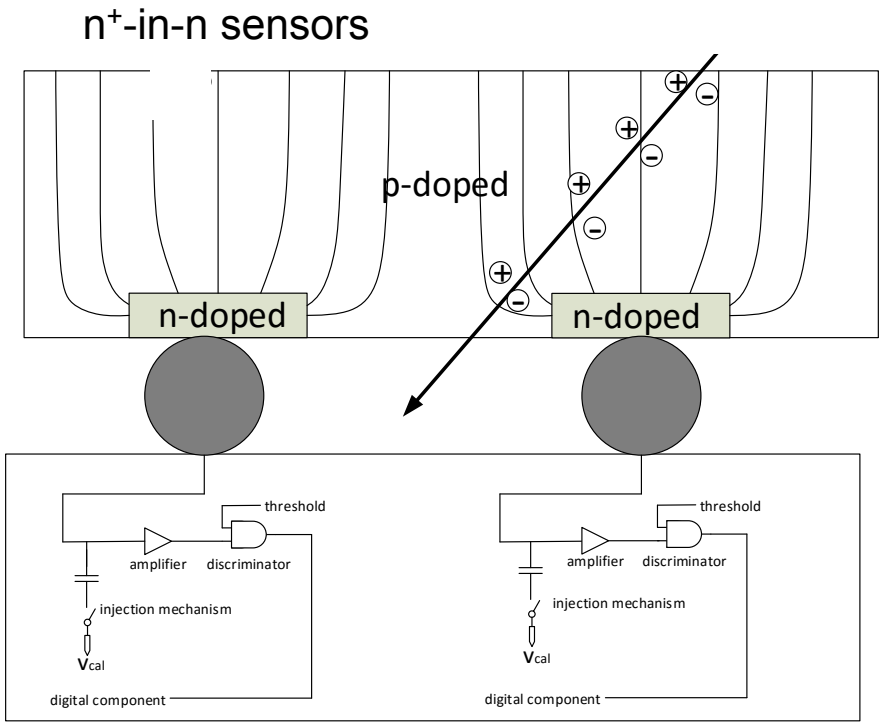
Inner Detector:

- innermost part of ATLAS
- situated in a 2T solenoidal magnetic field
- barrel and disk regions
  - hermetically coverage

Components:

- Pixel Detector (PD/PIXEL)
  - 4 space-points
- Strip Detector (SCT)
  - 4 space-points
- Transition Radiation Tracker (TRT)
  - 36 space-points

Silicon hybrid pixel detectors

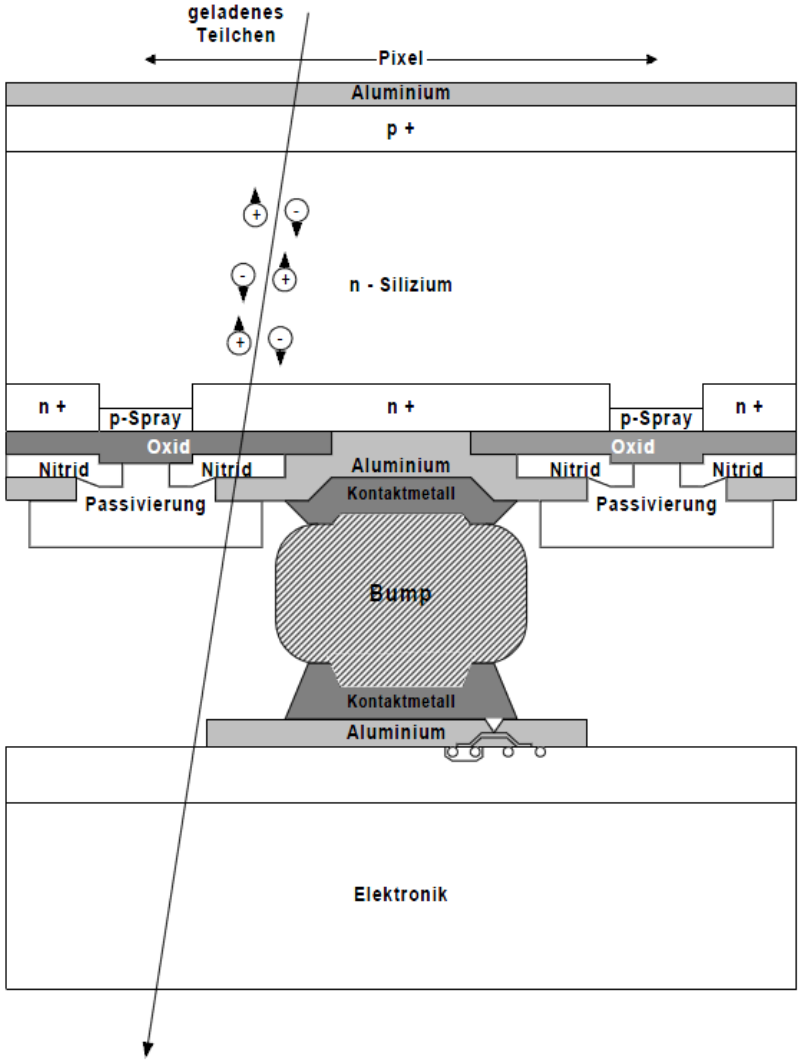


Detection mechanism:

- Apply high voltage in reverse direction to deplete the silicon bulk
- Charged particles generate electron/hole pairs
- Electrons move towards the n^+ electrode, holes towards backside inducing a signal
- Signal is read-out via an attached front-end chip

→ hybrid pixel detector

Silicon hybrid pixel detectors

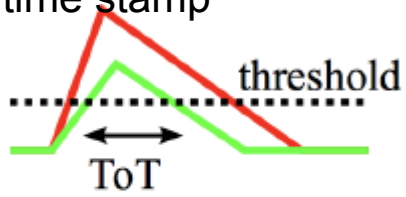


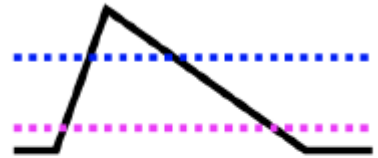
- Hybrid pixel detectors are composed of sensor and read-out chip connected by solder bump-bonds
  - Monolithic pixel detectors combine read-out and sensor in one chip→ evaluated for HL-LHC
- Hybrid approach is powerful in terms of speed and radiation tolerance

ATLAS chips working principle

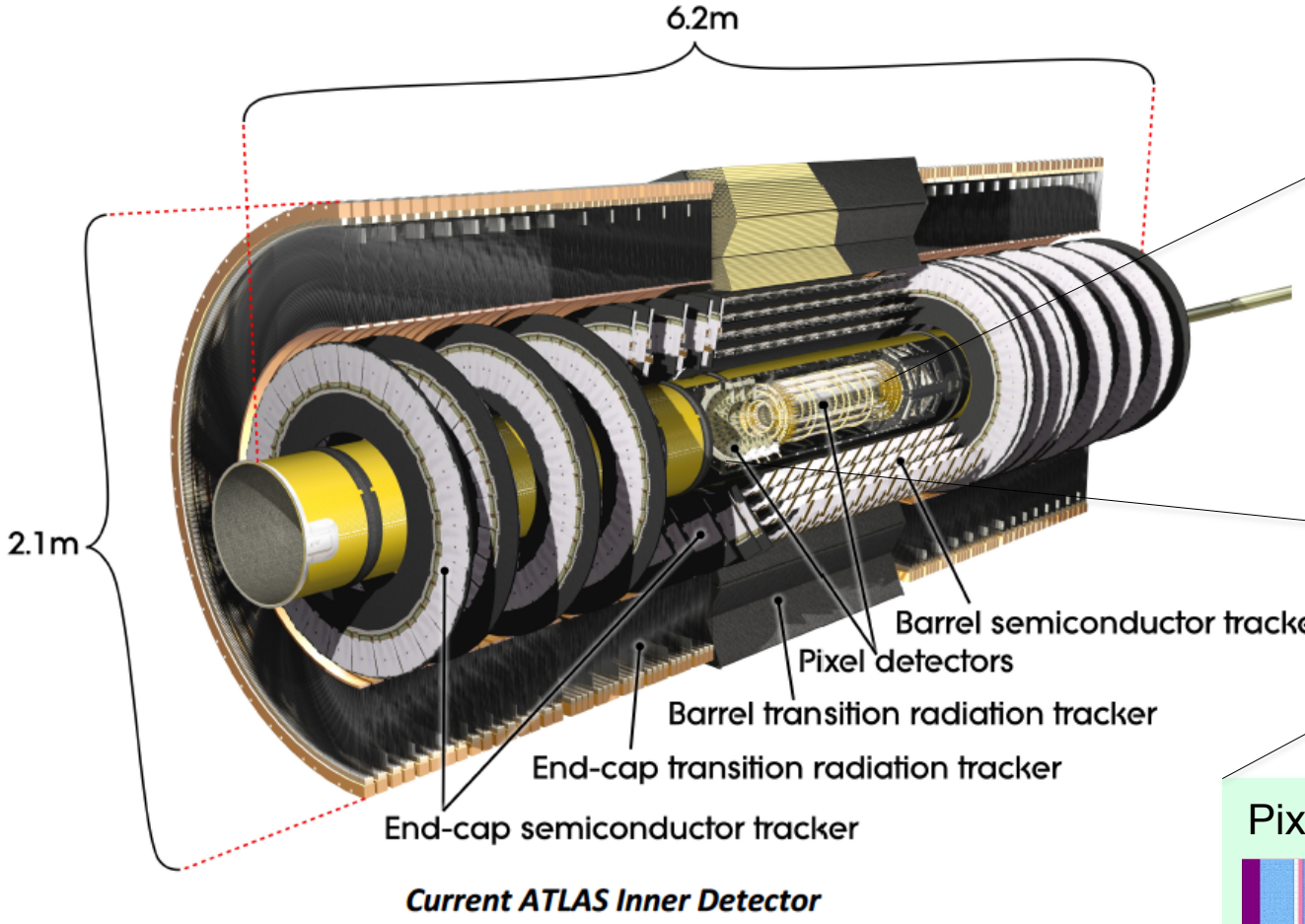
Analogue block: sensor charge signal is amplified and compared to a programmable threshold by a discriminator.

Digital part: calculates and transfers the the 'time over threshold' to chip periphery, together with a hit pixel address and time stamp

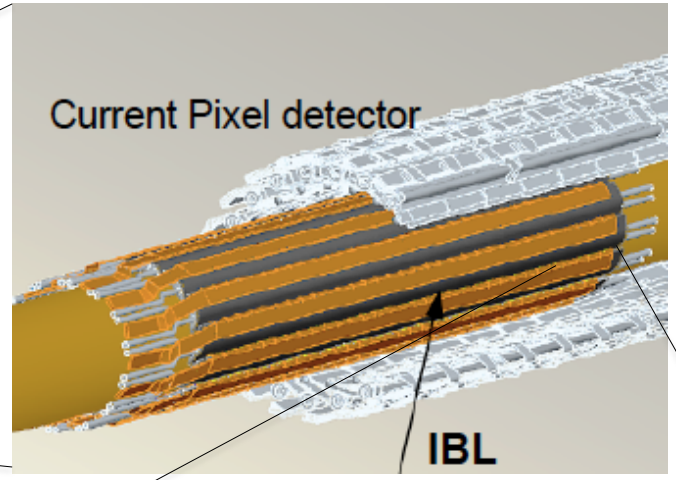




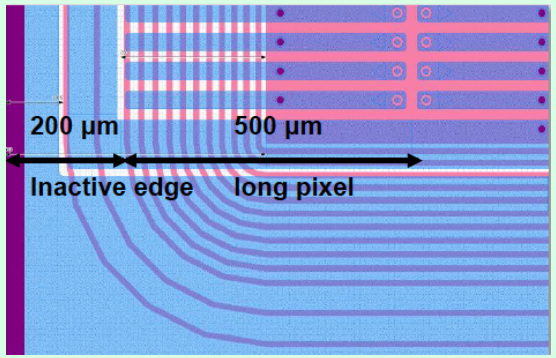
First upgrade of the present ATLAS pixel detector

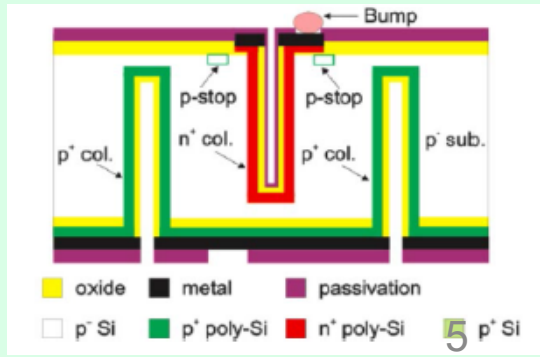


Current ATLAS Inner Detector



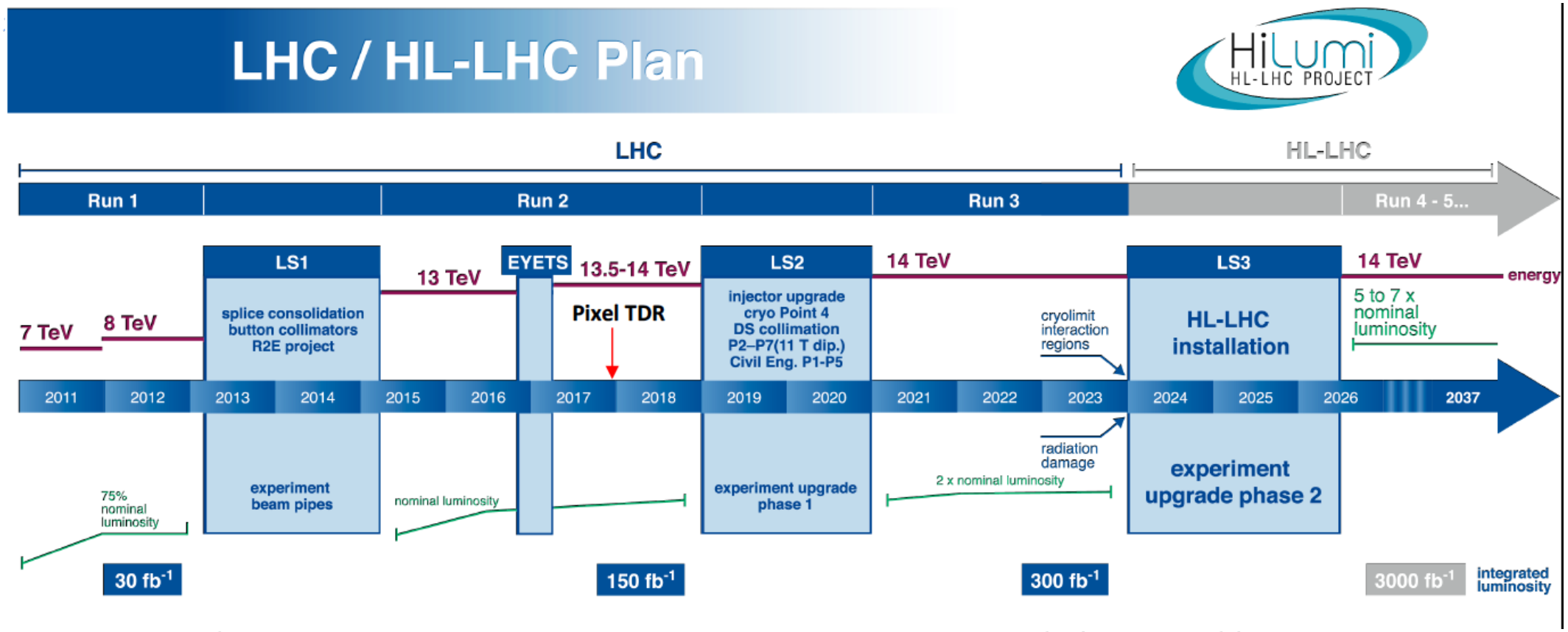
Pixel cell size in IBL: 50x250 μm²





- New sensor technologies for IBL:
  - 200 μm thin planar sensors with reduced inactive edges
  - 3D sensors operating for the first time in HEP!

The High Luminosity LHC: Roadmap

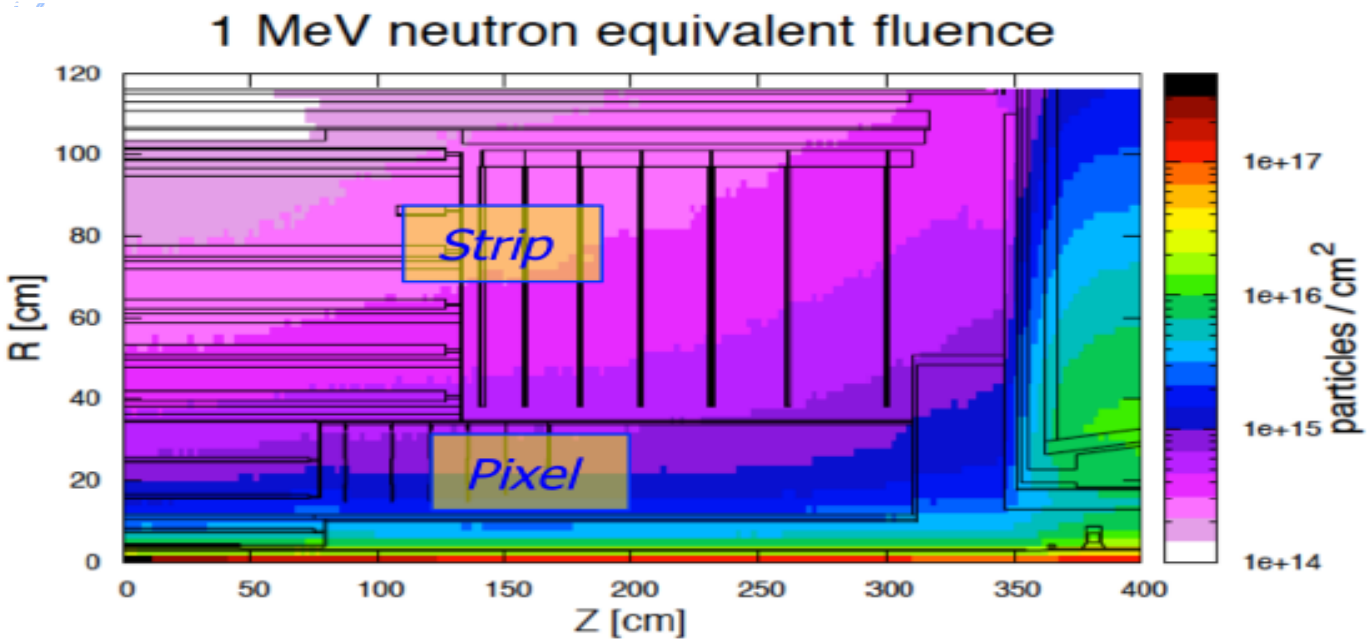


The LHC will be upgraded to the High Luminosity-LHC (HL-LHC) to produce up to 4000 fb^{-1} of integrated luminosity until 2035

– benefits precision measurements in many physics channels

– allows studies of rare processes

ITk Pixel requirements

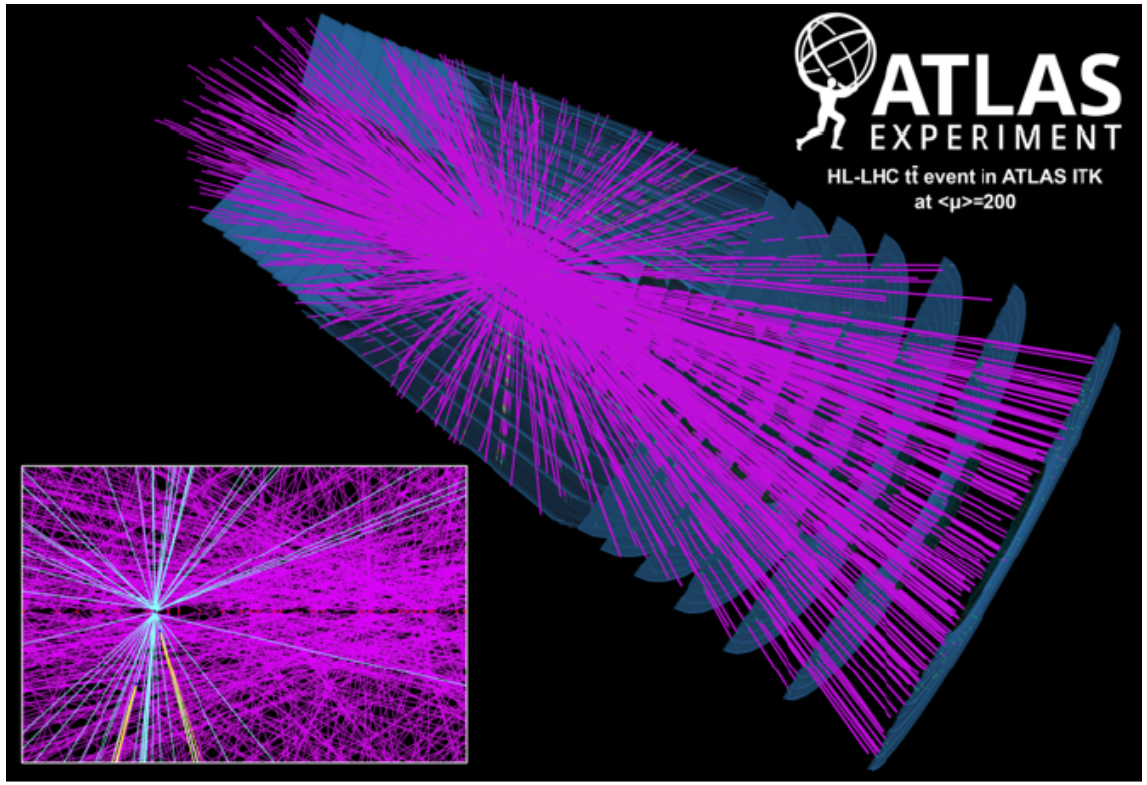


Sustain / improve excellent performance of ATLAS Run2 also in HL-LHC environment

Radiation environment

- Ultimate integrated luminosity considered ~ 4000 fb^{-1}
  - Non-ionizing energy loss (NIEL) in the innermost layer: $\Phi_{eq} \approx \sim(2.5\text{-}3)\times10^{16}$ cm^{-2}
- At least one replacement needed for the two innermost pixel layers
- Radiation hard sensors and new read-out electronics

ITk Pixel requirements



Luminosity of up to 7.5×10^{34} $cm^{-2}s^{-1}$,

up to 200 interactions / 25 ns bunch crossing

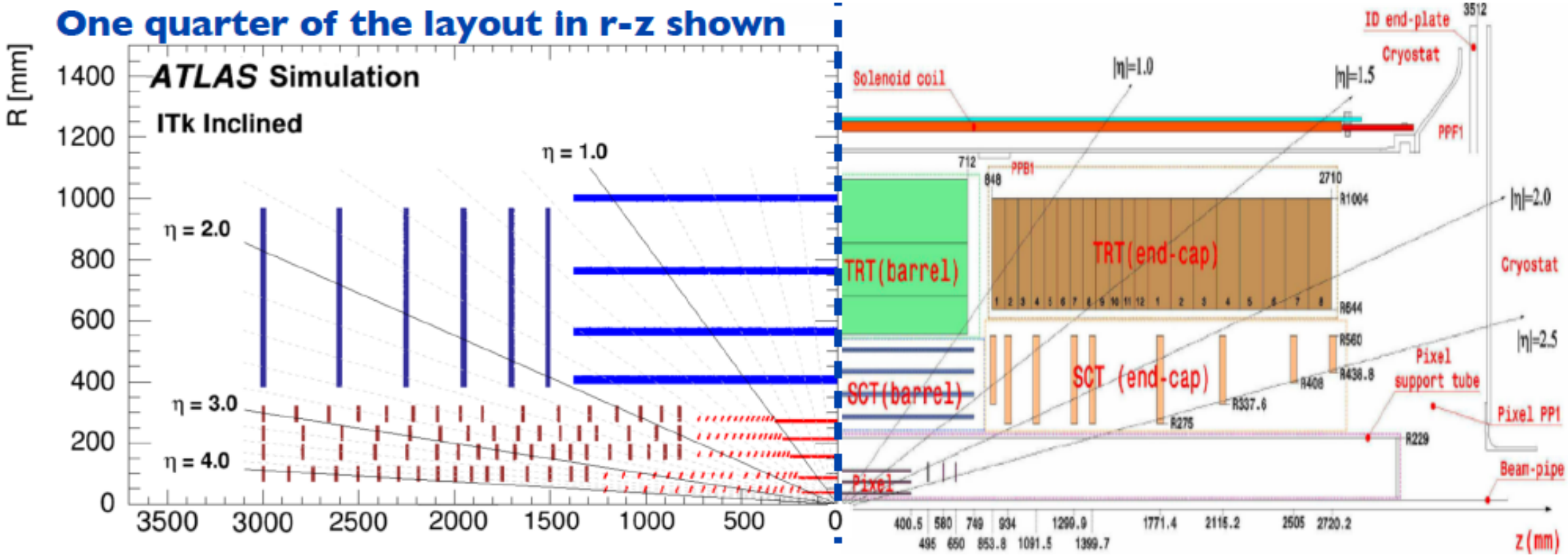
→ Higher track density

- ID-TRT would have 100% occupancy at HL-LHC
- ID readout links would be saturated at HL-LHC

- A replacement of the present detector is by far not enough!

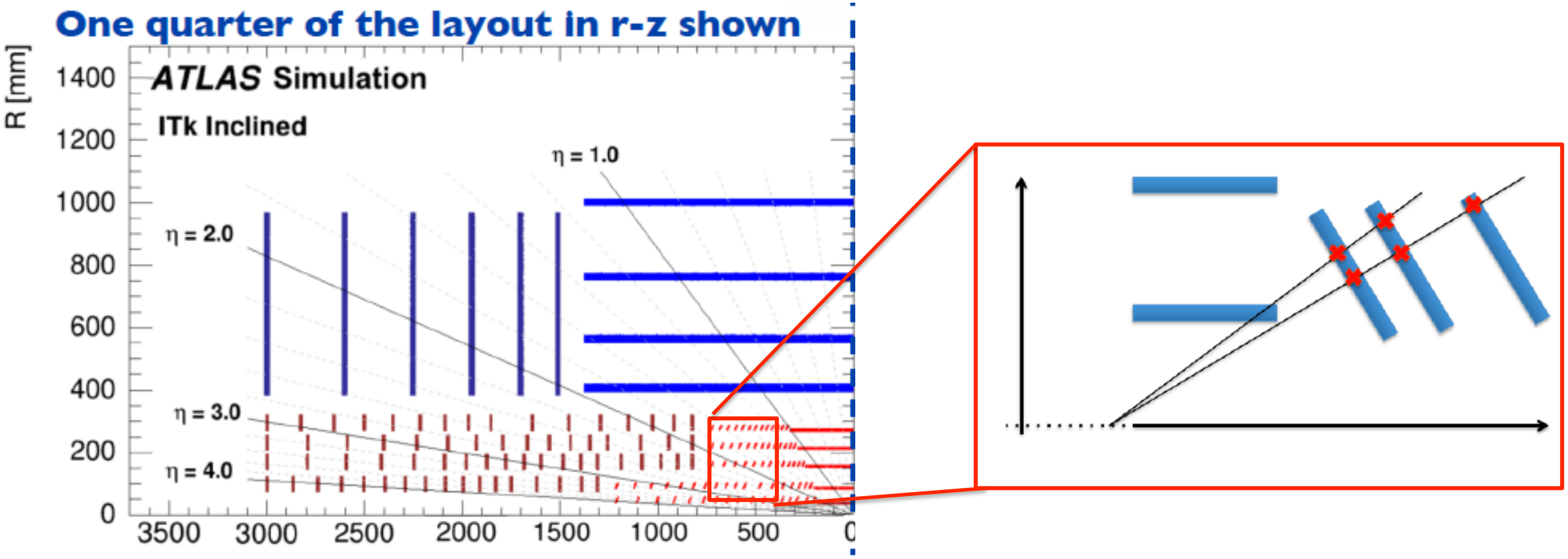
- Goal: Maintain occupancy at ≈ % (strips) and ‰ level (pixel), and increase spatial resolution
  - Higher granularity to keep occupancies low: 50x50 or 25x100 μm^2 pixels
  - Larger readout bandwidth capabilities

ITk Pixel layout



- Innermost central layer structure needs to cover full pseudo-rapidity range down to $|\eta|=4$
- 5 pixel layers → robustness against missing single hit

ITk Pixel inclined layout

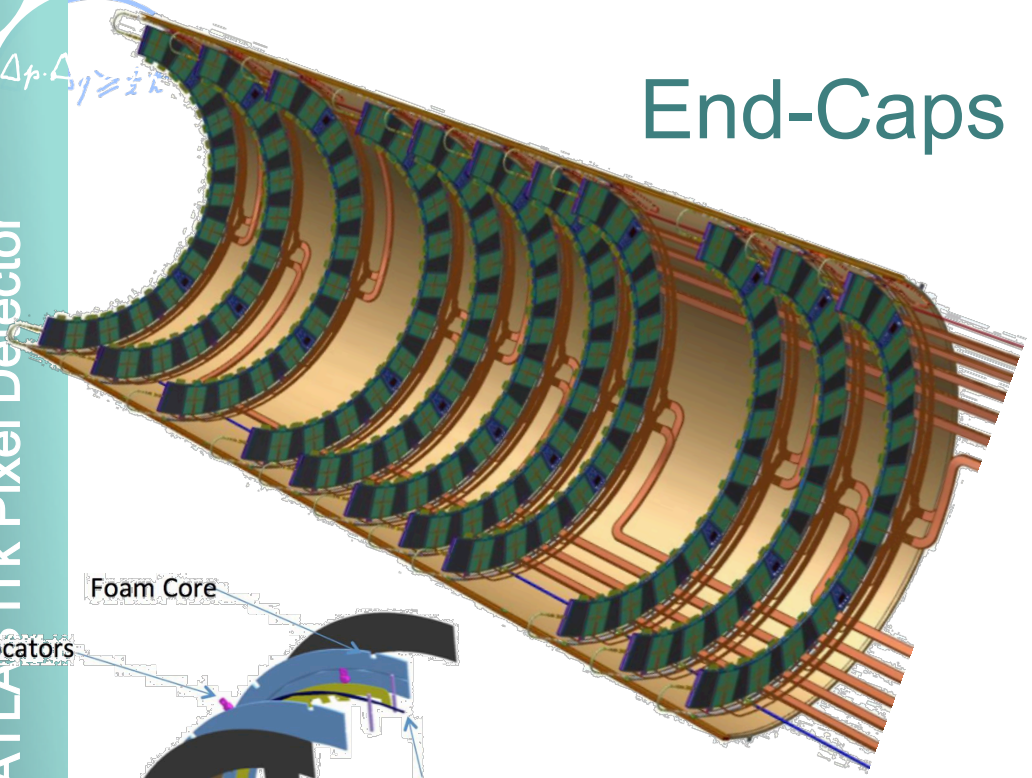


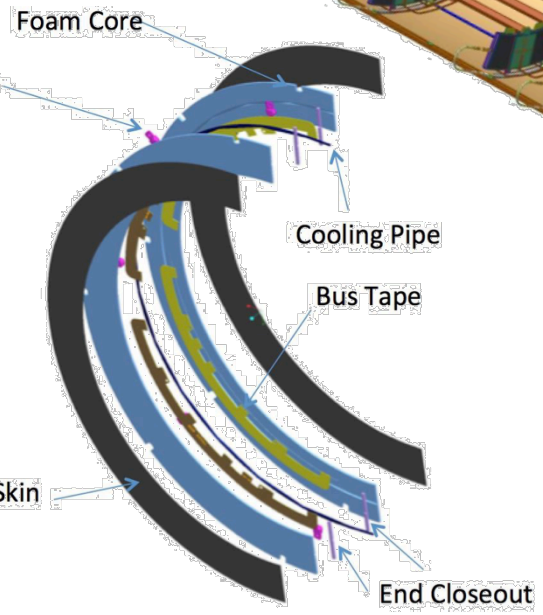
Inclined layout

- More hits per layer for one track
- Barrel and end-cap transition moved out in z → reduced material induced performance degradation
- Minimization of amount of silicon needed and of data rates

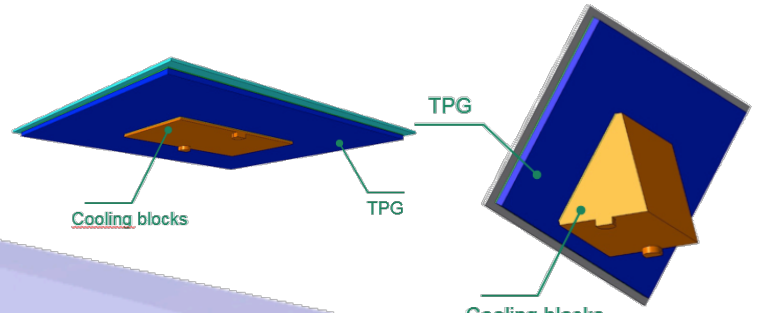
Local Supports

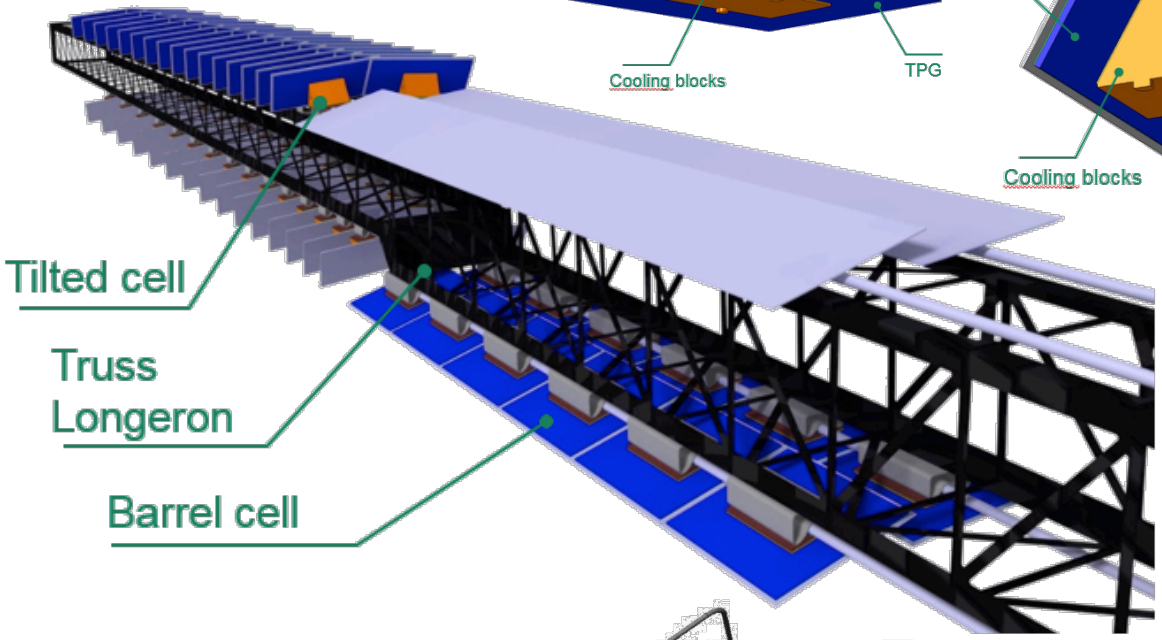
End-Caps



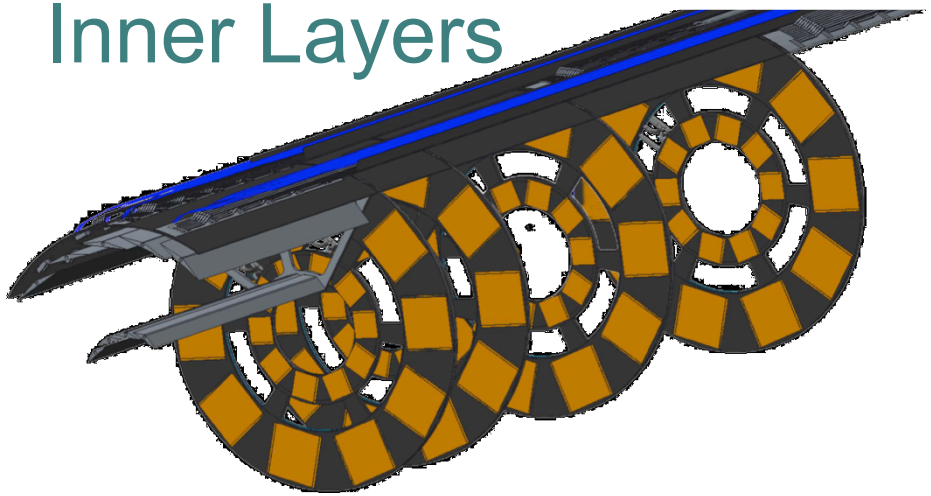


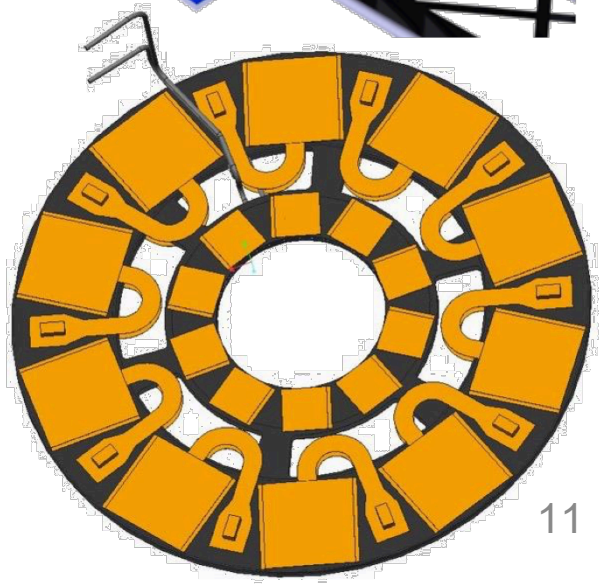
Outer Barrel



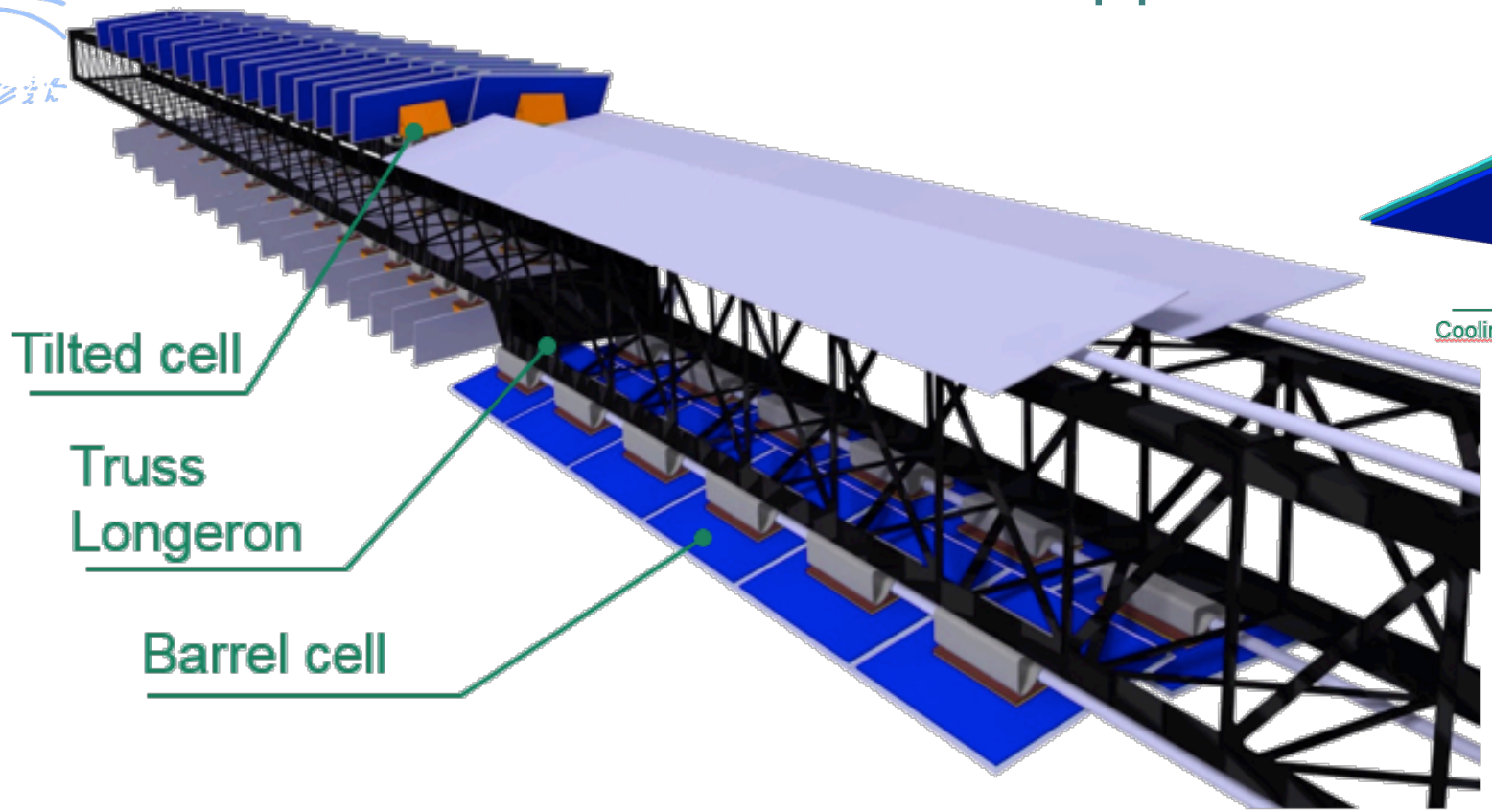


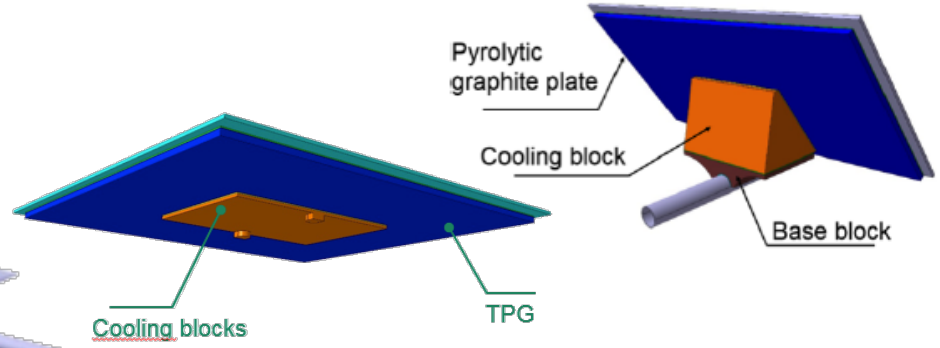
Inner Layers





Local Supports in the Barrel





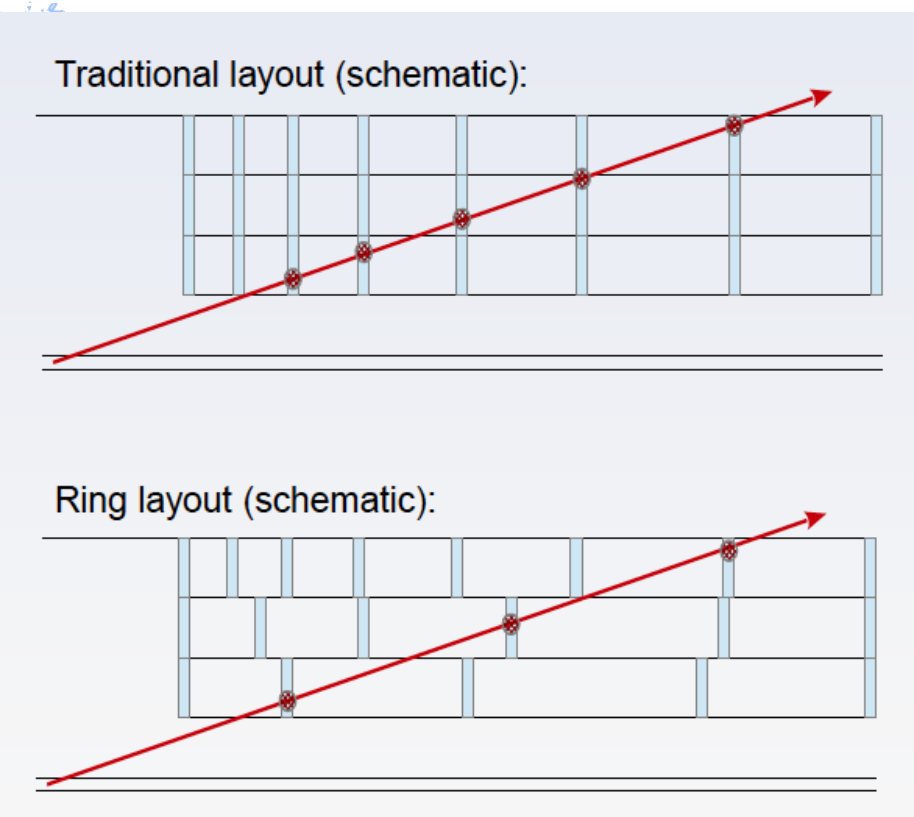
Pixel modules supported on longeron like structure:

$|\eta|<1.2$ Modules installed flat

$|\eta|>1.2$ Modules installed inclined, 56^{o} with respect to beam direction

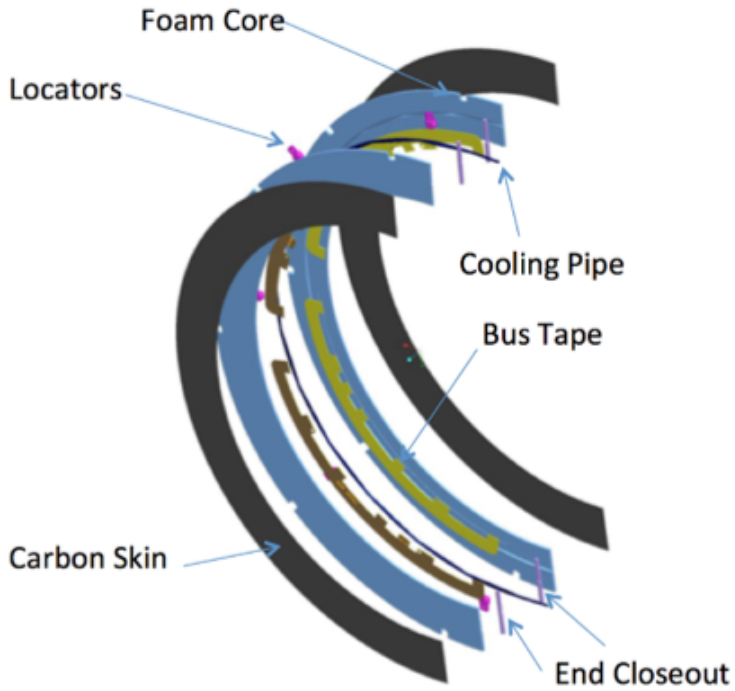
- Intense prototyping program :
- Validation thermal and mechanical performance of local support concepts
- Qualify loading procedures
- Electrical tests for serial powering, read-out systems and multi-module operations

Local Supports in the Pixel End-caps



Pixel rings cover the high η region

- The number of rings and positions in z are optimised for hermetic coverage of tracks for each pixel layer, separately
- The pixels rings gives flexibility in location and number without large engineering changes

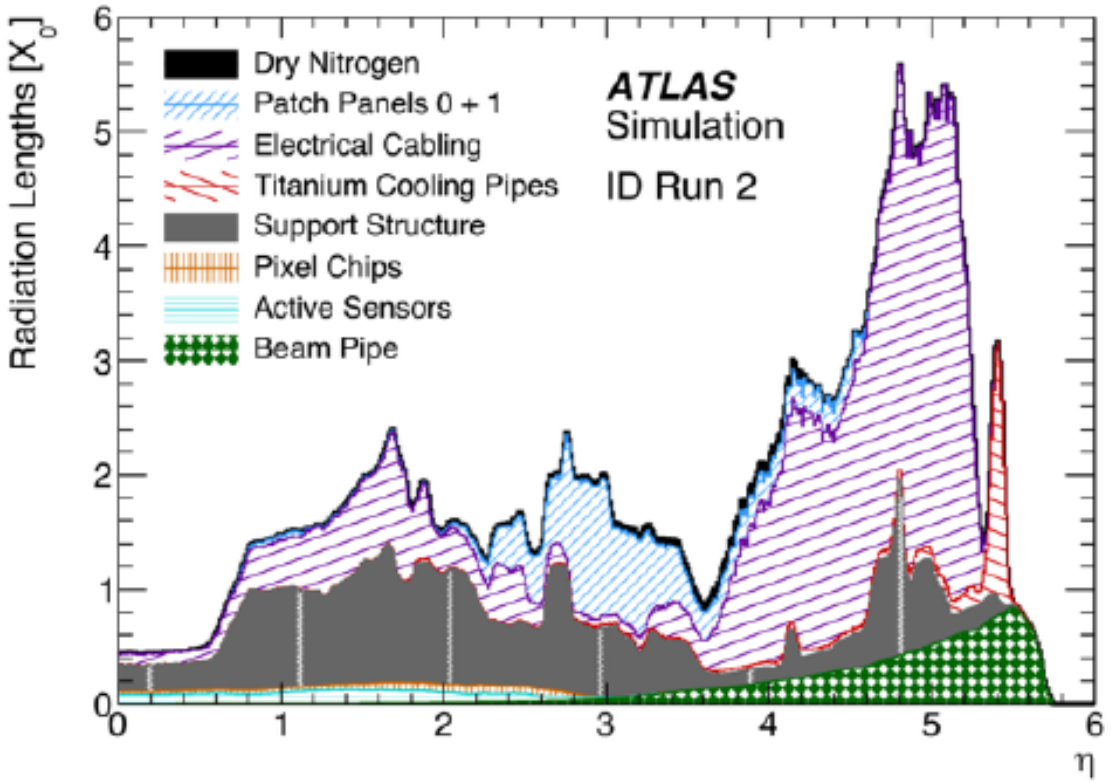


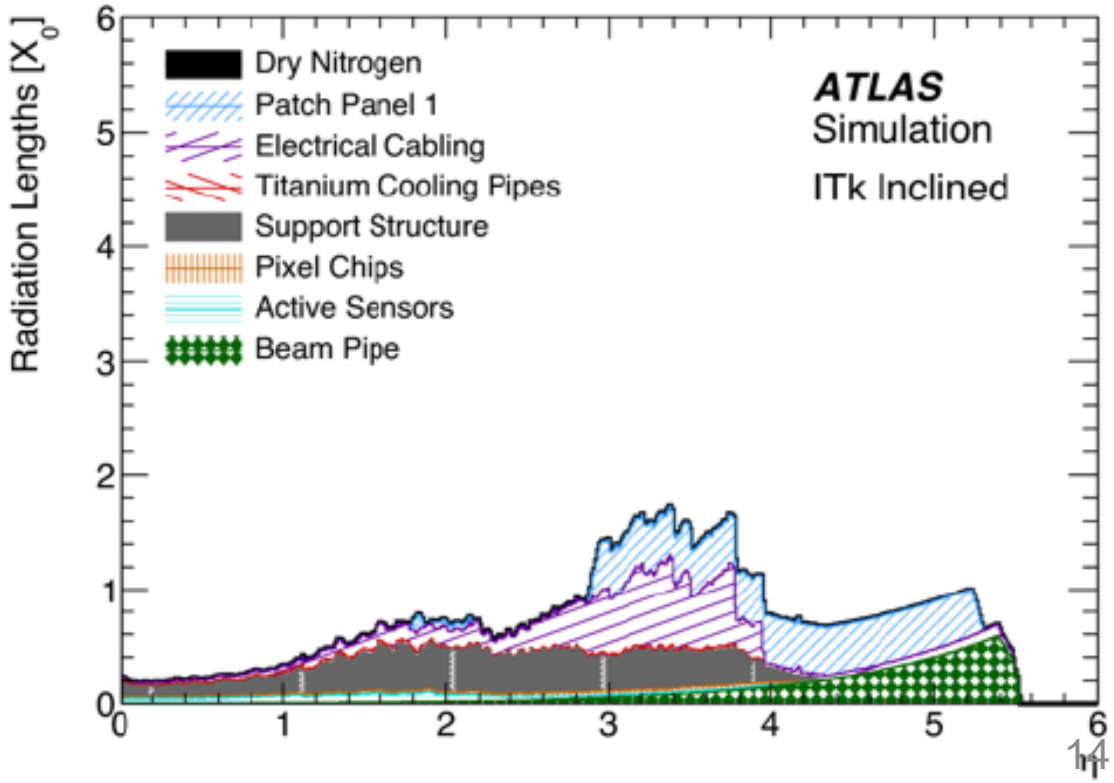
- Services routed on support structures
- Designed to minimize mass of ring system and to improve tracking at high eta

Material budget

After optimisation of tracker layout, innovations on delivering electrical power to sensors, and support mechanics, a significant reduction in the total radiation length

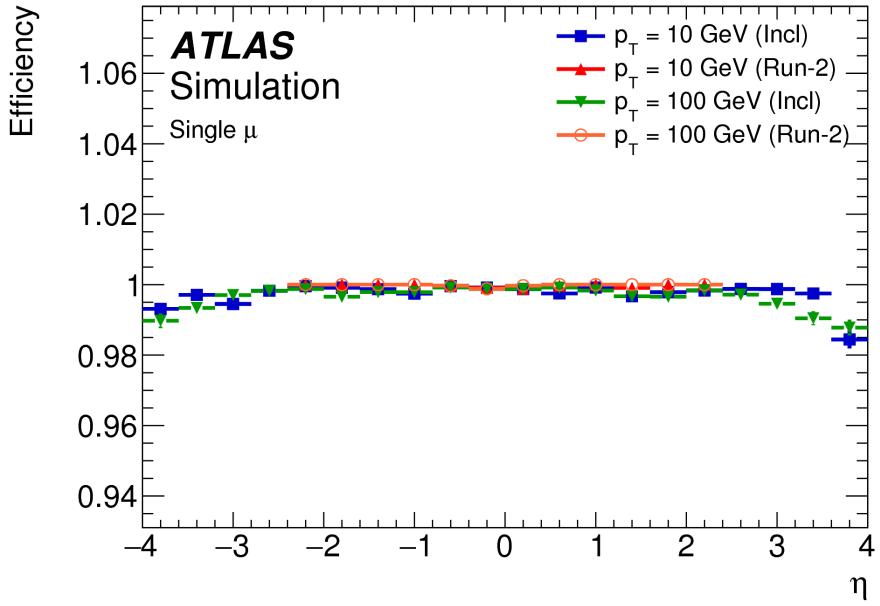
- ITk silicon surface area (165m^2) is 2.6 times large than the current ID, but the maximum radiation length reduced from 5.5X_0 to 2X_0

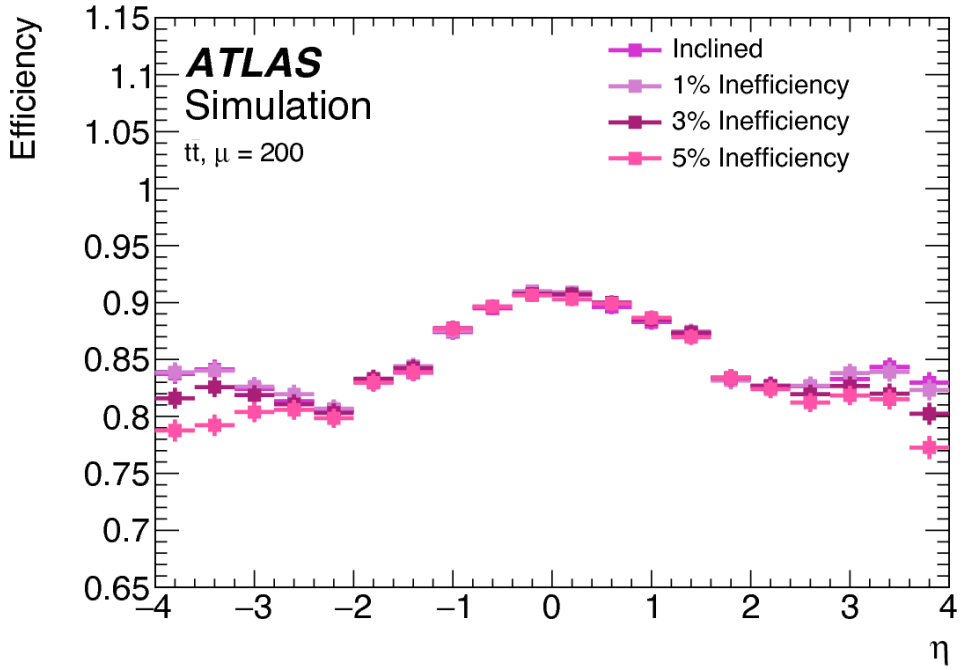


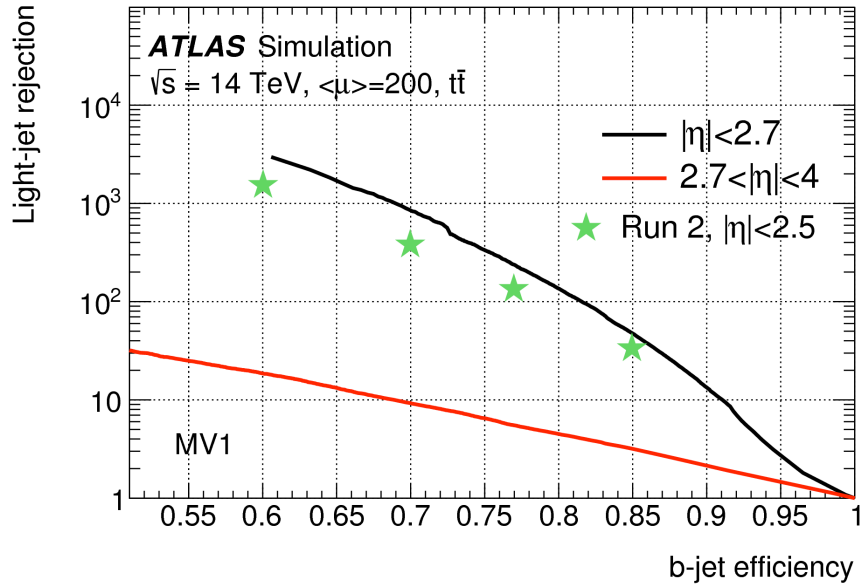


Examples of performance with ITk

- Particle identification performance comparable to or better than in Run-2, even with μ~200, for ITk Inclined layout
- Shows that our reconstruction algorithms are performing well in this challenging environment, and correct choices have been made in terms of optimal layout geometry



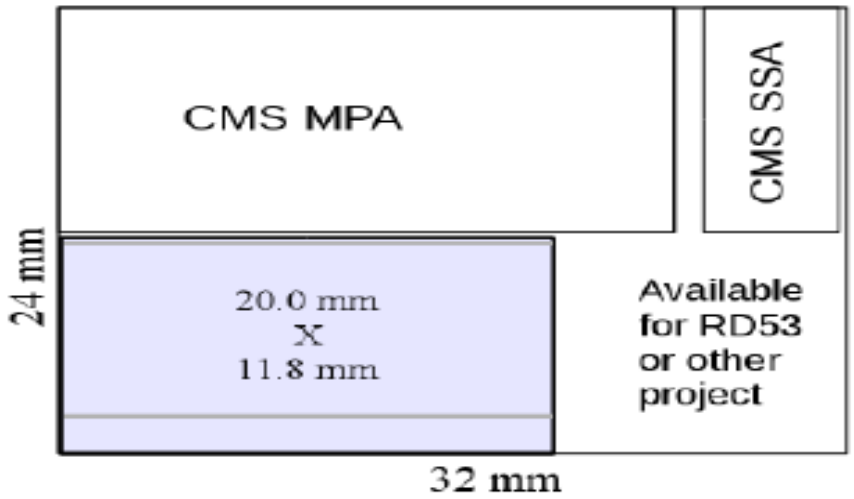




Read-out chip and sensor technologies

The RD53 read-out chip for the ITk pixels

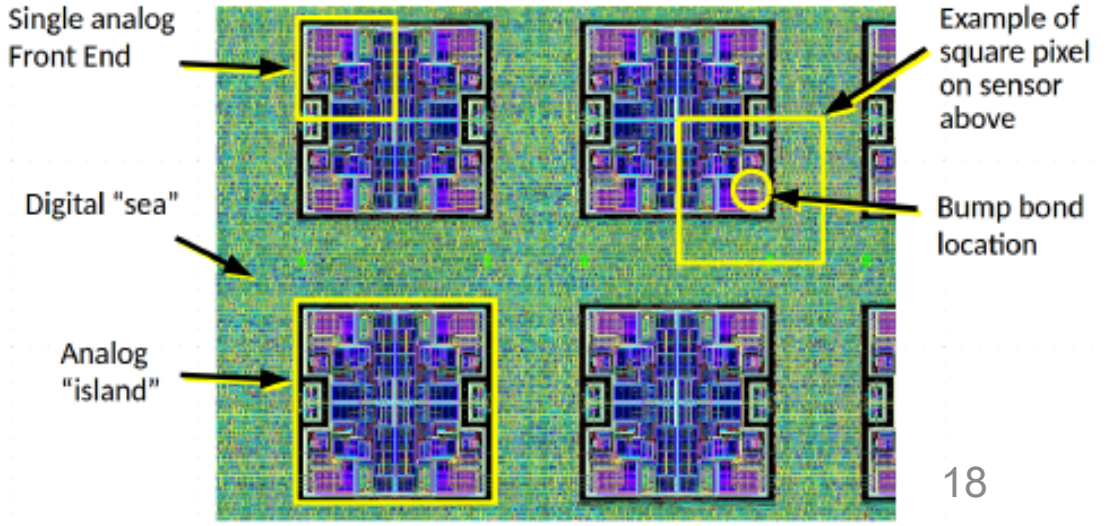
- Joint effort between CMS-ATLAS communities to deliver a large scale front-end
- ASIC prototype for Pixel-Phase 2 detectors.
- Full scale prototype RD53A: first wafers ready and are now being tested
  - 65nm CMOS design
  - 50 μm x 50 μm grid → drives the sensor design



- 20x11.8 mm² → 400 columns x 192 rows of 50x50 μm² pixels
- Final ATLAS Pixel chip size → 400 columns x 384 rows → 10% larger than the FE-I4 (IBL) chip

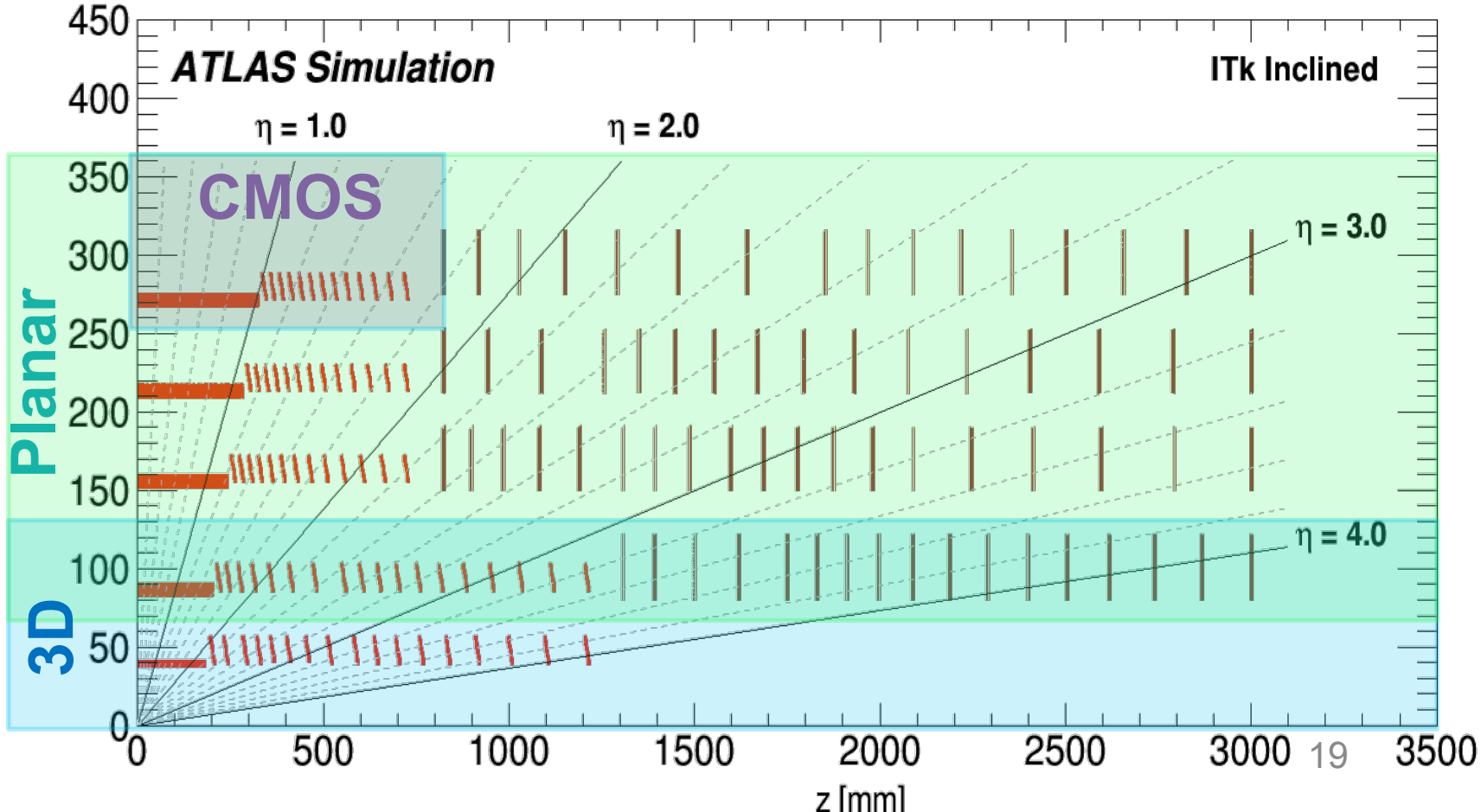
The ATLAS read-out chip for the ITk pixels

- Radiation hardness 500 Mrad: only lower limit, it will be measured on the full scale prototype
- In-time threshold <1200 e
- Serial output lines at 1.28, 2.56, 5.12 Gb/s, depending on the module location
- Support of serial powering with implementation of regulators
- Reduce data volume by grouping together group of pixels (2x2 or 1x4, matching cluster shape)



Sensor technologies for ITk

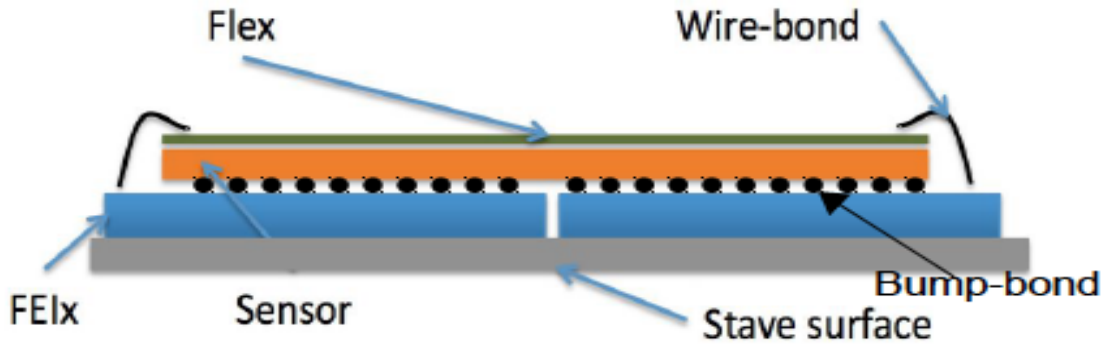
- 3D sensors – radiation hard
- Planar - reduced cost
- CMOS - lower material budget, power consumption and cost

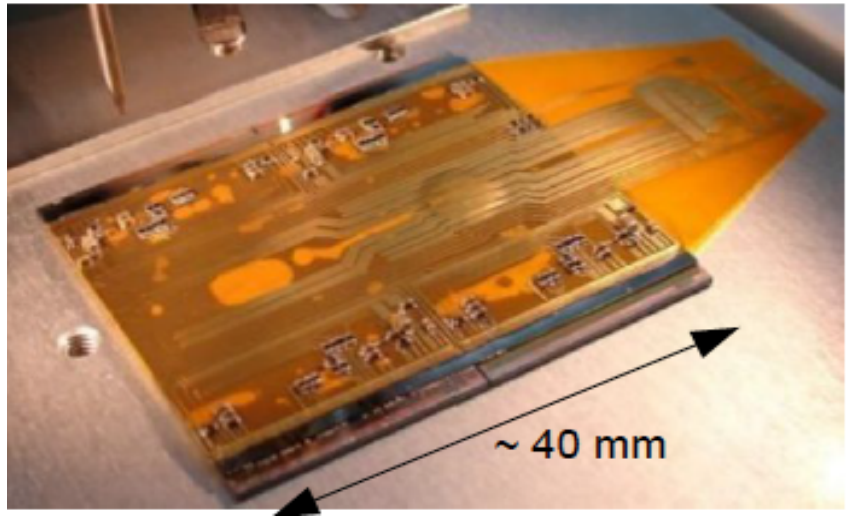


Hybrid pixel module concept

- Basic building block is the pixel module:
- Bare module assembly consisting of sensor and FE chip
- Flex hybrid for interconnection of data, LV, HV

Around 10k modules needed for ITk pixel system

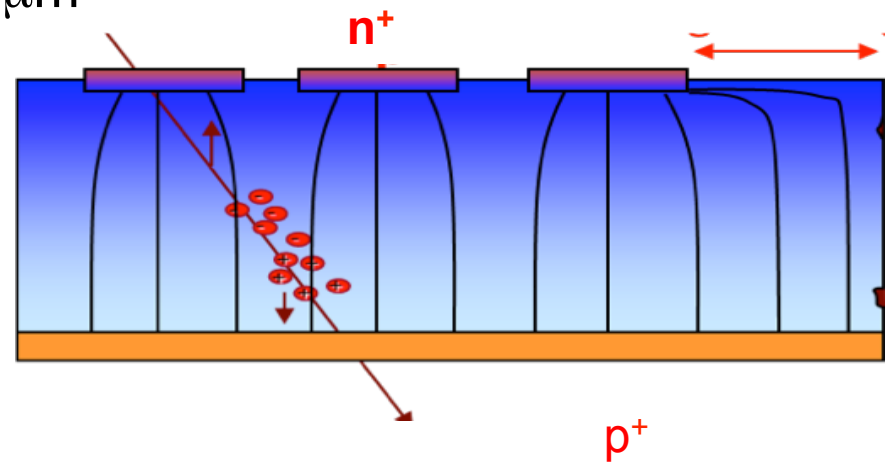




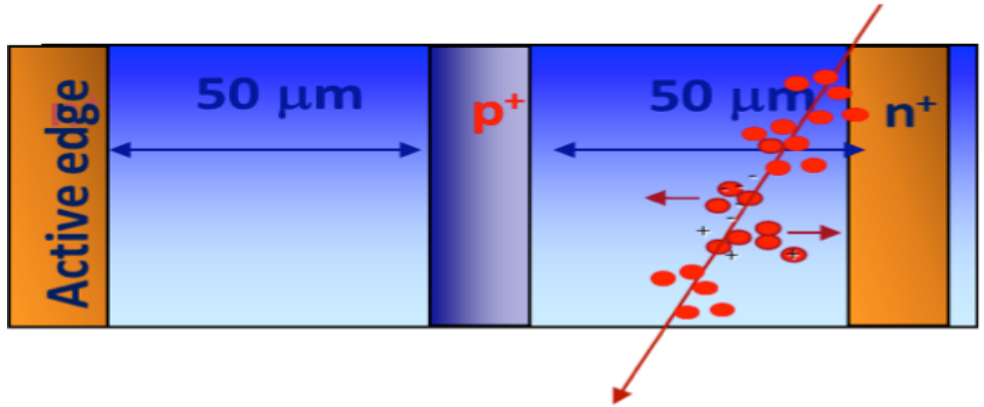
- Intense quad pixel module prototyping with 4 FE-I4 chips
  - Bump-bond
  - Assembly of bare module and readout flex advanced
  - Irradiation study of glues and composite materials started

Comparison between the sensor baseline technologies

Thin planar sensors – 100-150 μm



3D sensors – 150 μm



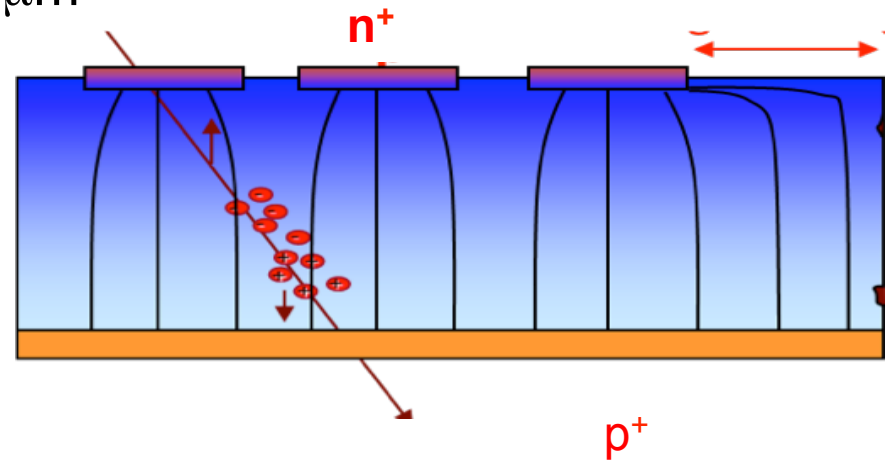
Smaller distance between the electrodes leads to higher radiation tolerance:

→ Higher electric field for the same applied Voltage → saturation of the drift velocity

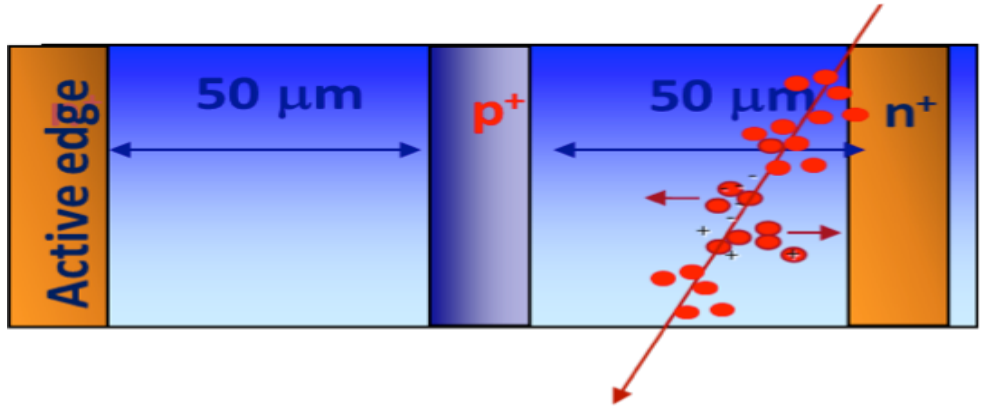
→ Smaller drift time and reduced effect of the trapping on the charge carriers

Comparison between the sensor baseline technologies

Thin planar sensors – 100-150 μm



3D sensors – 150 μm



Thin planar sensors (n-in-p):

- Lower power dissipation than thicker planar sensors
- Simple production process than 3D

Drawbacks:

- Smaller initial signal (76 e^-/μm)

3D sensors:

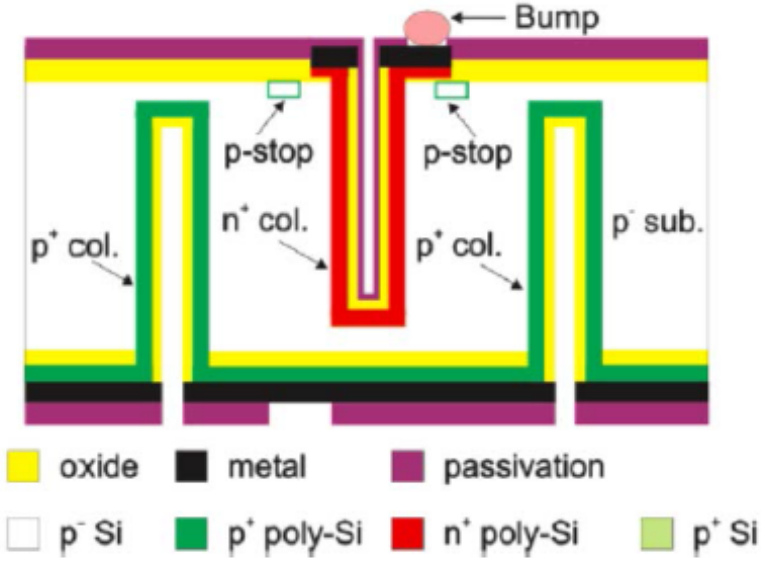
- Low power dissipation thanks to reduced operational V_{bias}

Drawbacks:

- Higher capacitance
- Lower yield, higher cost

Different 3D technologies

- Double sided (available on 4” at CNM)
- IBL/AFP proven technology
- No handling wafer needed → thickness limited to ≥200 μm

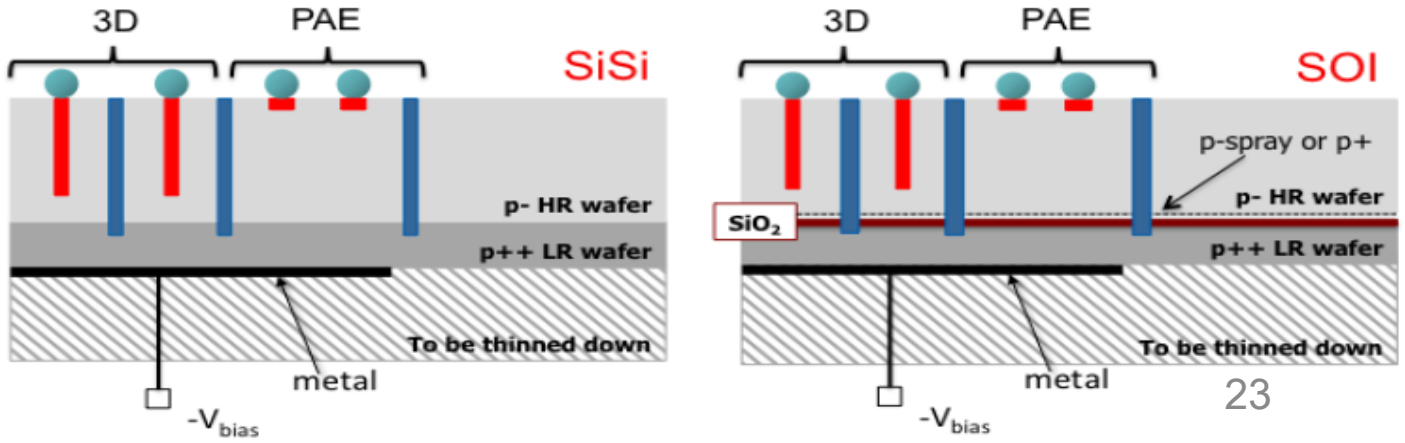


Double-sided

G. Pellegrini, CNM

Single-sided process
- “Thin” active layer (130 μm): Si-Si or SOI
- Ohmic columns depth > active layer
- Junction columns depth < active layer
- Column diameter ~ 5 um
- Holes partially filled with poly
- Very slim edge (100 μm)

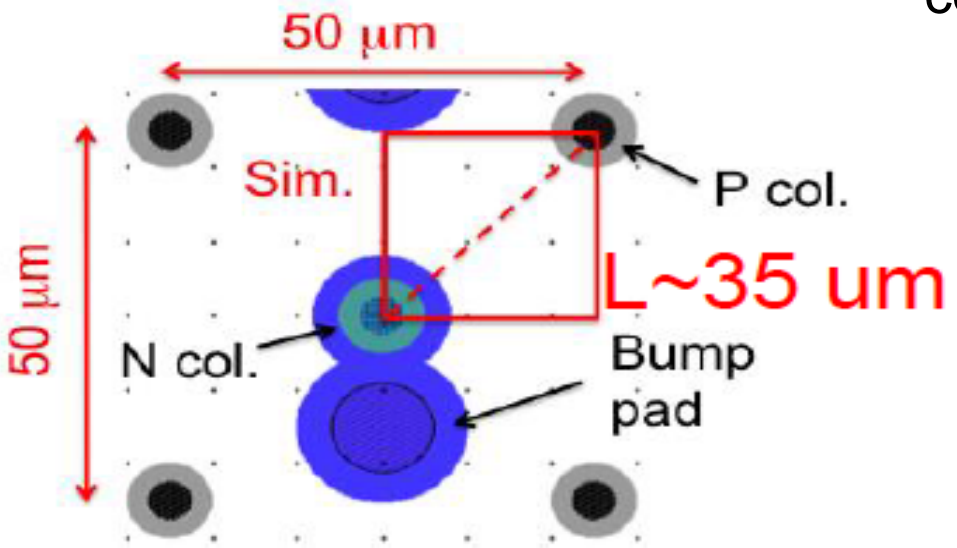
6” wafers at FBK



R. Mendicino, 12th Trento Workshop on Advanced Silicon Radiation Detectors

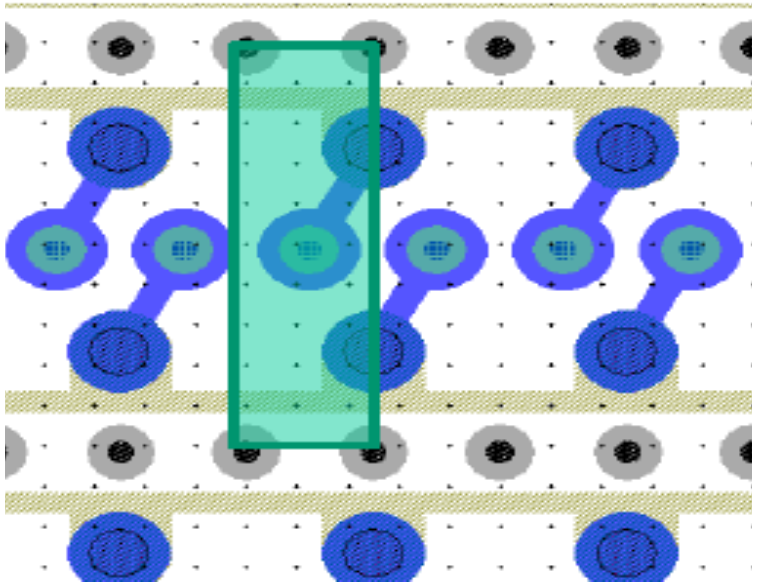
3D sensor design for ITk geometries

50 x 50 (1E)



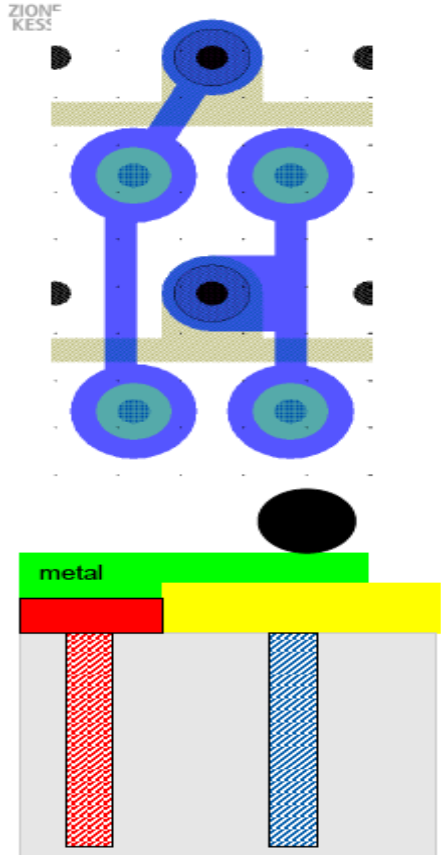
50x50 μm² can be designed with relaxed distances between bump and columns

- 25x100 μm² can be difficult in 2E configuration:
  - Place bumps on ohmic column
  - Study radiation hardness of 1E configuration

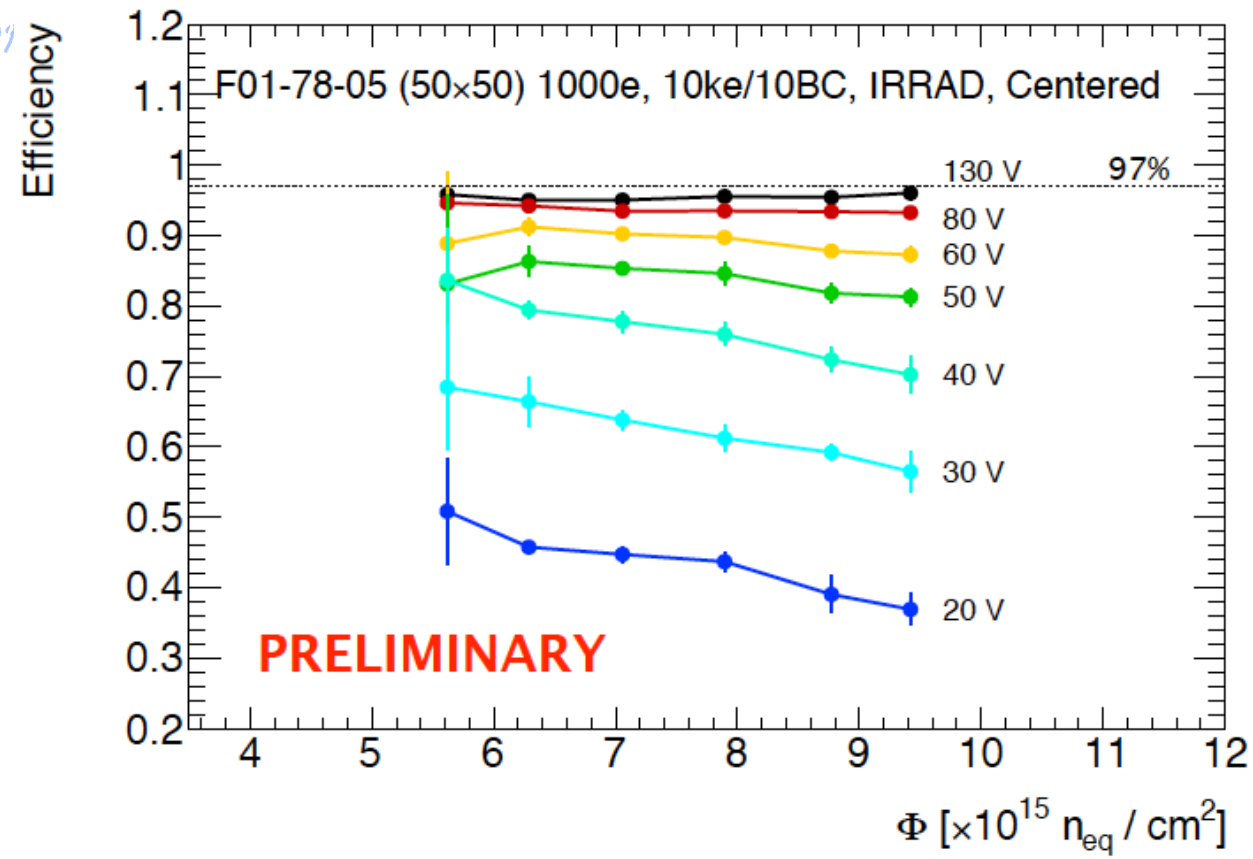


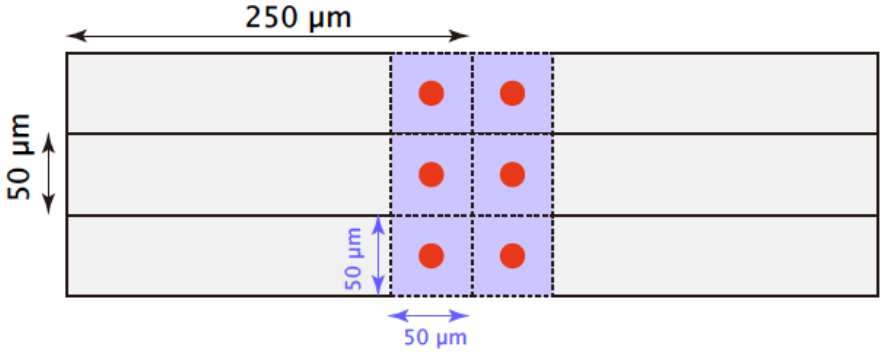
25 x 100 (1E)

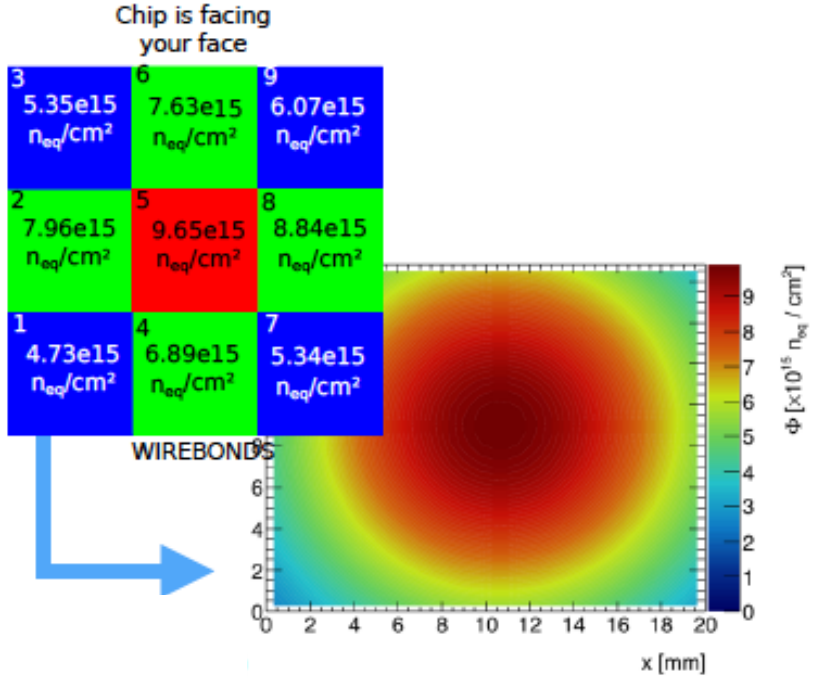
25 x 100 (2E)



Results with 3D sensors at FBK



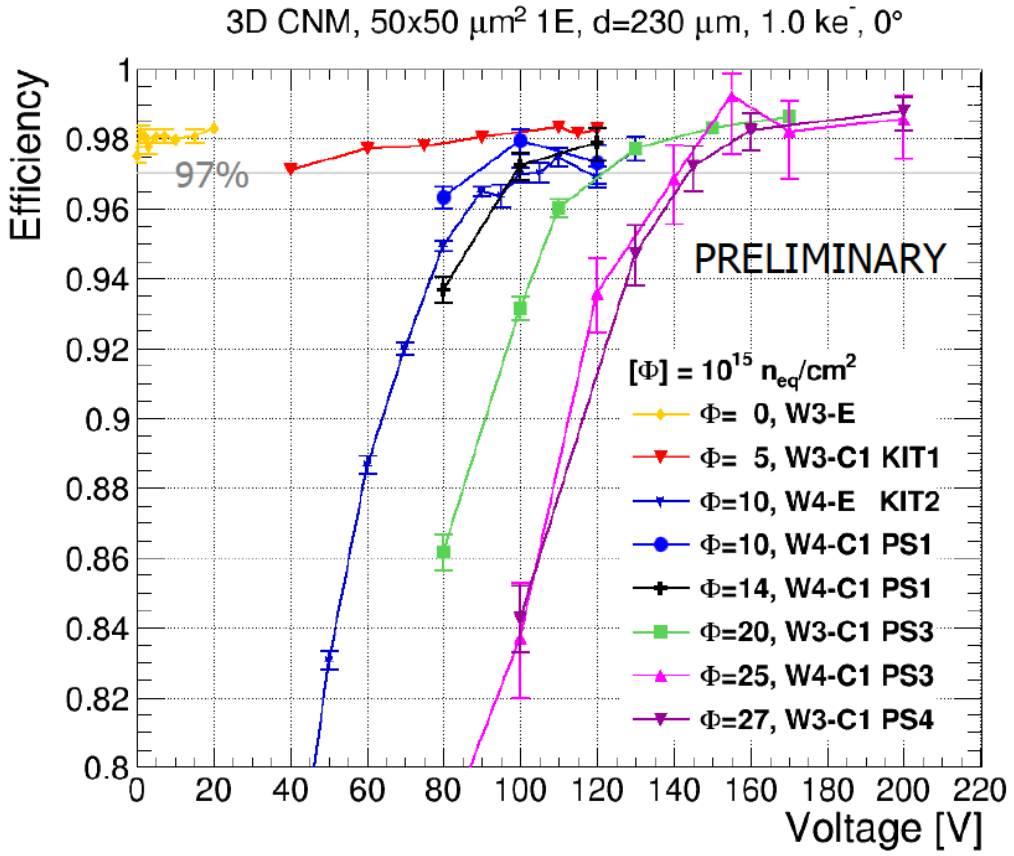


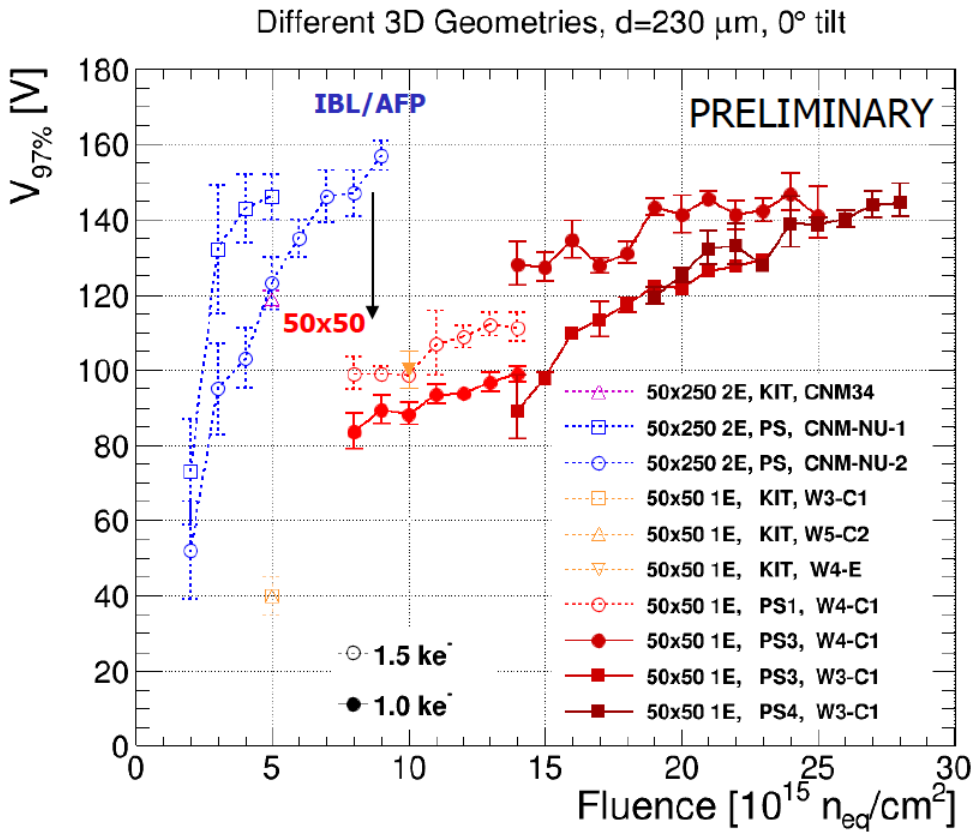


- Hit efficiency of 130 μm thin 3D FBK sensors: FE-I4 modules where a fraction of columns have a modified geometry with RD53 cell sizes
- The efficiency reaches ~95% for HV>80V up to a fluence of 10^{16} n_{eq}/cm^2

H. Oide.
11th Hiroshima Symposium HSTD 11

Results with CNM 3D sensors

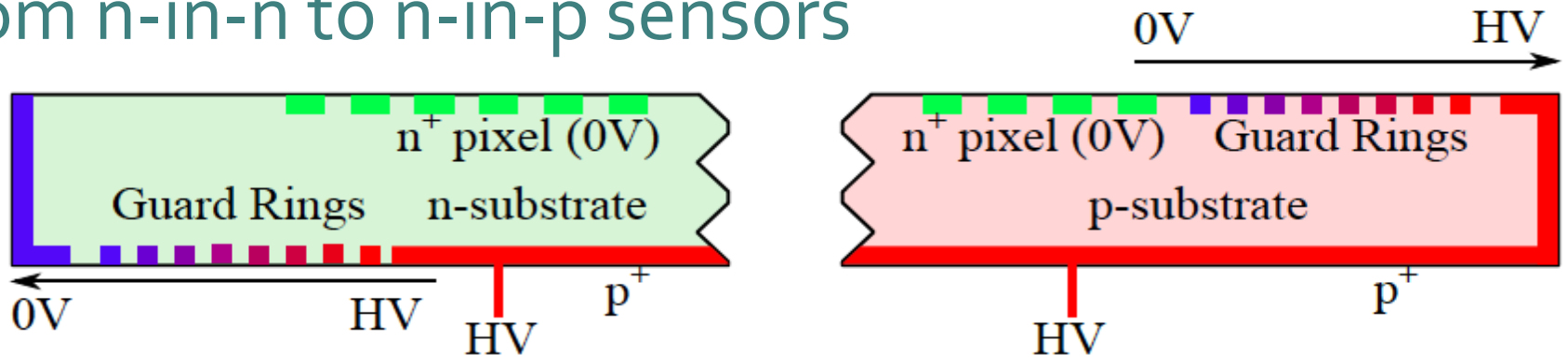




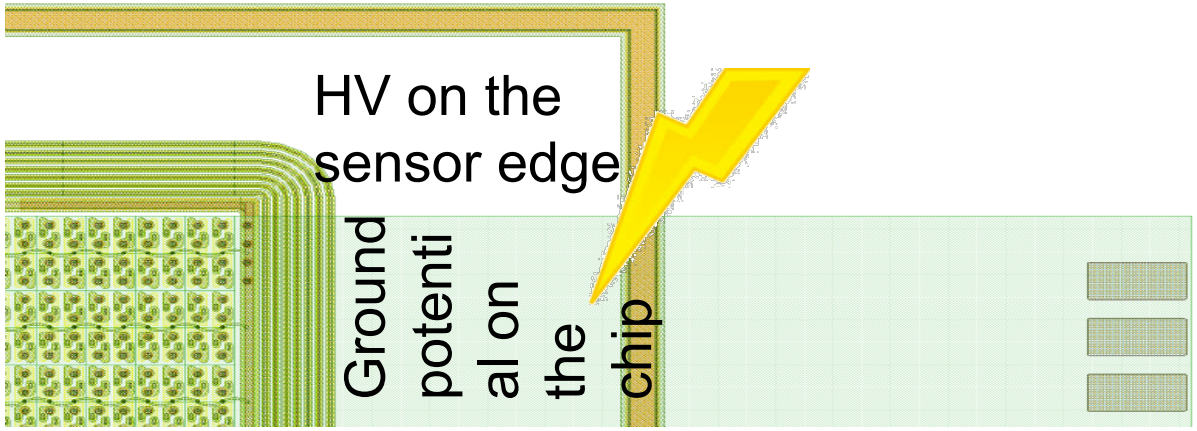
Results with 230 μm thin sensors, double sided technology, non passing through columns

- 98% plateau efficiency @ 1ke threshold reached also at a fluence of 2.7×10^{16} n_{eq}/cm^2
- Lower operational bias voltages for new geometries *J. Lange 11th Hiroshima Symposium HSTD11*

From n-in-n to n-in-p sensors



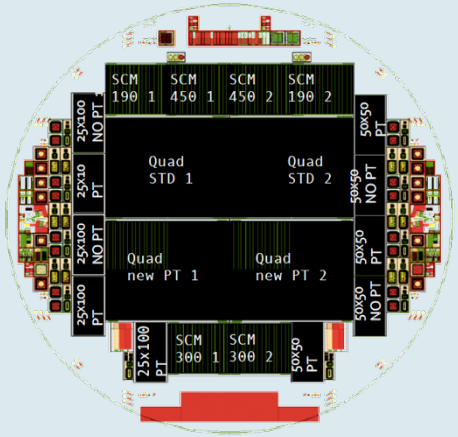
- n-in-p sensors are the baseline choice for ATLAS Pixels L1-L4
- Single sided processing → cost reduction and easier handling
  - Possible drawback
    - Sparks between chip at ground and sensor edges at HV

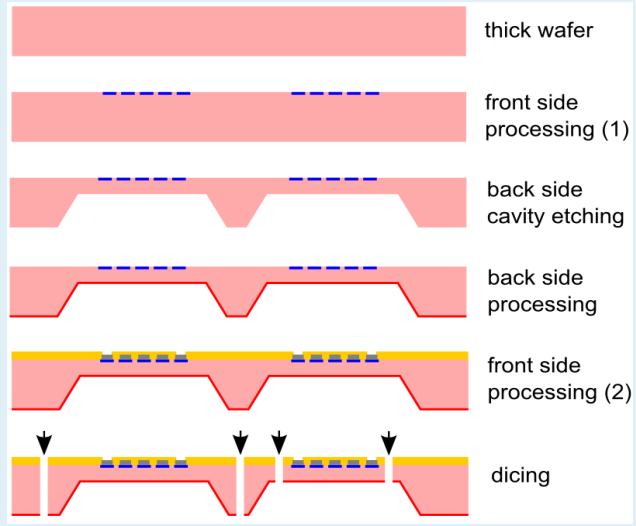


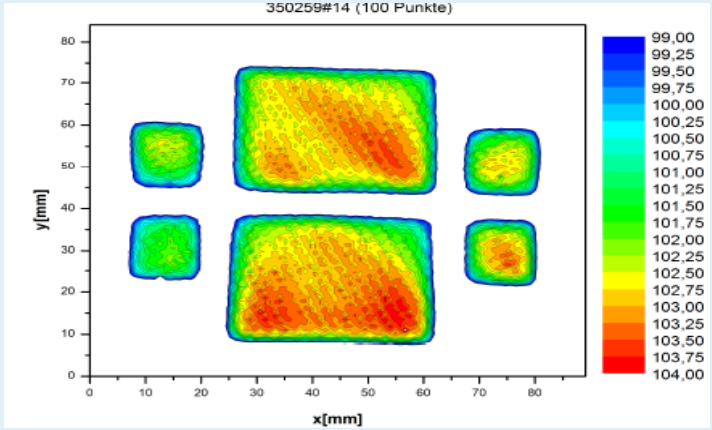
- Sensor coated with BCB have shown HV stability after interconnection up to 900-1000V
- Now MPP is also investigating the feasibility of BCB deposited on chip wafers

Technologies for thin planar pixel sensor productions

- SOI technology as a reliable method to obtain thin sensors
- Different productions with RD53 compatible sensors and sensors for quad module prototyping



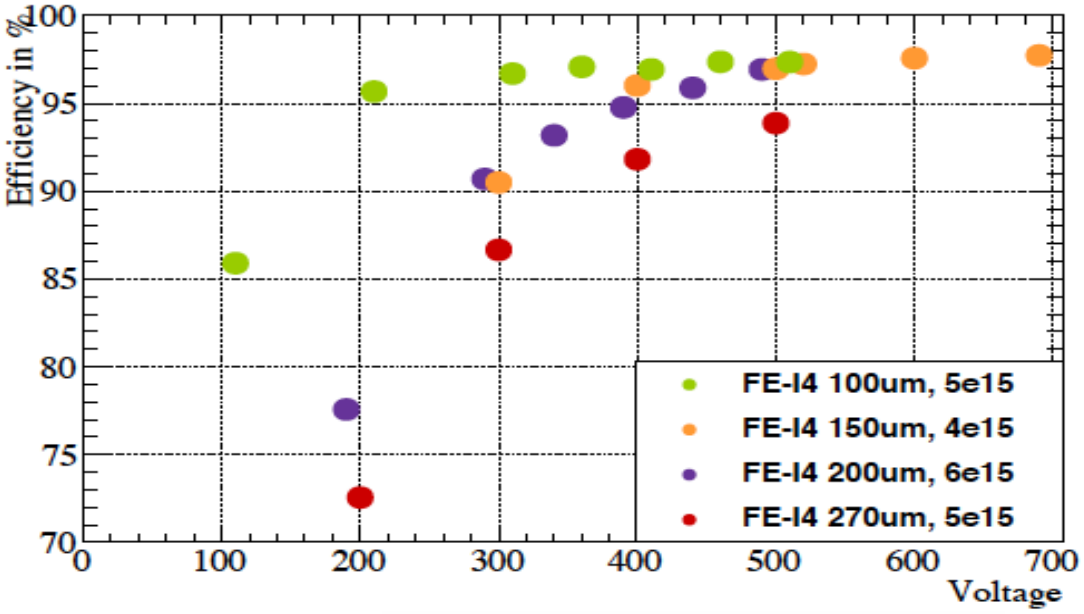


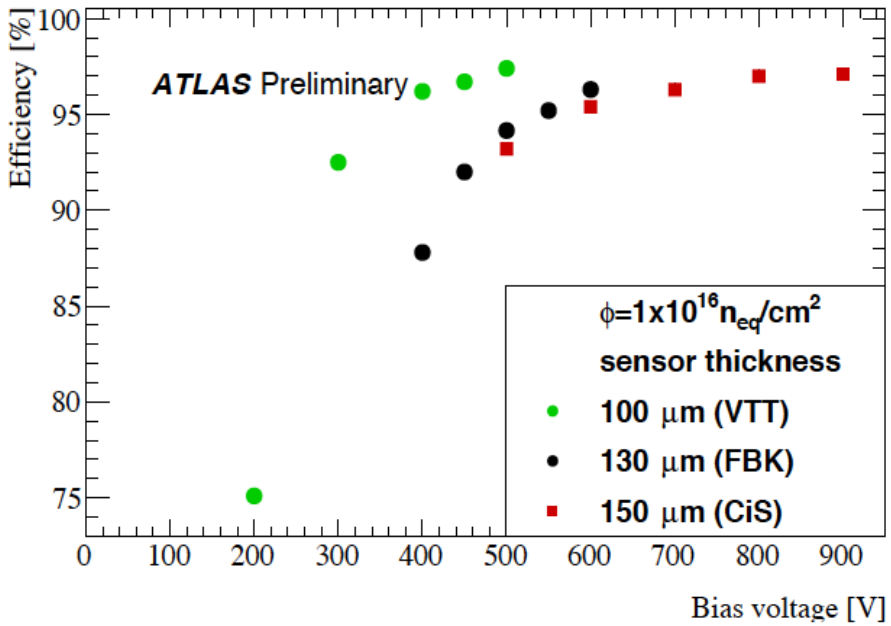


- Backside cavities etching → no need of handle wafer

Comparison of hit efficiencies for 100 - 150 μm thick sensors

- Hit efficiency saturation at lower voltages for the modules with 100 μm thick sensor compared to mdoules with 130- 150 μm thick sensor.



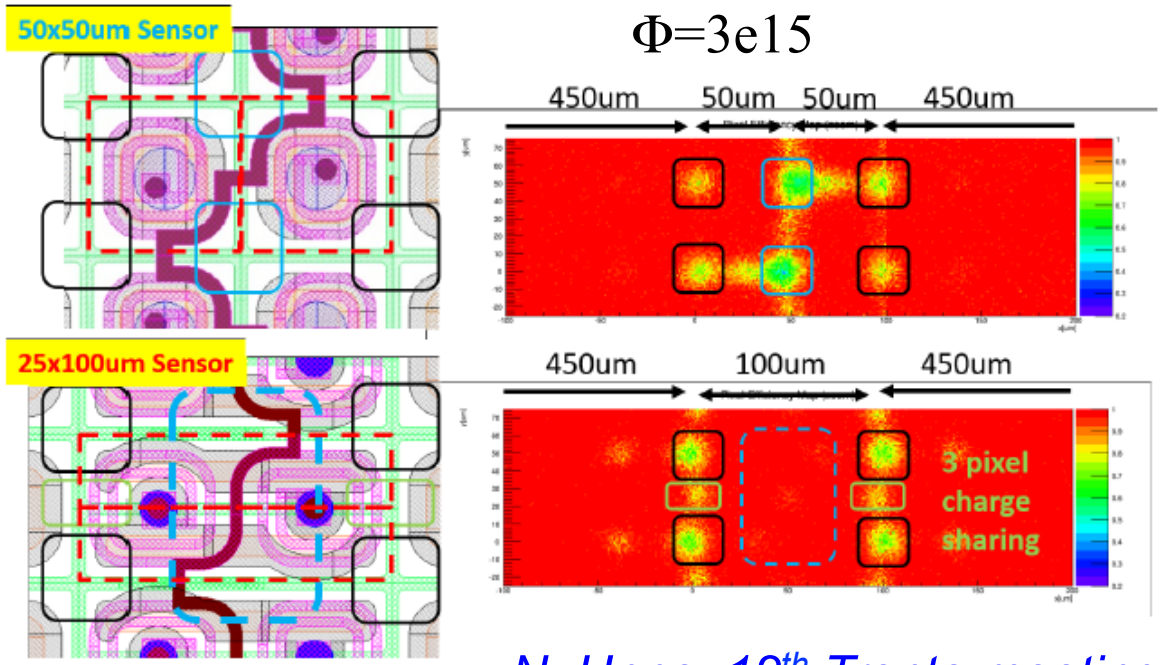


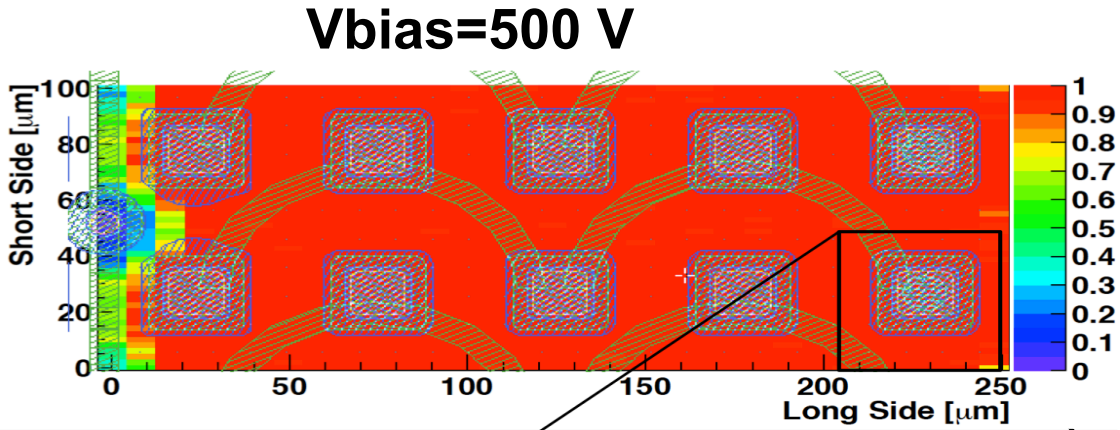
- Lower operation bias voltages at high fluence results in lower power dissipation and helps to relax the requirements on the cooling system

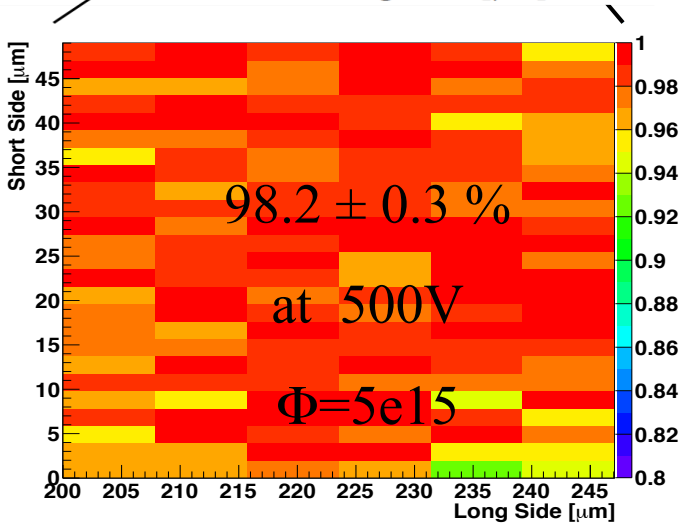
Baseline choice: 100 μm thin sensors in L1 - Option for L2 pixel layers

Estimation of the hit efficiency for a 50x50 μm² pixel

- Modified FE-I4 sensors to create 50x50 or 25x100 μm² pixel cells
- Higher effect of charge sharing and eff. decrease due to the biasing structures → need lower threshold ~600-800 e expected for the RD53A chip

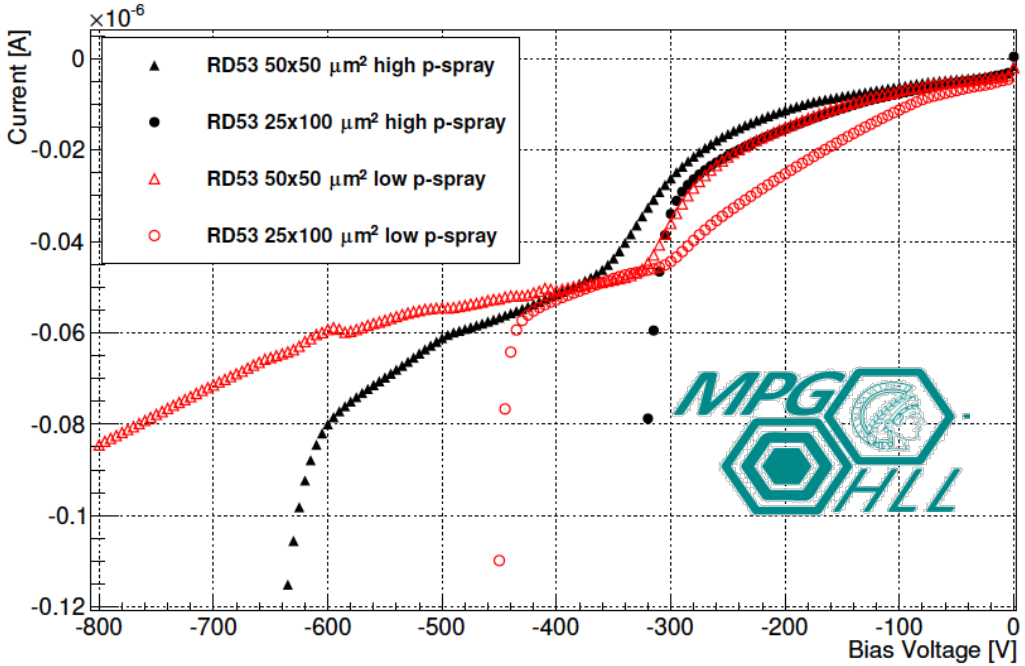


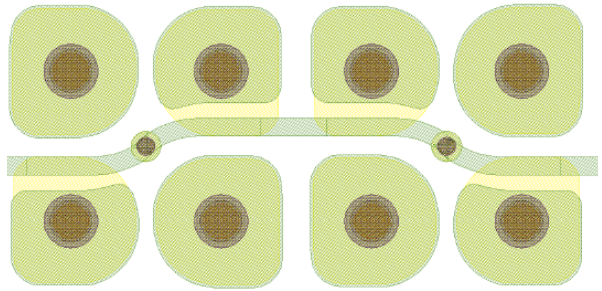




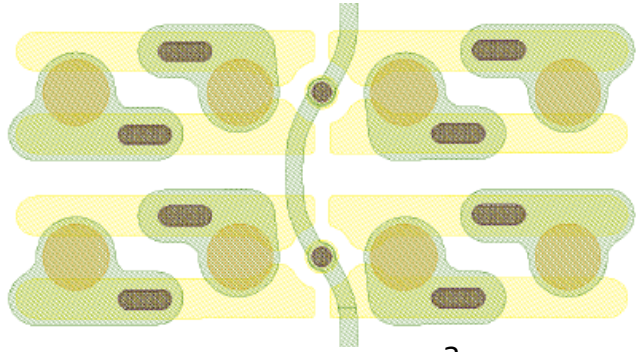
N. Unno, 12th Trento meeting, 2017

RD53 planar sensor design

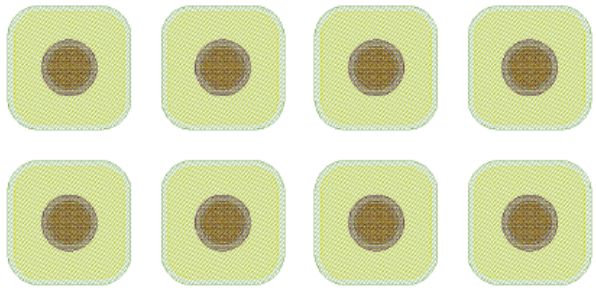


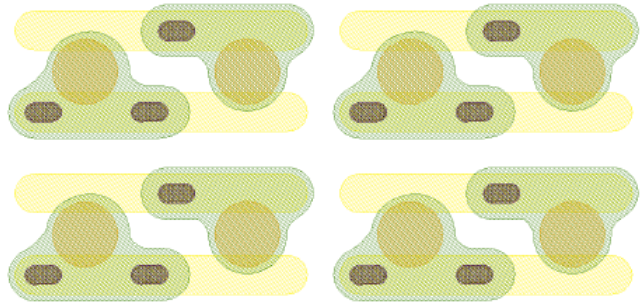


50 x 50 μm²

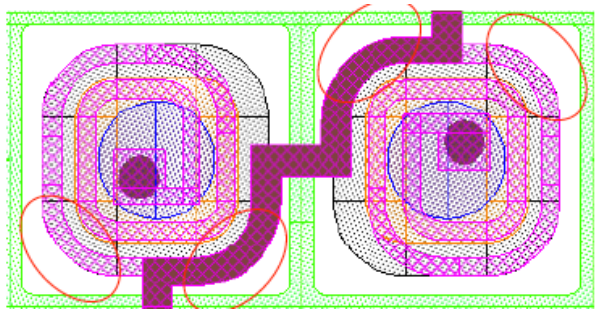


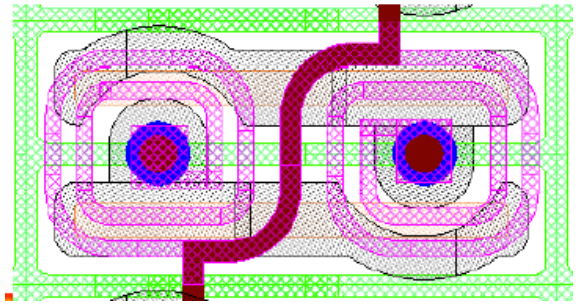
25 x 100 μm²





- Optimization of biasing structures
- Development of temporary metal technology to test the sensor without the need of implementing a biasing rail



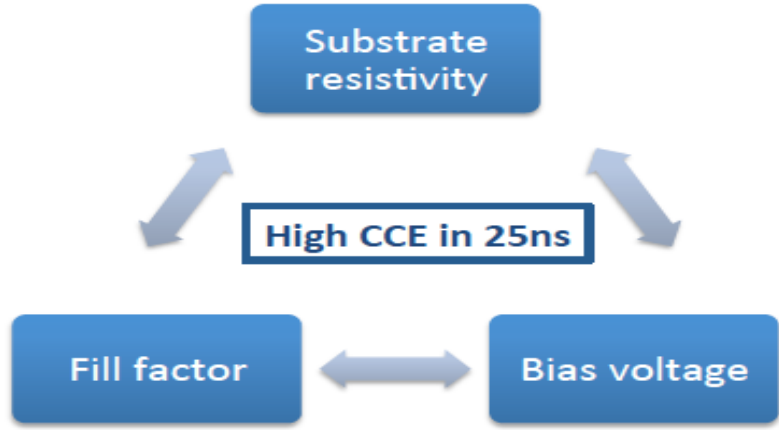


HPK-poly-silicon resistors

CMOS sensors for ATLAS ITk

- Applications for ATLAS need to optimize the charge collection for
  - Fast charge collection to avoid trapping after irradiation and be 25 ns in-time efficient
  - Large depletion region for high(er) signals
- Higher rate capability
- Enabling Technologies: High voltage process and high resistive wafers

- Much less elaborate assembly process (e.g. no hybridization)
- Much lower cost (factor 4 compared to hybrid pixel modules)
- Fast turn-around production at large volume producers
- Pixel size 50x50 μm^2 and smaller (25x25 μm^2 achievable)
- Thin modules (100 μm)



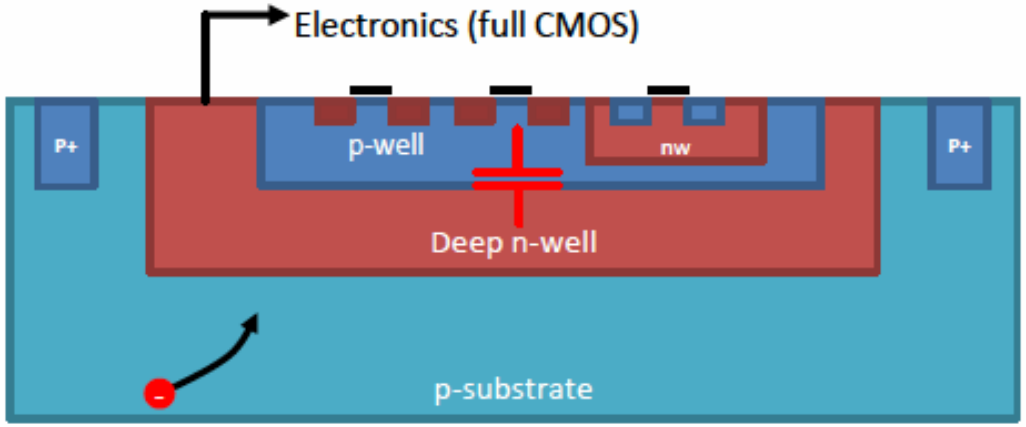
Large vs. small fill factor CMOS sensors

Electronics inside charge collection well

- Collection node with large fill factor → rad. hard
- Large sensor capacitance (DNW/PW junction!)→ x-talk,

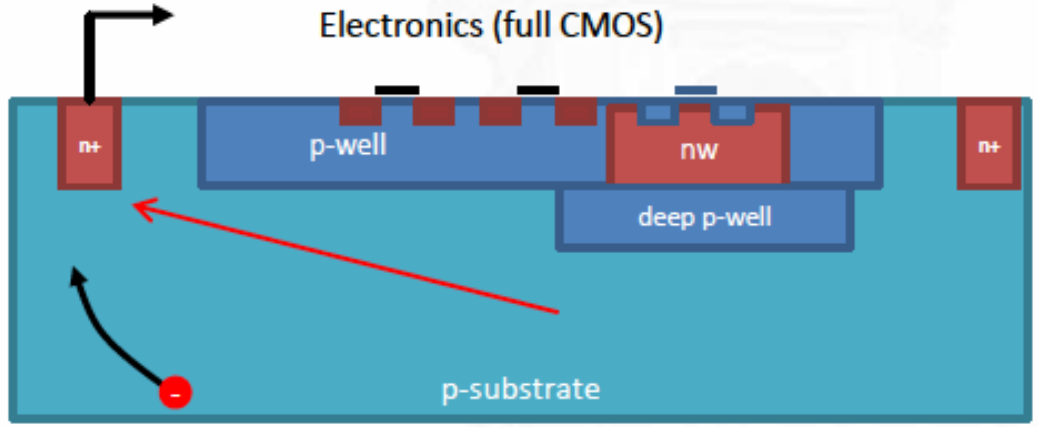
noise & speed (power) penalties

- Full CMOS with isolation between NW and DNW



Electronics outside charge collection well

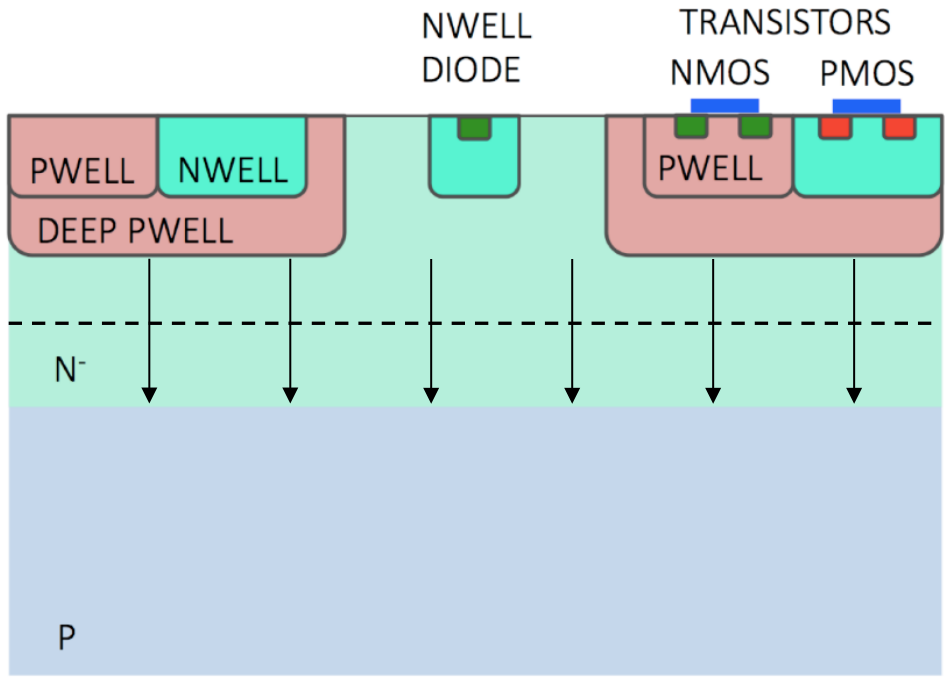
- Very small sensor capacitance→ low power
- Potentially less rad. hard (longer drift lengths)
- Full CMOS with additional deep p-implant



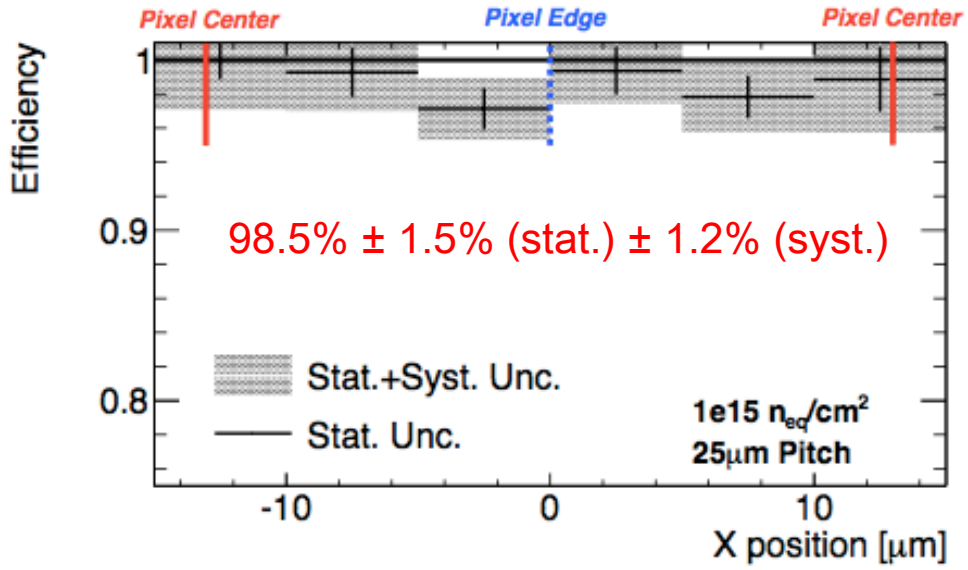
T. Hemperek, Vertex Workshop 2017

Modified process for small fill factor CMOS sensors

- Modified process at Towerjazz
- Novel modified process developed in collaboration with the foundry
- Adding a low dose planar n-type layer significantly improves depletion under deep PWELL
- Increased depletion volume → fast charge collection by drift
  - Better time resolution
  - Reduced probability of charge



W. Snoeys et al. DOI 10.1016/j.nima.2017.07.046



I. Berdalovic, PSD conference 2017

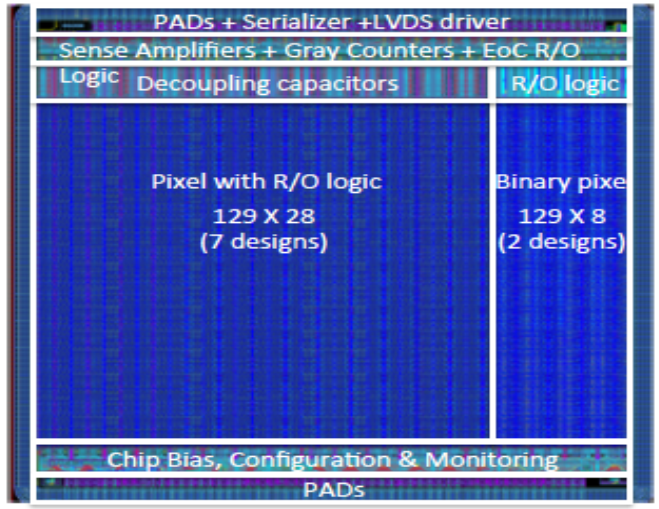
Large vs small fill factor – Monolithic submissions

Lfoundry (150 nm)

Resistivity > 2000 Ohm cm

Monopix01

- Received Apr. 2017
- "Demonstrator size"
- 50 x 250 μm² pixels
- Fast standalone R/O



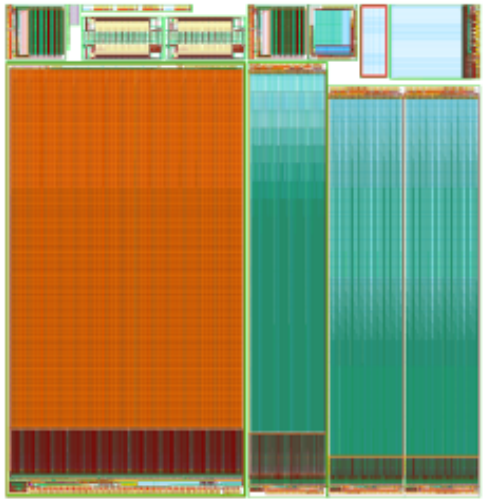
AMS aH18 (180 nm)

Resistivity 50-1100 Ohm cm

ATLASpix

- 4well CMOS process
- 56 x 56 μm² pixels

Asynchronous read-out to periphery

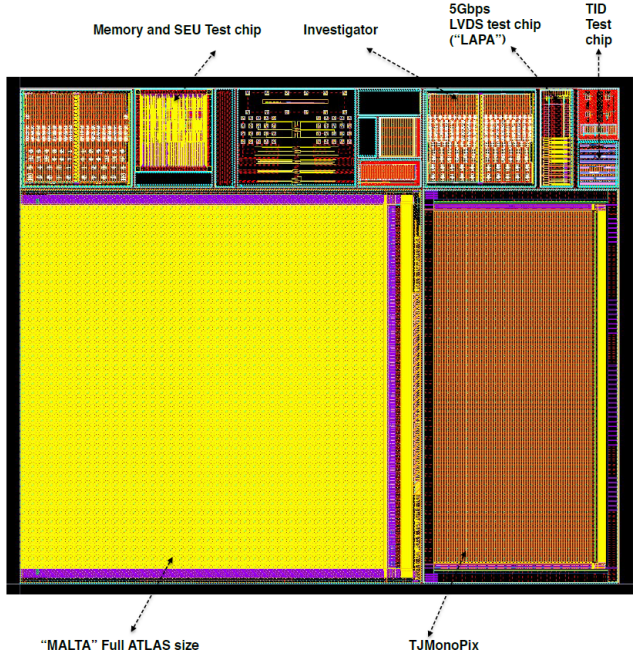


Towerjazz (180 nm)

- Two large scale demonstrators **MALTA and Monopix:**

– Asynchronous/synchronous matrix readout

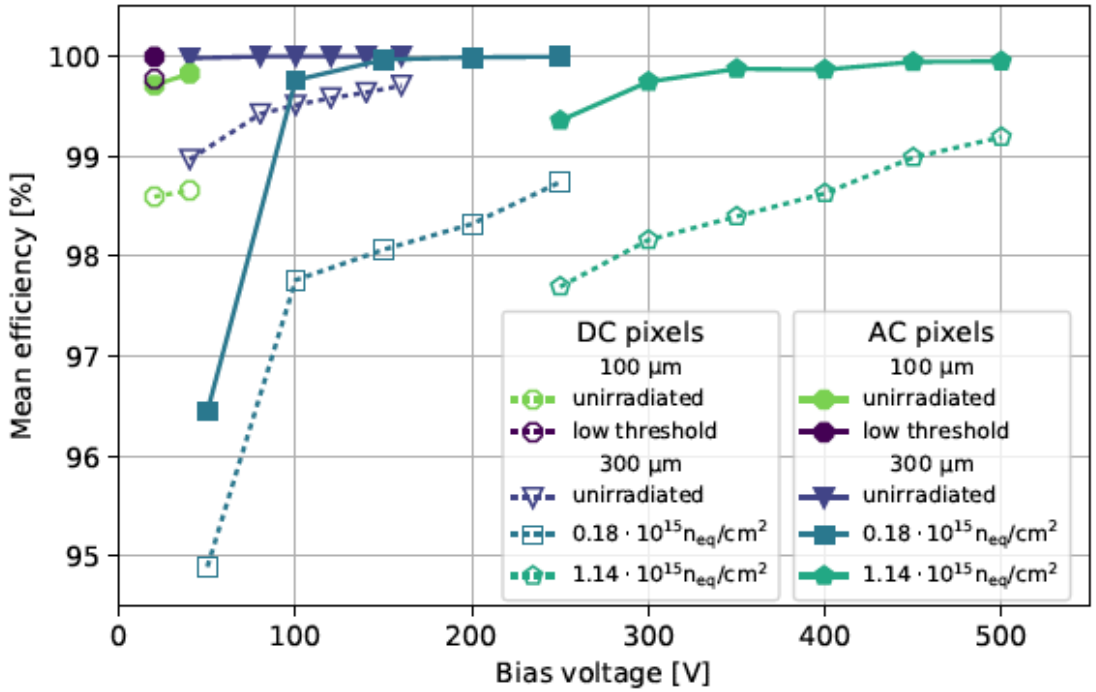
– Focus on small pixels < 50x50 μm²

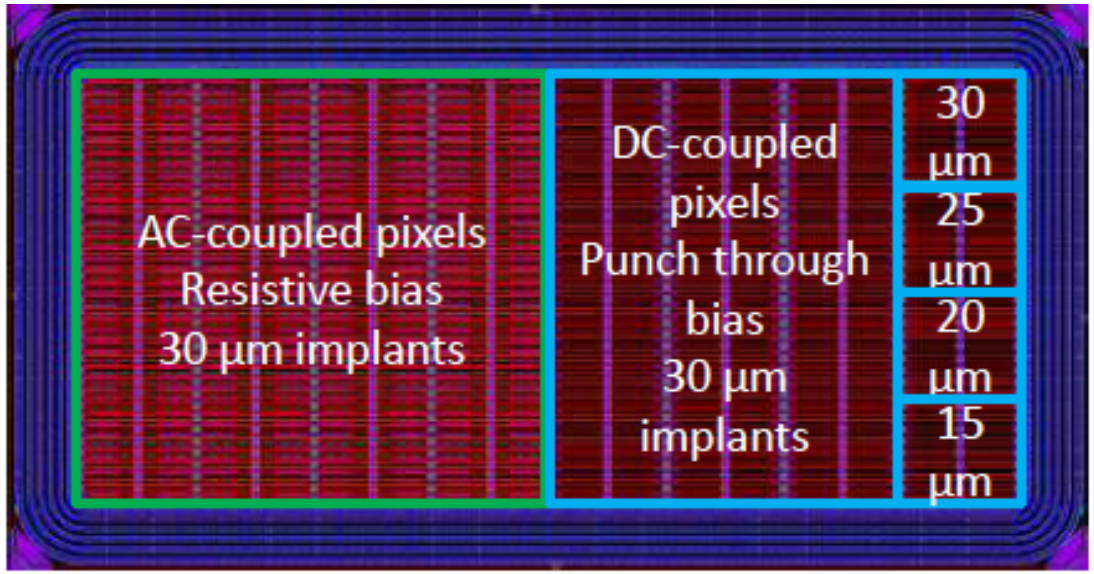


Passive CMOS sensors

LFoundry 150 nm CMOS technology

- 2kΩcm p-type material, CZ 8”
- Passive pixel, i.e collecting node w/o electronic
- 100/300μm thick, backside processed
- Bump bonded to ATLAS FE-I4
- Pixel size: 50 μm x 250 μm





- Multiple metal layers, poly-silicon layers, metal-insulator-metal (MIM) capacitors → special sensor features as AC coupling, redistribution of bump connections for inter-chip pixels …
- Excellent radiation hardness properties demonstrated at 10^{15} n_{eq} cm^{-2}

D. –L. Pohl et al, Radiation hard pixel sensors using high-resistive wafers in a 150 nm CMOS processing line

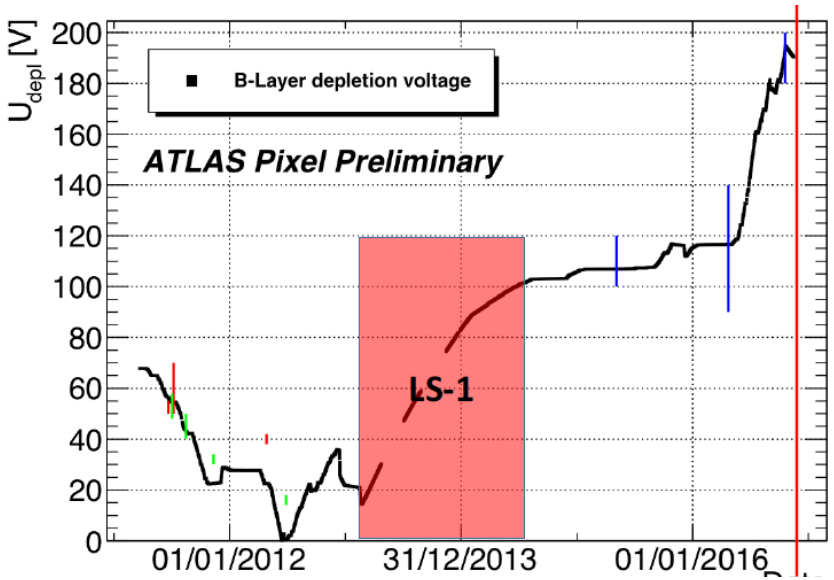
Conclusions and Outlook

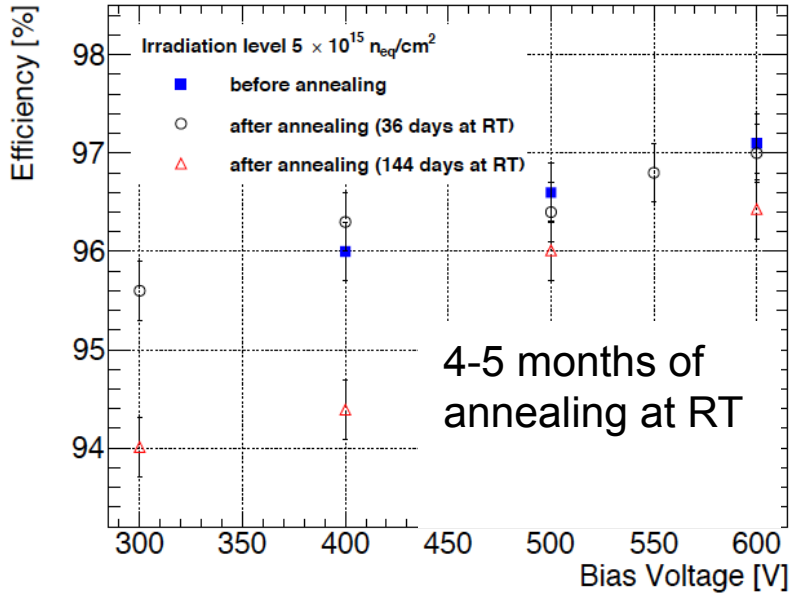
Many exciting opportunities for precision measurements and new discoveries with the HL-LHC

- Extreme environment poses many challenges
- Many years of work have now resulted in the design of an all-silicon tracking detector for ATLAS that is able to tackle these challenges
- Currently working on the finalization of the pixel detector layout
- A lot of R&D is currently on-going :
  - Sensors and Front-End chips
  - Readout
  - Powering and protection
  - Layout and mechanics
- An enormous amount of work to do before installation in a bit less than 10 years time!

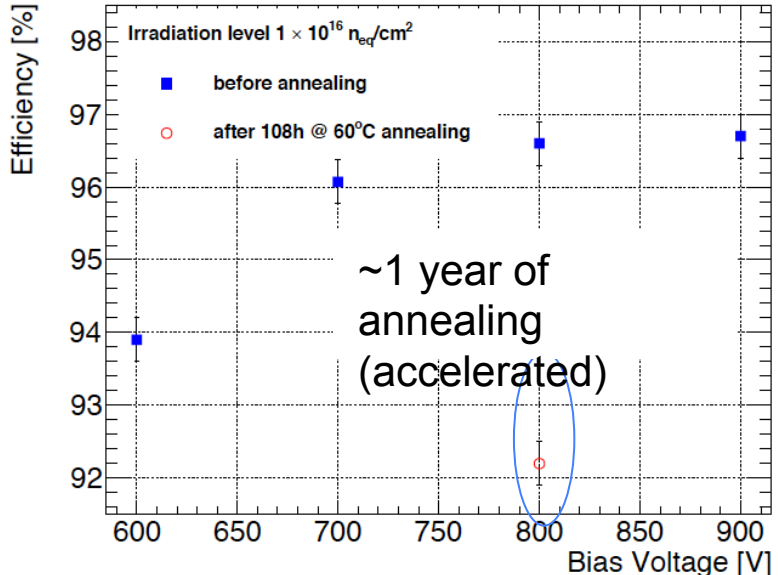
Additional material

Lessons learned from present detector
Annealing effects



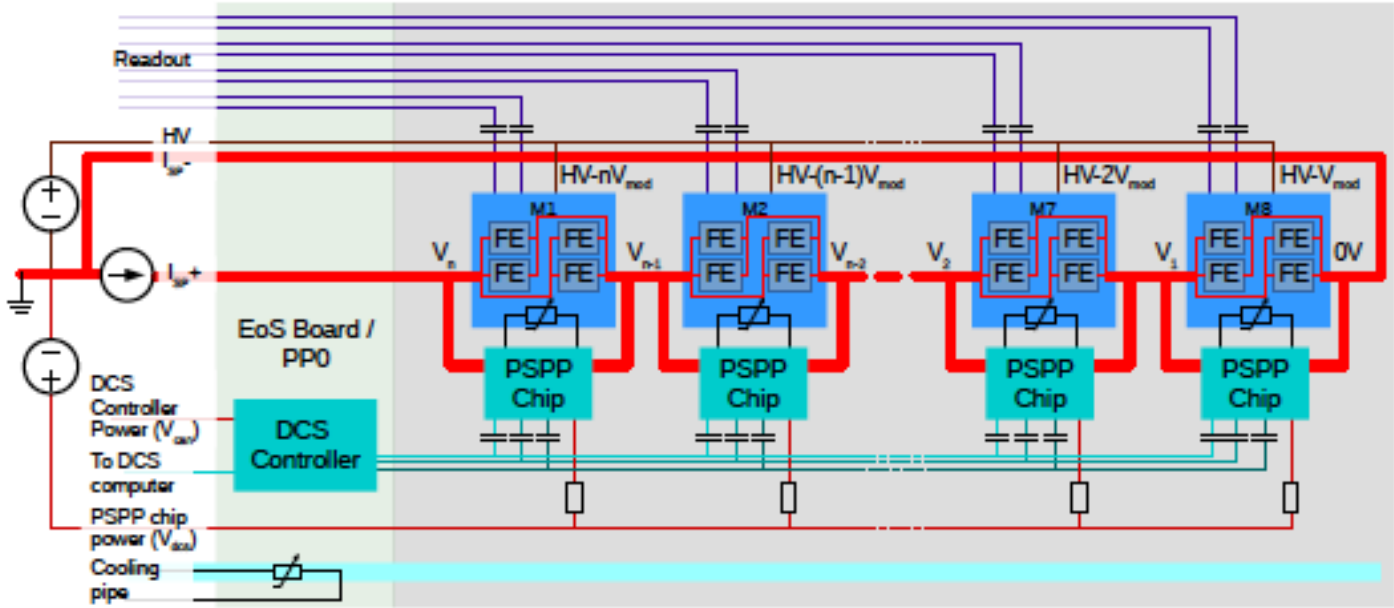


- Large influence of annealing on the measured and predicted V_{depl} *J. Beyer, 12th Trento Workshop*
- Need to maintain cooling on as continuously as possible
- Study annealing effects on pixel sensors at Itk fluences in realistic scenarios → outermost layers will be at RT during innermost section exchange



Power distribution and read-out electronics

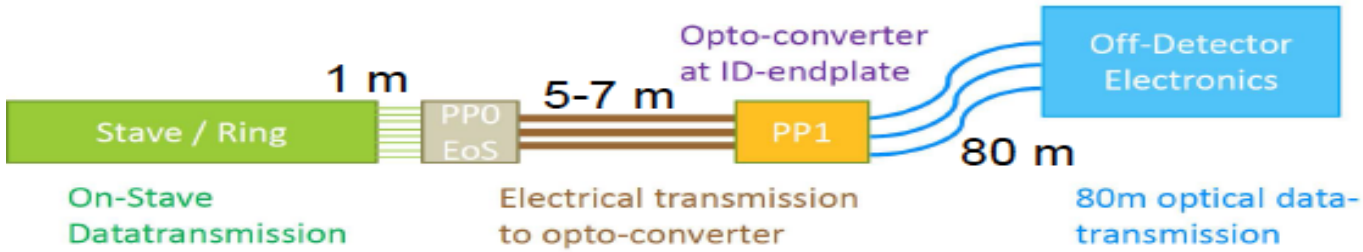
Serial powering for ITk pixel modules



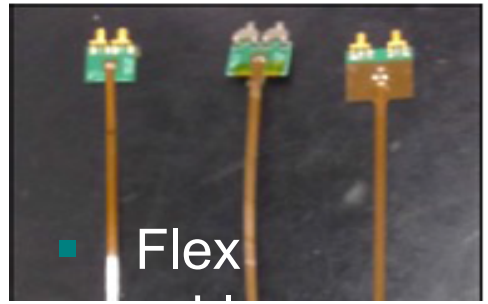
- Constant current source
- Shunt low-dropout regulator to control voltage across pixel module

- Serial powering of pixel modules with up to 16 modules per chain – average 8
- DCS functionality integrated in concept:
  - PSPP chip: monitor and control of module (by-passing)
  - Independent power and communication lines for the DCS
- HV protection: one line per module? Fuse? HV switch?

Pixel read-out electronics



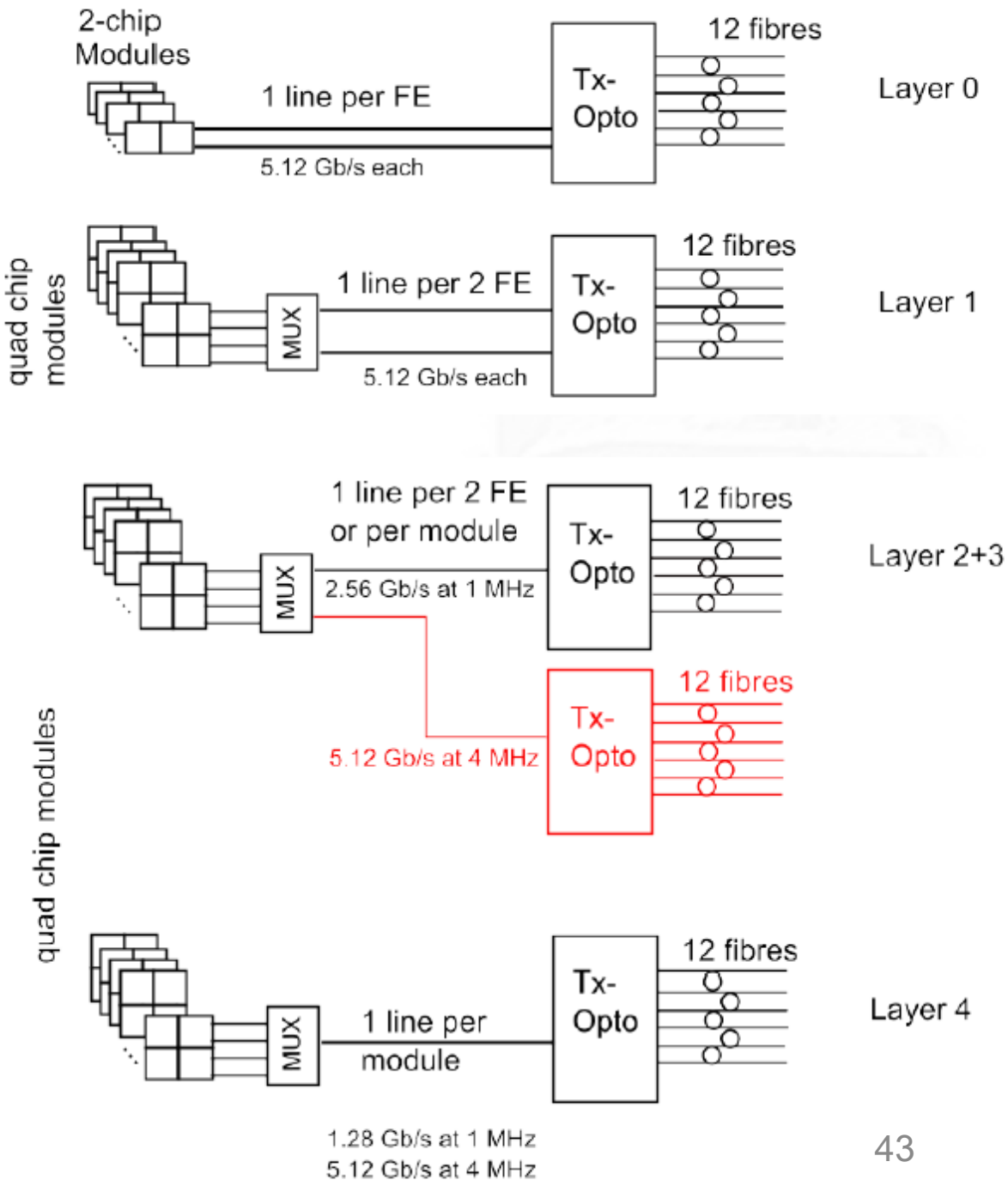
- Connection between on- and off-detector via electrical-optical link:
- Currently defining opto-converter location (rad.level @ innermost layer: ~10 MGy!)
  - Difficult to find laser diodes sufficiently radiation-hard
  - Present assumption is to have the optical conversion stage in a place accessible during long LHC shutdown
- From FE-chip to end of inner detector electrically (5-7 m) →
  - Due to serial powering electrical data transmission lines are AC coupled
- Then optically towards the off-detector electronics (~80 m)



Pixel read-out electronics

- **Uplink:** Large bandwidth spread between inner and outer layers:
  - 5.12 Gb/s per FE for innermost layer (3.3 Gb/s for innermost ring) from the 160 Mb/s of the present detector (IBL)

    → on-chip data compression is anyhow necessary
  - 640 Mb/s per FE for outer layer (1 Gb/s for outermost ring)
- Combining lines is done to optimize the material .



Trigger design

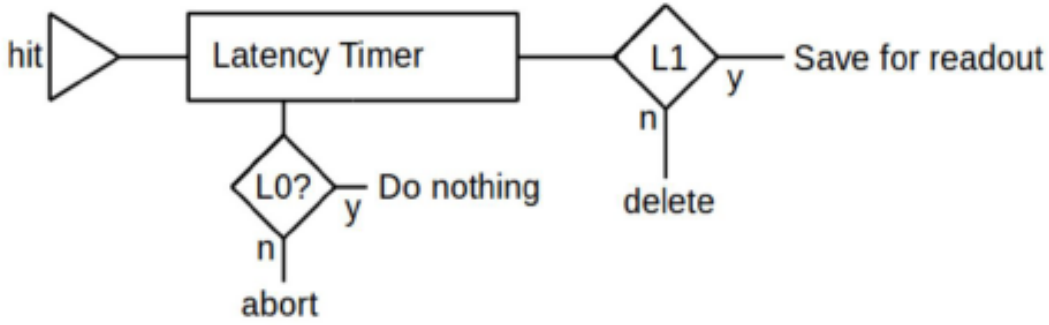
Complete ITk readout on L0 with 1 MHz rate and 10 μs latency or

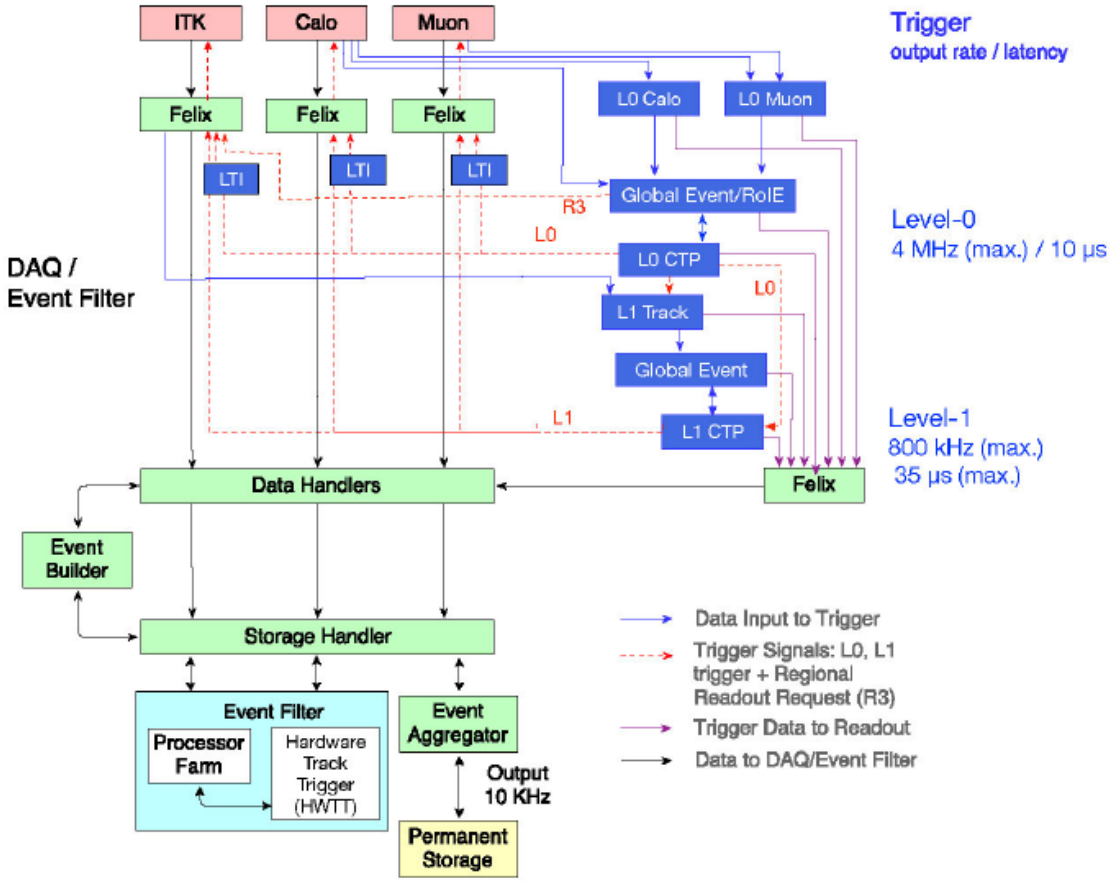
• Partial ITk readout on L0 with 4 MHz/10 μs and full readout at L1 with 800 kHz/35 μs

– outer pixel layers can provide full data on L0

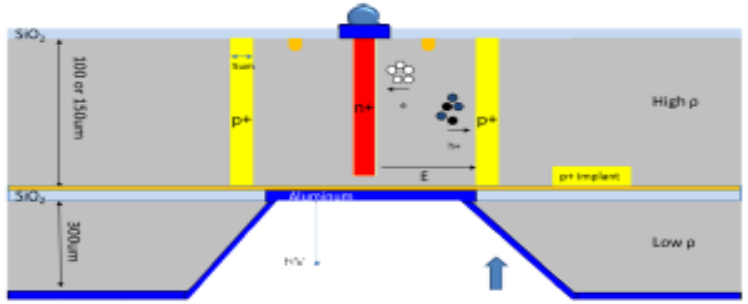
– inner layers can't due to bandwidth limitation of 5 Gb/s

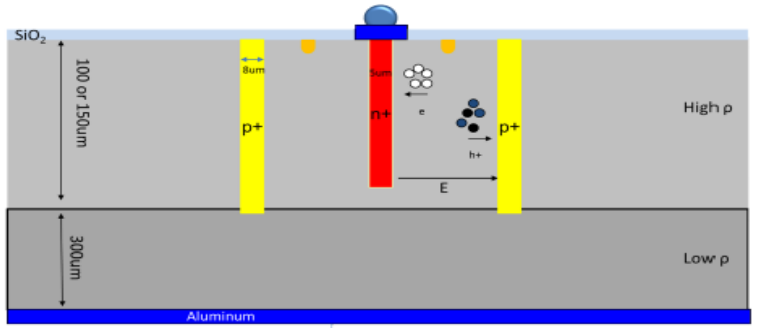
→ fast clear on L0, wait for L1



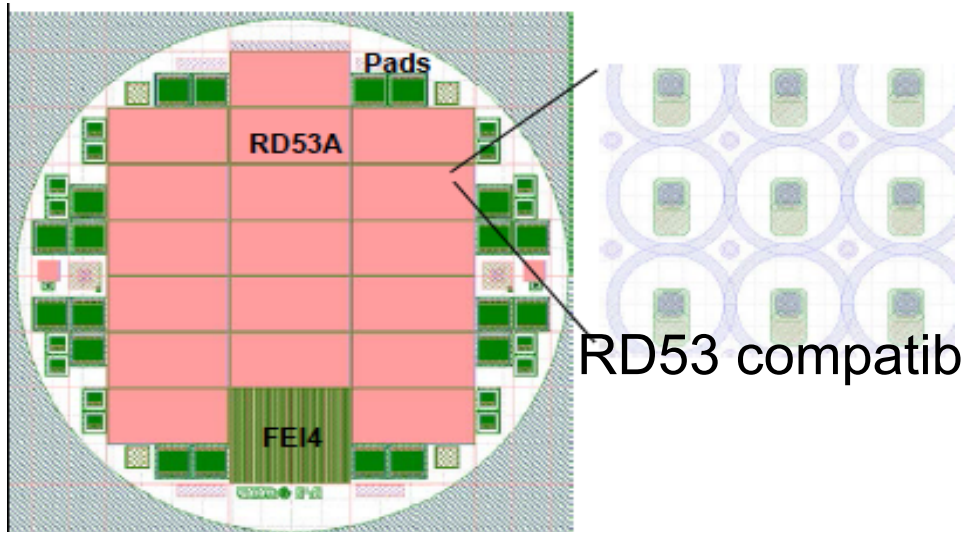


3D sensors at CNM

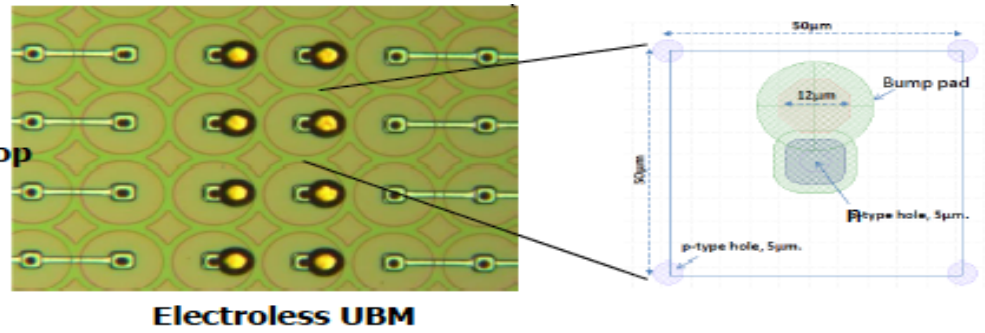




- New productions on 4” SOI or Si-Si substrates 100 and150 μm active thickness
- Leave ~100 μm of handle wafer



RD53 compatible devices



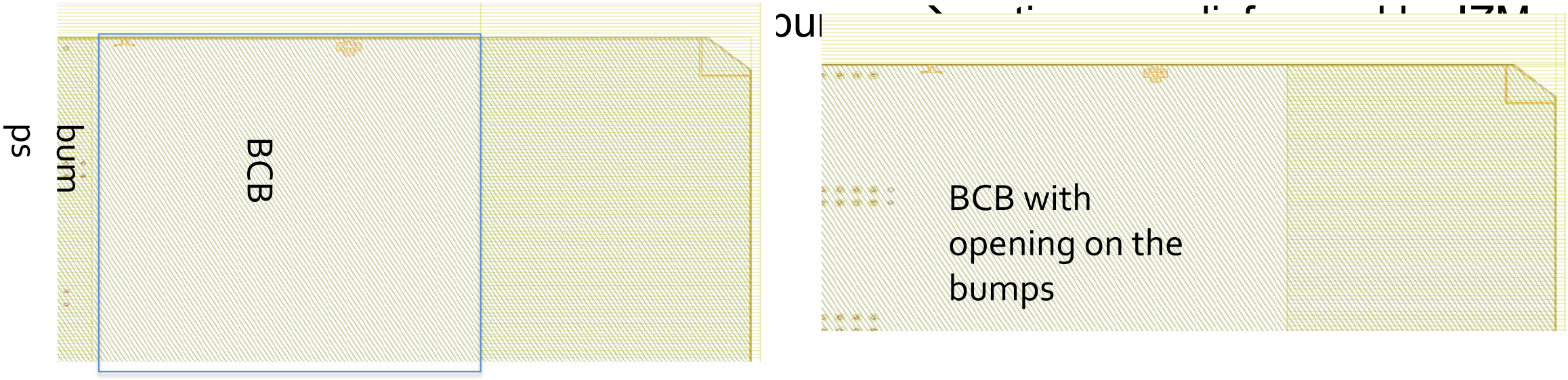
- At the moment only availability of 230 μm thick FE-I4 compatible sensors with a fraction of the pixel cells of 50x50 μm^2 geometry

J.Lange ,3D Silicon Pixel detectors for HL-LHC,

BCB isolation on chips

Fraunhofer IZM

- Two different implementations on a single wafer:
  - BCB only on the chip edges where the chip faces the not active area of the sensor at HV potential



- Further tests foreseen with BCB deposited on a daisy chain run on 12” wafers again at IZM in preparation for the RD53A processing

BCB isolation on chips

Fraunhofer IZM

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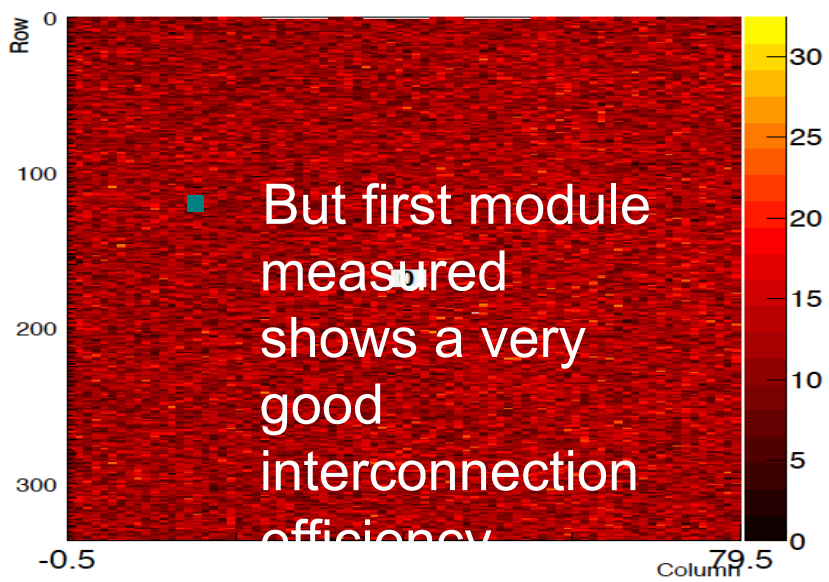
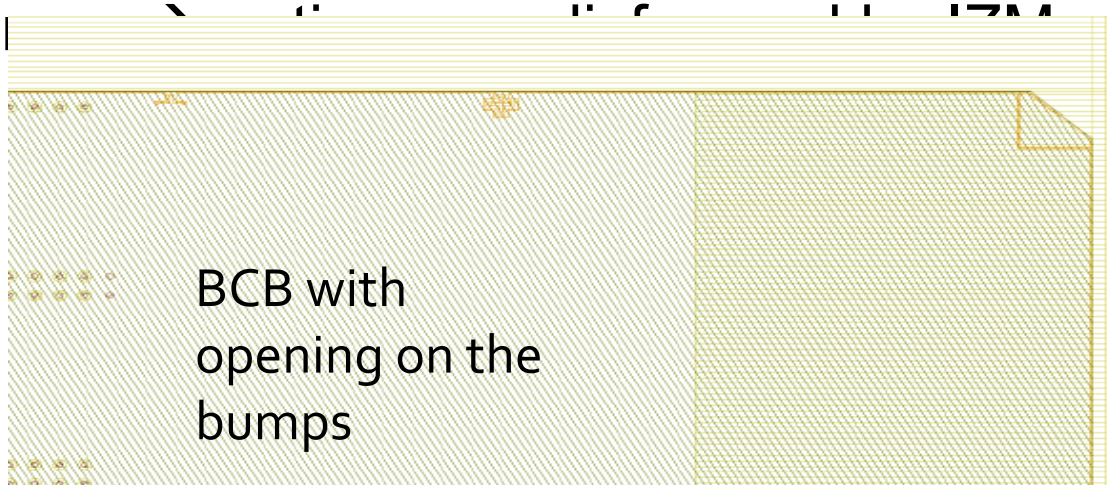


- But first module measured shows a very good interconnection efficiency

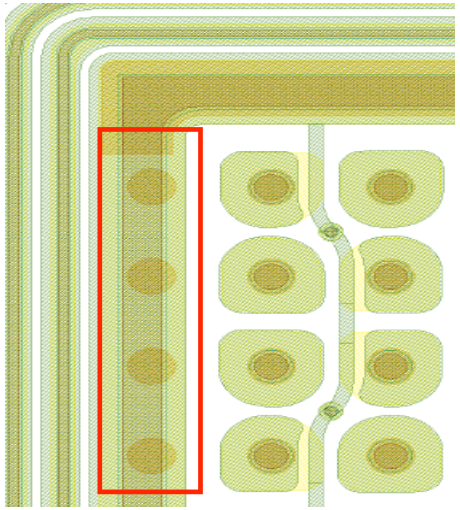


HLL SOI3 sensor 100 um thick

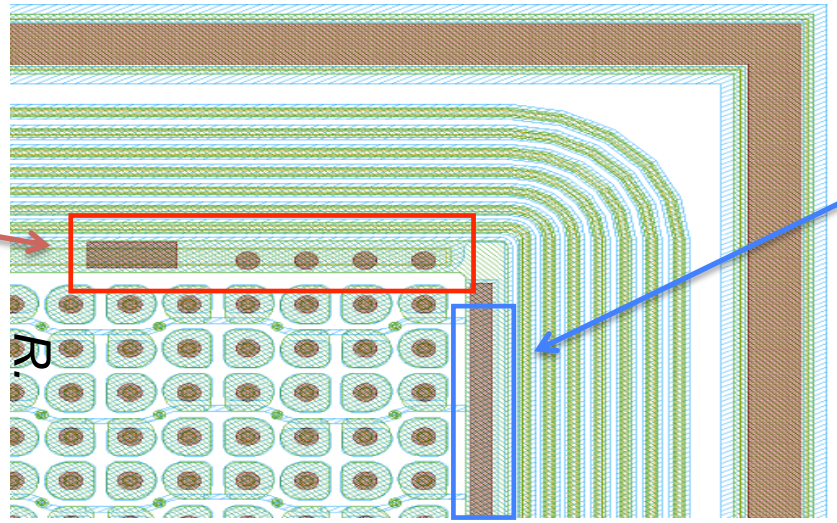
- Further tests foreseen with BCB deposited on a daisy chain run on 12" wafers again at IZM in preparation for the RD53A processing

New Bias Ring designs

- Some sensors without bumps on BR:
  - Investigate if it is possible to reduce the effect of PT on hit efficiency after irradiation leaving the BR floating
  - Drawback: currents from the edges will flow directly into edge columns
- Second bias ring design: decouple the testing functionality before interconnection from the grounding after flip-chipping
  - Bias rails are all linked to a metal line not connected through contacts to the implant
  - bumps on BR are in contact to the BR implant



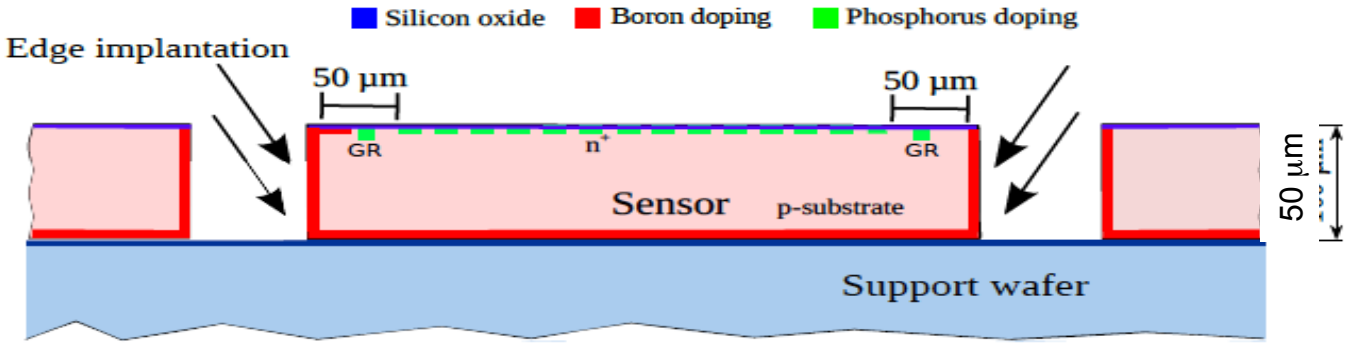
Bumps in contact with the BR implant



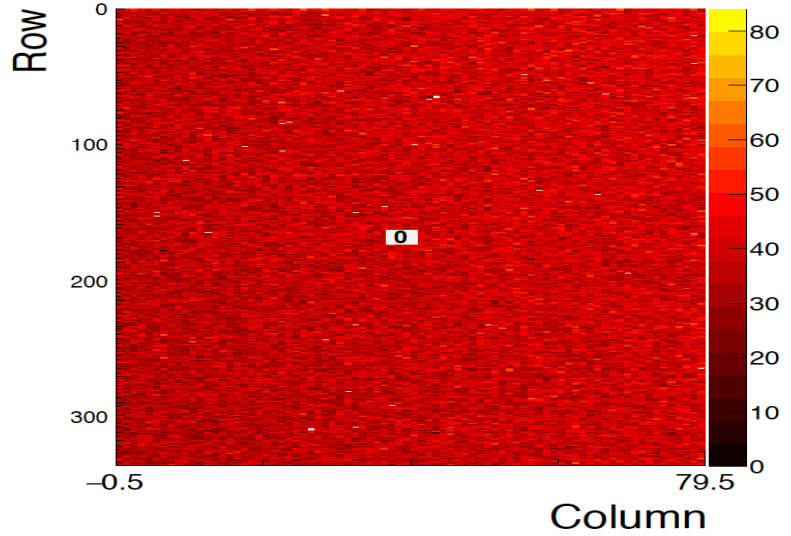
Testing metal line floating on the BR implant

ADVACAM: 50 μm thick sensors

- Active edge sensors produced on SOI wafers at ADVACAM

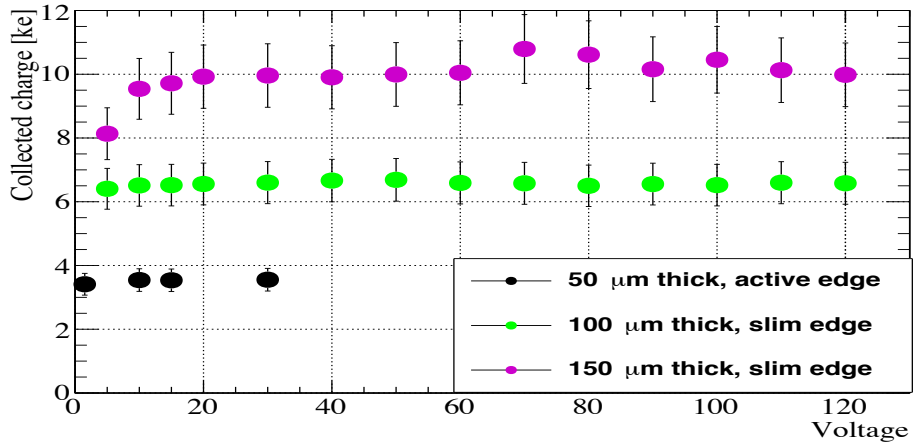


Occupancy map from Cd scan of a module with a 50 μm sensor



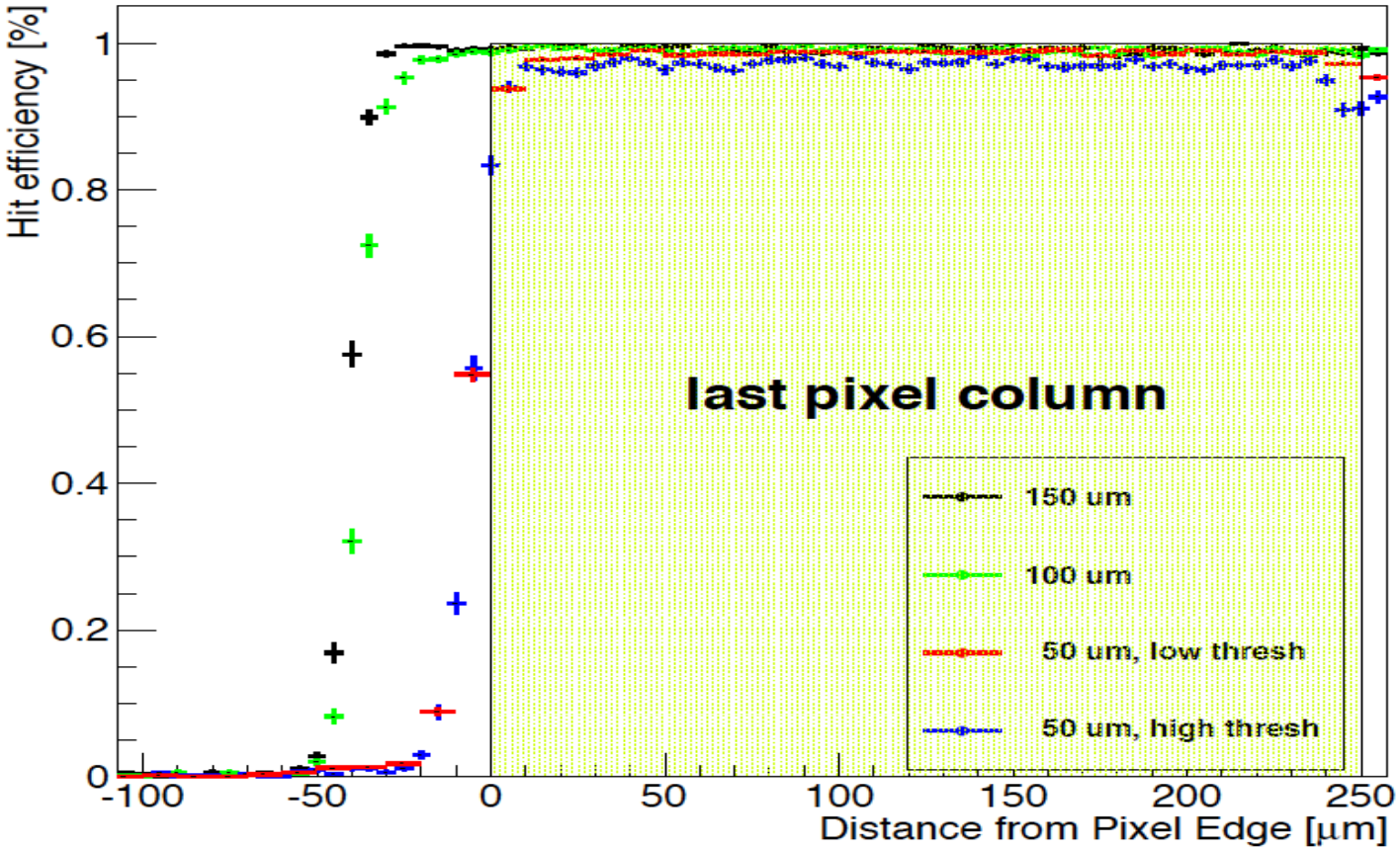
- Modules with 50 μm thin sensors and Cu-Au UBM show a perfect interconnection efficiency

- Collected charge by ^{90}Sr scans agrees with expectations for the three thickness
- 50 μm thin sensors needs a special tuning to very low thresholds ≤ 1000 e



Hit efficiencies for active edge devices

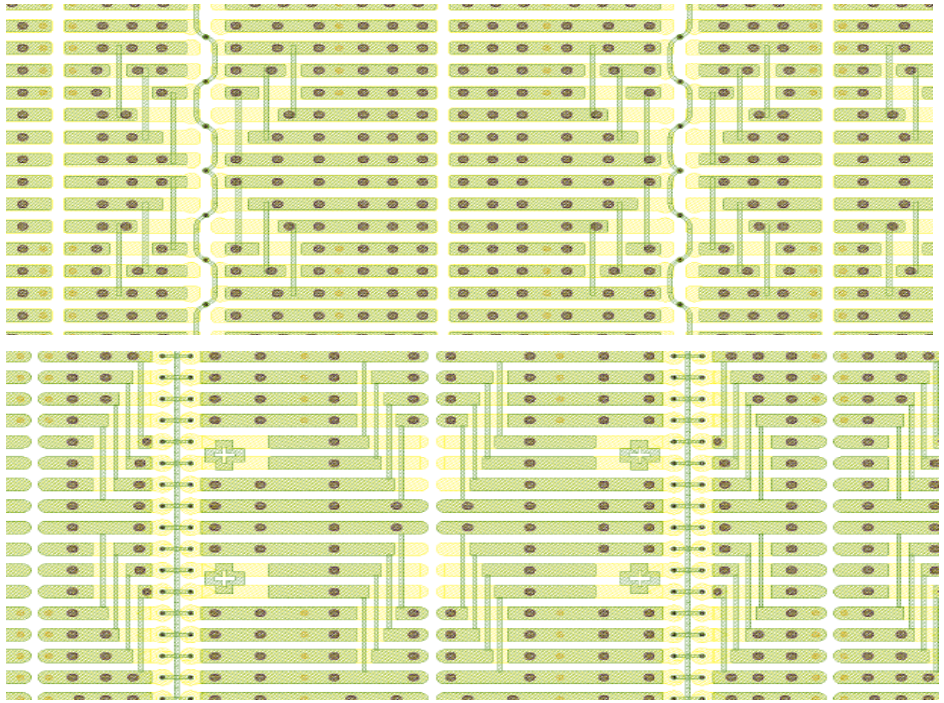
- August + October test-beam at CERN: systematic comparison of different sensor thicknesses

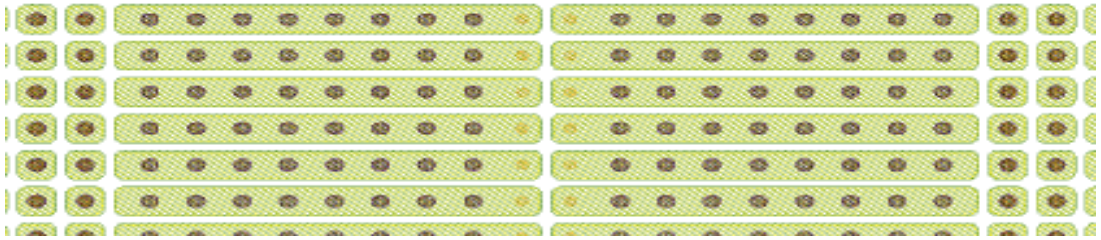


- Very good performance up to the edge of 100-150 µm thick sensors

- New measurements with 50 µm thin sensors at lower threshold then presented before (600 e- nominal instead of 800 e-)
- Higher efficiency on pixel implant with lower threshold (~98.8%) but still worse edge eff. with respect to thicker sensors

FE-I4 sensors in CIS 6" wafers and SOI4 production



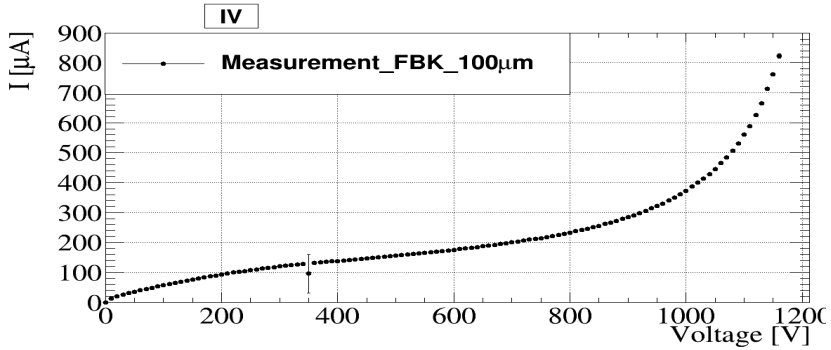


- FE-I4 quad with common PT and 3 ganged rows each chip → 180 μm distance between physical edges of the chips
- 400 μm long pixels per side

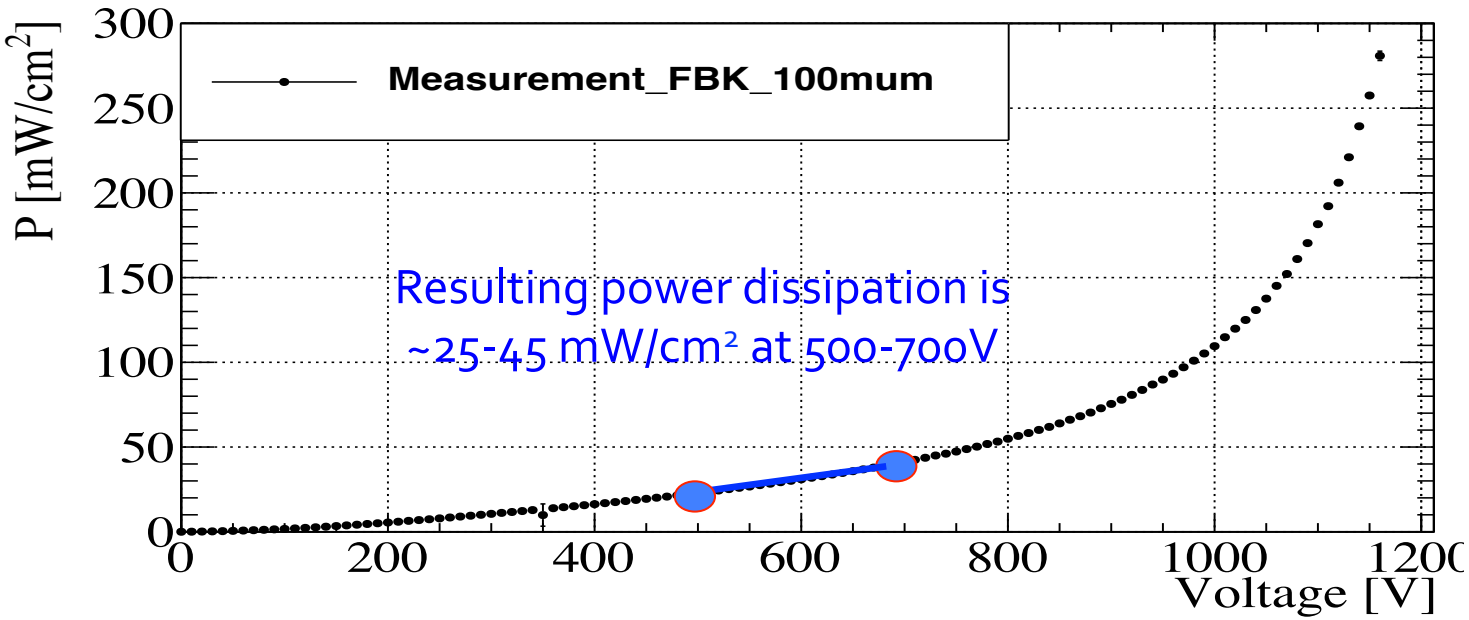
  - Quad with standard PT and 4 ganged rows → 280 μm distance between chips
  - 450 μm long pixels per side

  - FE-I4 compatible sensors with half the cells of 50x50 μm² pitch and no biasing structures
  - Especially important to study post-irradiation performance of small cell sizes while waiting for the RD53A chip

Power dissipation for thin planar sensors at high fluences



IV curve of bare FE-I4 sensor at -25˚C irradiated to **1x10^{16} n$_{eq}$/cm^2** after 11 days of annealing, as measured in direct thermal contact in a probe-station



Estimated power dissipation per cm^2 at -25˚C for a 100 μm thin sensor irradiated to **1x10^{16} n$_{eq}$/cm^2**

- The possible range of operation bias voltage for a pixel module with a 100 μm thick sensor is **500-700 V**
- The resulting power dissipation at 500-700 V is **~25-50 mW/cm^2** at 1x10^{16} n$_{eq}$/cm^2 irradiation