The SuperB Silicon Vertex Tracker

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on behalf of the SuperB Group

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OUTLINE

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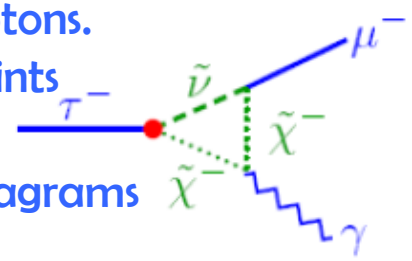
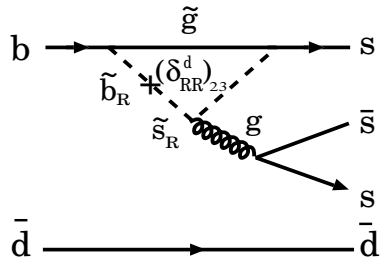
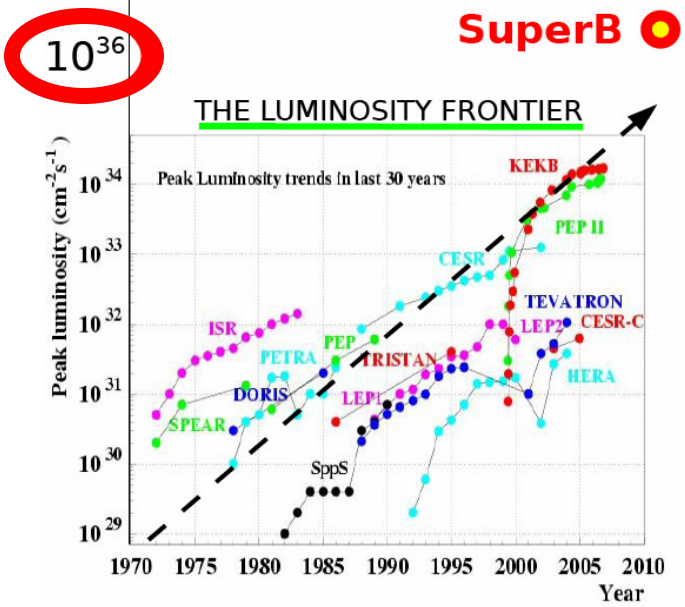
SuperB Physics

- Main motivation to undertake a new generation of e+e- experiments: measure the effects of New Physics on the decays of heavy quark and leptons.
- High luminosity is crucial to reach the sensitivity needed to set constraints on the models of the NP by flavour physics.
- Search for the effects of physics beyond the standard model in loop diagrams
  - Potentially large effects on rates of rare decays, time dependent asymmetries, lepton flavour violation, ...
  - Sensitive even to large New Physics scale, as well as to phases and size of NP coupling constants





- A luminosity of 50 – 100 ab^{-1} (x 100 than existing B-Factories) opens windows on NP:
  - Precision measurements to detect discrepancies from the standard model
  - Rare decay measurements
  - Lepton flavour violation
  - CP violation in Charm
  - Unique feature: Polarized e- beam: τ CPV, EDM, g-2
  - Possibility to run at tau/charm threshold
- Complementarity and synergy with LHC program.



References:

- New Physics at the Super Flavor Factory (arXiv:0801.1312v2)
- The Discovery Potential of a Super B Factory (Slac-R-709)
- Letter of Intent for KEK Super B Factory (KEK Report 2004-4)
- Physics at Super B Factory (hep-ex/0406071)
- SuperB report (hep-ex/0512235)
- SuperB CDR (INFN/AE-07/02, SLAC-R-856, LAL 07-15)

Two different ways to increase luminosity by two order of magnitude:

KEKB

- High currents
- Small damping time
- Short bunches
- Crab cavities for head-on collisions

→

- Large RF power
- High order modes
- High backgrounds

Brute-force method not approved. Now investigating "the Italian approach"

↓

SuperB:

- Very small emittance (ILC-DR)
- Small β^* at IP
- Large Piwinski angle
- Crab waist technique
- Currents similar to present ones

→

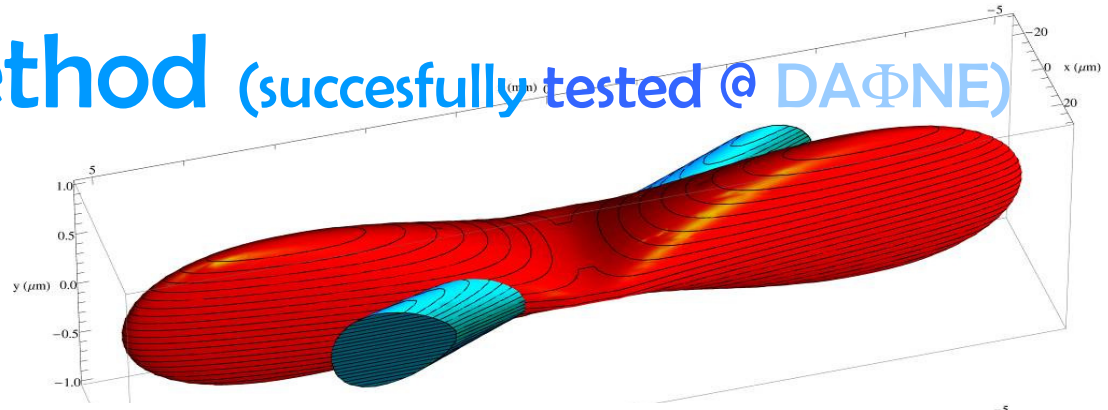
- Small collision area
- No parasitic crossing
- No synchro-betatron resonances
- Moderate backgrounds

Reuse many PEP-II components

Crab waist method (succesfully tested @ DAΦNE)

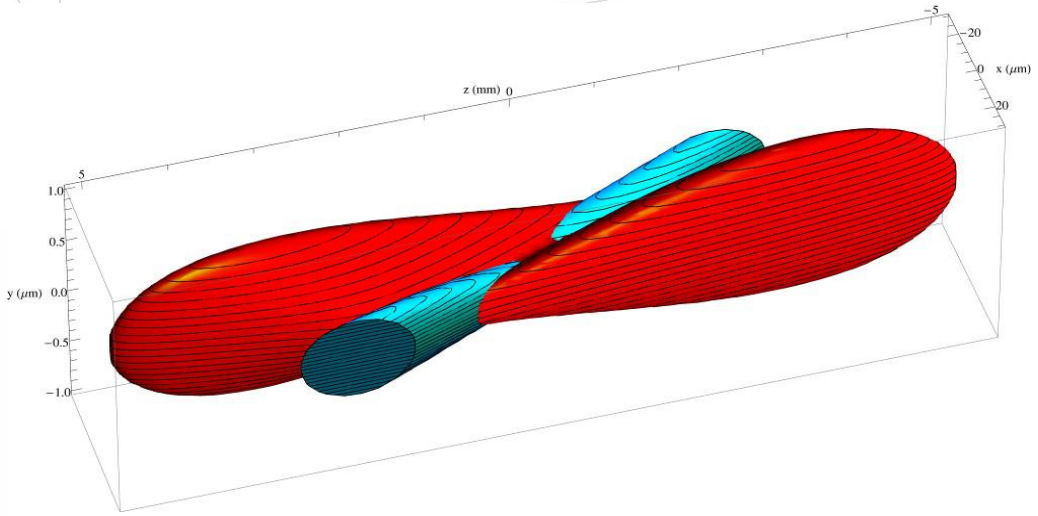
Crab sextupoles OFF

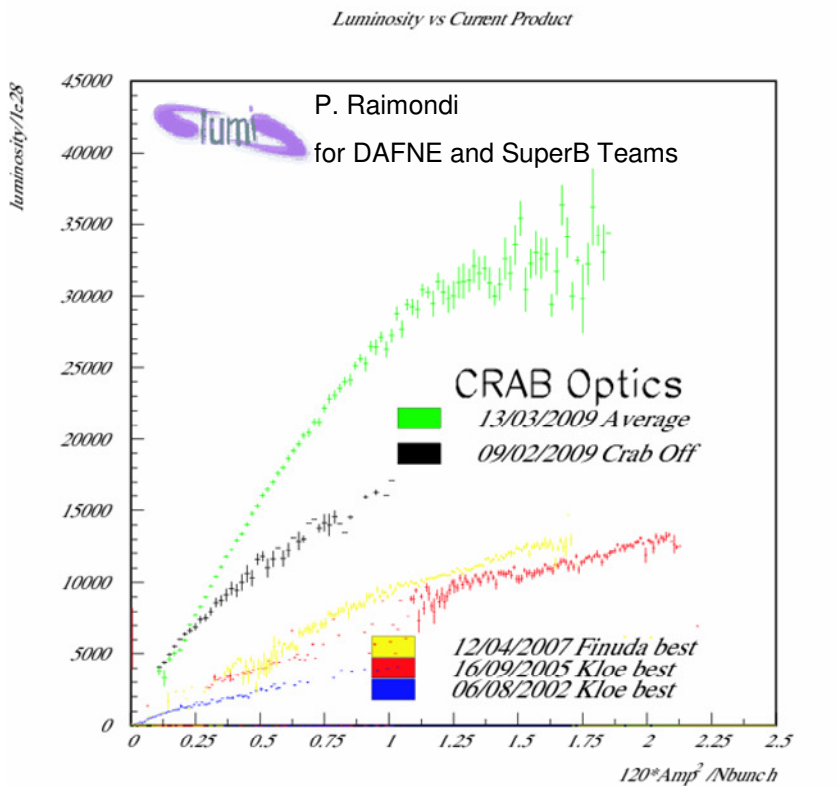
waist line is orthogonal
to the axis of one bunch



Crab sextupoles ON

waist moves to the
axis of other beam





All particles from both beams collide in the minimum β^*_y (betatron vertical amplitude@ i.p.) region:

- net luminosity gain (geometrical factor)
- removal of dangerous synchrotron-betatron resonances (allows higher currents)

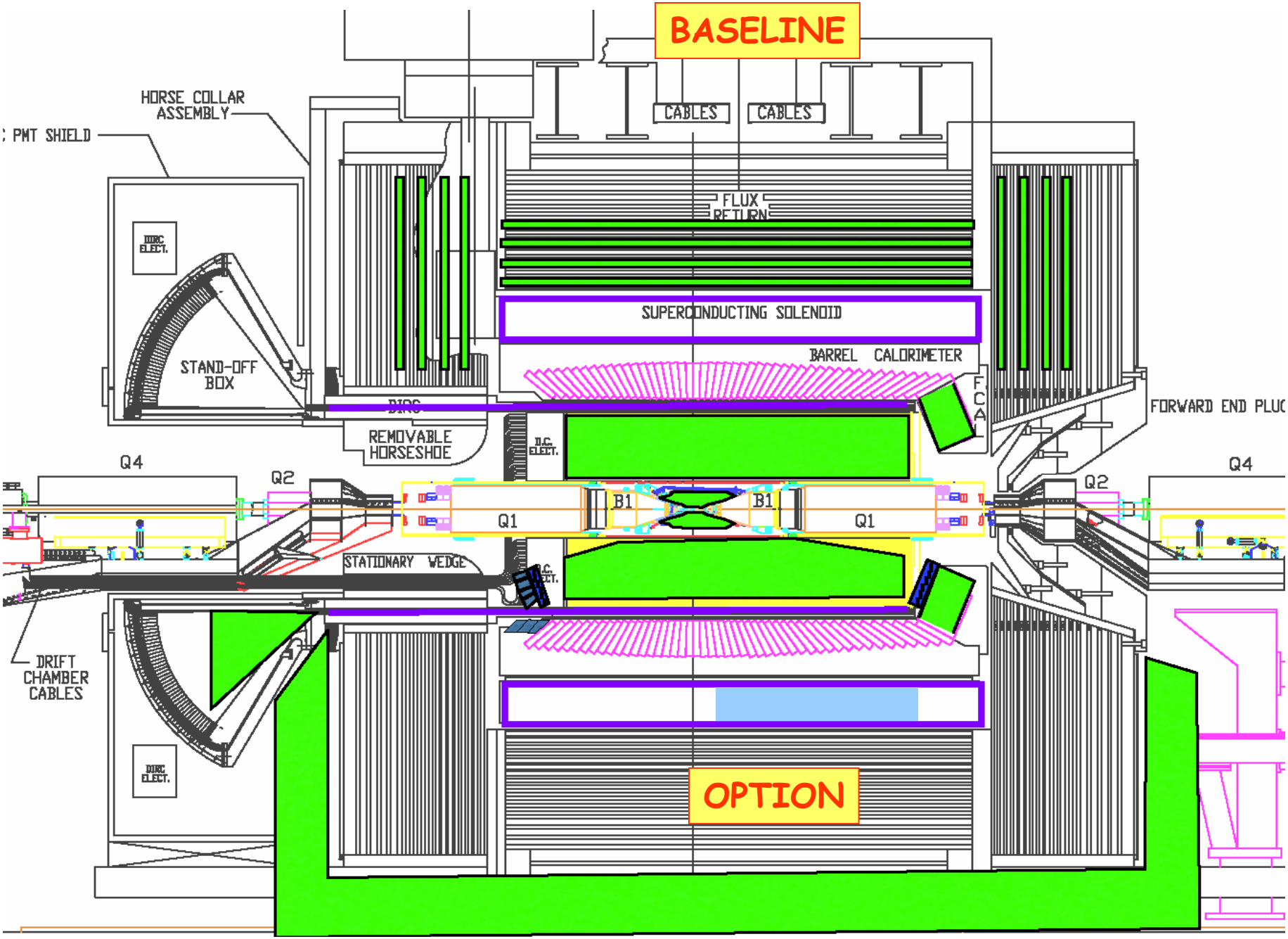
SuperB Detector Concept

- Babar and Belle designs have proven to be very effective for B-Factory physics
  - Follow the same ideas for SuperB detector
  - Try to reuse same components as much as possible
- Main issues
  - Machine backgrounds – somewhat larger than in Babar/Belle
  - Beam energy asymmetry:
    a bit smaller
  - Strong interaction with machine design
- A SuperB detector is possible with today's technology
  - Baseline is reusing large (expensive) parts of Babar
  - Quartz bars of the DIRC
  - Barrel EMC CsI(Tl) crystal and mechanical structure
  - Superconducting coil and flux return yoke.
- Some areas require moderate R&D and engineering developments to improve performance
  - Small beam pipe technology
  - Thin silicon pixel detector for the first layer
  - Drift chamber CF mechanical structure, gas and cell size
  - Photon detection for DIRC quartz bars
  - Forward PID system (TOF or focusing RICH)
  - Forward calorimeter crystals (LSO)
  - Minos-style scintillator for Instrumented flux return
  - Electronics and trigger – need to revise Bfactory "½-track" trigger style
  - Computing – large data amount

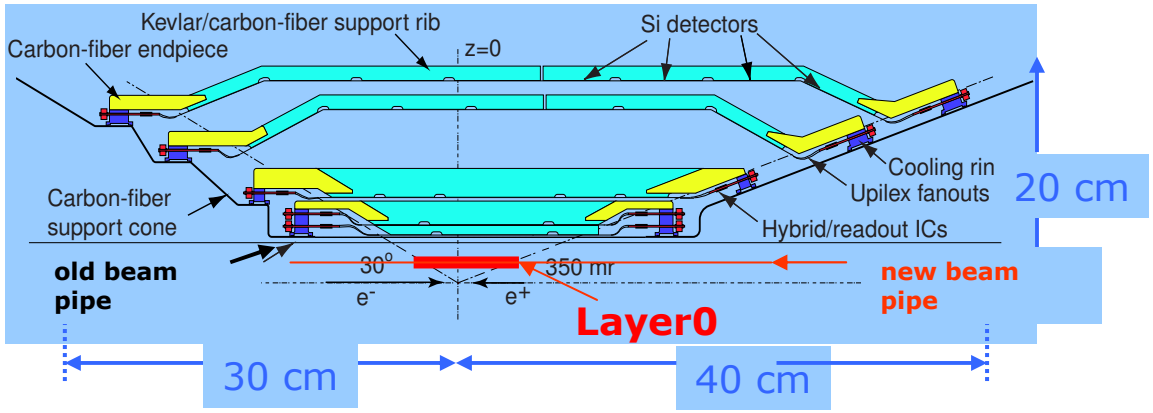
More details in:

- www.pi.infn.it/SuperB/CDR - SuperB Conceptual Design Report
- http://agenda.infn.it/categoryDisplay.py?categId=109 - SuperB Workshops

Detector Layout – Reuse parts of Babar

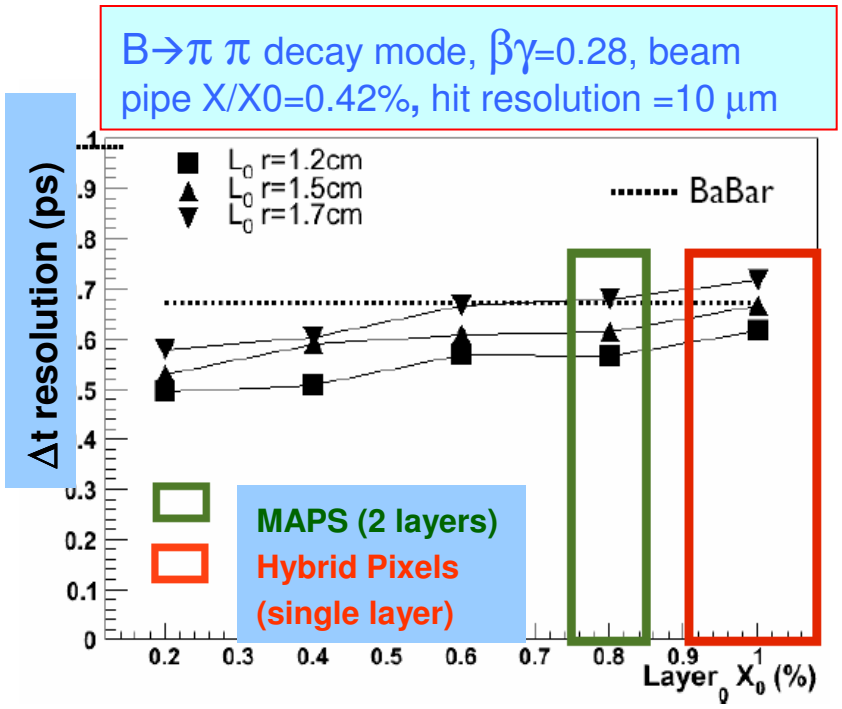


The SuperB Silicon Vertex Tracker



BaBar SVT

- 5 Layers of double-sided Si strip sensor
- Low-mass design. (P_t < 2.7 GeV)
- Stand-alone tracking for slow particles.
- 97% reconstruction efficiency
- Resolution ~15μm at normal incidence

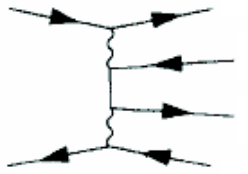


- The BaBar SVT technology is adequate for R > 3 cm: design similar to BaBar SVT
- Reduced beam energy asymmetry (7x4 GeV vs. 9x3.1 GeV) requires improved vertex resolution:
  - Layer0 very close to the IP (R~ 1.5 cm) with low material budget
- Background levels depends steeply on radius
  - Layer0 needs to have fine granularity and radiation tolerance
- Layer0 subject to large background and needs to be extremely thin: < 1 %X0

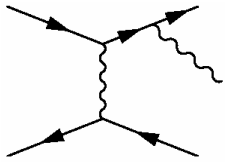
Main background sources

- BKG from luminosity

- **Pair (e+e-e+e-) production**
  - Low P_t make magnetic shielding effective
  - Issue for first layer of SVT
  - Hit Rate (hit/track multiplicity included) ~20MHz/cm^2 @ 1.5cm
  - equivalent fluence di 1 MeV neutron/yr (1 yr=10^7 s) = 3.7 10^{12} n/cm^2/yr
  - dose = 3 Mrad/yr

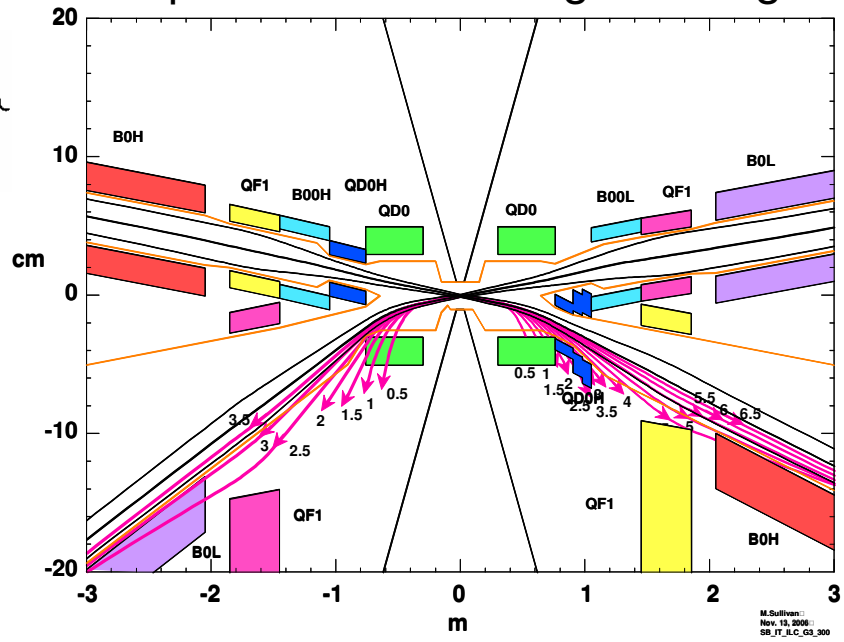


- **Radiative Bhabhas**
  - Beamline and shielding
  - Showering and backscattering extends to large radius
  - Rate 100kHz/cm^2 @ R=1.5 cm



- **Touschek Background**
  - Produced all along the ring, depending on emittance and bunch volume
  - Beam optics and collimator setting essential in controlling this background
  - Rate <10 kHz/cm^2 @ R=1.5 cm

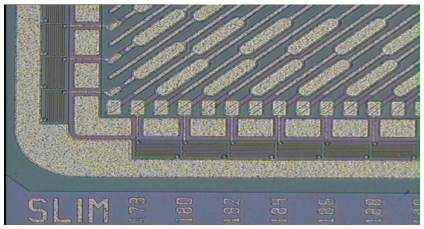
SuperB Interaction region design



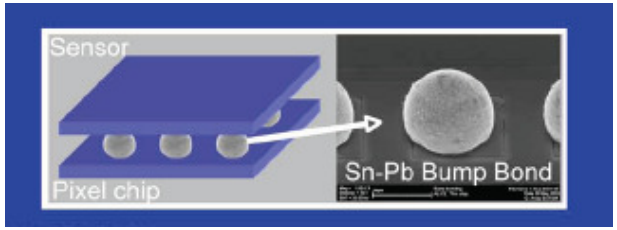
Layer0 Technology options

Complexity & performance

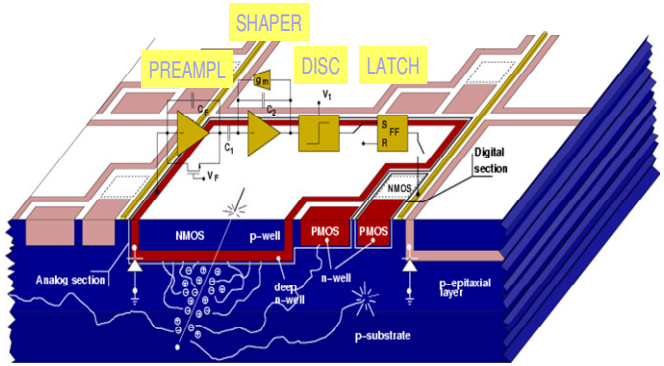
- **Striplets option:** mature technology, not so robust against background
  - Marginal with background rate higher than ~ 5 MHz/cm^2
  - Moderate R&D needed on module interconnection/mechanics/FE chip (candidate:FSSR2)



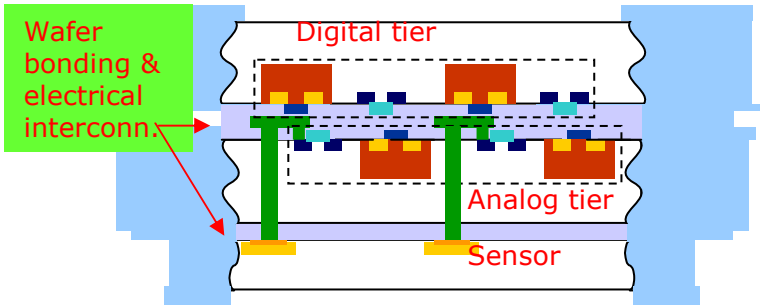
- **Hybrid Pixel Option:** viable with some R&D on pitch and material reduction→ baseline option for TDR in 2010
  - Reduction in the front-end pitch to 50x50 μm2 with data push readout developed for CMOS DNW MAPS.
  - First prototype FE chip submitted October 2009.



- **CMOS MAPS option:** new & challenging technology
  - Sensor & readout in 50 μm thick chip!
  - Extensive R&D (SLIM5-Collaboration) on
    - Deep N-well devices 50x50μm^2 with in-pixel sparsification.
    - Fast readout architecture implemented
  - CMOS MAPS with 4k pixels successfully tested with beams.



- **Thin pixels with Vertical Integration:**
  - Reduction of material and improved performance possible with the technology leap offered by vertical integration.
  - DNW MAPS with 2 tiers (Chartered/Tezzaron 130 nn submitted in August 2009.

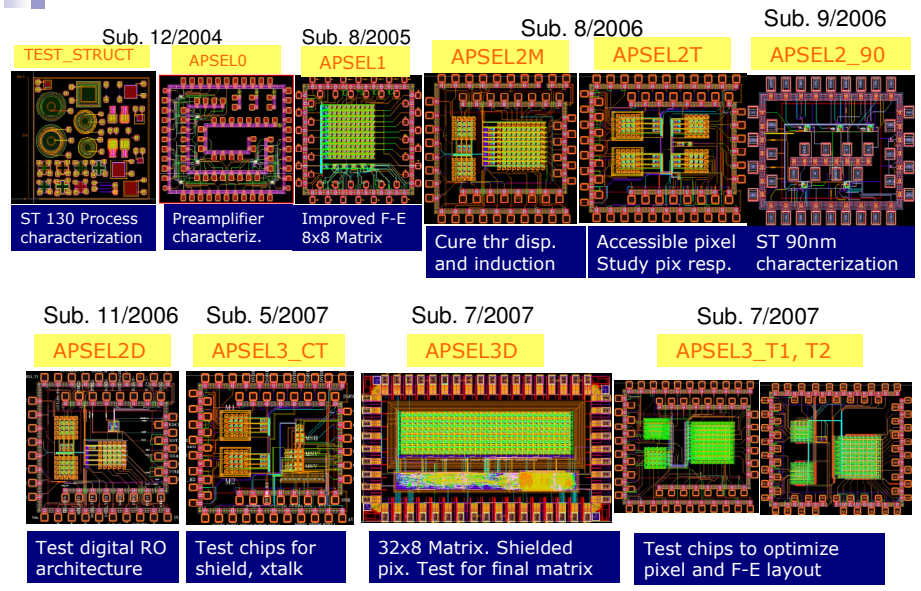


MAPS R&D

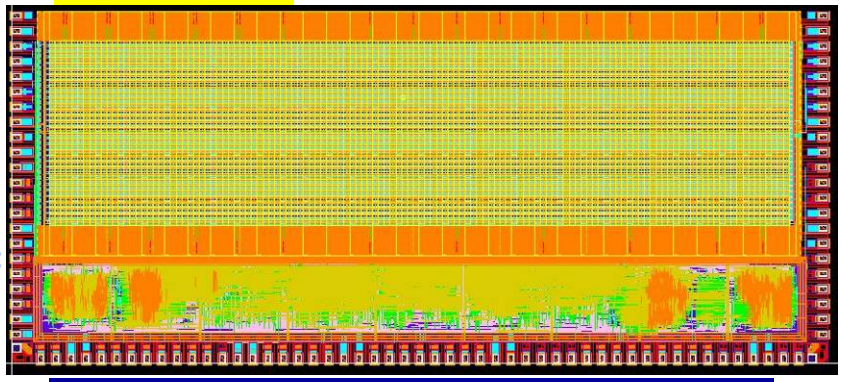
SLIM5 Collaboration

- Proof of principle (APSEL0-2)
  - first prototypes realized in 130 nm triple-well ST-Micro CMOS process
- APSEL3
  - 32x8 matrix with sparsified readout
  - Pixel cell optimization (50x50 um^2)
    - Increase S/N (15→30)
    - reduce power dissipation x2
- APSEL4D: 4K(32x128) 50x50 μm^2 matrix
  - data-driven sparsified readout + timestamp
  - Pixel cell & matrix implemented with full custom design and layout
  - Sparsifying logic synthetized in std-cell from VHDL model
  - Periphery inlcudes a "dummy matrix" used as digital matrix emulator
- Beam test in Sep 2008
  - Prototype MAPS module + striplets
- Radiation tests up to 10MRad
- Beam test in July 2009 (with ATLAS-LUCID):
  - New MAPS devices (APSEL5T, APSEL4D1)

Submitted MAPS Chips



APSEL4D sub 11/2007- rec 3/2008



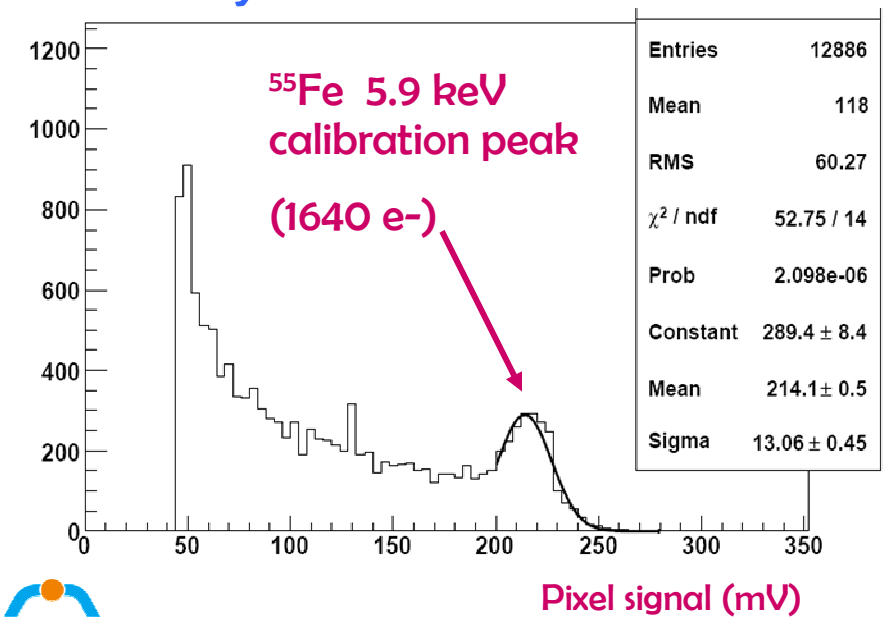
32x128 4k pixel matrix for beam test

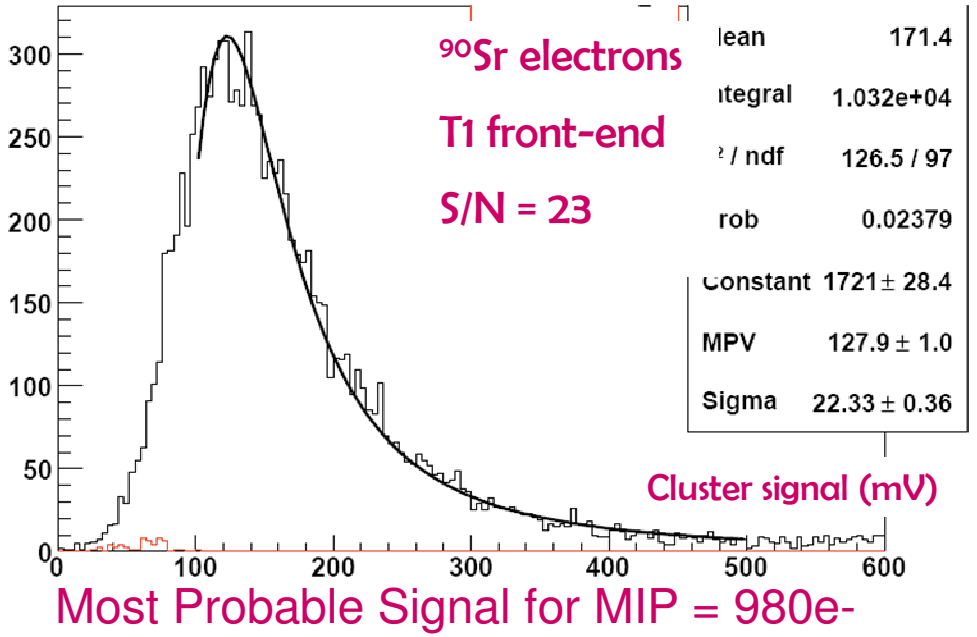
APSEL3 Chip Results

- Substantial redesign of the pixel cell in the APSEL3 chips with improved S/N and reduced power consumption (30 uW/ch)
- Major source of digital crosstalk reduced inserting a metal shield between digital lines and sensor
- But some digital crosstalk still present in the APSEL3 series, not fully understood.

Results obtained on 3x3 matrix with full analog readout

Front-end	ENC (e-)	Gain (mv/fC)	S/N (MIP)
T1	40-52	860	19-23
T2	27-36	1000	27-33

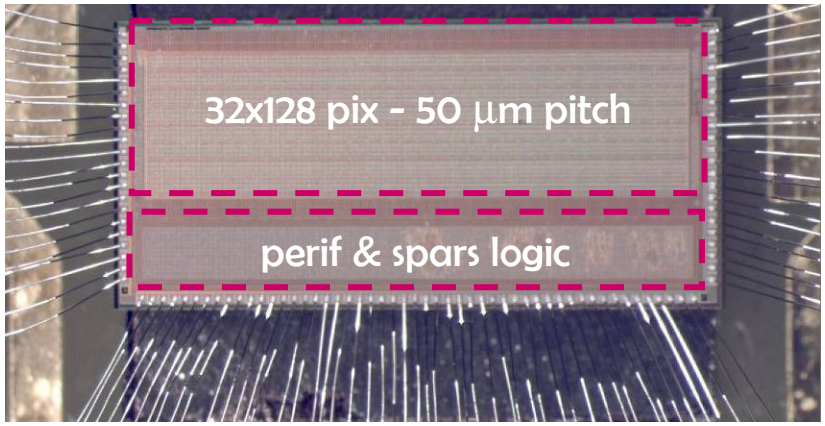


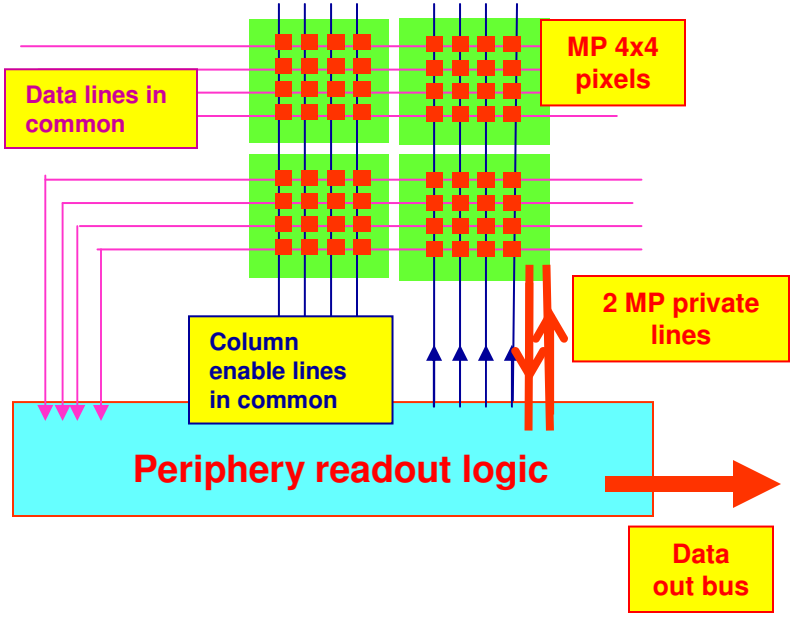


Most Probable Signal for MIP = 980e-

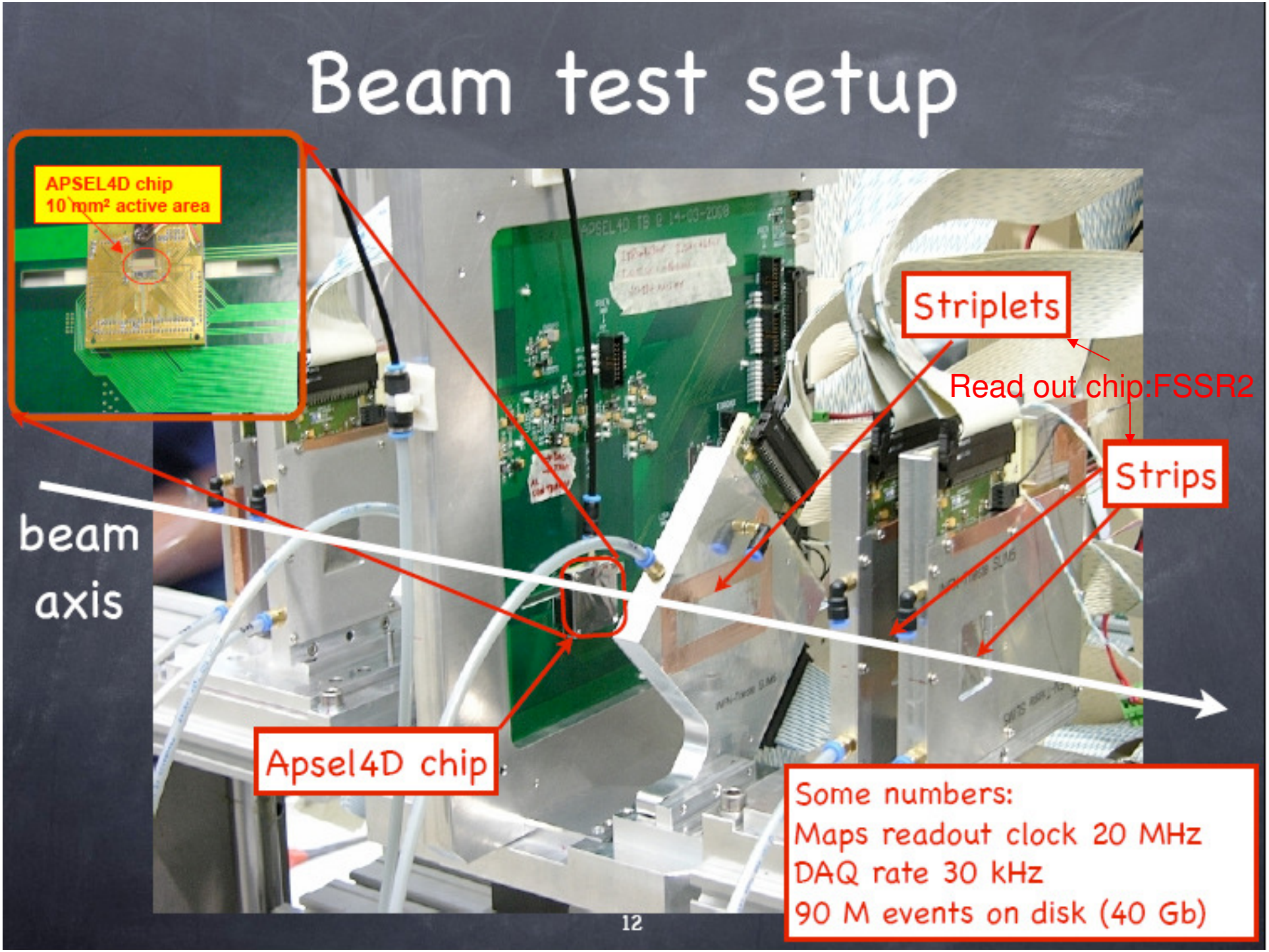
APSEL4D

- 4K(32x128) 50x50 μm² matrix subdivided in MacroPixel (MP=4x4) with point to point connection to the periphery readout logic:
  - Register hit MP & store timestamp
  - Enable MP readout
  - Receive, sparsify, format data to output bus
- Data driven architecture
  - Interface to Associative memory trigger boards (CDF style)
  - Useful for Bhabha rejection trigger
- Readout tests
  - All readout functionality tested with dummy matrix.
    - Dummy pixels can be set and correctly readout, with the right timestamp associated.
  - The readout is working properly even with 100% occupancy.
  - Three clocks are used: the BCO clock, used for the timestamp counter, a faster readout clock, and a slow control clock.
  - Test performed with RDCLK up to 50 MHz



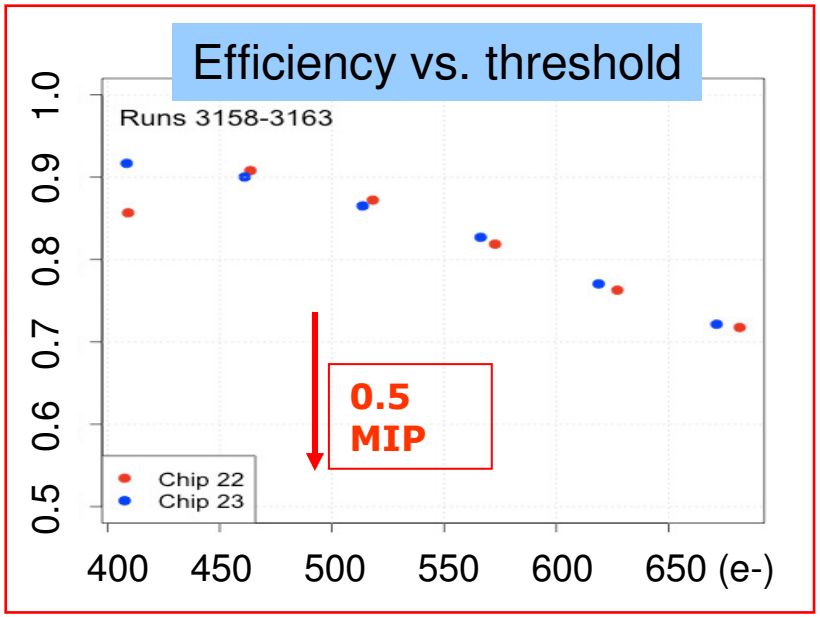


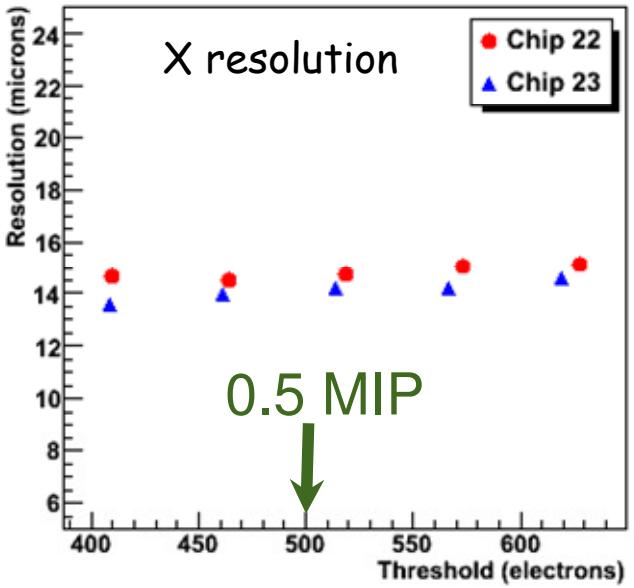
Beam test setup

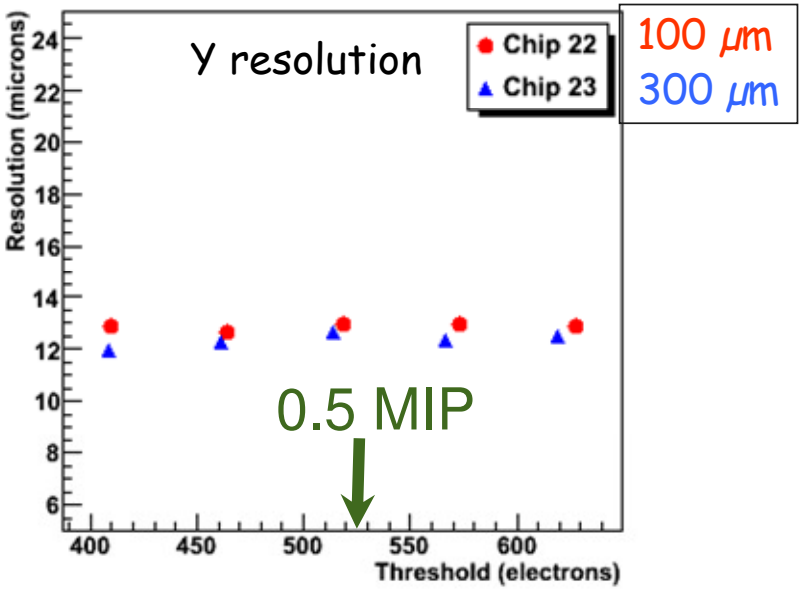


APSEL4D Beam Test Results

- Hit efficiency about 92%
  - The competitive N-wells in pixel cell steal charge, reducing the hit efficiency
- Room for improvement by acting on the collecting electrode geometry (satellite N-wells surrounding competitive N-wells)
- Intrisinc resolution ~ 14 μm compatible with digital readout.
- Data-push r.o. architecture → first demonstration of LVL1 capability with silicon tracker information sent to Associative Memories

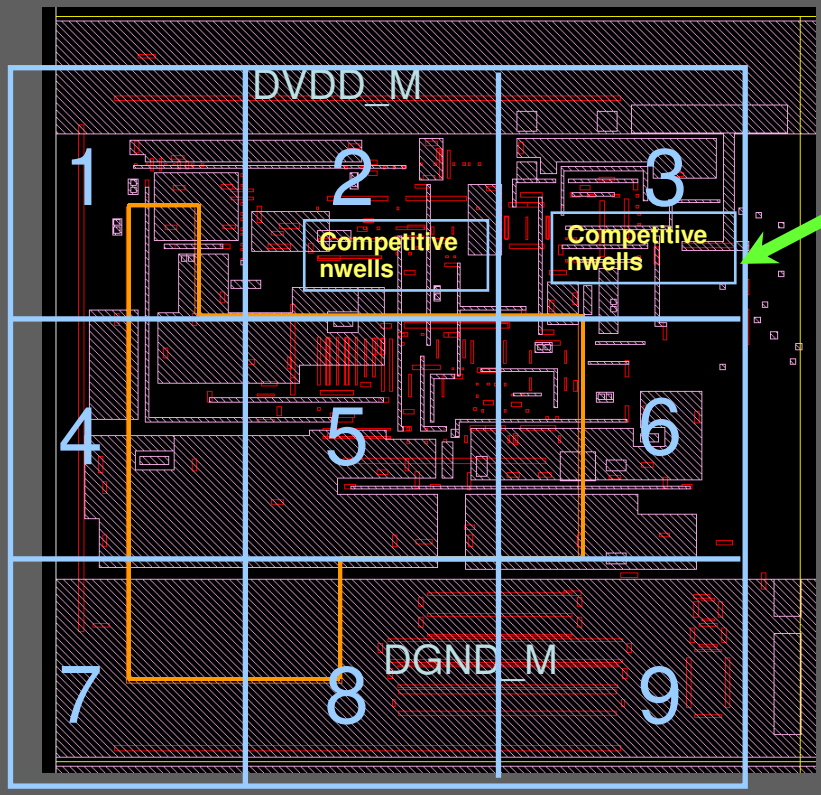




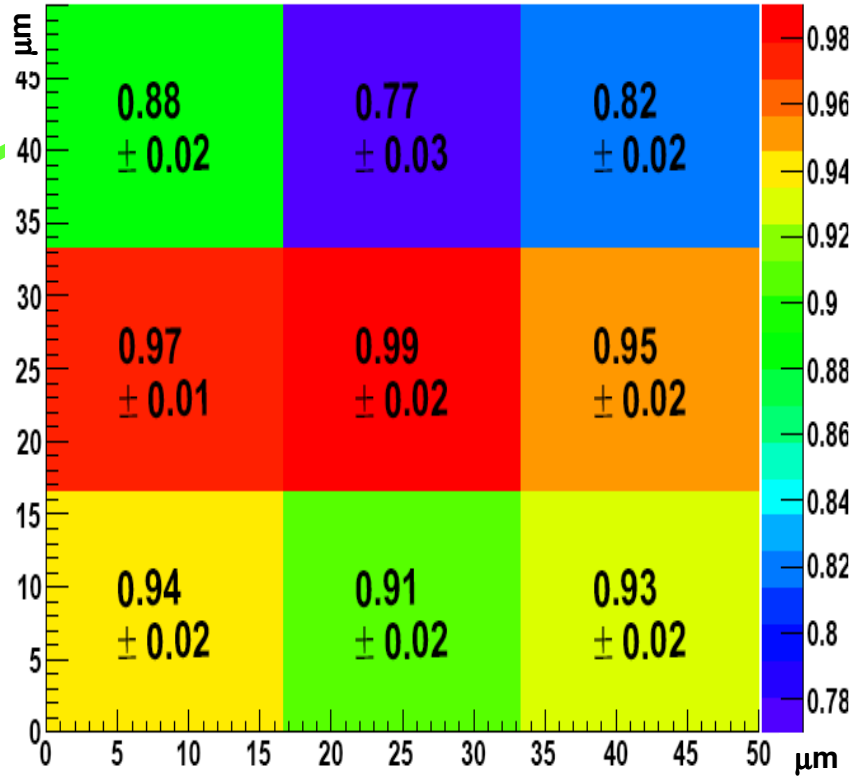


(chip-thickness independent)

MAPS efficiency vs position within pixel



Correspondence between the pixel layout and the efficiency map.



Efficiency map inside pixel cell. Cross feed unfolded results.

Radiation Damage Tests

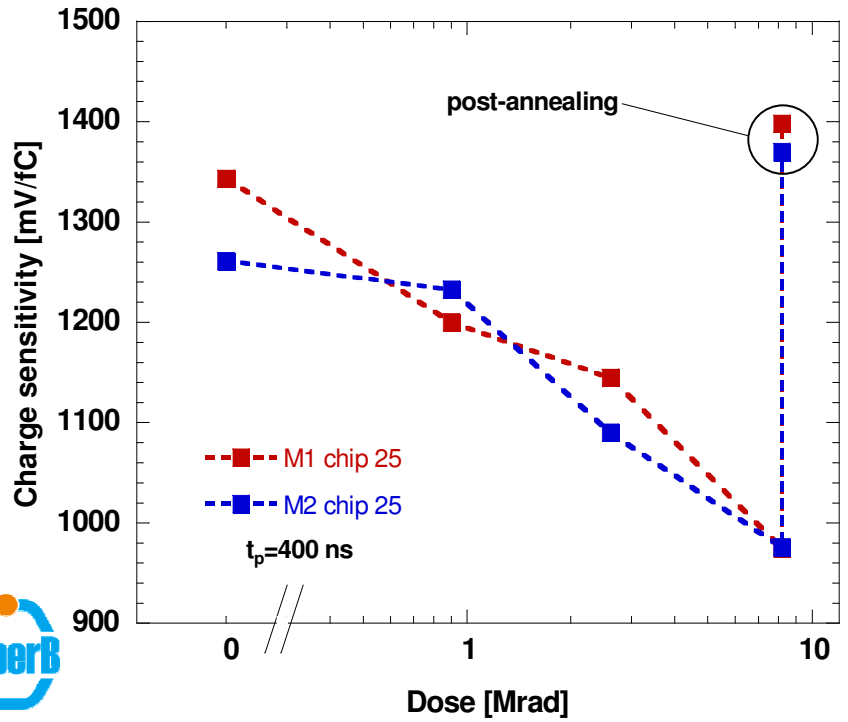
^{60}Co γ-ray irradiation, with final 100°C/168h annealing

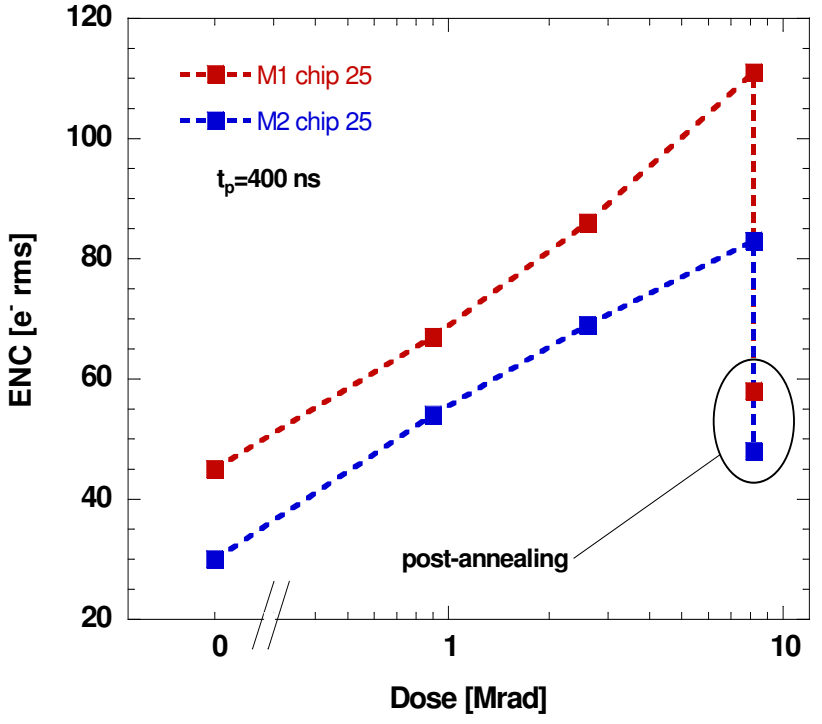
- ~10 Mrad maximum integrated dose, 9 rad/s dose rate, MAPS biased during irradiation as in real application

• Charge sensitivity G_Q decreases with dose; the decrease after 900 krad is compatible with the decrease observed in Apsel2T after 1.1 Mrad

• ENC increases with dose; the increase after 900 krad is larger than the increase detected in Apsel2T after 1.1 Mrad at similar peaking times (due to different W, finger number and drain current in the input device)

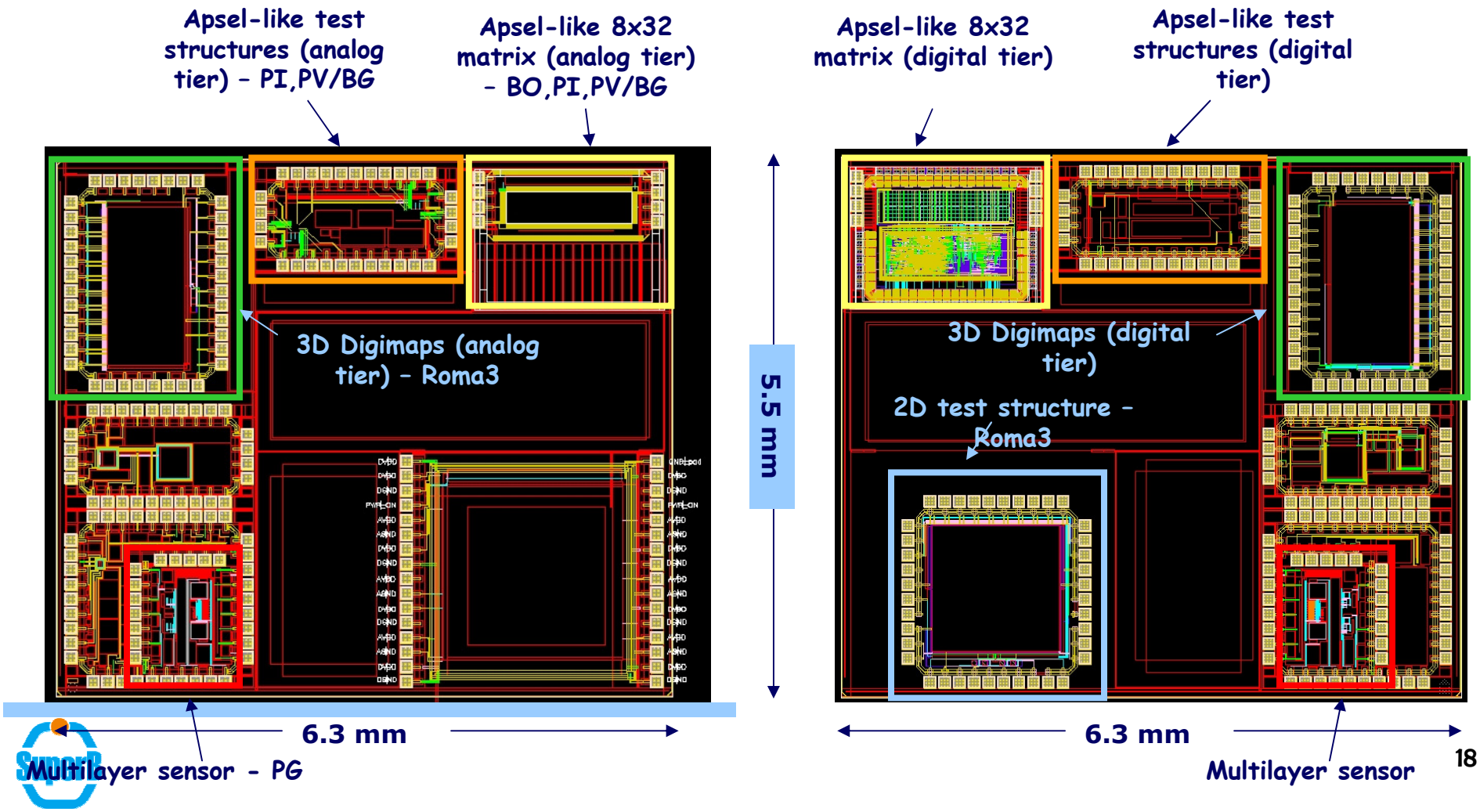
• Significant recovery after 100°C/168h annealing cycle





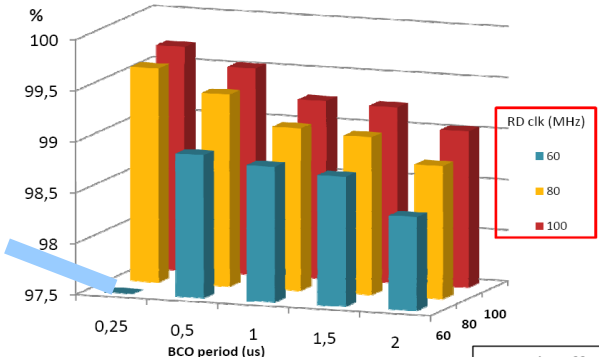
CMOS MAPS with Vertical integration

First MAPS devices realized on 2 layers (analog/digital) submitted for Chartered/Tezzaron 130 nm run.
Now in production → results Fall 2009 (VIPIX)



Activities on Hybrid Pixel

VHDL simulation:
r.o. Efficiency > 98%
@ 60 MHz RDclk

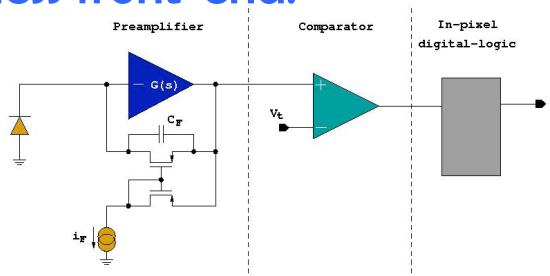


Produce a prototype front-end chip for high-Ω pixels with 50x50 um² pitch & fast enough readout (bkg rate~ 100 MHz/cm²)

Front-end Chip & Pixel sensor matrix layout almost completed (in production Oct. 09):

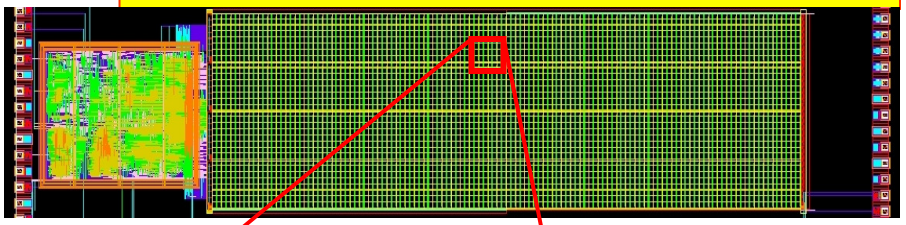
- FE chip: ST 130 nm process
- Sensors(200 um): FBK-IRST

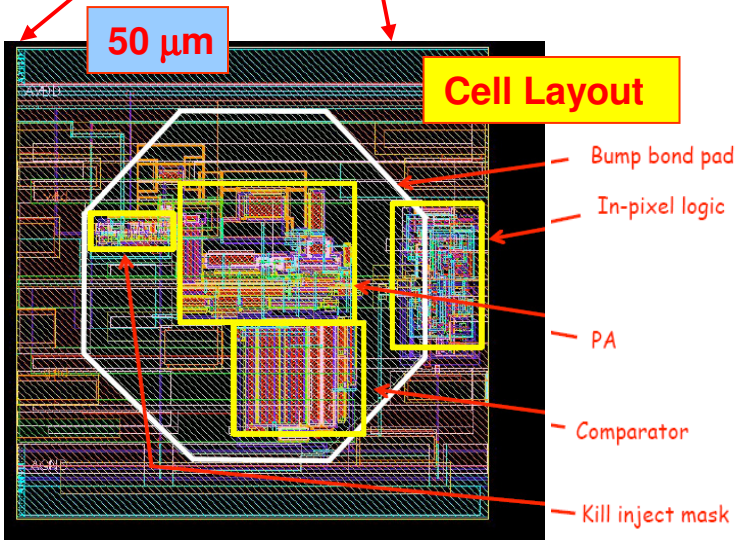
Shaper-less front-end:



- I_{AVDD}~ 2.1 uA → P ~ 2.5 uW/ch
- G ~ 50 mV/fC
- ENC = 150e- with C_D=100 fF (200e- @200fF)
- V_{th} dispersion ~ 350 e-
- Recovery time linear with signal amplitude

FE chip Layout (32x128) – preliminary





Sensor + chip bump-bonding next spring (IZM-Berlin) → Test-beam Sept. 2010.

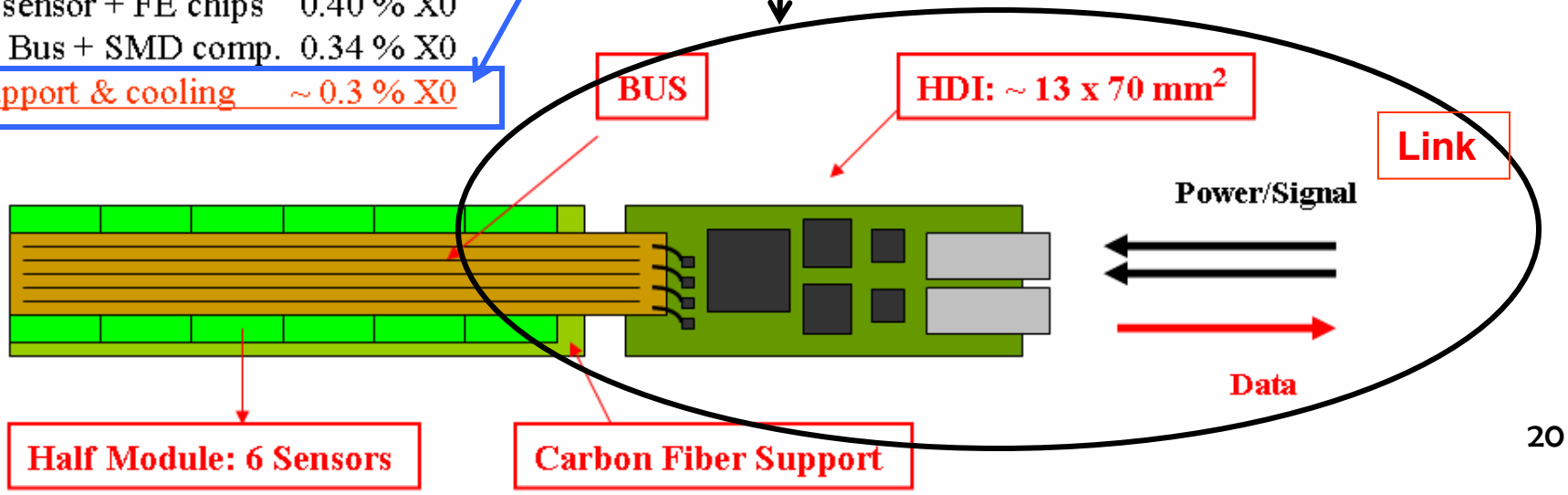
Pixels L0 Module Specifications

Key R&D items on Layer0 for TDR

1. Front-end chip for high resistivity pixels
2. Multichip pixel module interfaces
3. Light Module support and cooling

Layer 0: Hybrid Pixels		
Radius:	~ 1.5 cm	
Module length:	~ 10 cm	
Pixel Pitch:	50x50 µm2	
Hit Rate:	110 MHz/chip	(safety > 5)
Module Rates:	660 MHz	
Link Bandwidth:	20 Gbps	Full Rate (FE data push)
	3 Gbps	Triggered Rate
Power consumption:	~ 2 W/cm^2	in the active area
	~ 50 (mW/Gbps)/cm^2	in HDI
Total material budget:	~ 1% X0	

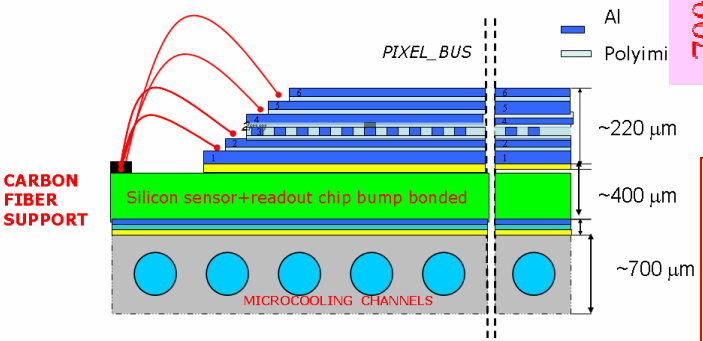
- Si sensor + FE chips 0.40 % X0
- Al Bus + SMD comp. 0.34 % X0
- Support & cooling ~ 0.3 % X0



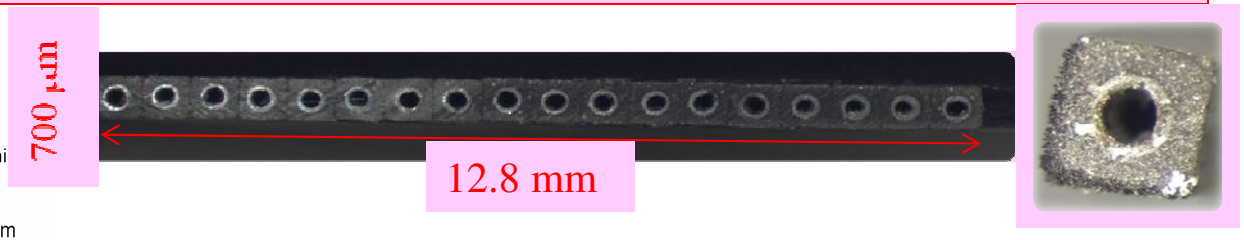
Light pixel module support & cooling

- Light support with integrated cooling needed for pixel module: P=2W/cm^2
- Carbon Fiber support with micro-channel for coolant fluid developed:
  - **Total support/cooling thickness = 0.28 % X_0 (reduction to 0.2% X_0 possible)**

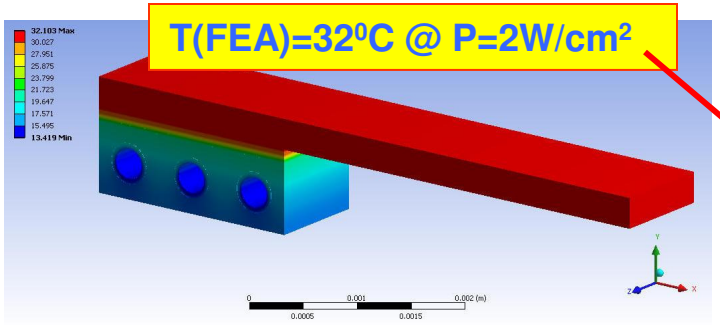
Layer0 module cross section

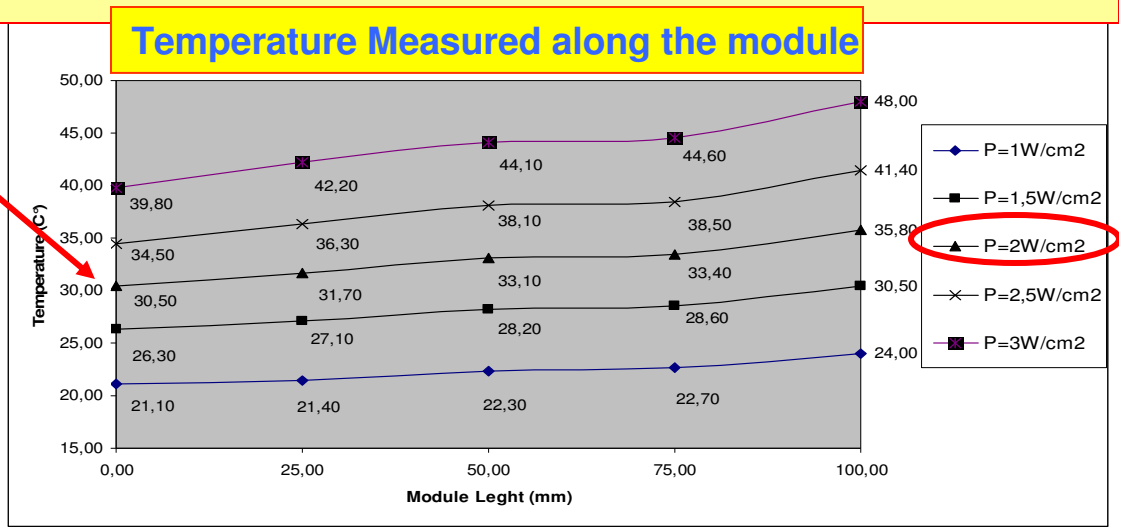


Note: drawing not to scale



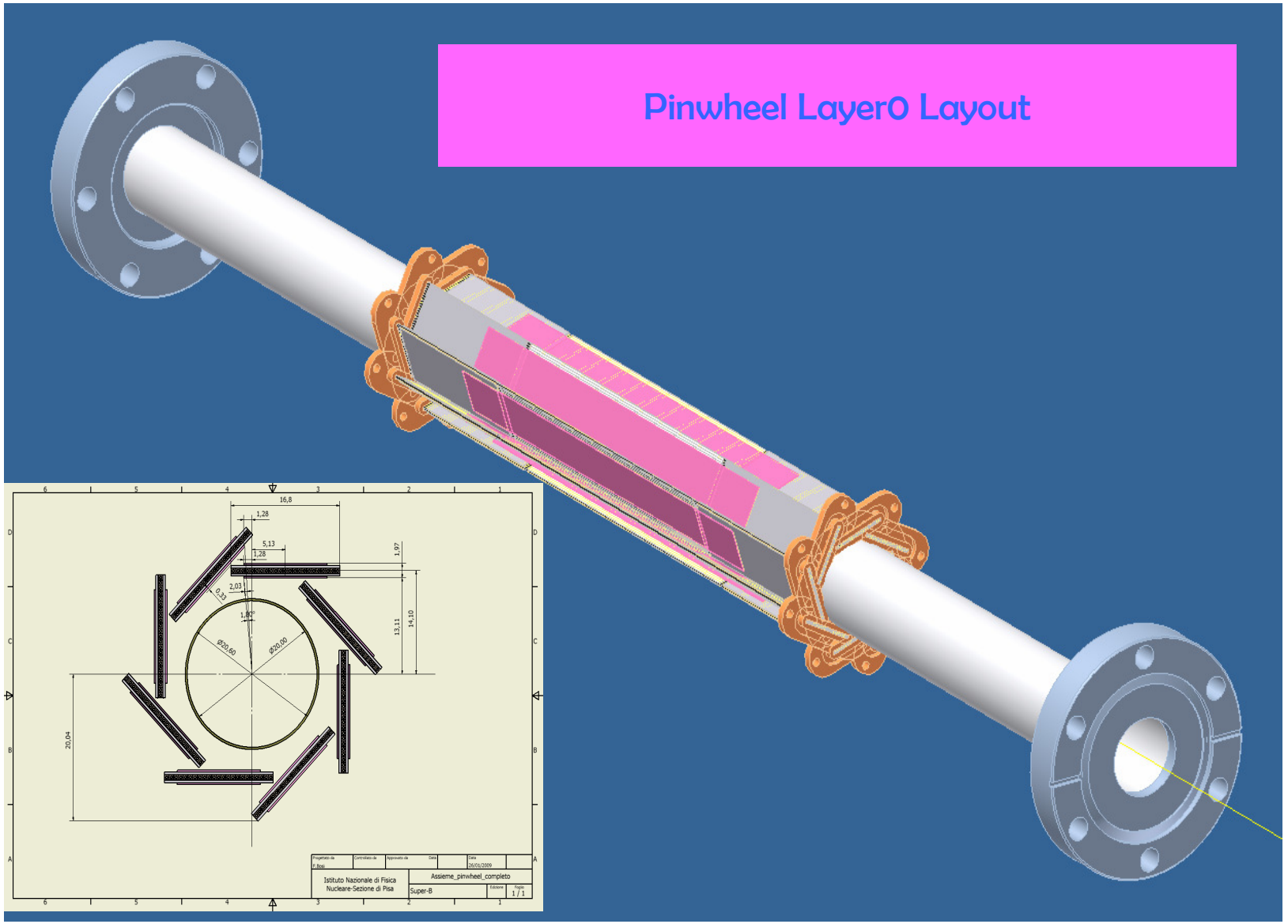
- Prototypes characterized in the Thermo-fluid-dynamics LAB in Pisa varying the specific input power (1-3W/cm2)
- Measurements confirmed FEA simulation results: T_meas=30-36°C @ P=2W/cm^2





L0 Mechanical integration

Pinwheel Layer0 Layout

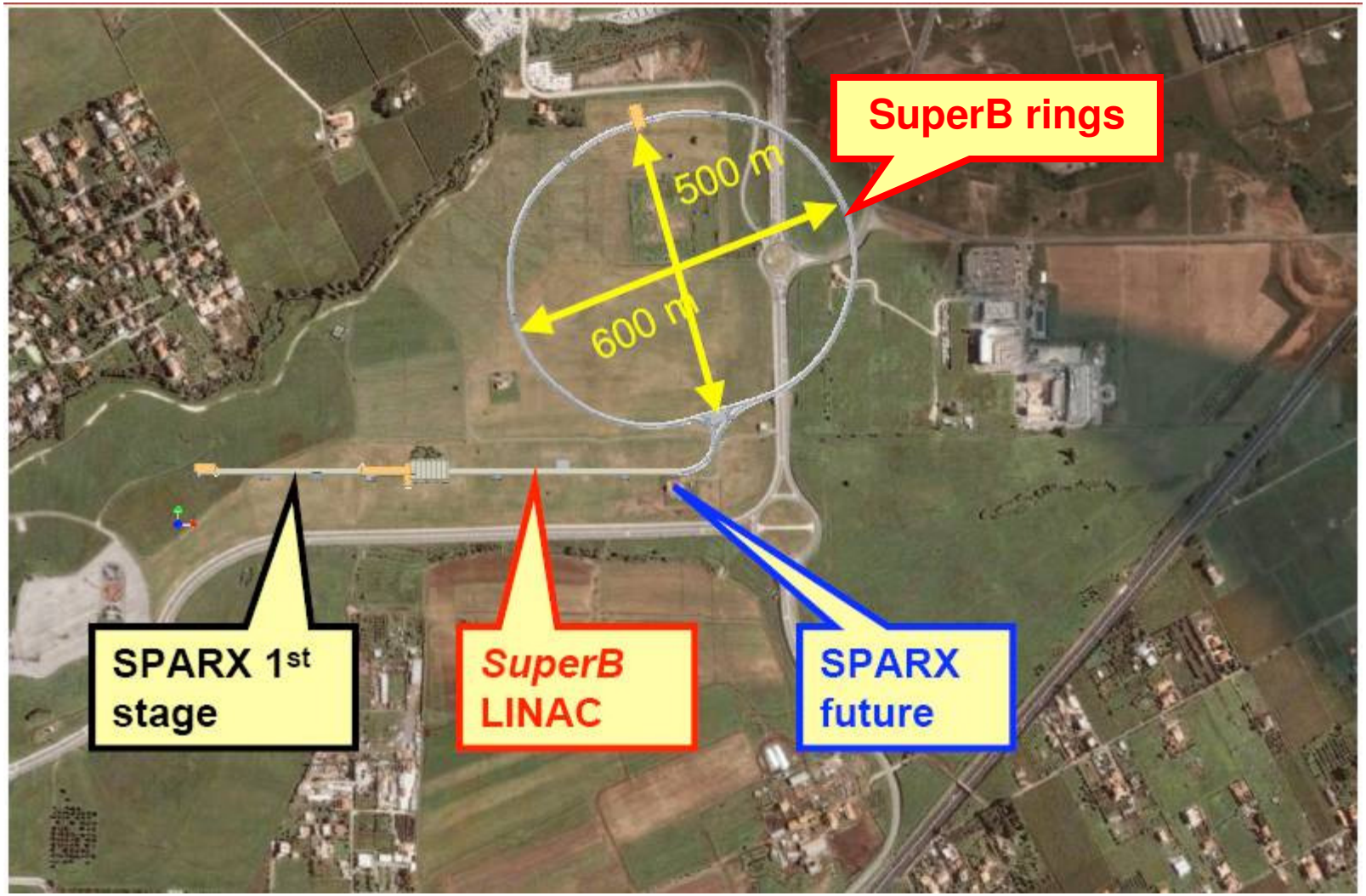


SuperB Status and outlook

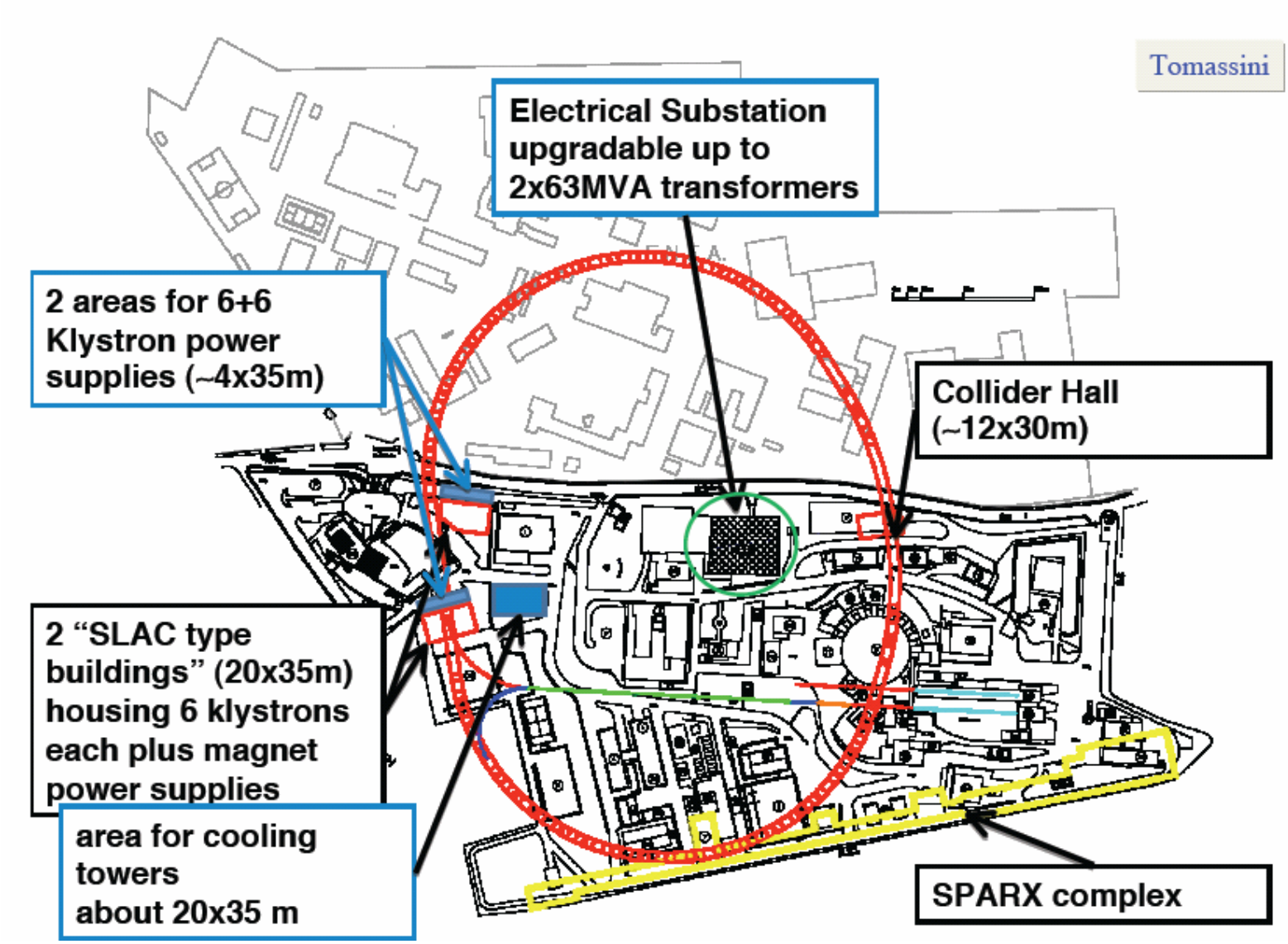
- The physics case for a high luminosity B Factory is clearly established.
- The SuperB accelerator concept (verified with the tests on Dafne) allows to reach and exceed the 10^{36} threshold.
- All scientific reviews are positive. Presented to CERN Council and approved for preparatory phase.
- Growing international interest and participation with formal international collaboration being formed. Project structure defined.
- R&D is proceeding on various items (eg. SVT Layer0)
- TDR phase approved by INFN. MOUs in preparation
- Next steps are:
  - Intermediate report: end of 2009
  - Government DECISION on project approval in very few months: presented as major scientific infrastructure
  - Technical Design Report by 2010
- Start operation by 2015.

BACKUP SLIDES

SITES : Tor Vergata……..



LNF option


Tomassini
Electrical Substation upgradable up to 2x63MVA transformers
2 areas for 6+6 Klystron power supplies (~4x35m)
Collider Hall (~12x30m)
2 "SLAC type buildings" (20x35m) housing 6 klystrons each plus magnet power supplies
area for cooling towers about 20x35 m
SPARX complex

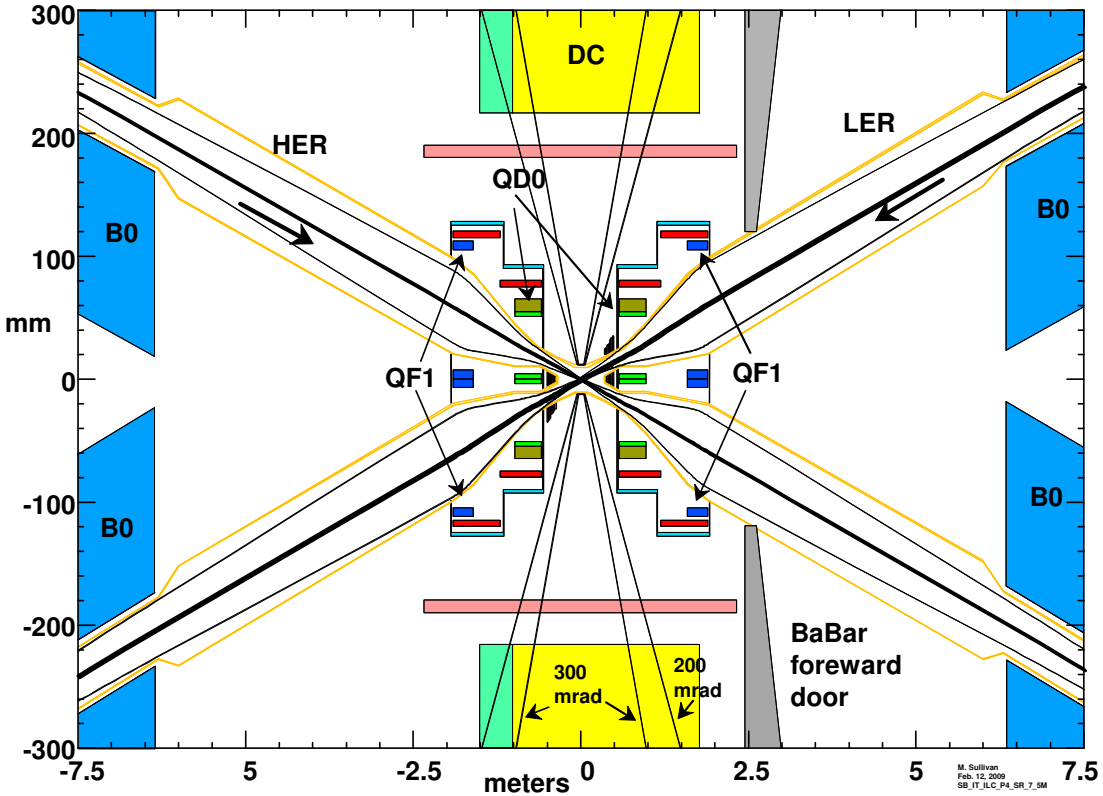
Mini Mac report – Apr 24

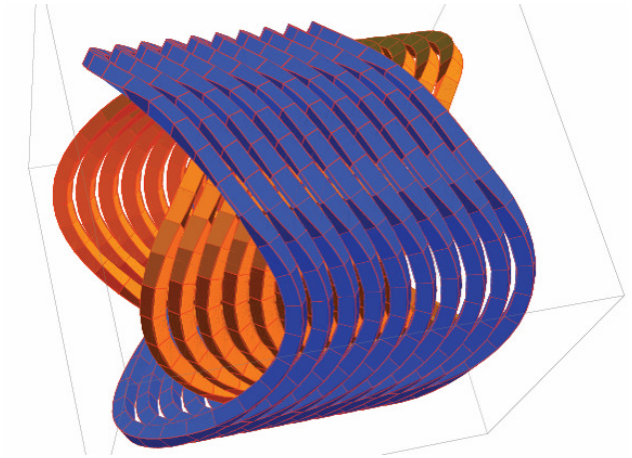
Committee: Klaus Balewski (DESY), John Corlett (LBNL), Jonathan Dorfan (SLAC, Chair), Stuart Henderson (ORNL), Tom Himel (SLAC), Claudio Pellegrini (UCLA) , Daniel Schulte (CERN), Ferdi Willeke (BNL), Andy Wolski (Liverpool), Frank Zimmermann (CERN)

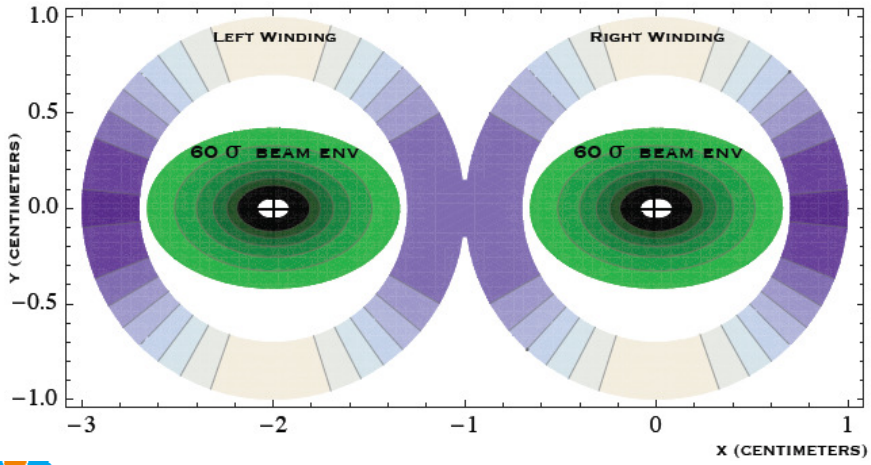
- "The MAC now feels secure in enthusiastically encouraging the SuperB design team to proceed to the TDR phase, with confidence that the design parameters are achievable." Recent strong progress:
  - Crab waist tests at DAFNE
  - Beam-beam measurements (DAFNE) and simulations
  - IR design
  - Lattice
  - Polarization spin rotators

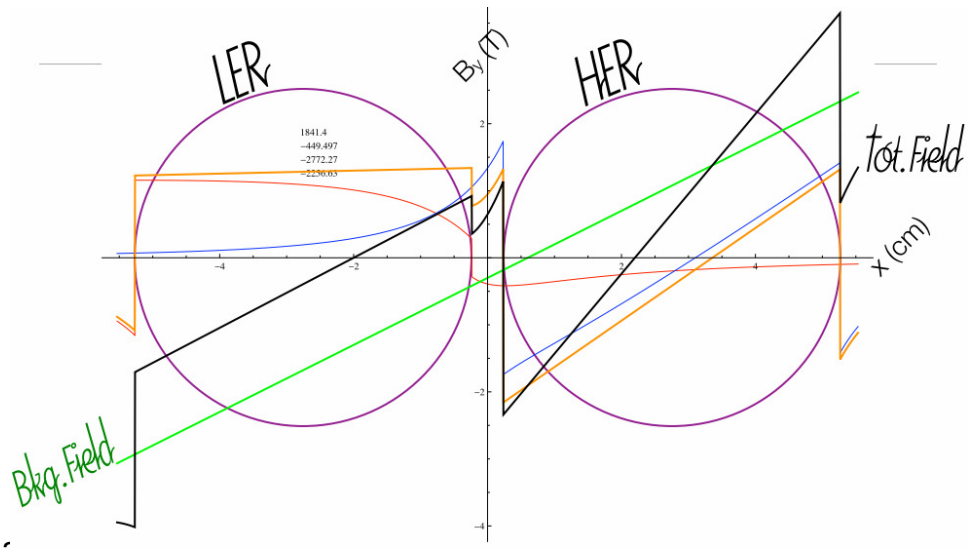
- "Nonetheless, much detailed work remains to bring the design to the level where (a) *ground-breaking,* (b) *final engineering of accelerator components* can commence." Further needed work areas:
  - Emittance tuning and evaluate tolerances
  - Dynamic aperture calculations
  - IR and arc vacuum systems
  - Injection system
  - Vibration studies
  - Polarization lattice

Interaction Region and SC Quadrupoles

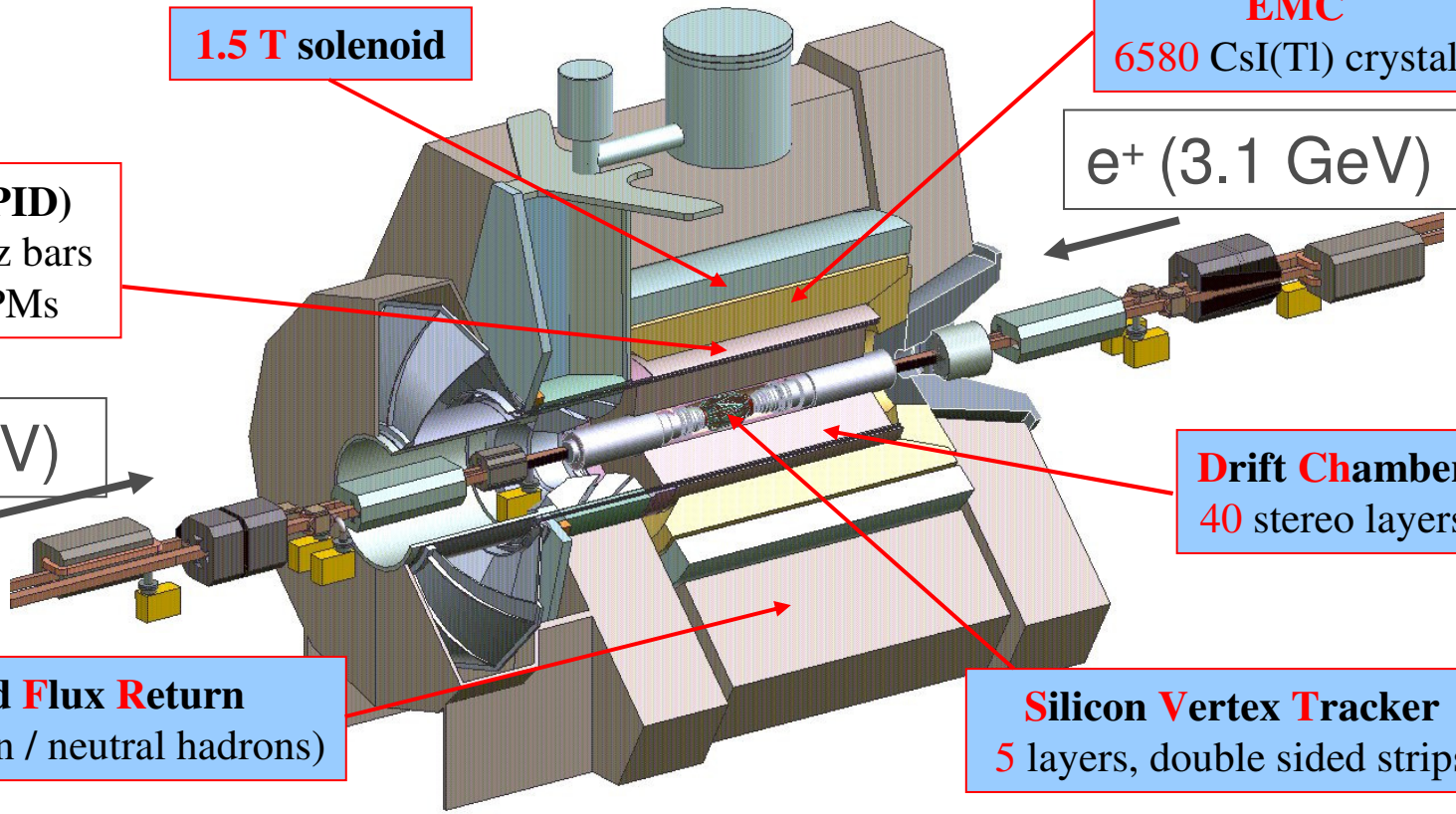








The BABAR Detector



SVT: 97% efficiency, 15 μm z hit resolution (inner layers, perp. tracks)

SVT+DCH: $\sigma(p_T)/p_T = 0.13\ \% \times p_T + 0.45\ \%$, $\sigma(z_0) = 65$ @ 1 GeV/c

DIRC: K-π separation 4.2 σ @ 3.0 GeV/c → 2.5 σ @ 4.0 GeV/c

EMC: $\sigma_E/E = 2.3\ \% \cdot E^{-1/4} \oplus 1.9\ \%$

PARAMETERS

J.Seeman @MiniMac

LER/HER	Unit	June 2008	Jan. 2009	March 2009	LNF site
E+/E-	GeV	4/7	4/7	4/7	4/7
L	$cm^{-2}\ s^{-1}$	$1x10^{36}$	$1x10^{36}$	$1x10^{36}$	$1x10^{36}$
I^+/I^-	Amp	1.85 /1.85	2.00/2.00	2.80/2.80	2.70/2.70
N_{part}	$x10^{10}$	5.55 /5.55	6/6	4.37/4.37	4.53/4.53
N_{bun}		1250	1250	2400	1740
I_{bunch}	mA	1.48	1.6	1.17	1.6
$\theta/2$	mrad	25	30	30	30
β_x^*	mm	35/20	35/20	35/20	35/20
β_y^*	mm	0.22 /0.39	0.21 /0.37	0.21 /0.37	0.21 /0.37
ε_x	nm	2.8/1.6	2.8/1.6	2.8/1.6	2.8/1.6
ε_y	pm	7/4	7/4	7/4	7/4
σ_x	µm	9.9/5.7	9.9/5.7	9.9/5.7	9.9/5.7
σ_y	nm	39/39	38/38	38/38	38/38
σ_ε	mm	5/5	5/5	5/5	5/5
ξ_x	X tune shift	0.007/0.002	0.005/0.0017	0.004/0.0013	0.004/0.0013
ξ_y	Y tune shift	0.14 /0.14	0.125/0.126	0.091/0.092	0.094/0.095
RF stations	LER/HER	5/6	5/6	5/8	6/9
RF wall plug power	MW	16.2	18	25.5	30.
Circumference	m	1800	1800	1800	1400

An example of sensor optimization

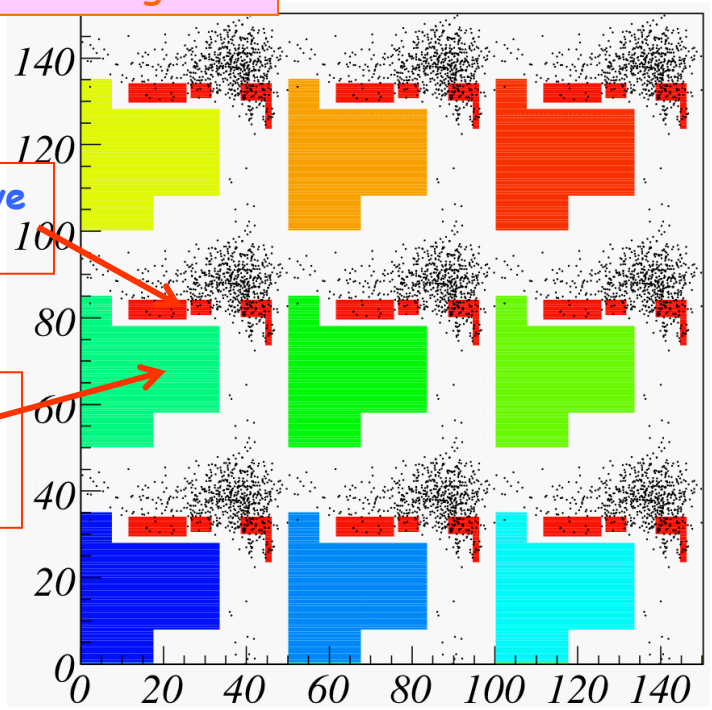
Optimize sensor geometry for charge collection efficiency with fast simulation developed:

- Locate low efficiency region inside pixel cell
- Add ad hoc "satellite" collecting electrodes

3x3 MATRIX present sensor geom

Competitive Nwells

DNW collecting electrode



3x3 MATRIX sensor optimized

Satellite nwells connected to central DNW elect