

Radiation detection: novel approaches and readout capabilities exploiting latchup topology via bipolar, MOSFET and MESFET transistors

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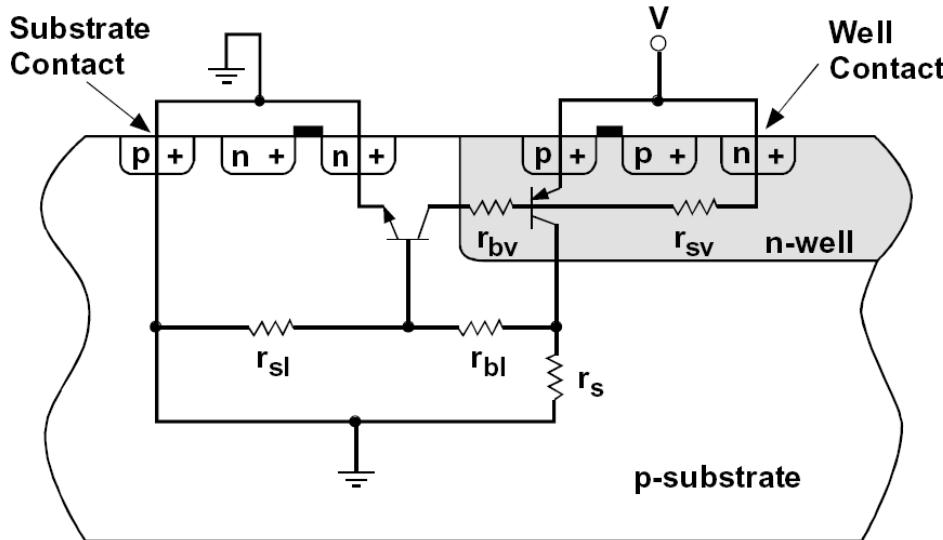
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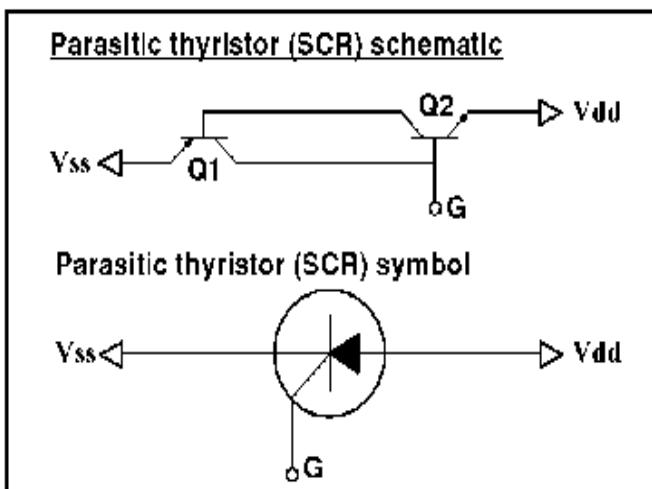
Outline

- Introduction to the Latchup Effect
- First tests via commercial **BJTs**
- Collaboration: Bologna, RAL(STFC), Poli_Turin
 - Use of **MOS** transistors
- The CREE 24010 **SiC MESFET**

What the “Latchup Effect” is

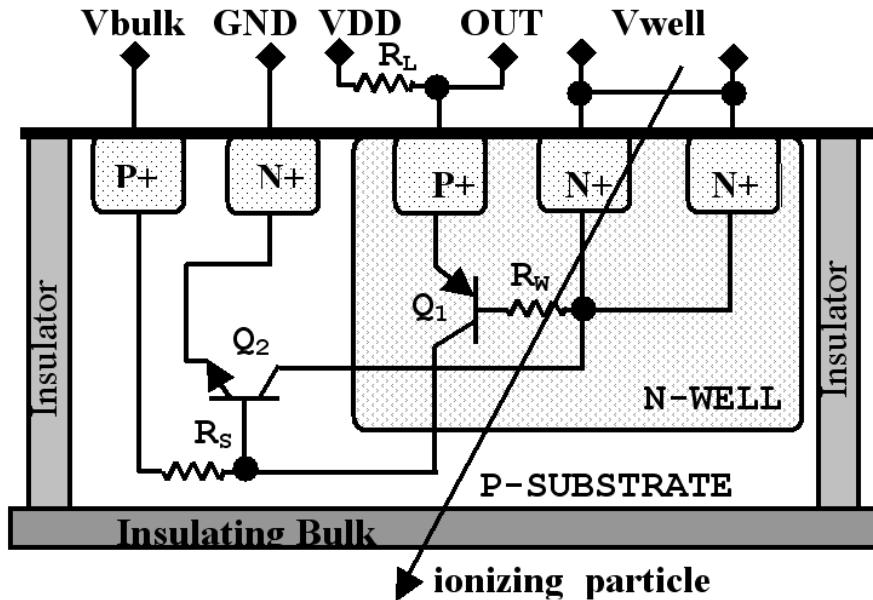


Basically, it is an ignition of a parasitic thyristor-like structure within a CMOS device and is ignited by induced charges inside the silicon whatever their origin.



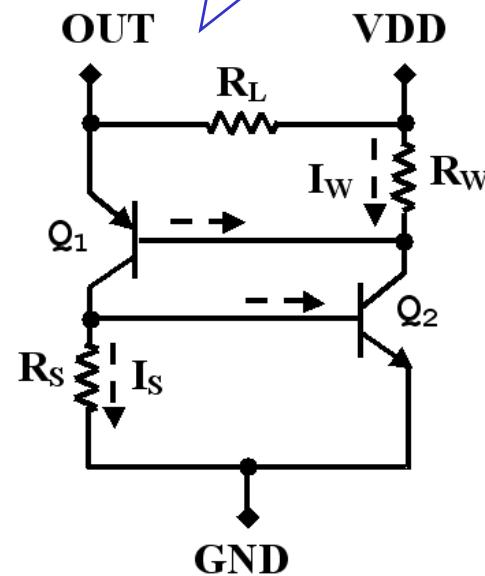
Traditional CMOS technologies into radiation environments may be susceptible and damaged by latchup

First study since 2005

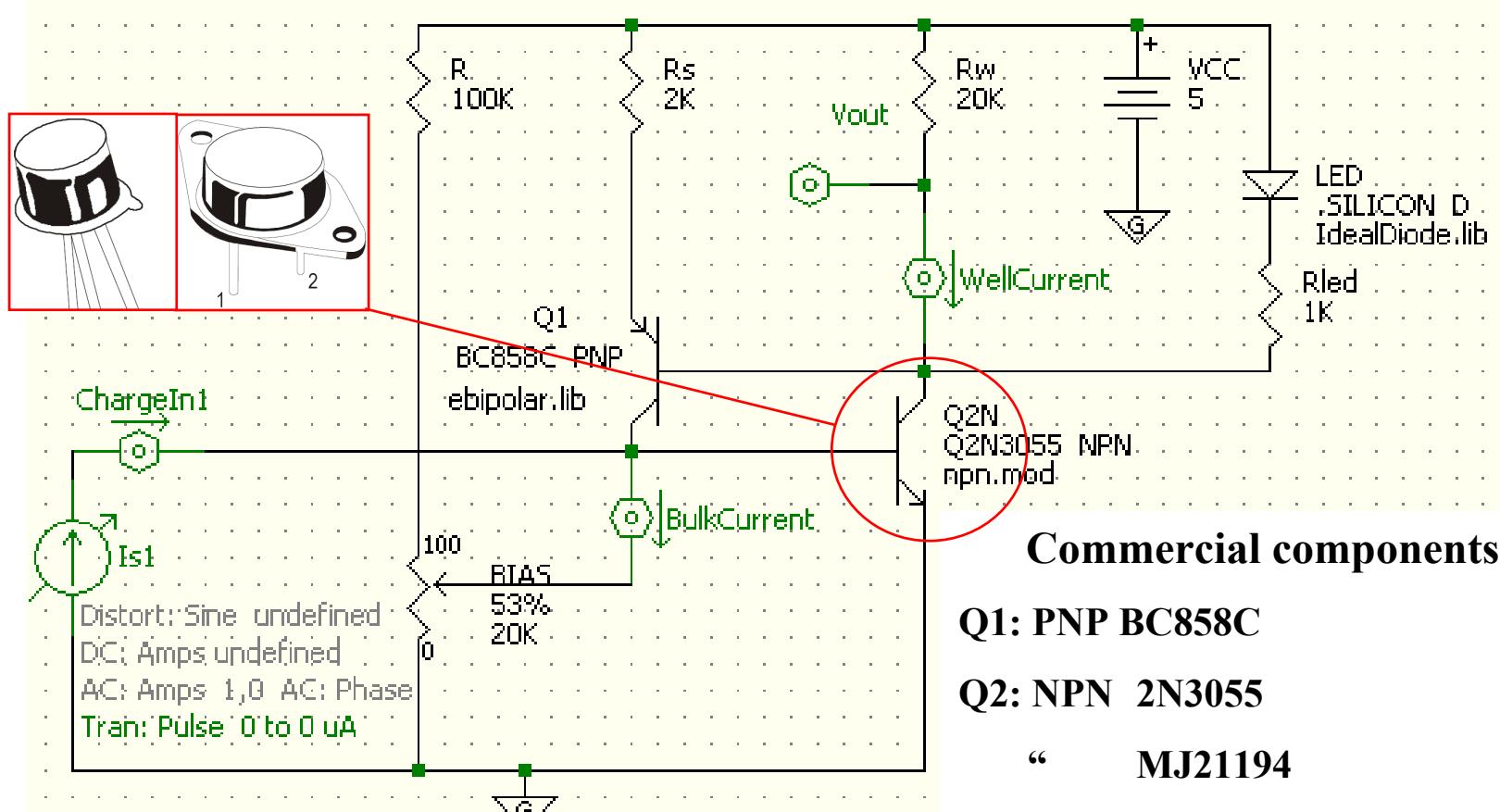


It is not a reverse-biased diode plus the transistor has an internal current gain

If (V_{WELL} is V_DDD) and
(V_{BULK} is GND) then



A Prototype



Commercial components

Q1: PNP BC858C

Q2: NPN 2N3055

“ **MJ21194**

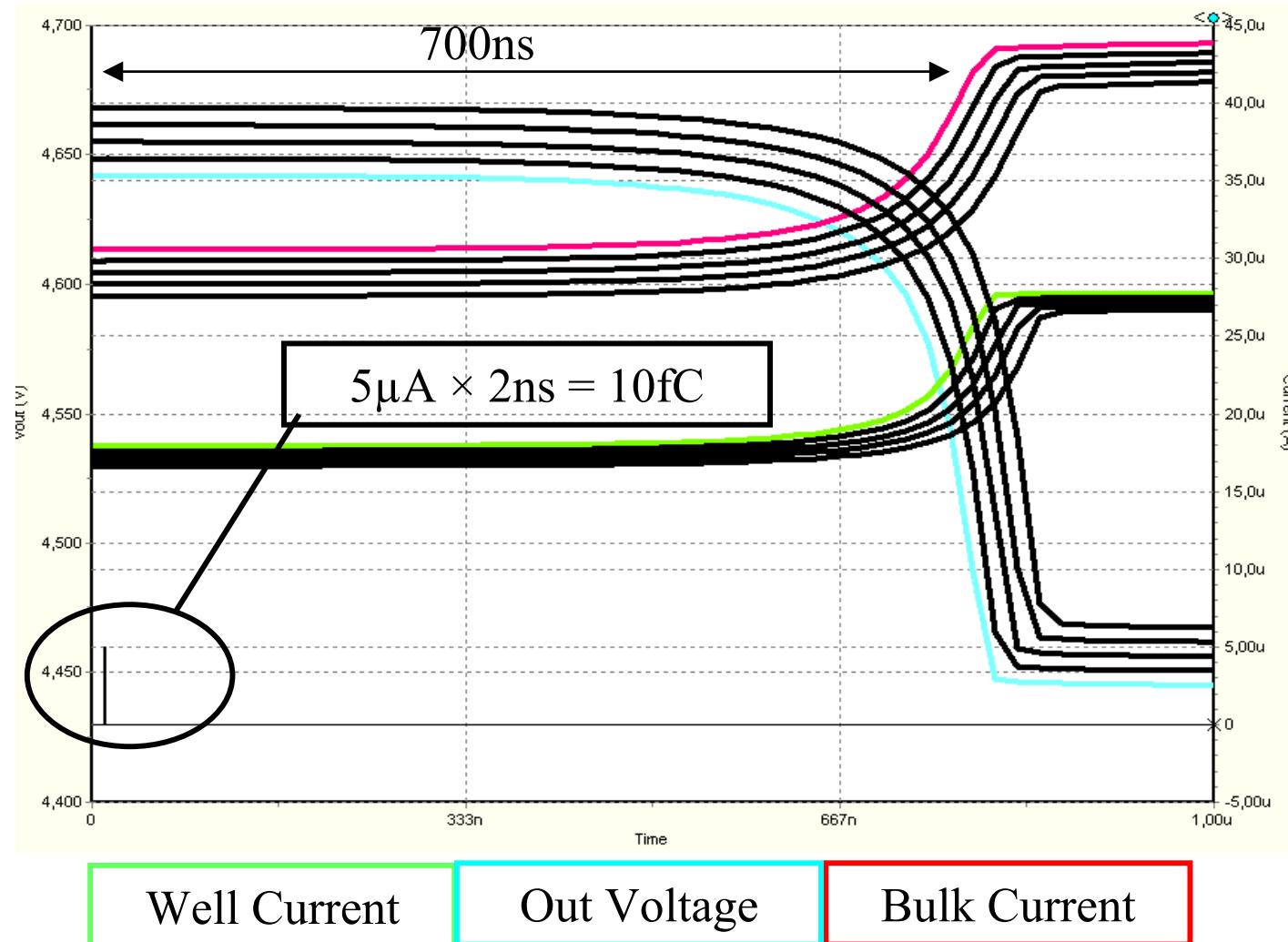
“ **BFY52**

“ **2N2222A**

R_N : multturn variable resistors

Spice simulation (Q2=BFY52)

Temperature from 30 to 40°C



Commercial bipolars used

Q2 = 2N2222A BFY52 2N3055



TO-18 metal can

Estimated B-E
charge collection
area

$10 \div 100 \mu\text{m}^2$

TO-39 metal can

Estimated B-E
charge collection
area

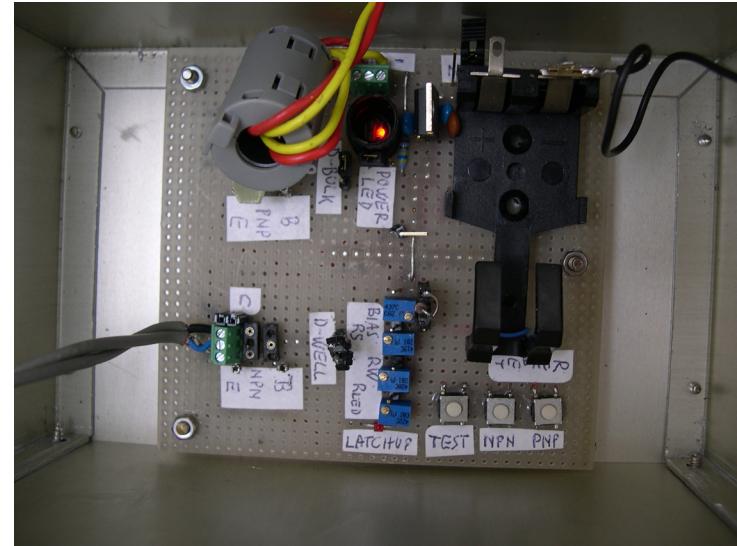
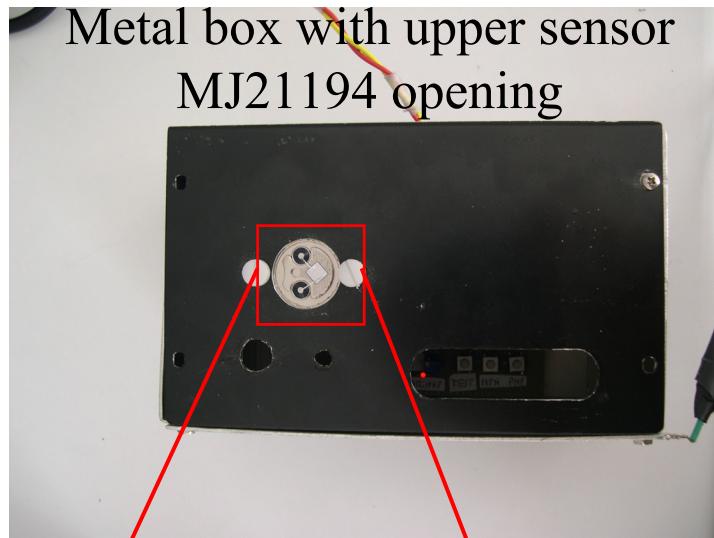
$100 \div 10000 \mu\text{m}^2$

TO-3 metal can

Estimated B-E
charge collection
area

1 mm^2

Prototype Construction (Q2=MJ21194)



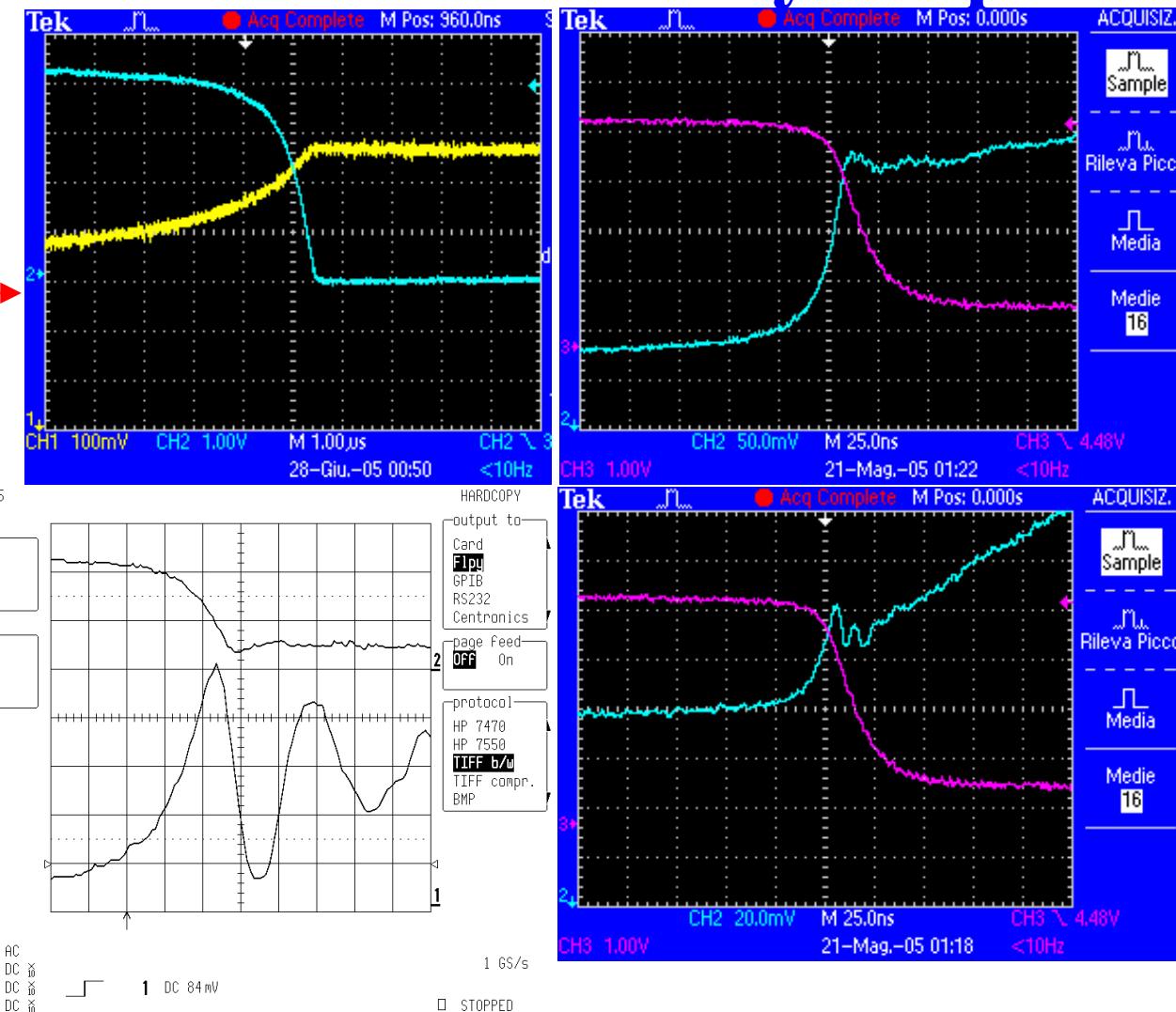
The latchup circuit inside the box

Transistor Base-Emitter bondings of the power bjt MJ21194

Laboratory test

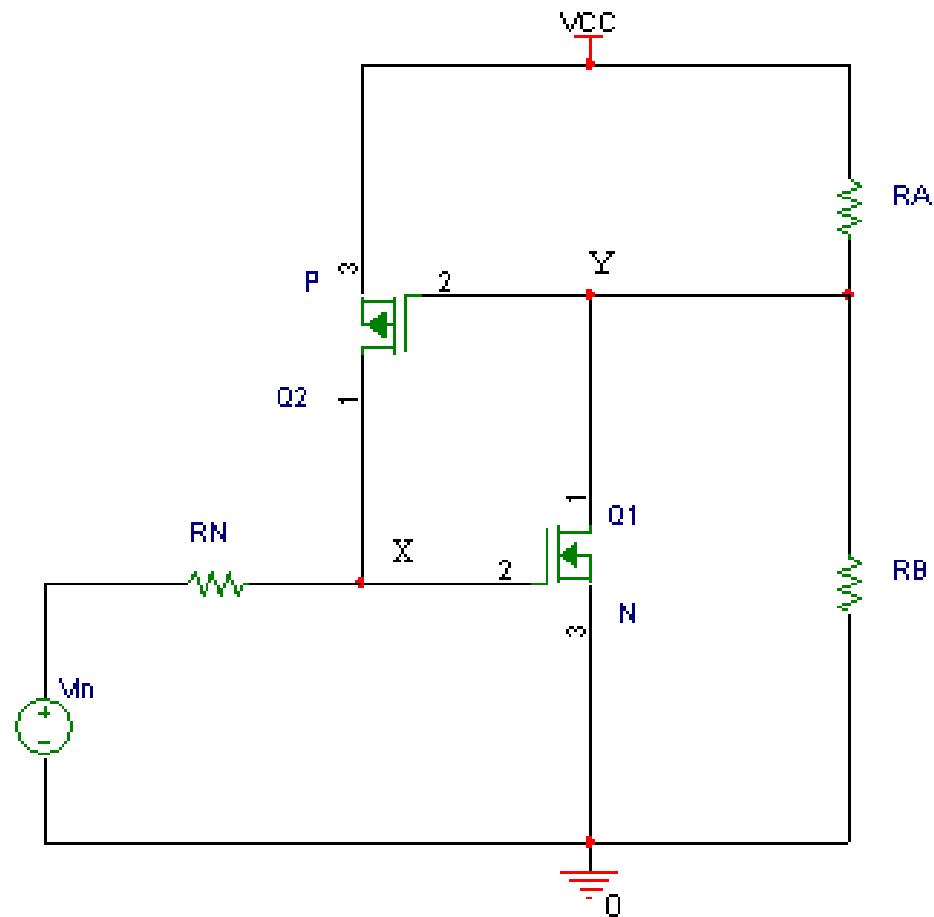
Estimated sensitivity: $\approx 1\text{pC}$

Out signal →
 Transistor B-E
 1pC-estimated
 injected charge →

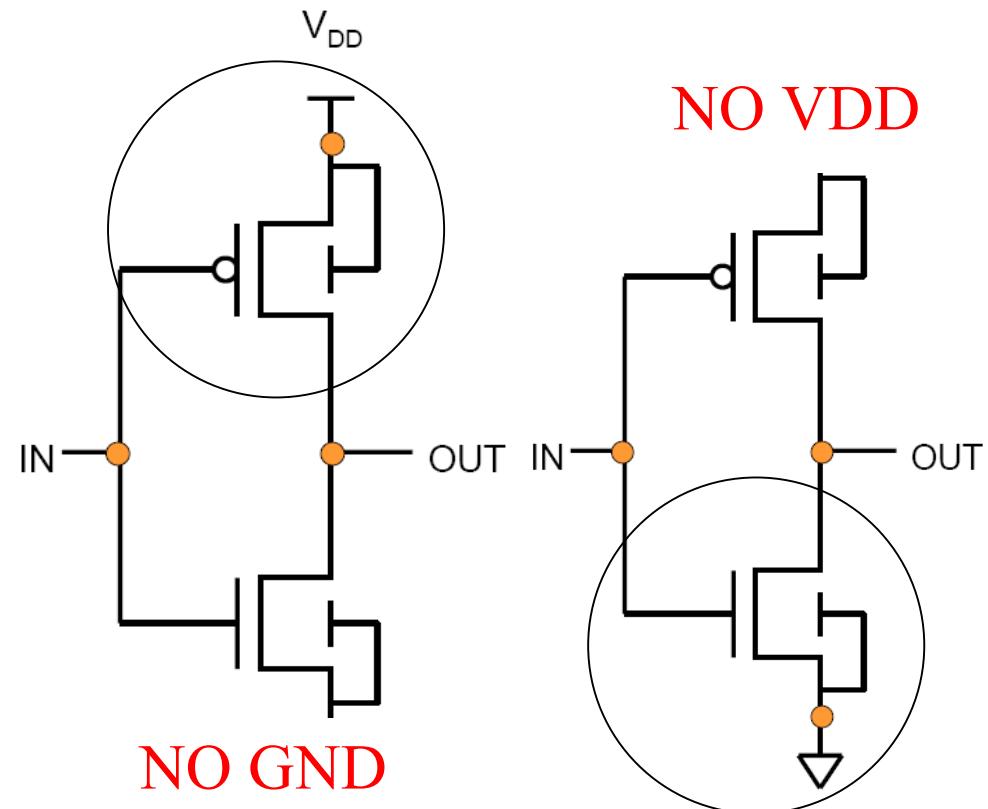
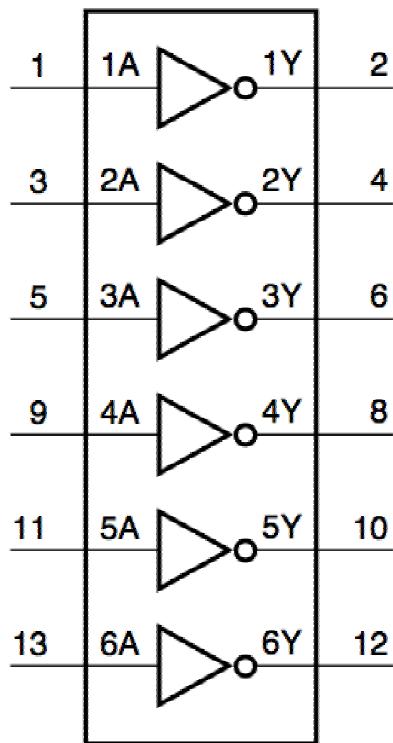


BJT to MOS transistors

All that has been investigated via bipolar transistors (BJT) can be obtained using Metal-Oxide Semiconductor (MOS) transistors

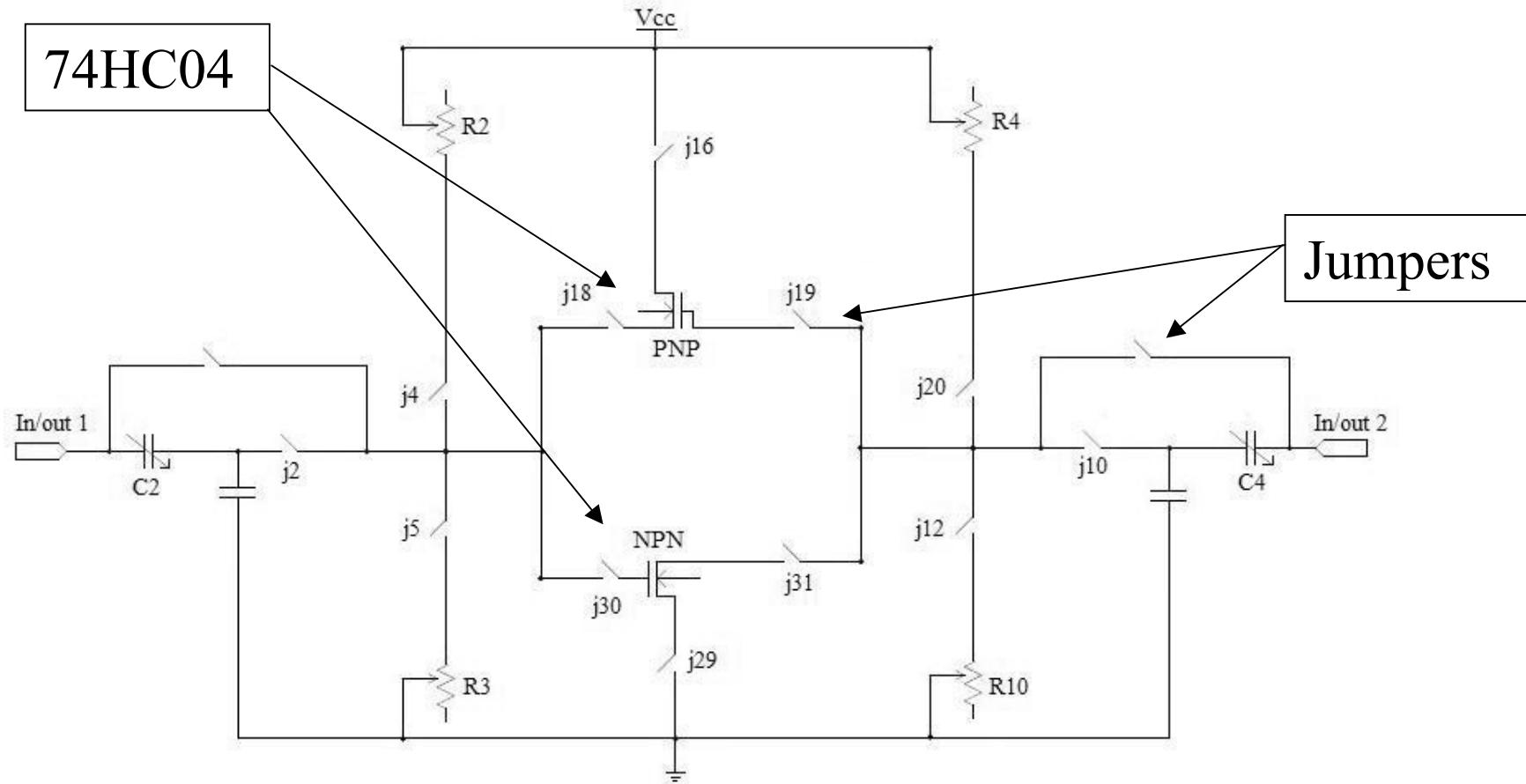


Here is how to use individual commercial MOS transistors (74HC04)

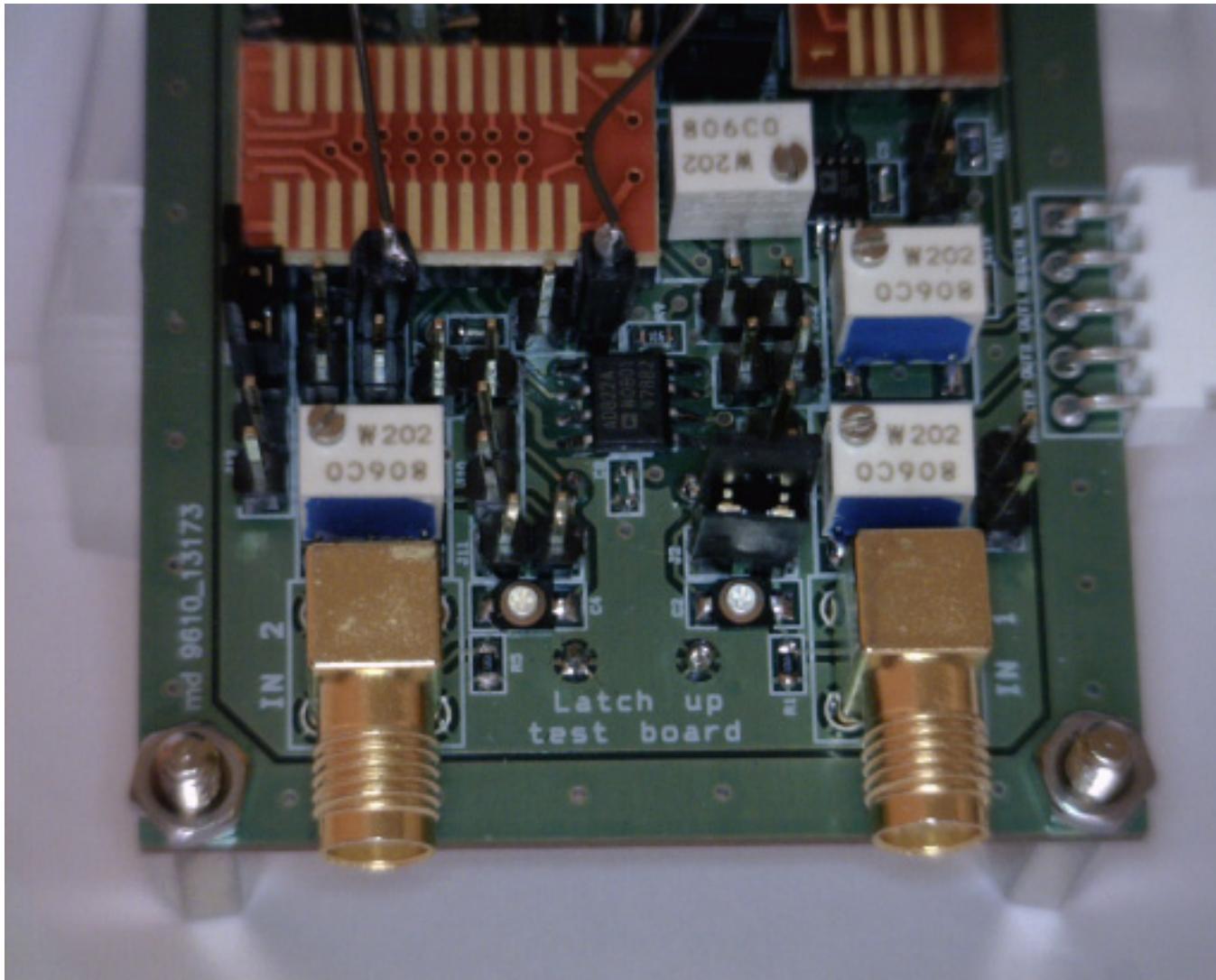


..with some difficulties, honestly

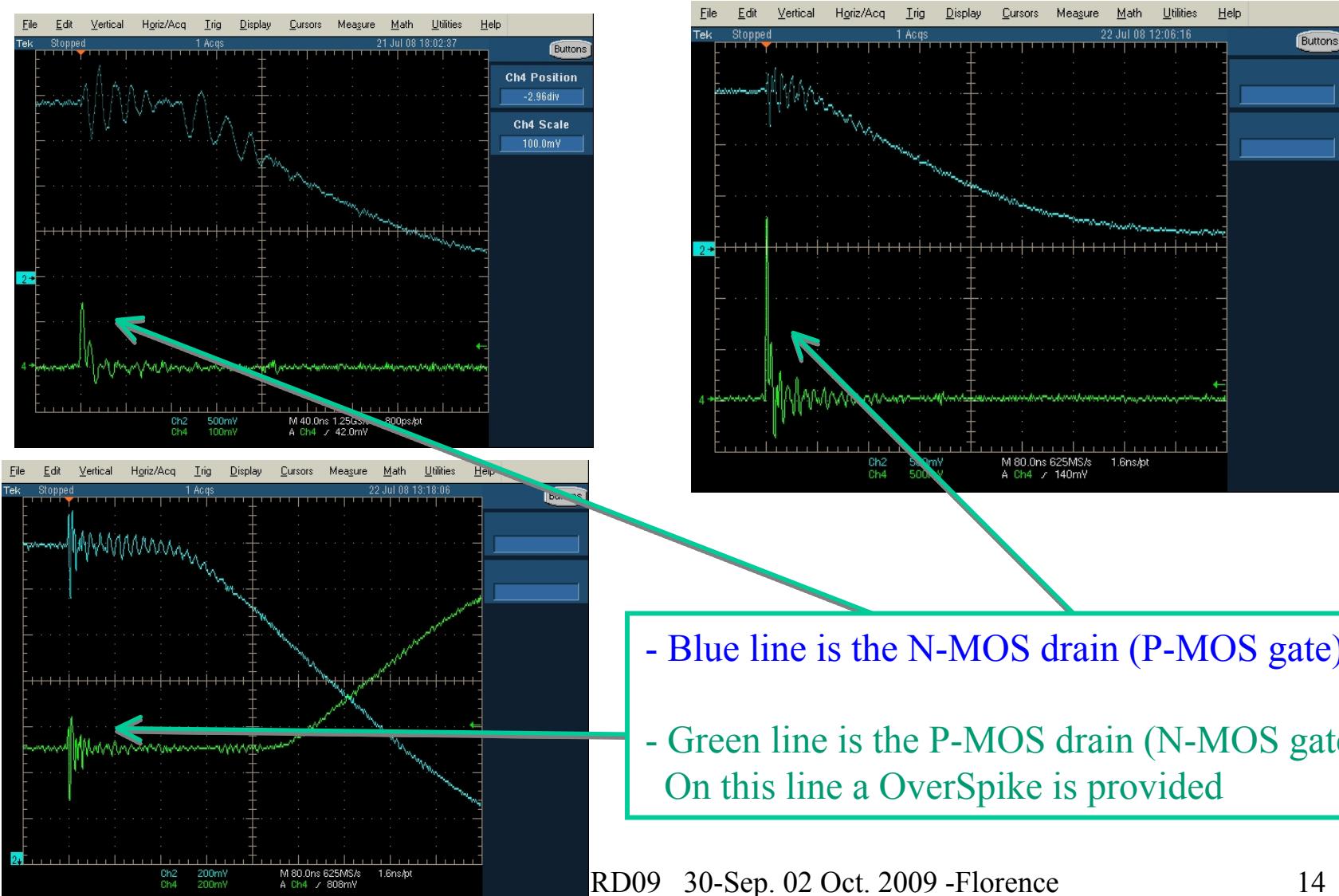
The schematic for many configuration and tuning capabilities



The Test-Board for MOS transistors

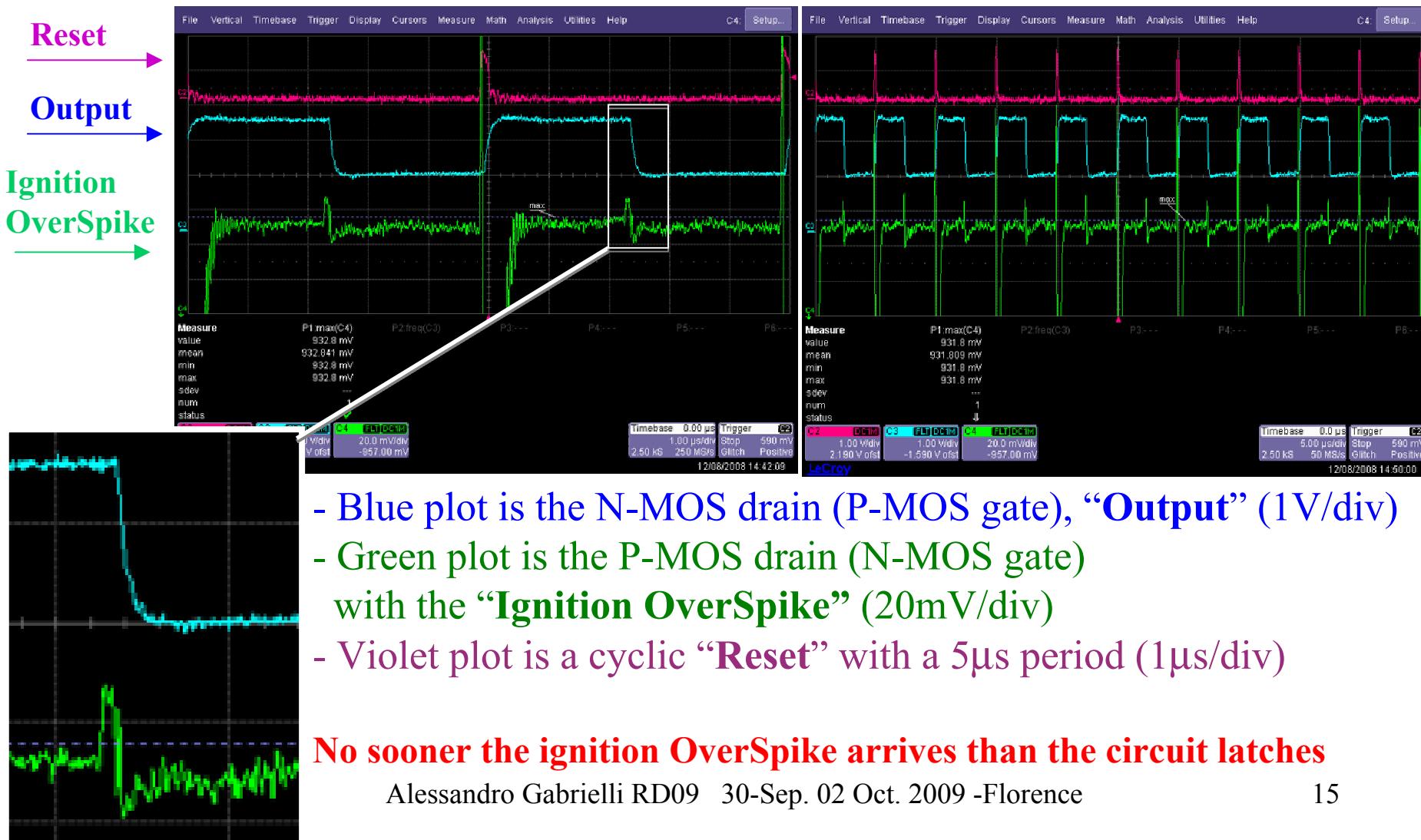


Single Latchup ignition

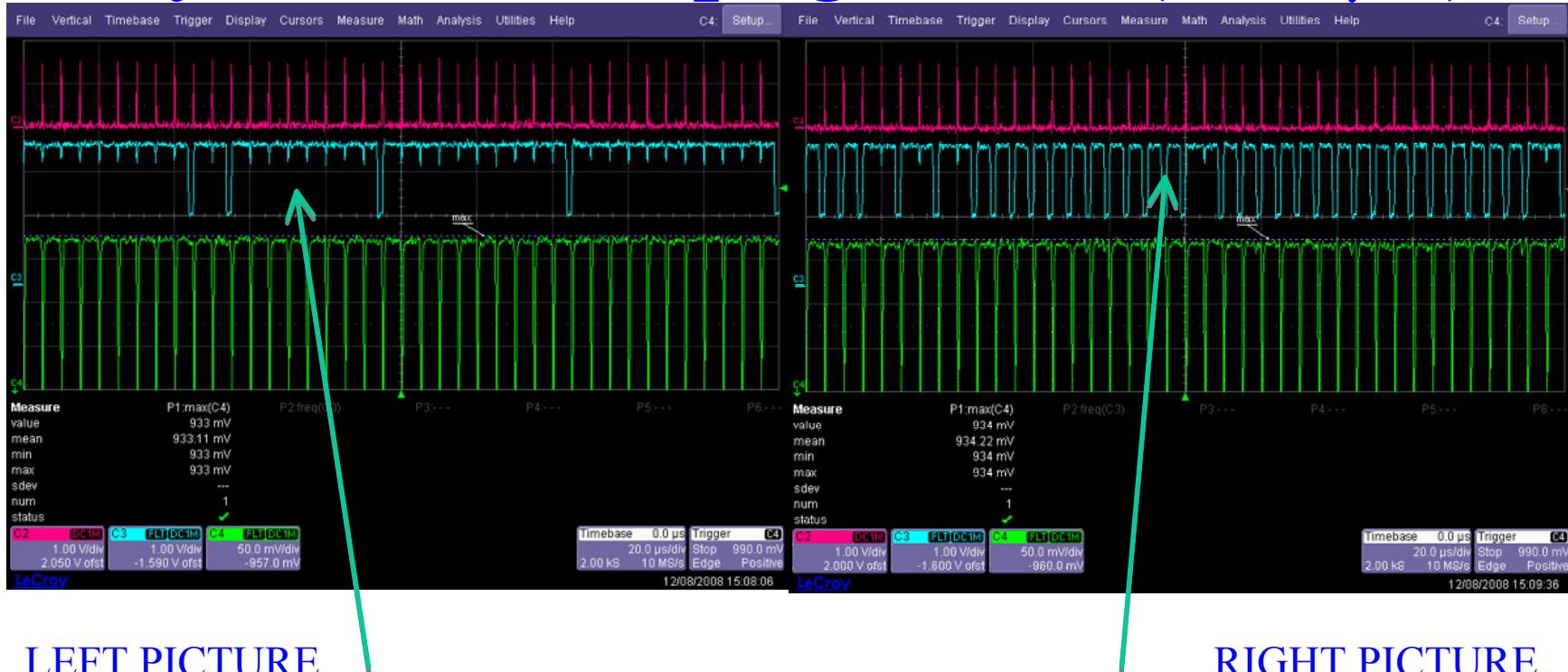


Cyclic Latchup ignition ($T=5\mu s$)

RESET – IGNITION OVERSPIKE - RESET – IGNITION OVERSPIKE



Cyclic Latchup ignition ($T=5\mu s$)



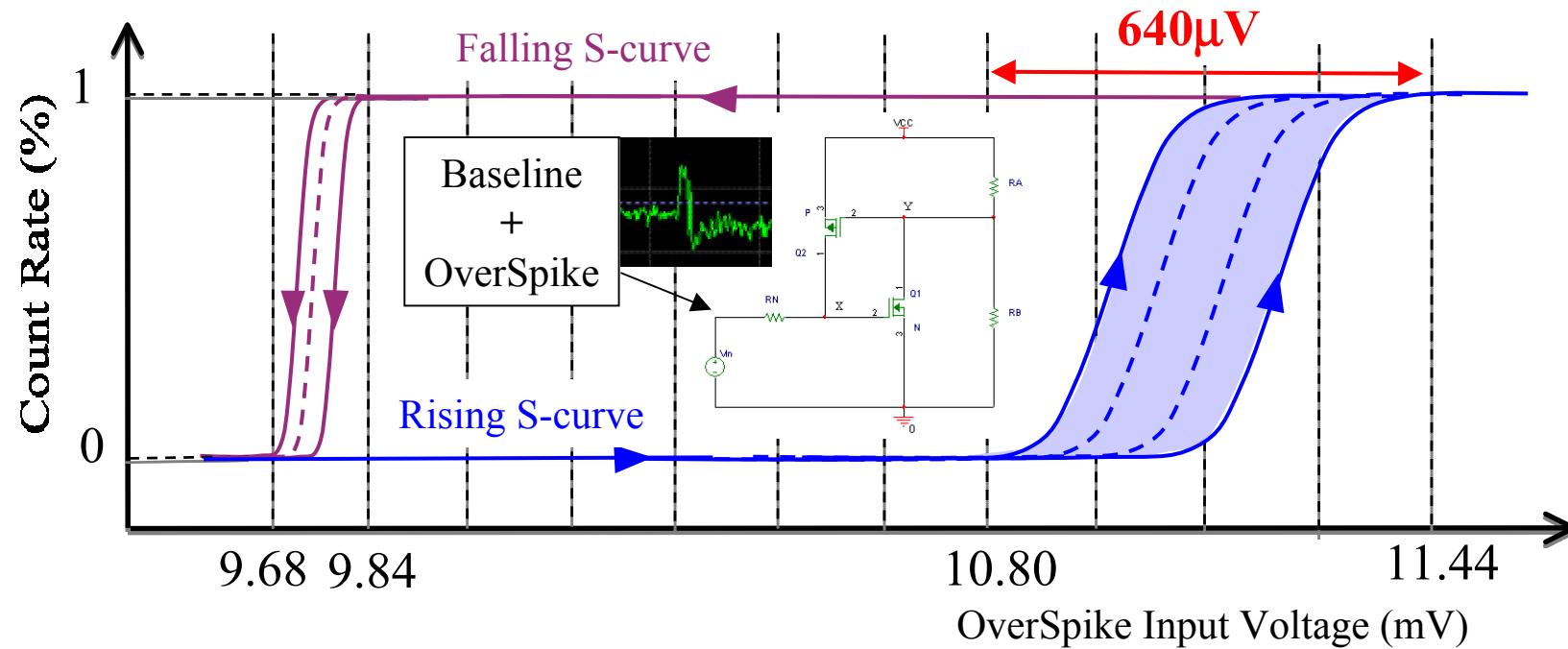
LEFT PICTURE

- The ignition OverSpike is **too weak**
- Only a few % of the times the circuit latches

RIGHT PICTURE

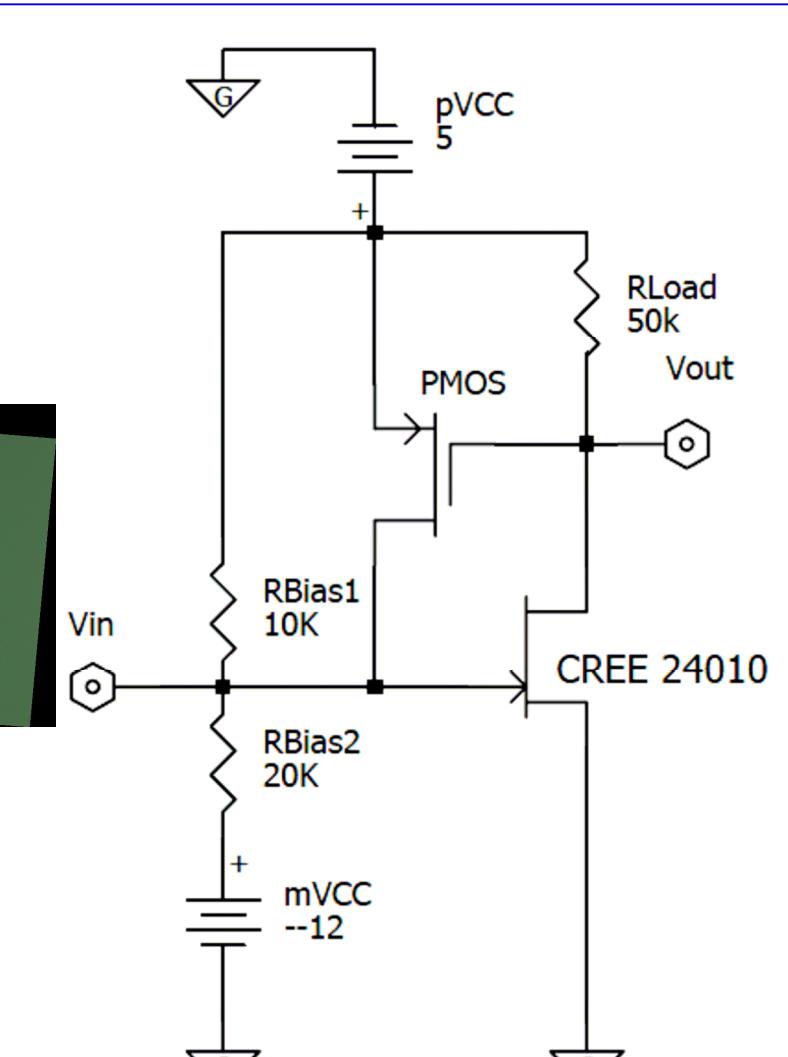
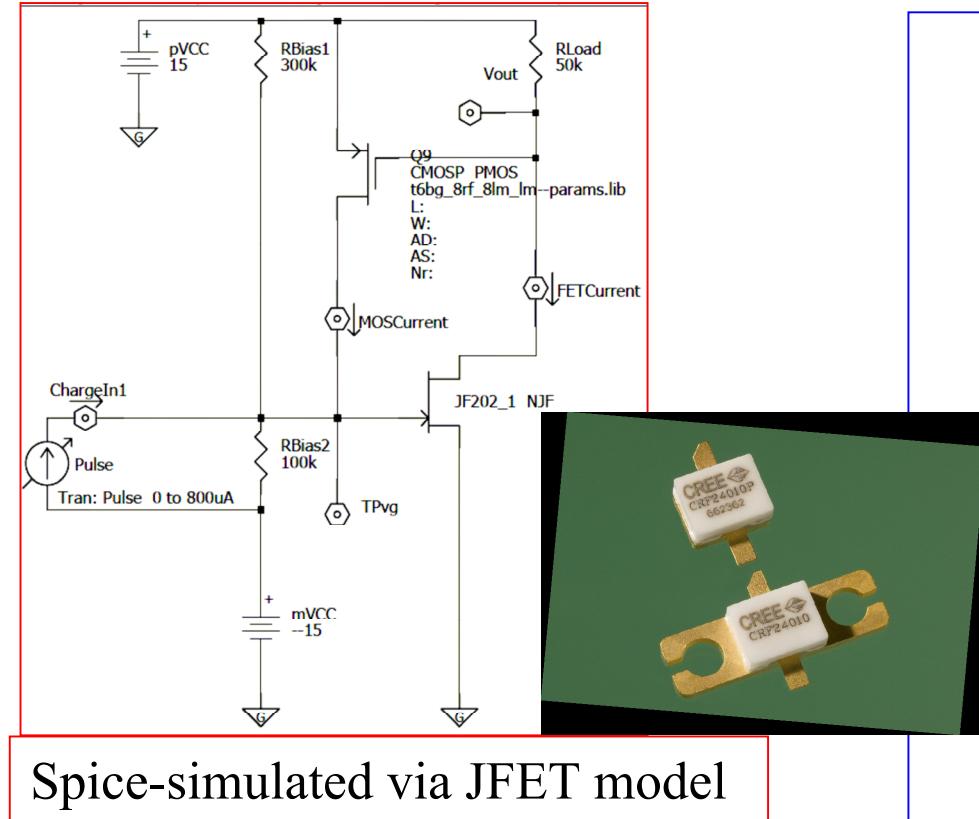
- The ignition OverSpike is **high enough**
- Most of the times the circuit latches

Noise Figure for MOS- Summarized S-curve



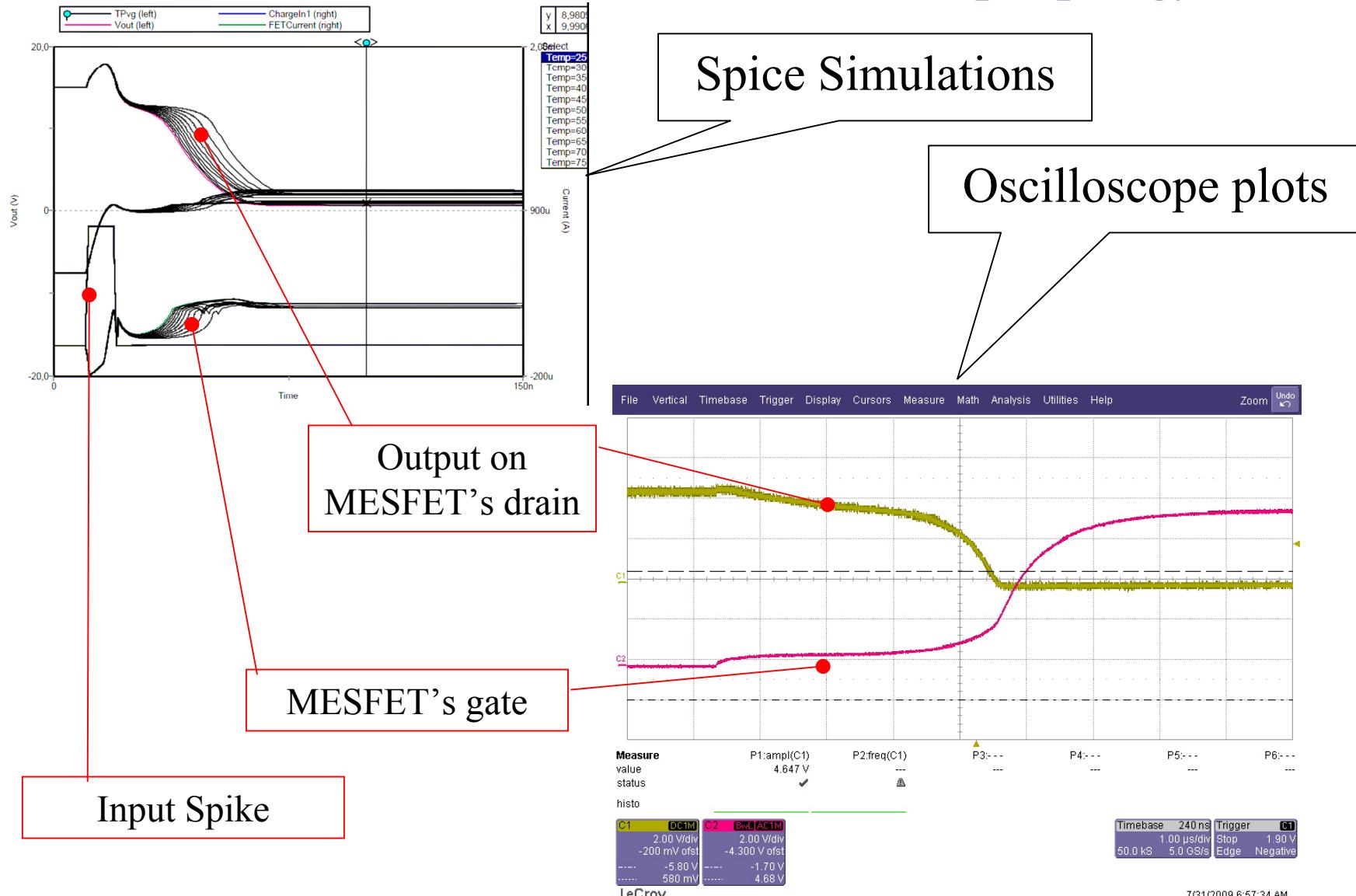
- A biasing gate **baseline** of about **950mV** was used
- Raising curve has an **noise figure** estimated in $\approx 640\mu\text{V}$, **SAY LOWER THAN 1 mV**
- The S-curve has an **hysteresis**
- The estimated **sensitivity**, by measuring the input impedance, was confirmed to be $\approx 1\text{pC}$

The CREE 24010 SiC MESFET via latchup topology



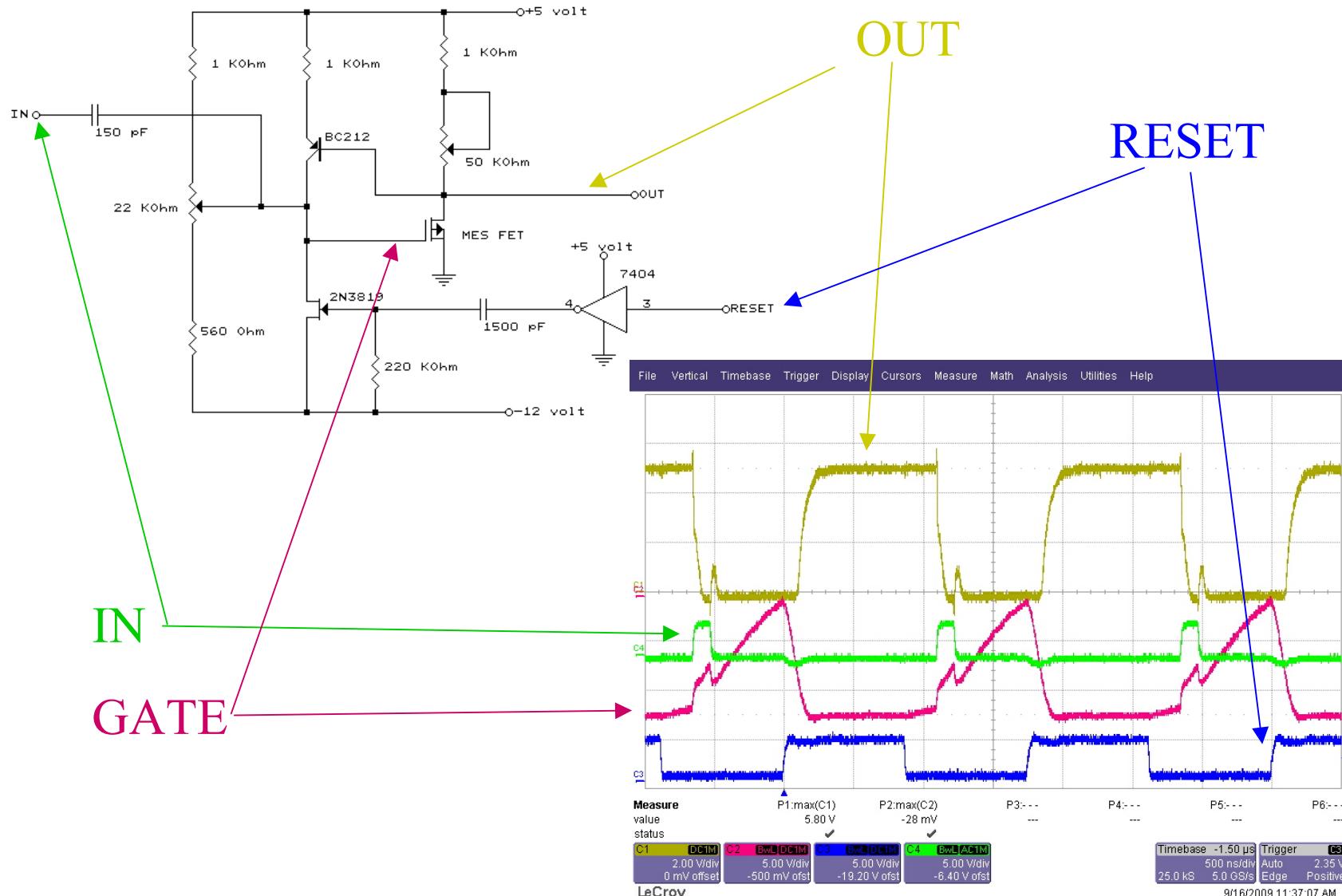
Actual circuit via MESFET CREE 24010
Mounted on test-board

The CREE 24010 SiC MESFET via latchup topology



Alessandro Gabrielli RD09 30-Sep. 02 Oct. 2009 -Florence

The CREE 24010 SiC MESFET via latchup topology



CONCLUSION

Using commercial state-of-the-art **MOS** transistors we have obtained:

- an Error Figure of about **640 μ V**,
- a sensitivity of the order of **1pC**, confirmed like for BJTs,
- a readout speed of the order of **1 μ s**.

Using commercial **SiC MESFET** transistors we have confirmed the topology and the latchup ignition obtained with BJTs and MOSSs

Latchup Mechanism can be exploited in future applications for :

- particle detection in high-energy physics,
- radiation monitoring,
- high-temperature, rad-hard applications for SiC

Advantages: SIMPLE and LOW POWER

An integrated version is required since 2005to go ahead