A low mass pixel detector upgrade for CMS

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Outline

- Scope of upgrade
- New Barrel Design
- New End Disk Design
- Detector Module Changes
- Changes to the readout chip
  - Design
  - Tests

LHC upgrade plans

By 2014:

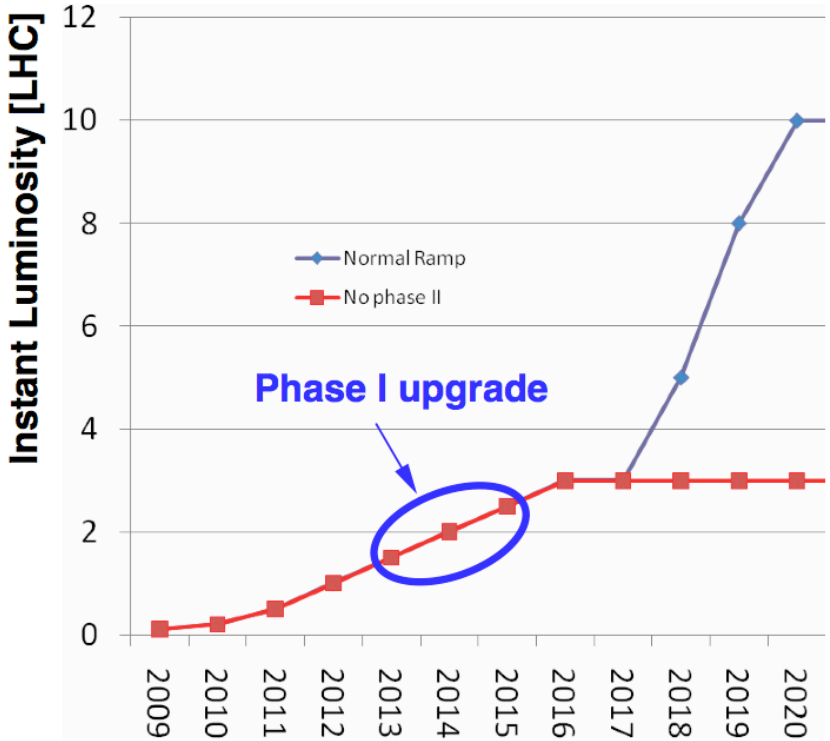
- ~2xLHC luminosity
- Upgrades in (longer) shutdown

Consequences for CMS:

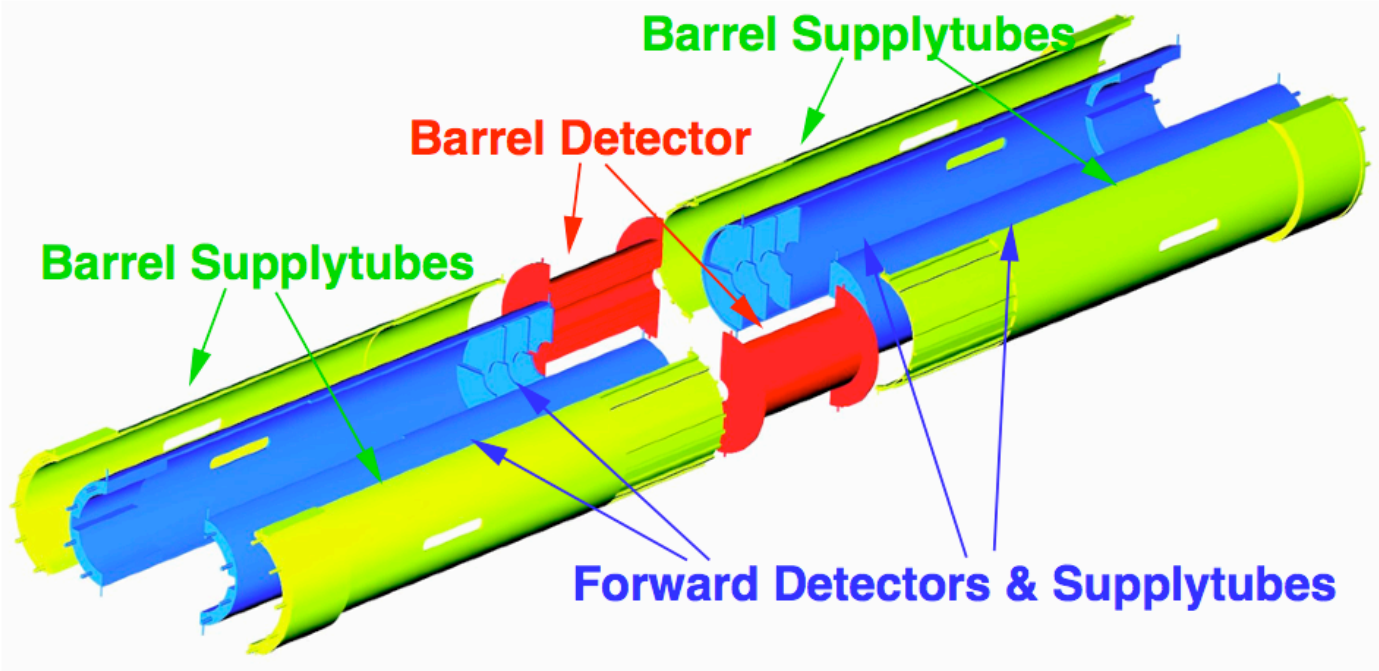
- Most subdetectors min. changes
- Replace pixel system (rad damage)

By 2018:

- ~10xLHC luminosity
- very long shutdown
- replacement of complete (CMS) Tracker



CMS Pixel System



- Designed for fast insertion (beam pipe bake out)
- Will be done in regular shutdown
- Can be replaced by improved system

Constraints and Requirements

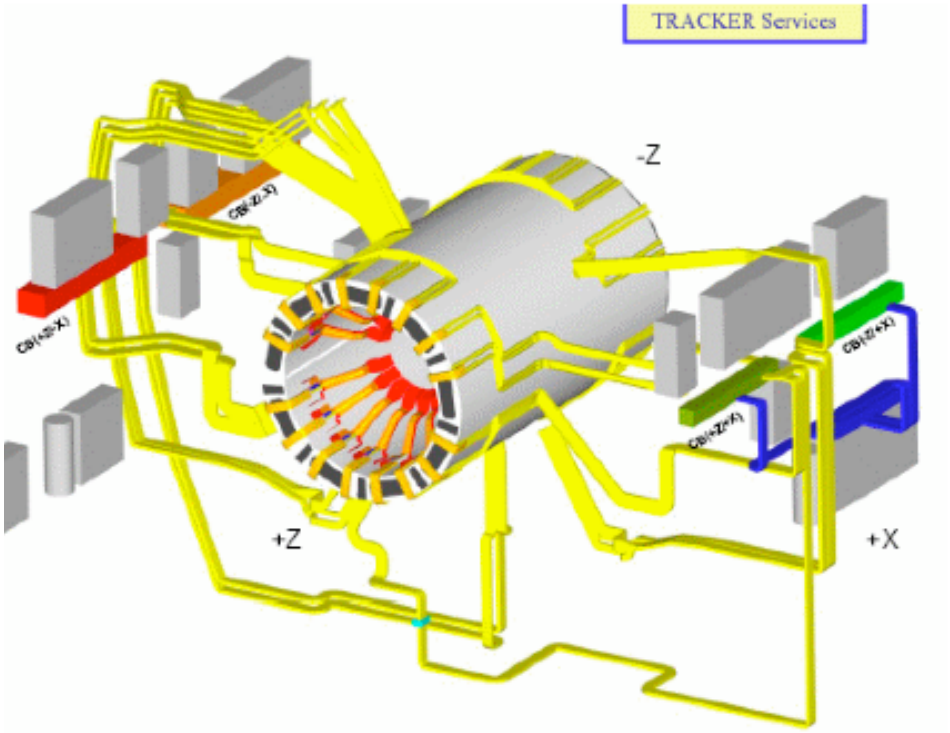
Same/better performance:

- less inefficiency at high rates
- reduce material effects

Have to use existing services:

- Cooling pipes, cabling, fibers
- power supplies, readout hardware

Stay in old envelope



Leave system unchange as much as possible:

•keep ROC core untouched

→ minimise recovery time in competetive physics situation

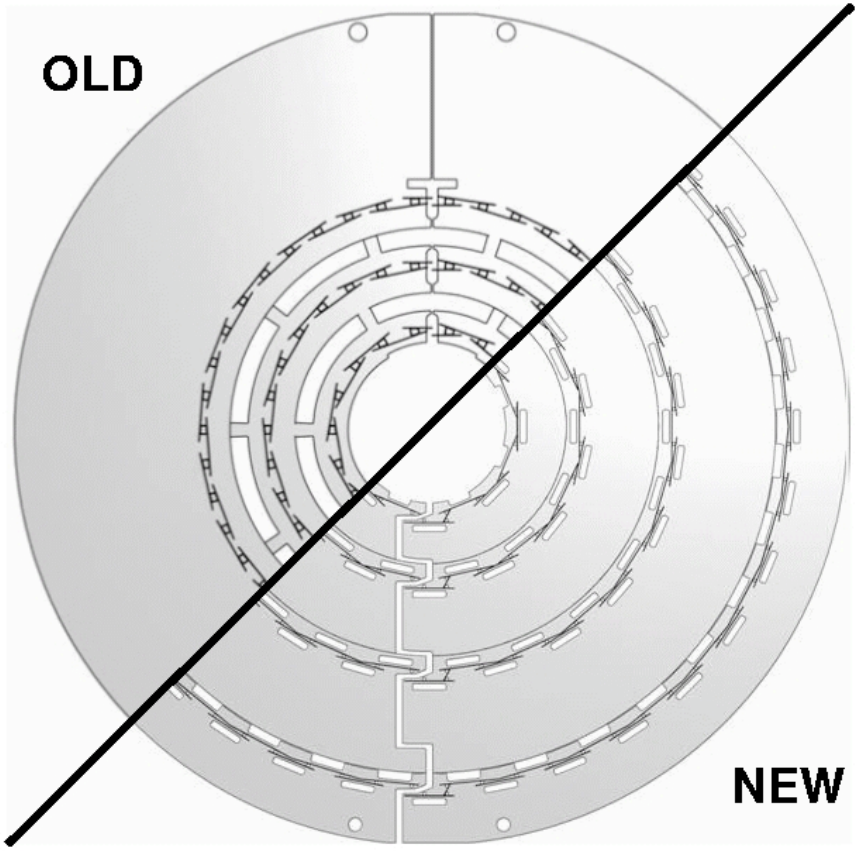
Mechanics of Barrel

Add 4th layer :

- layers @ 39,68,109 & 160 mm
- beam pipe clearance 4 mm
- 8 modules along z (1216 total)
- ‘ultra‘ light support structure

CO_2 based cooling system

→ more robust (standalone) tracking
→ better connection to strip tracker

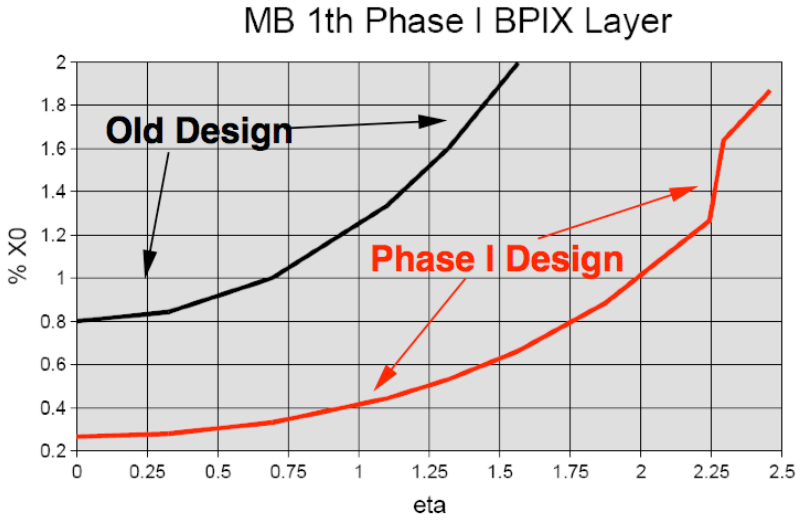


Prototype

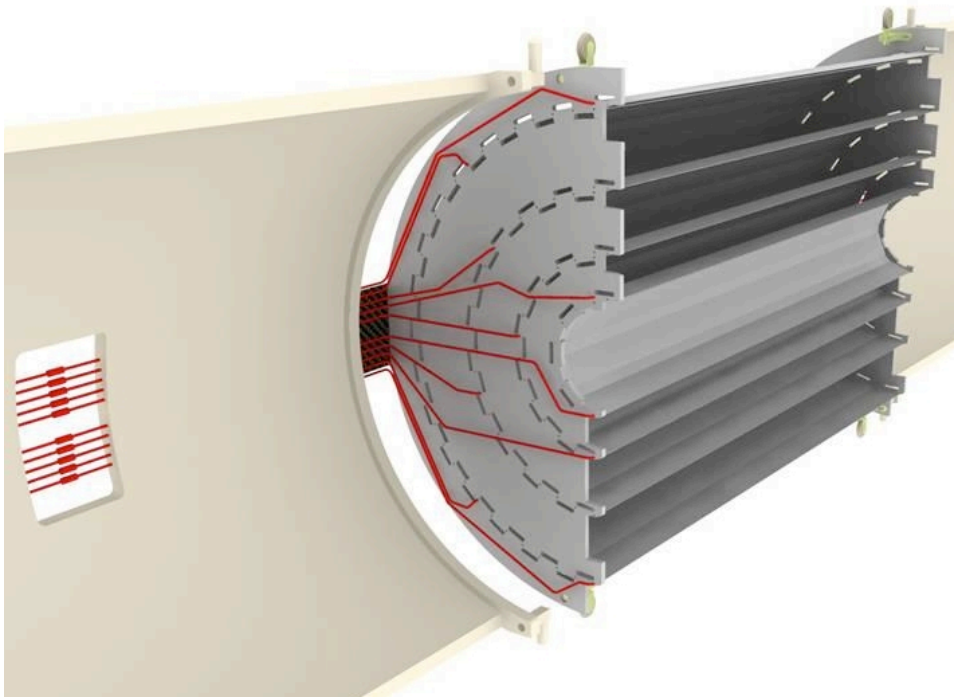
Layer 1 prototype:

- 200 μm carbon fiber
- 4mm Airex foam
- Stainless steel tubes:
  - 1.5 mm OD, 50μm wall
  - Tube bends: 1.8mm OD, 100μm wall
- tested: ~100 bar & -10°C..10°C

- Factor >3 gain in material budget
  →4 layer system will have half of MB of old 3 layer system



CO_2 cooling



Advantages:

- long cooling lines ~ 5m
- no manyfolding needed
- very small tubes

  →big MB reduction

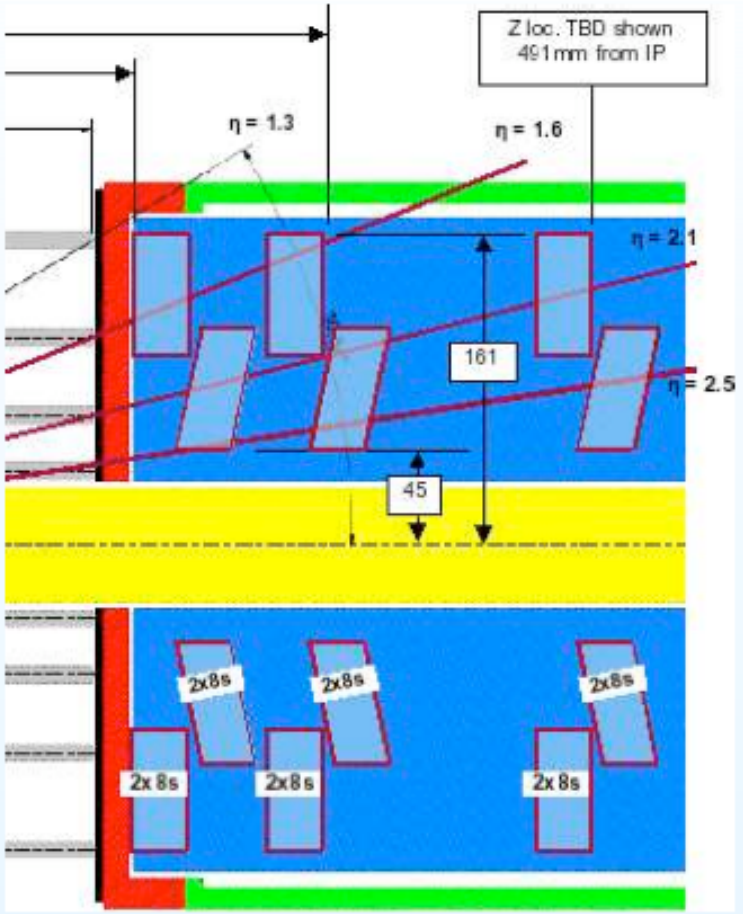
BUT:

- system with relatively high pressures (~60 bar @ room temperature)
- CMS cooling tubes ok up to 40 bar

  → special star tup/safety

Mechanics of Disks

- 3 + 3 discs @ barrel ends
- Each disc consists of:
  - 2 half discs
  - inner & outer ring of modules
  - inner ring tilted by 12°
- 4 point coverage up to η= 2.5
  - very small gap ~ η= 1.3



Mechanics of Disks

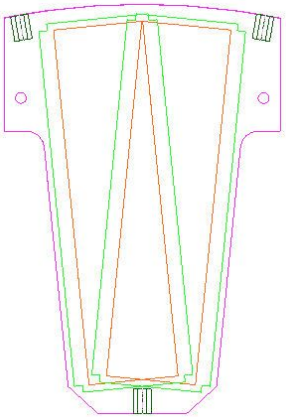
Inner & outer ring of blades

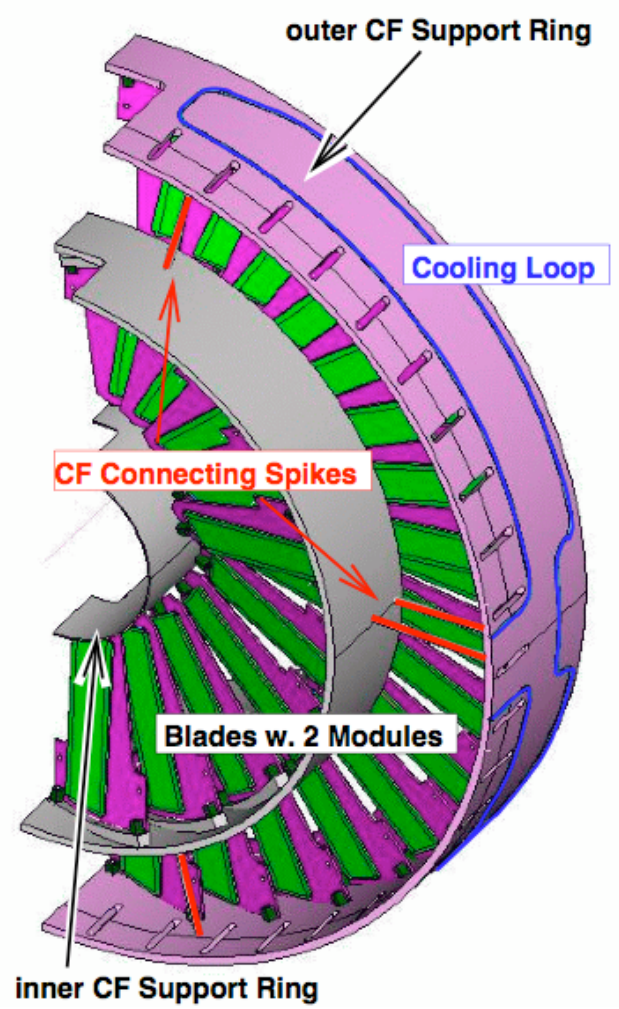
CO_2 tubes embedded in half disk support:

- support cylinder:
  - Carbon carbon
  - Grooves for cooling tube
  - Stainless steel tube:
  - 1.8mm OD, 100μm wall

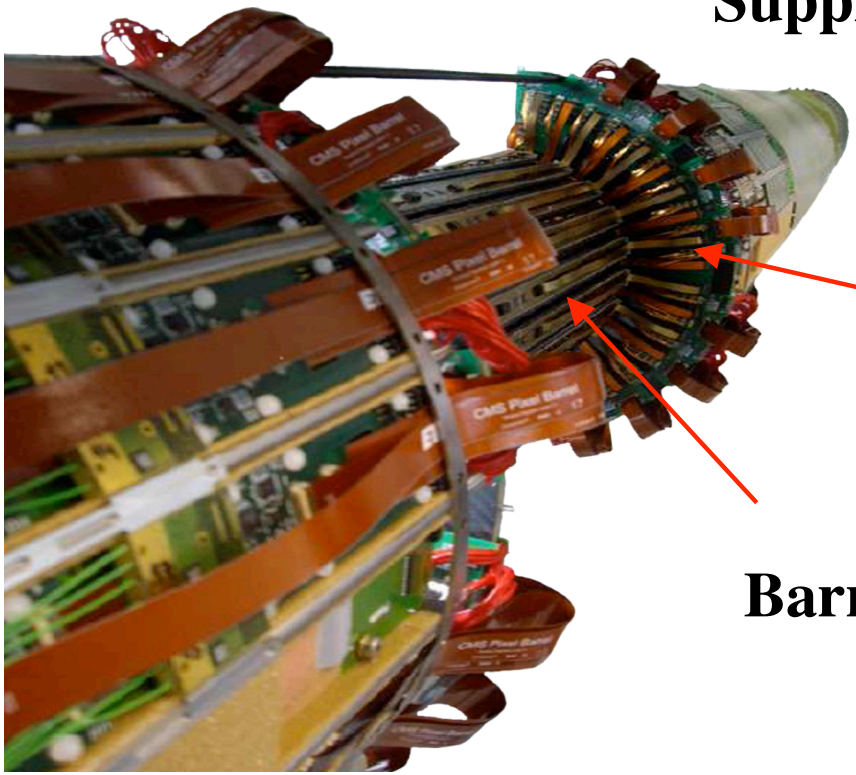
Blades:

- all identical
- Rotated by 20^o radial
- Tilted by 12^o (inner ring)
- 2 modules per blade (ϕ overlap)
- individually replaceable





Reduction in Services



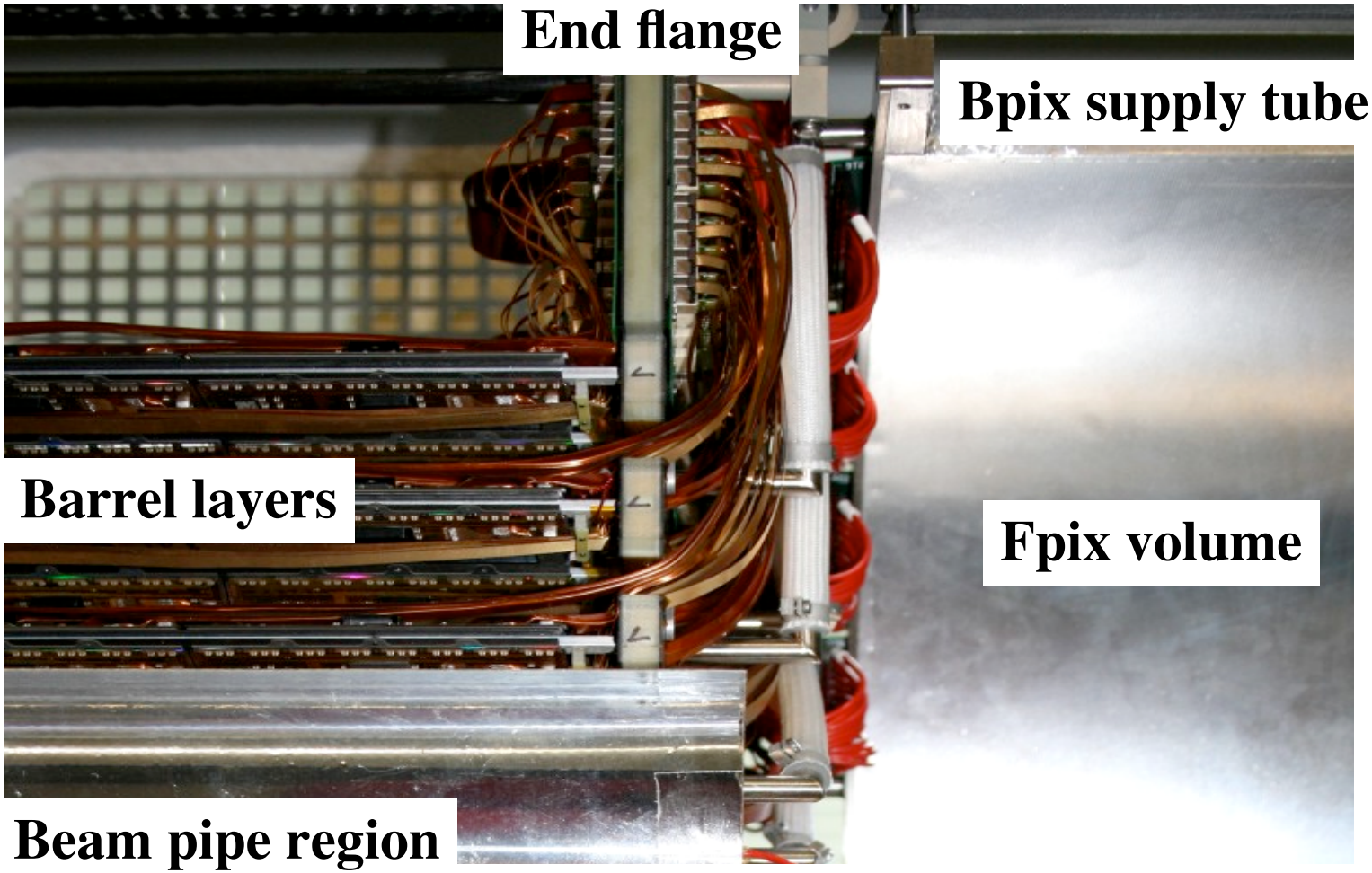
Supply Tube (-Z)

End flange with Prints, plugs and cables

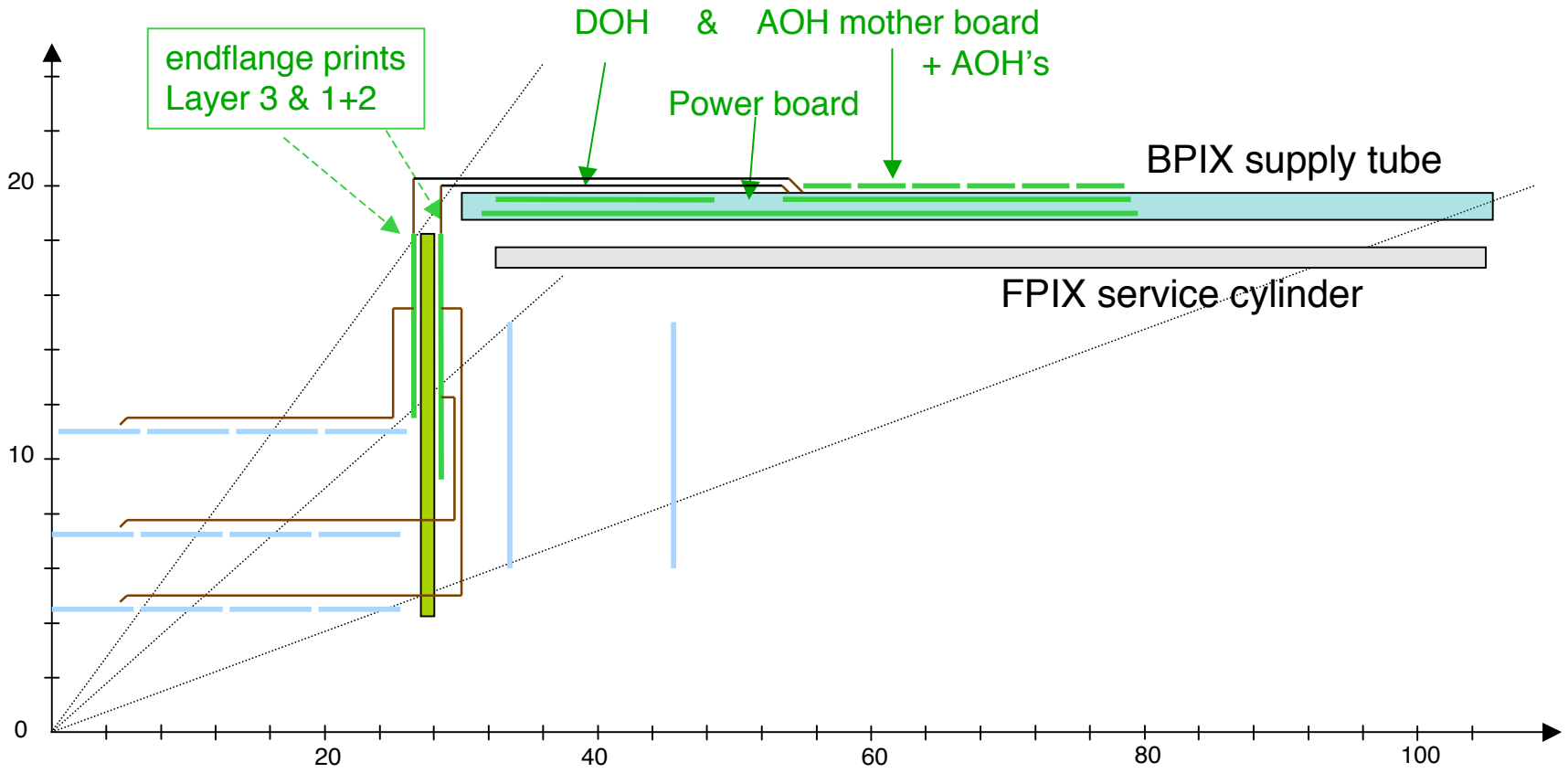
Barrel detector

Supply Tube (+Z)

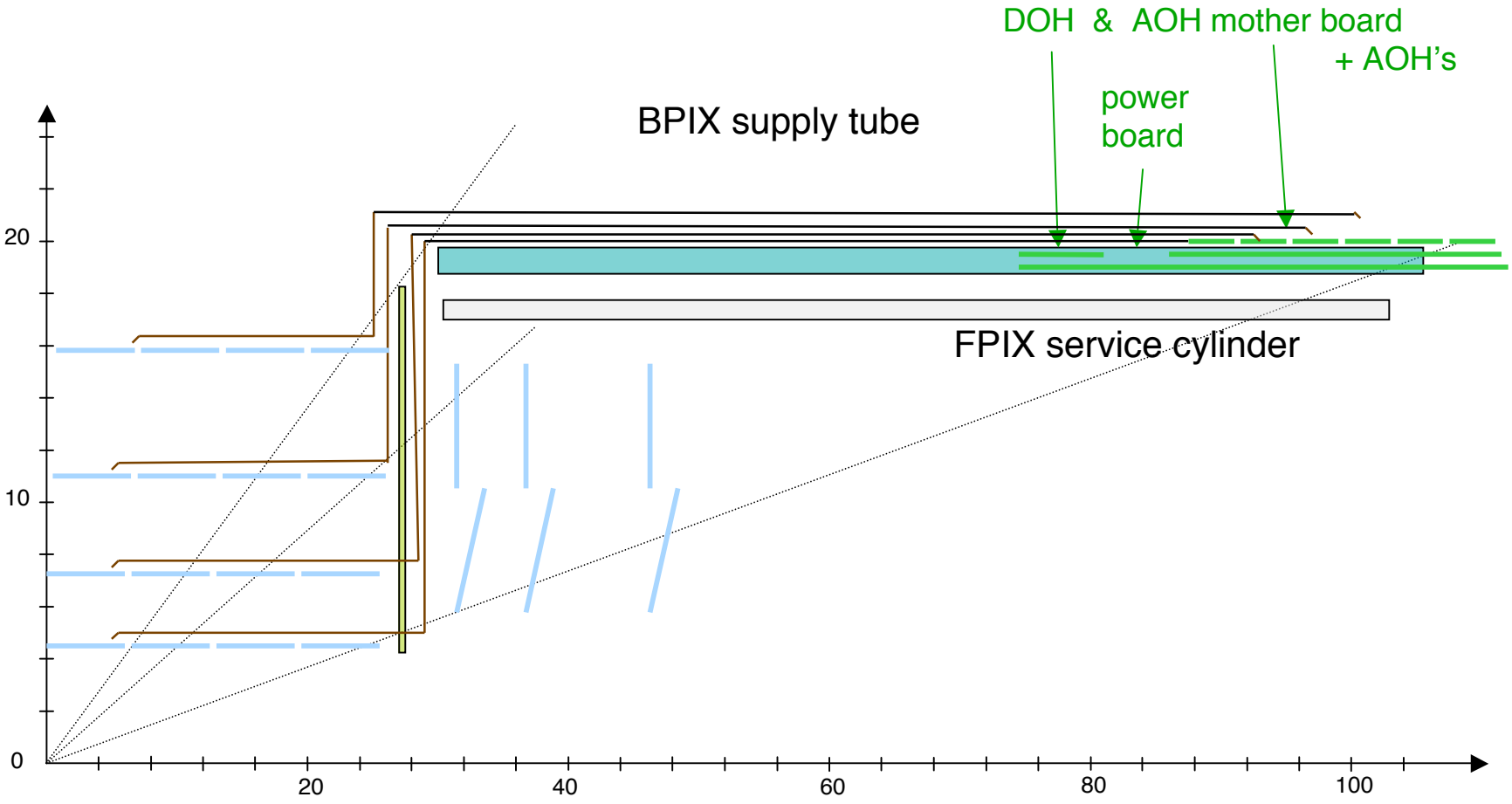
Reduction in Services



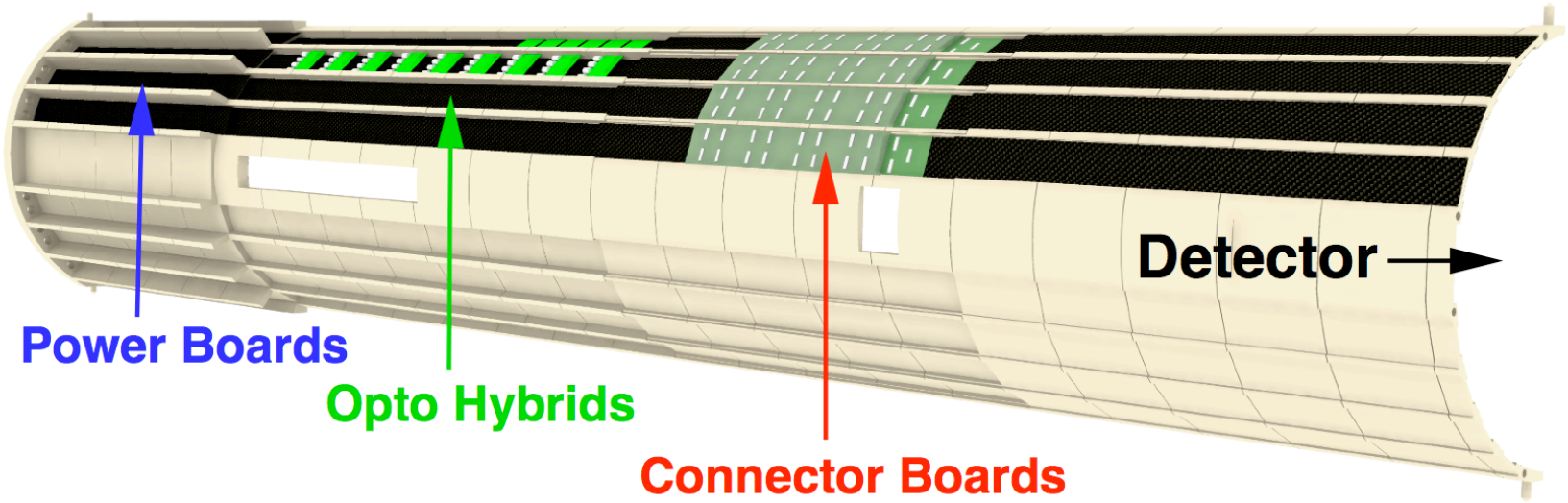
Reduction in Services



Reduction in Services



New Supply Tube



- Very low mass cable trenches
- Module connectors:
  - Layer 3+4 outside
  - Layer 1+2 inside
- New opto hybrids
- 2:1 DC/DC converters

Module Design Changes

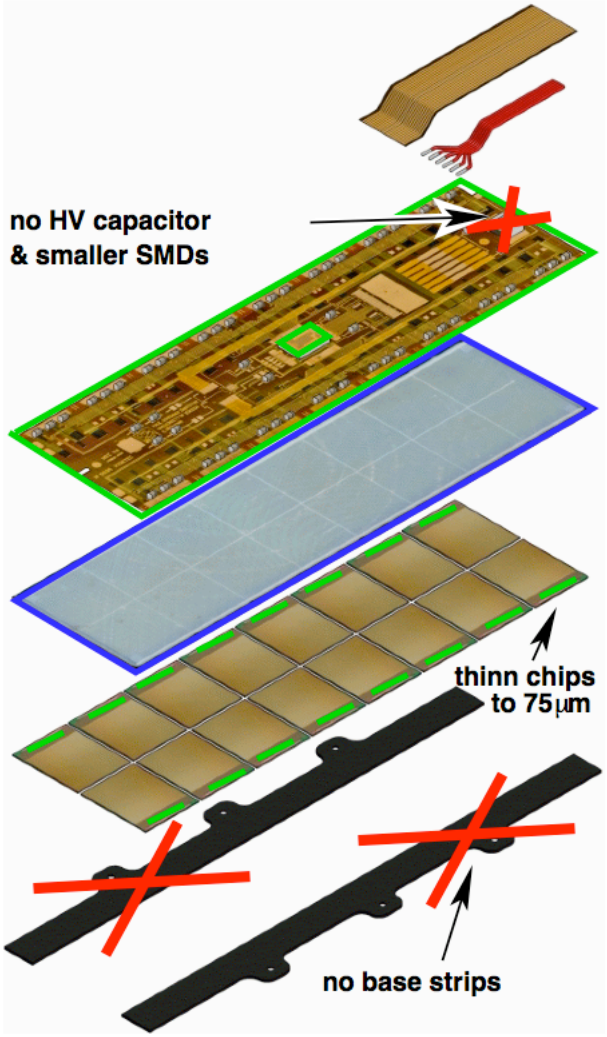
One design(barrel +endcap)

Based on present barrel module

Changes:

- No basestrips
  →Better cooling contact

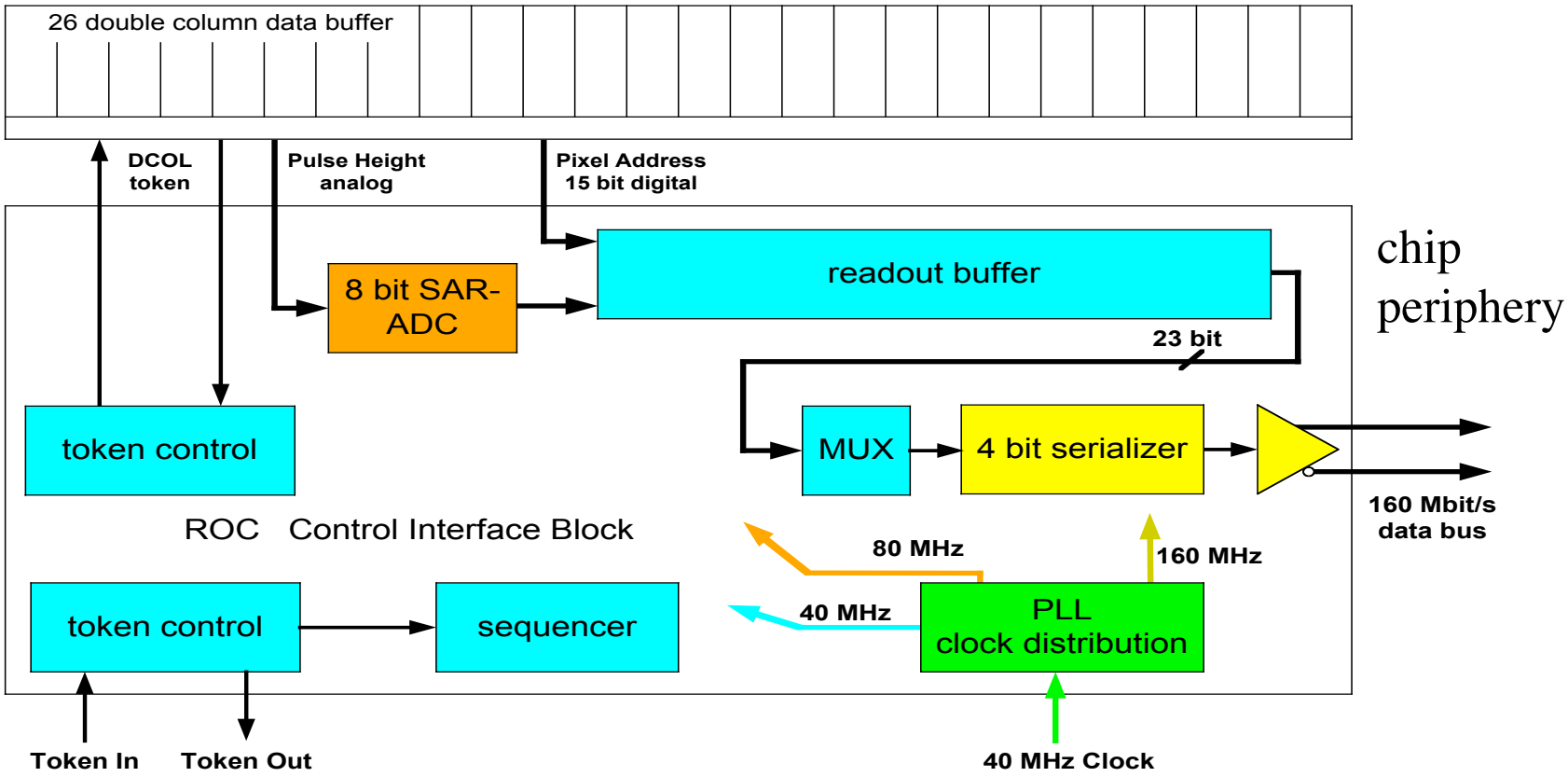
- ROC:
  - thickness 175μm ⇨ 75μm
- HDI:
  - No HV-capacitor
  - Miniaturize SMD-components



Changes in the ROC

- **Larger data buffers to cope with higher rates**
- **Digital readout links at 160 Mb/s**
  - **Now 2x analog link at 40 MHz in layer 1&2**
- **Very low power electrical link of O(1m)**
- **ADC on chip operating at 80 MHz**
  - **Now analog transmission of pulse height information**
- **New readout buffer stage to reduce dead time**
- **PLL to provide 80/160 MHz**

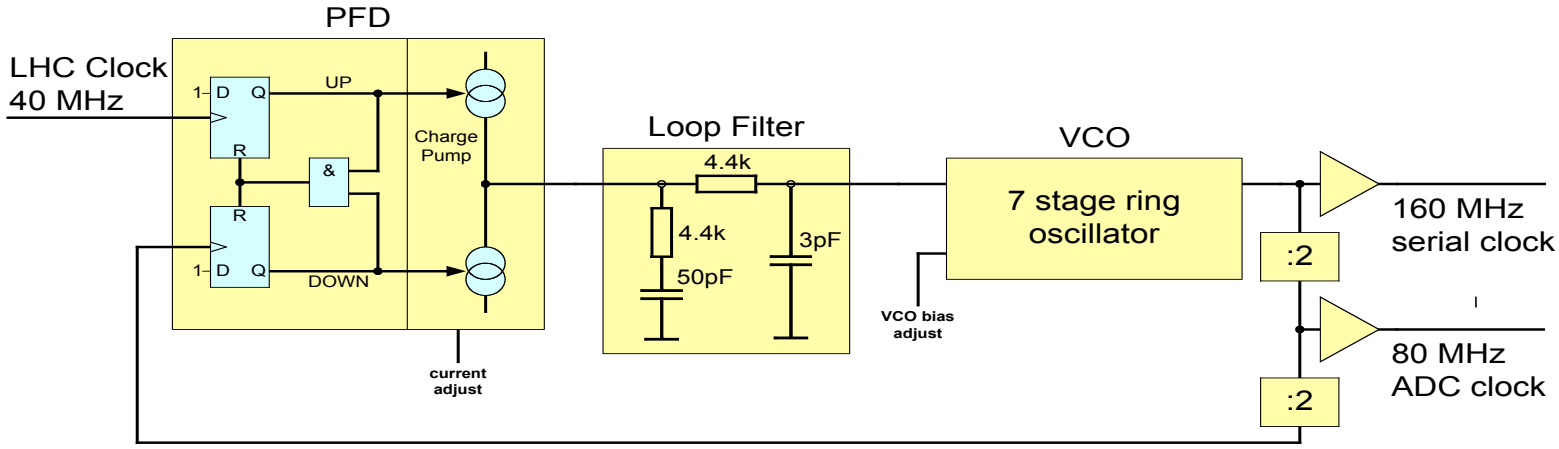
Changes in the ROC



Frequency Multiplier PLL

Technical Data:

- 250 nm ASIC Design
- Reference input: 40 MHz
- Outputs: 80 MHz (ADC), 160 MHz (serializer)
- No external components needed (includes loop filter, capacitors)

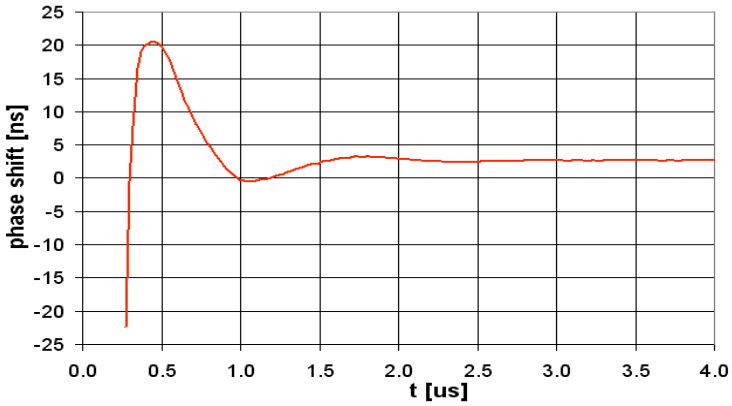


PLL Results

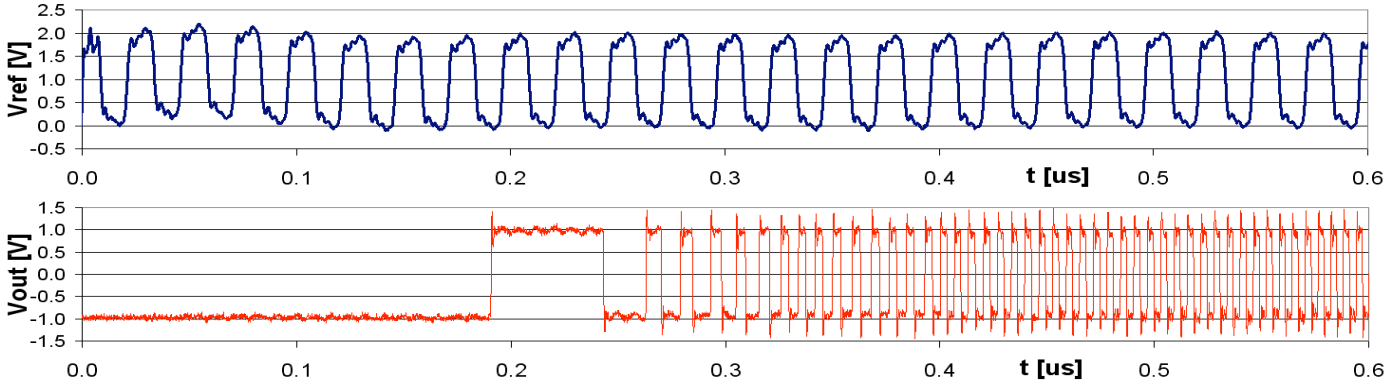
Test results:

- PLL locks for 10 … 75 MHz reference frequency
- Supply current: 720 µA
- Lock time: 3 us
- Jitter < 30 ps

start up phase vs time

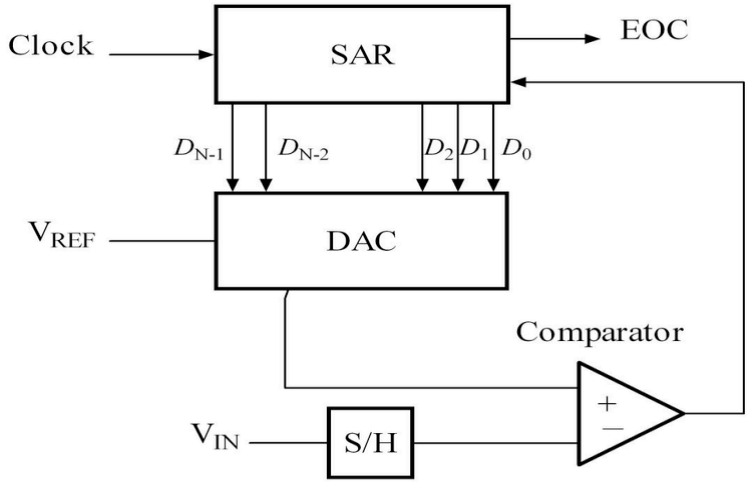


reference and output signal at start up



8-bit ADC: design

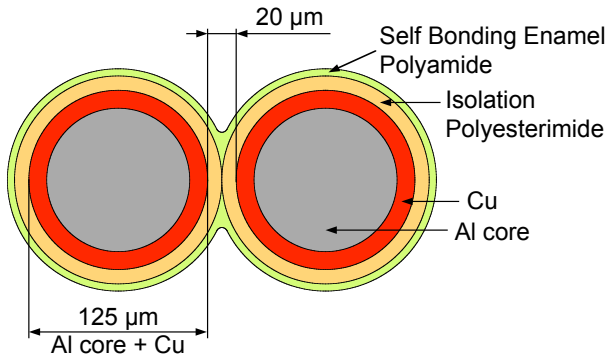
- Successive approximation 8 bit ADC with S&H
- Clock frequency: 80 MHz
- Conversions time: 8 clock cycles



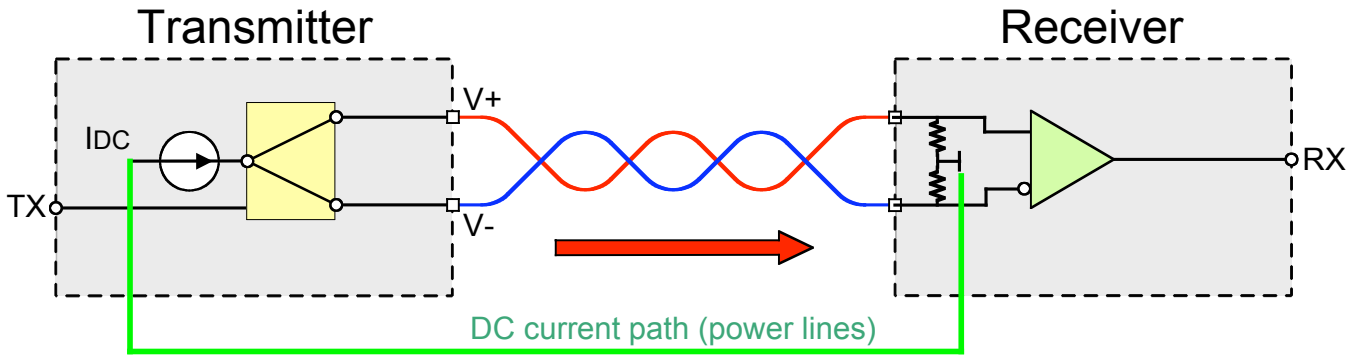
- Prototype designed and under test
- Results:
  - Works well up to 40 MHz
  - Good linearity
  - But: is unstable at 80 MHz
    - → good diagnostic possibilities
    - → could reproduce in simulation by adding parasitics
    - → are about to understand problem

Electrical Low Power Data Link

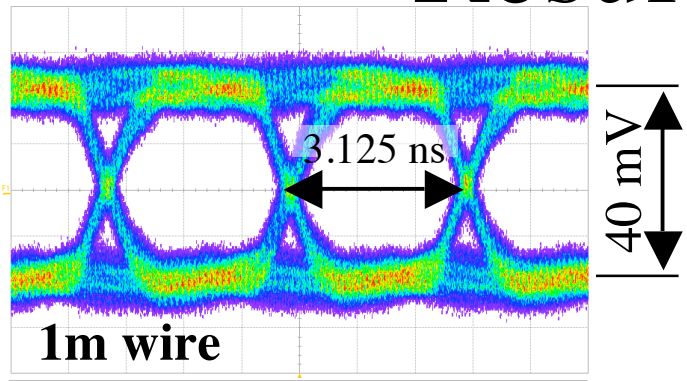
- 1216 Up links from module to outside the tracking area
- 320 MBit/s over 1 m
- Unshielded micro twisted pair cable (125 μm wire diameter, low mass)

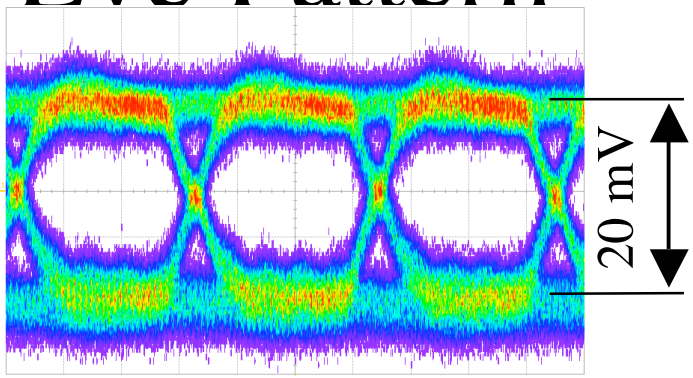


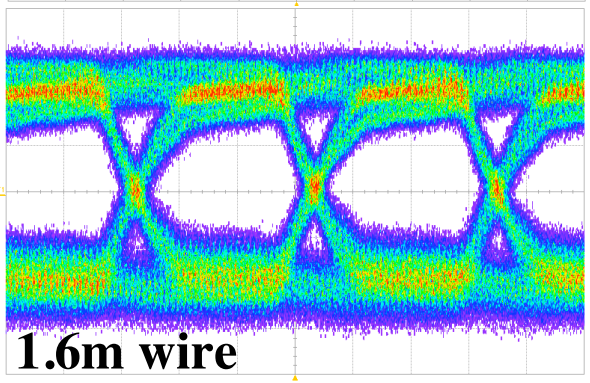
- Low power differential driver and receiver (LCDS)
- Bundled with power and control wires to one module cable

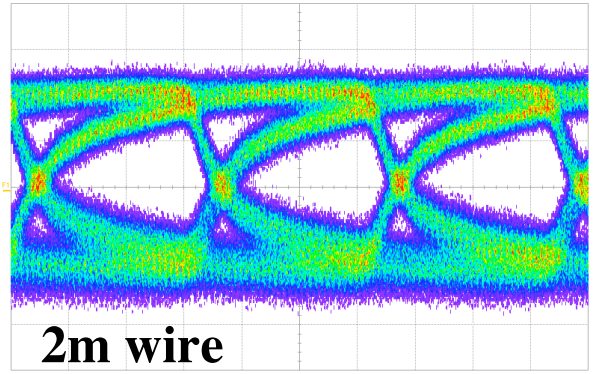


Results: Eve Pattern









- Wire length: 1 m
- 320 Mbit/s
- Minimal amplitude: 20 mV (+/- 10mV)
- +/- 500 mV DC offset between driver and receiver
- Bit error rate < 10e-12 (different condition)
- Crosstalk: -27 dB
- Power consumption / link: 4mW (12 pJ/bit)

Conclusion

New improved design for CMS pixel detector shown

- **4 barrel layers and 3 disks**

Huge reduction in material budget

- **Factor 3 per barrel layer**
- **Factor 2 per disk**
- **Largest gain due to CO_2 cooling**

Large extra savings by moving material out of tracking volume

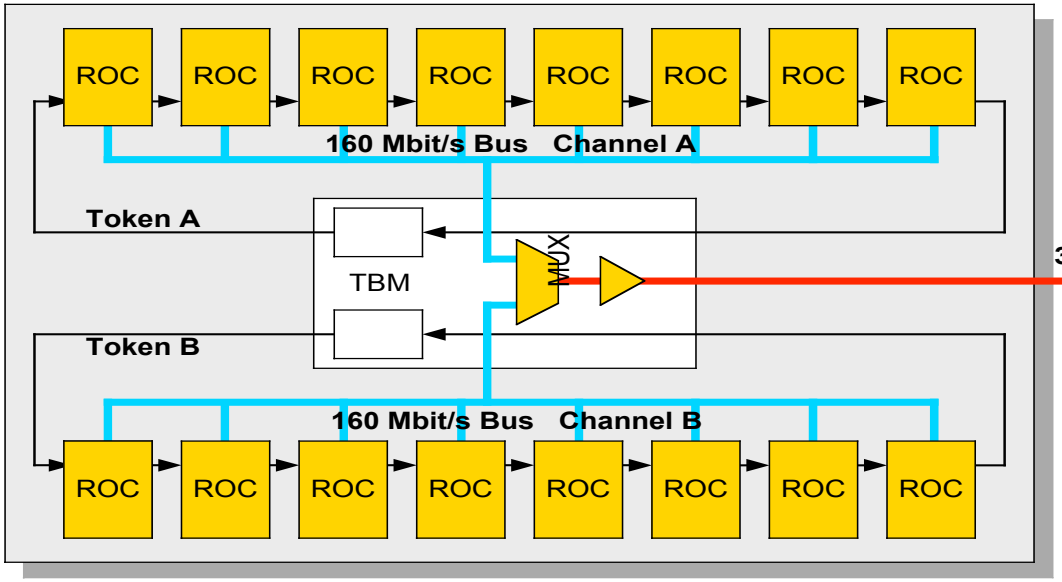
Status:

- **Barrel: Design finished**
  - **Prototype for layer 1 mechanics built**
  - **Prototype for supply tube in production**
- **Disks: Design advanced**
- **ROC: all new cells prototyped and tested.**
  - **ADC needs more work**
- **TBM (module controller chip): need new design of uplink part**
  - **Core unchanged.**

Target date for insertion: 2014

Backup Slides

Digital Readout Overview



- ROC with digital readout & data buffers
- 160 Mbit/s: ROC to TBM
- Digital multiplexer in TBM

- 320 MBit/s non standard electrical link from TBM to supply tube (1216 links in tracking area)
- 320 Mbit/s optical fibres

New module mounting