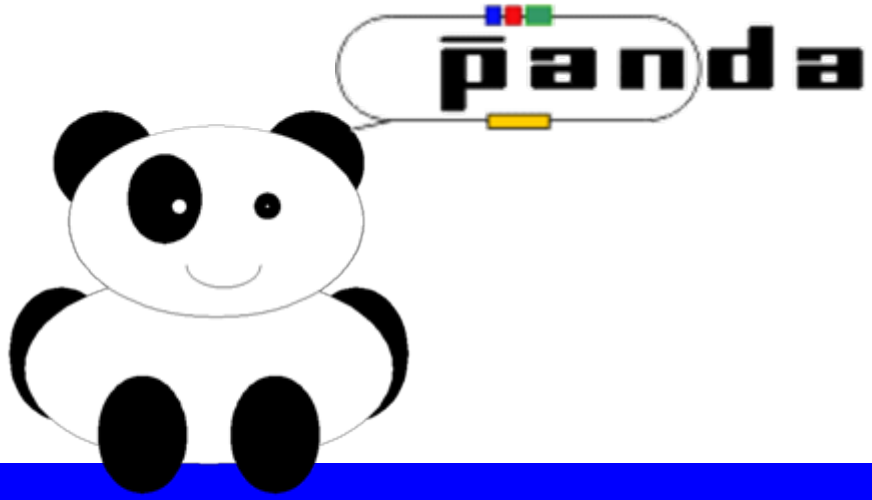
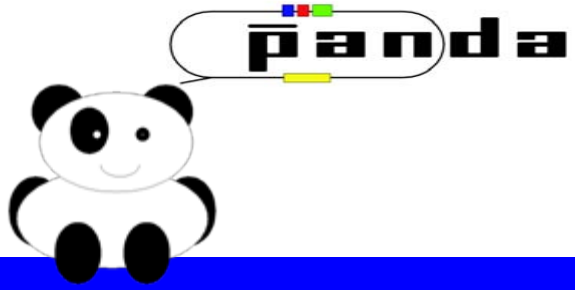


Hybrid pixel detector in the PANDA experiment

D. Calvo, S. Coli, P. De Remigis, G. Giraudo,
T. Kugathasan, G. Mazza, A. Rivetti, R. Wheadon
(INFN-Torino)
in the PANDA Collaboration

RD09 – 9° International Conference on Large Scale Applications and Radiation Hardness of Semiconductor Detectors
Firenze, 30 September – 2 October 2009



Overview

- Introduction – the MVD in PANDA
- Custom hybrid pixel detector
  - detector layout and cooling system
  - epitaxial silicon devices - results
  - pixel readout prototype - results
- Conclusion

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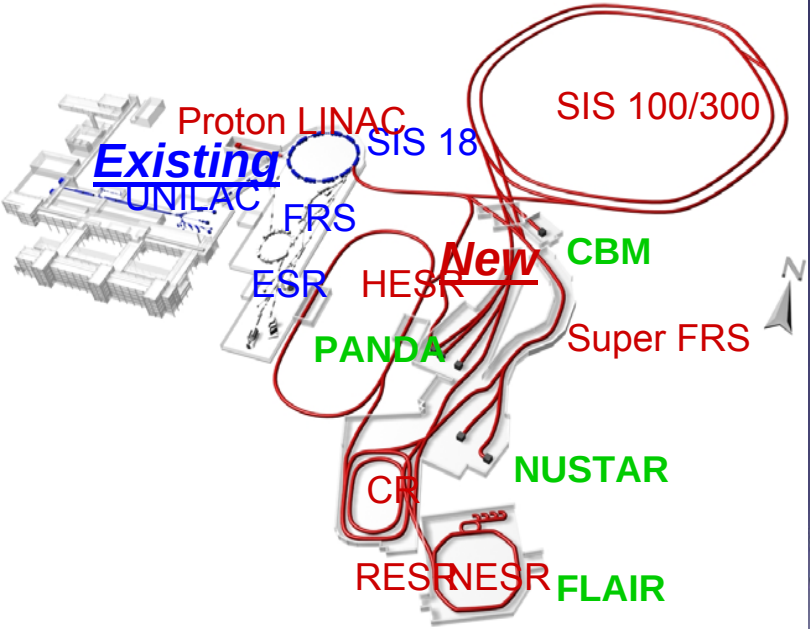
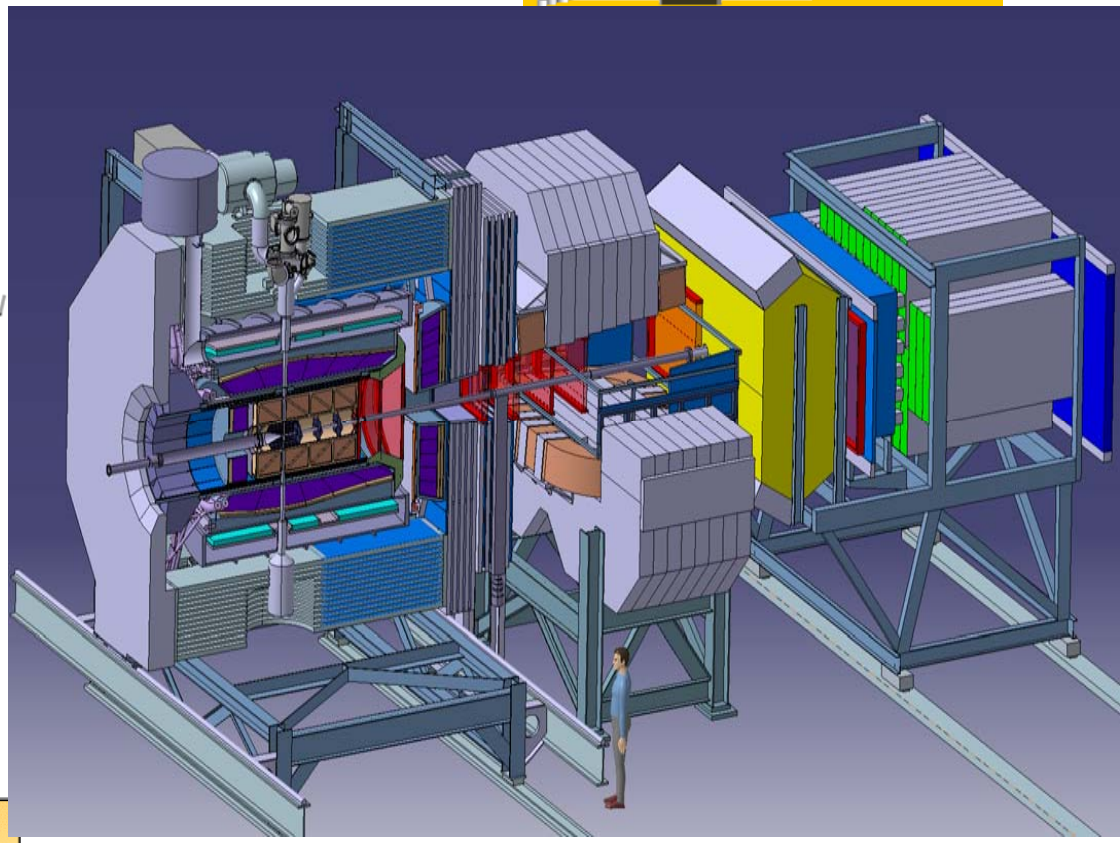
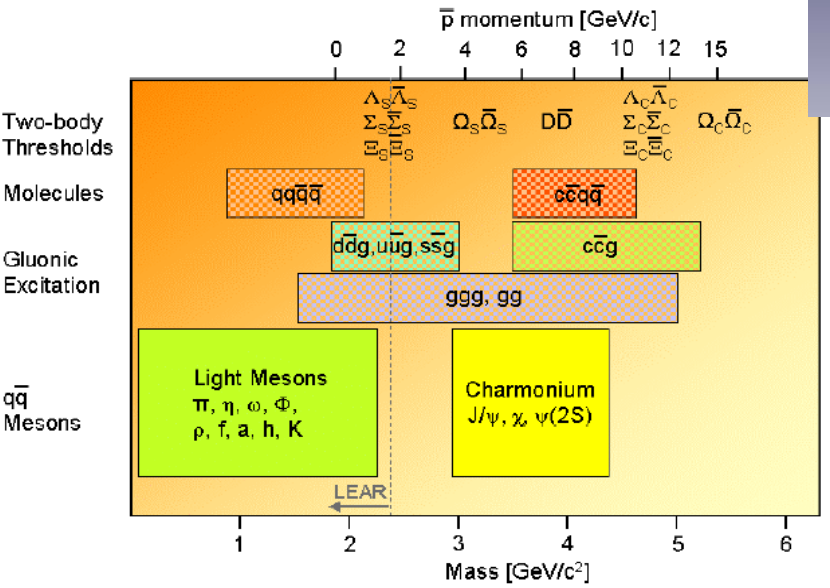
Facility for Antiproton and Ion Research

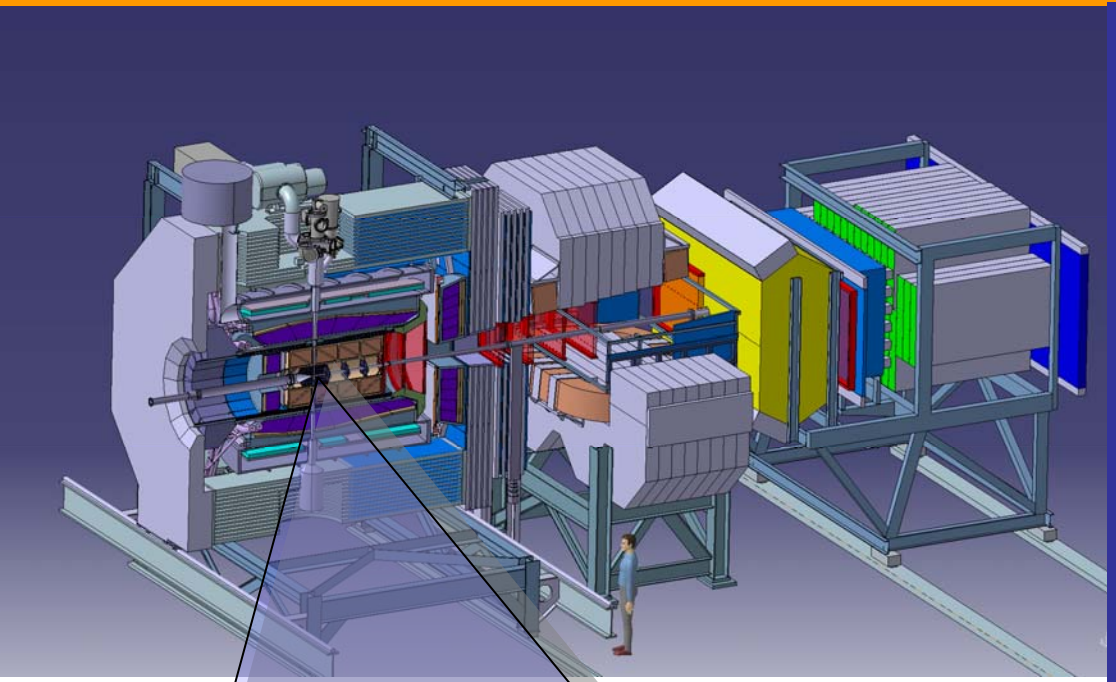


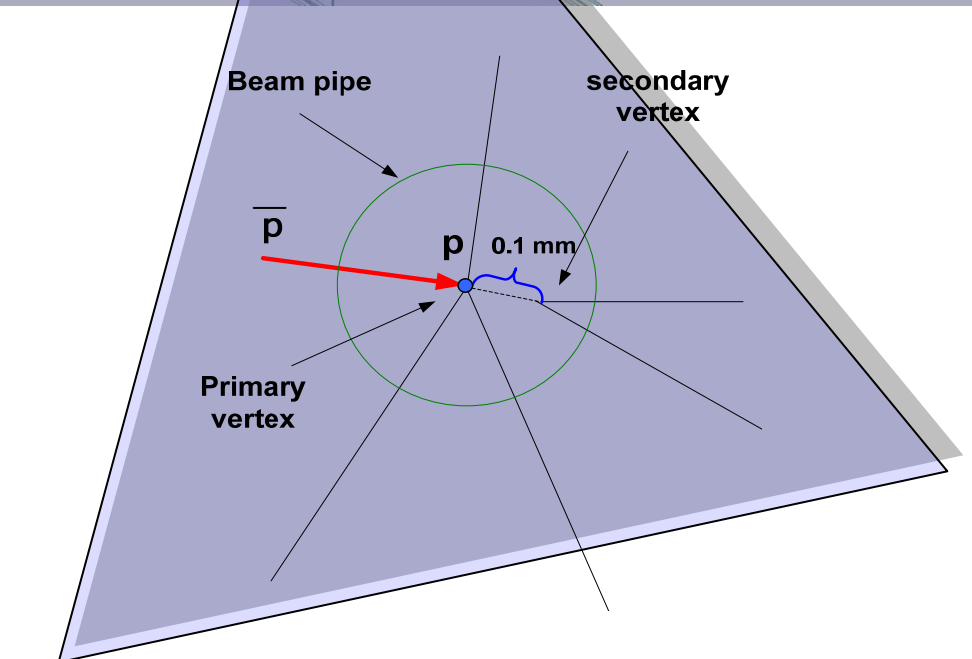




- Nearly 4π solid angle
- High rate capabilities ($2 \cdot 10^7$ annihilations /s)
- Continuous readout and Efficient event selection
- Moment resolution (1%)
- Vertex info for D, K^0_s, L (c_τ = 317 μm for D^{+-})
  - good tracking
- Good PID (γ, e, m, π, k, p) with Cherenkov, tof, dE/dx

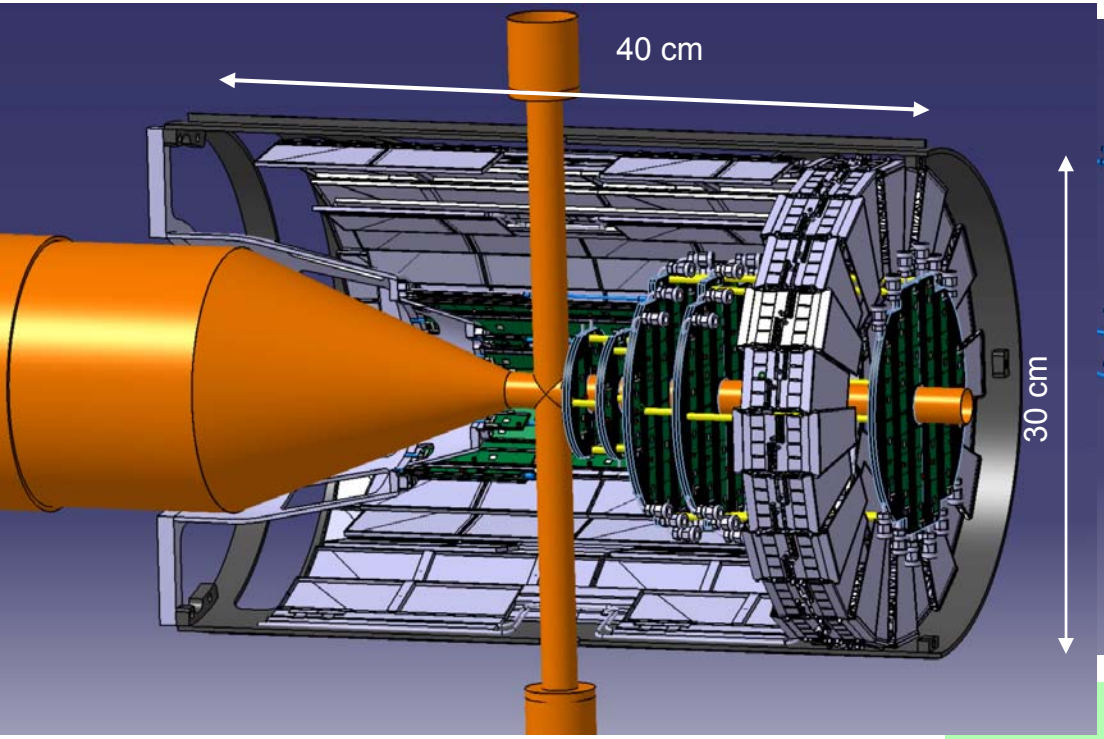
Micro-Vertex-Detector requirements

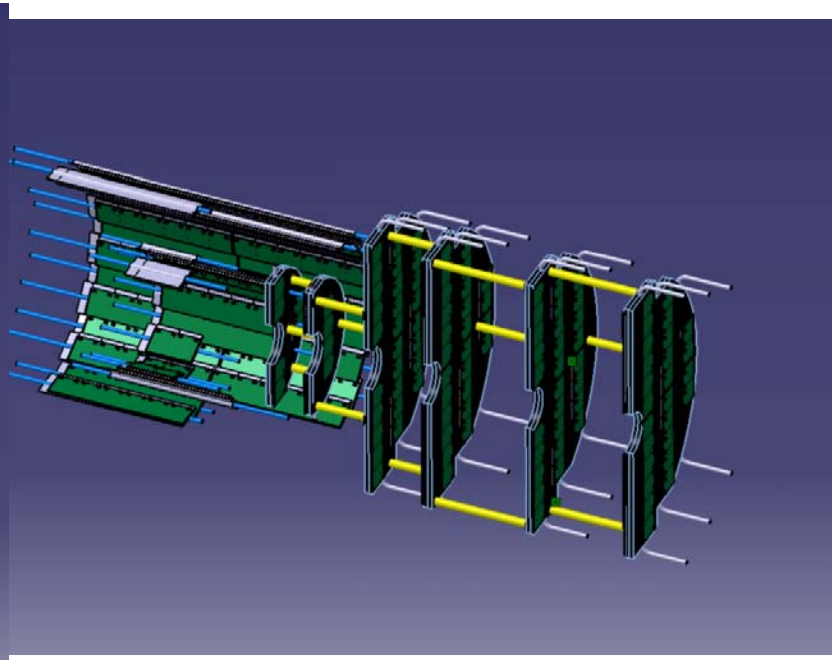




- Good spatial resolution in r-phi
  - Momentum measurement of pions from D* decays
- Good spatial resolution specially in z
  - Vertexing, D-tagging
- Good time resolution
  - ≤ 10 ns with $2 \cdot 10^7$ ann/s
- Triggerless readout
- Energy loss measurement
  - dE/dx for PID
- Low material budget
  - low momentum of particles (from some hundreds of MeV/c) (<1% X_0 for each layer)
- Radiation hardness (~$4 \cdot 10^{13}$ n $_{1MeV\ eq}$ /cm^2) (half year data taking, 15 GeV/c antip-p)
  - Different radiation load

MVD layout





Micro Vertex Detector

4 barrels

Inner layers: hybrid pixels

Outer layers: double sided strips

and 6 forward disks

4 disks: hybrid pixels

2 disks: pixel and strips mixed

Custom Pixel Detector:

- Hybrid pixel made by thin epitaxial sensors and readout with130 nm CMOS technology
- 100 μm x 100 μm pixel sizes;
- ~ 850 FE readout chip (12760 pixels);
- continuous data transmission without trigger
- max. chip data rate : ~ 0.8 Gb/s (40 bit/pixel)
- energy loss measurement: time over threshold; dynamic range: →100 fC

Hybrid pixel detector layout

D. Calvo

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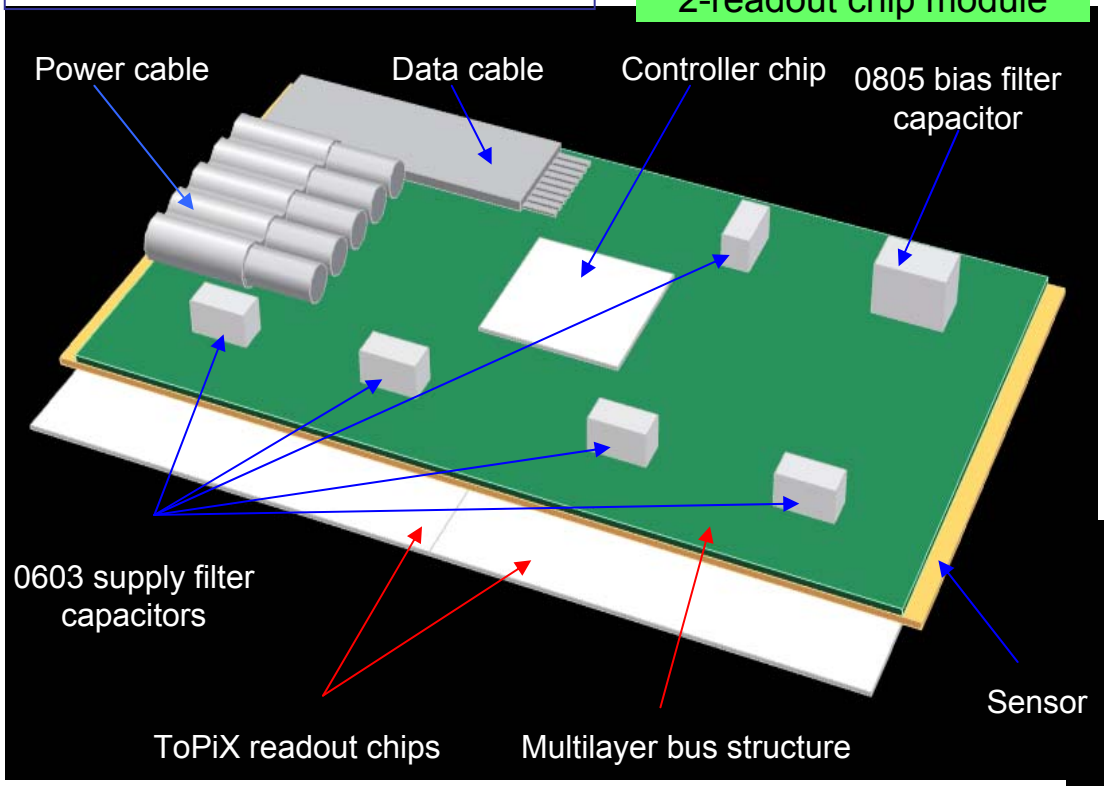
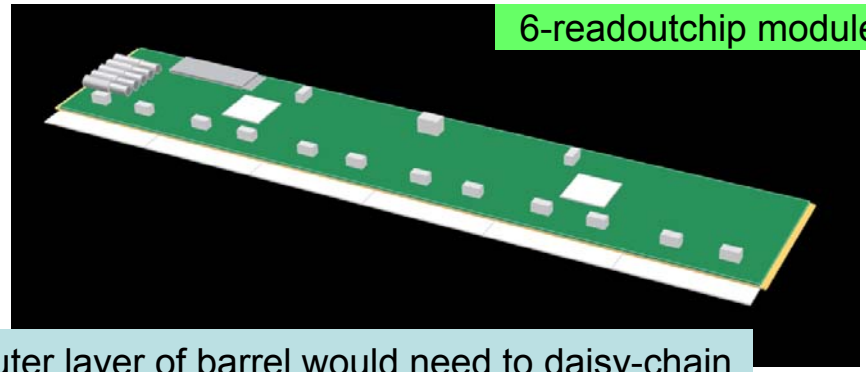
Assembly layout on the disks

Assembly scheme

2-readout chip module





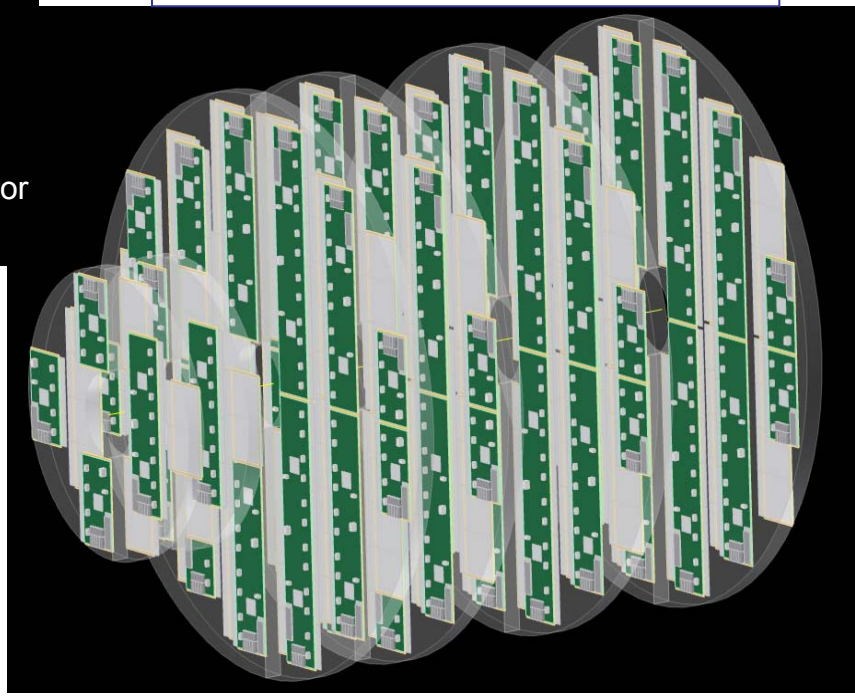
For outer layer of barrel would need to daisy-chain two 6-chip modules (power and controller chips) to keep cables out of active region

• Controller chips serve two or three ToPiX readout chips

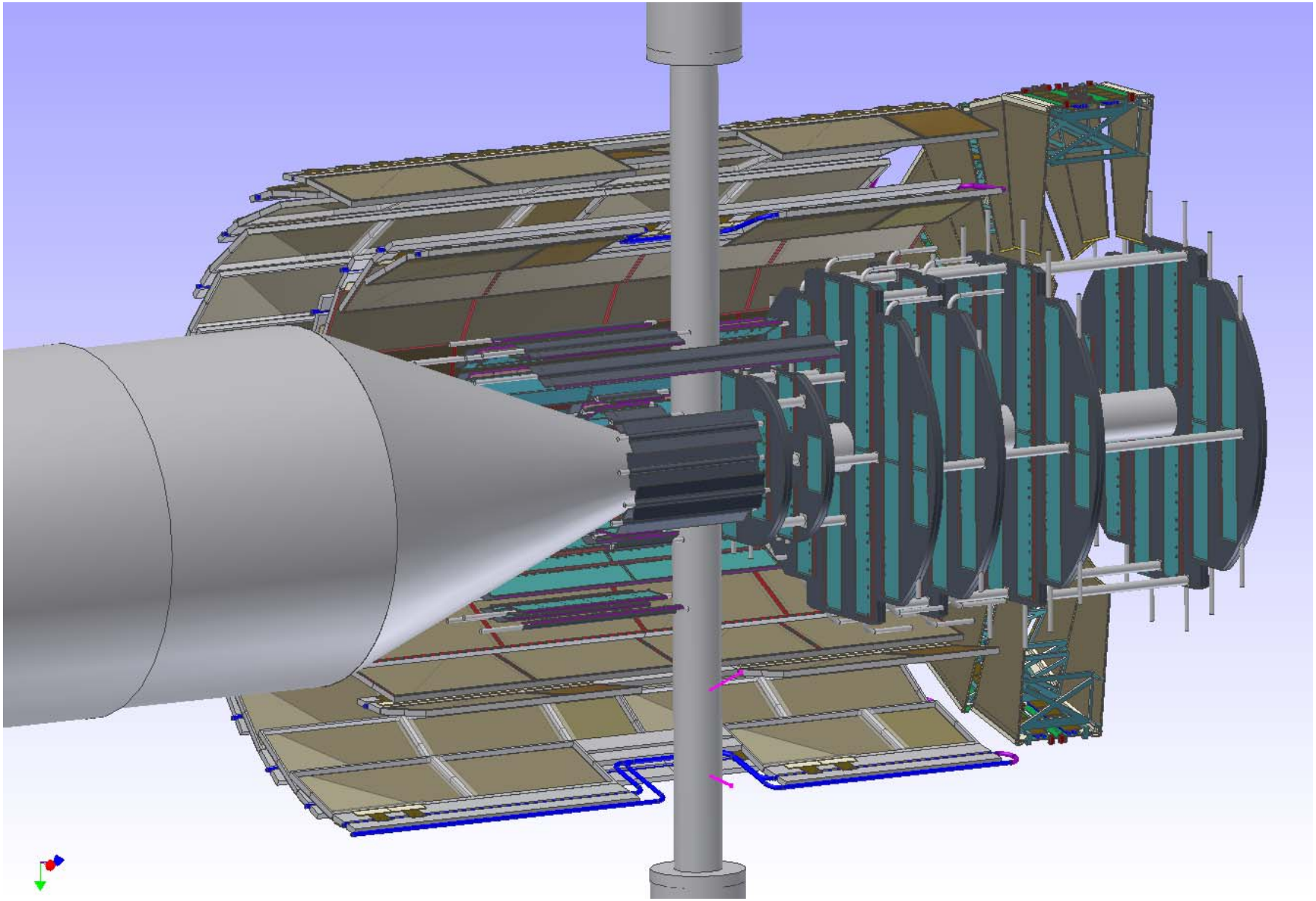
Possibility of daisy-chaining controllers to save on cables (where data rates allow)

Keeping cables out of active region means that some modules may require two designs according to which end the cables have to be connected

Layout of forward disks

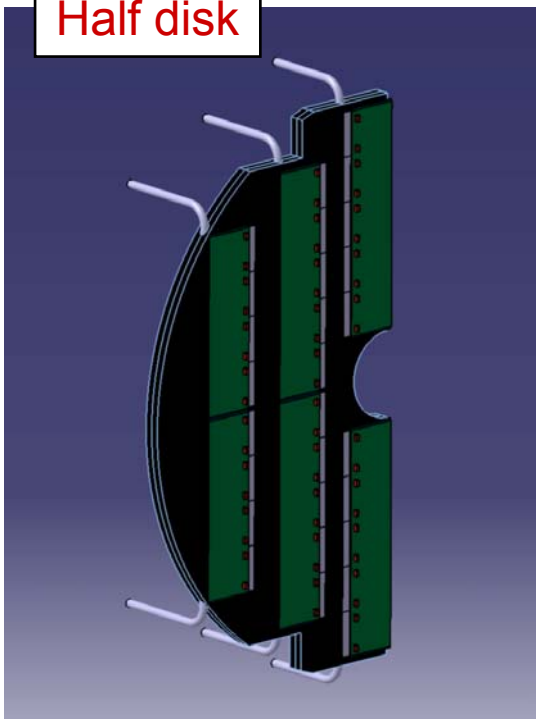


Pixel detector scheme



Disk and stave layout

Half disk



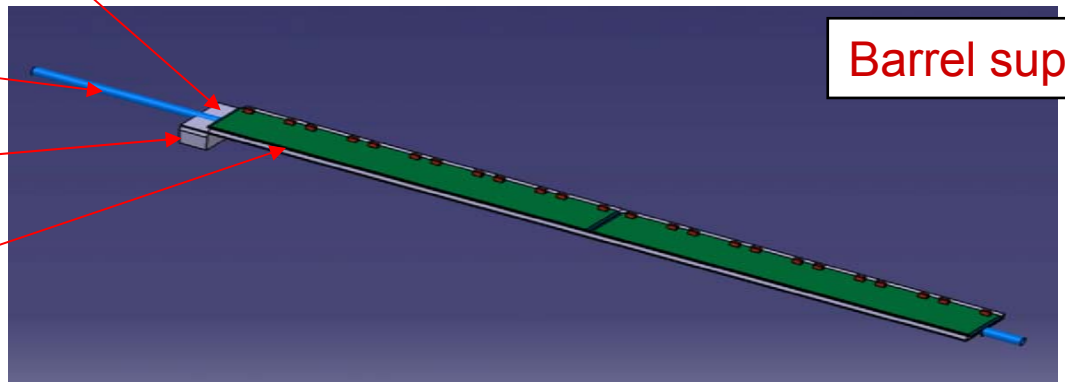
- Disk split in two halves along the mid-plane
- Material for heat dissipation/support: carbon foam
- Embedded cooling capillary between the two halves
- All elements glued with thermal glue
- Problem: large glued area -> test have to be performed

“Ωmega” support (CFRP – thermal & structural)

cooling capillary

reference block

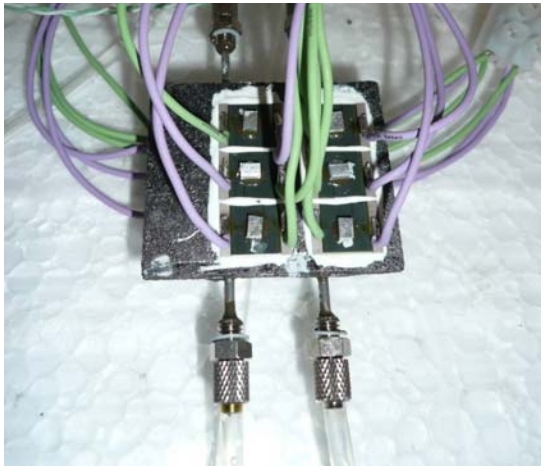
foam substrate

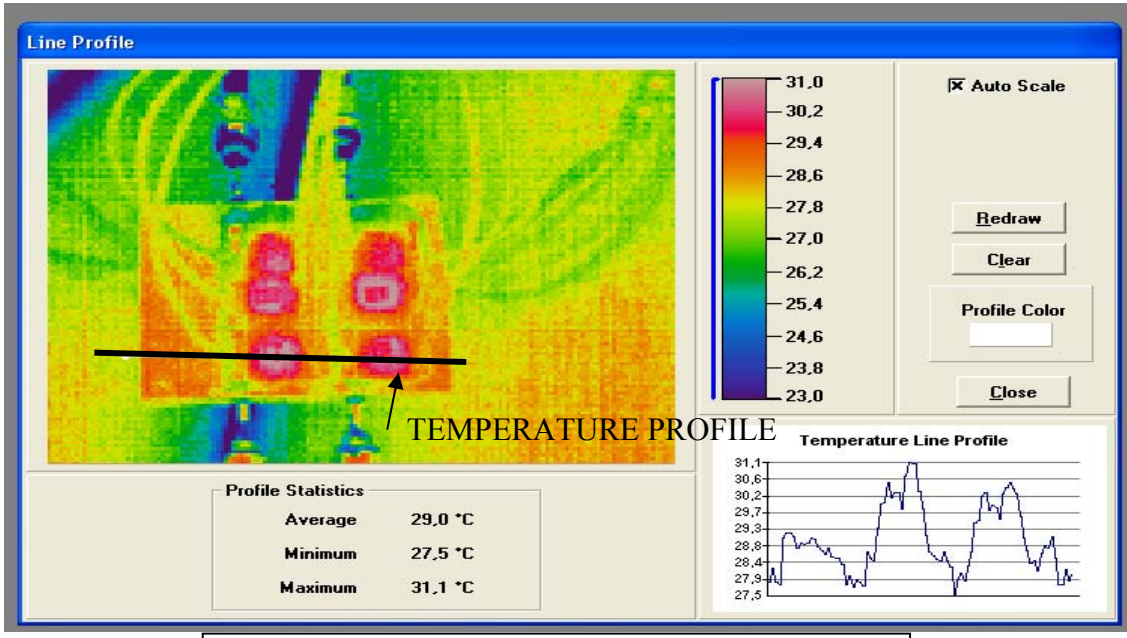


Barrel super-module

First study on water cooling system

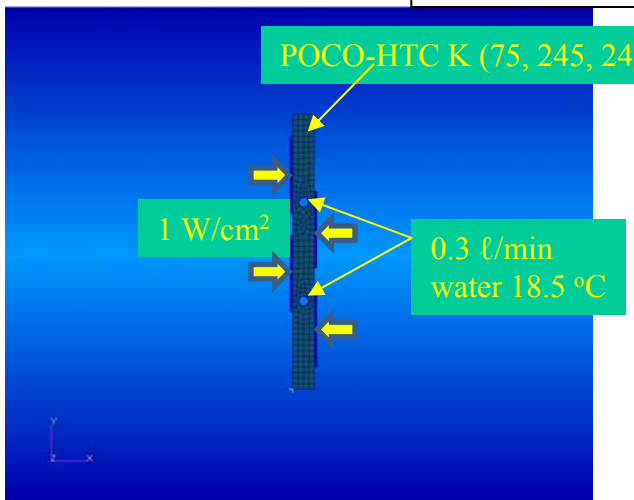
Small and partial prototype of a disk
Cooling fluid: water @ 18.5 °C
12 resistors (1 W/cm^2 each resistor)
POCO-HTC foam support (4 mm thick)
Stainless steel pipes ($ø_e$2mm, $ø_i$1.84mm)

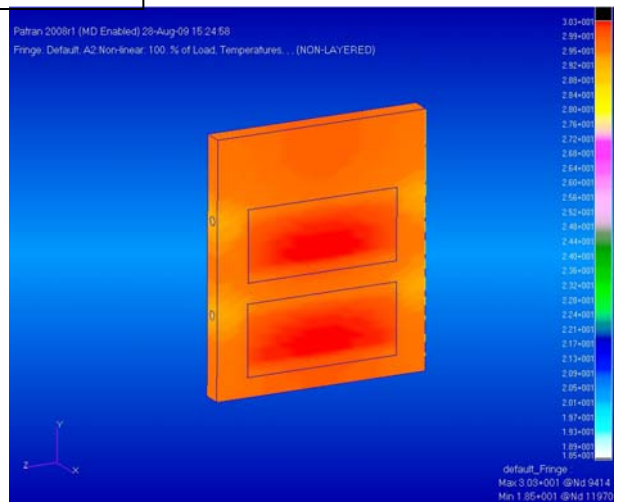


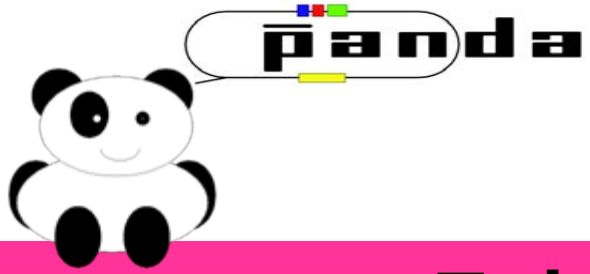


Cooling test results – IR image

Results from simulations





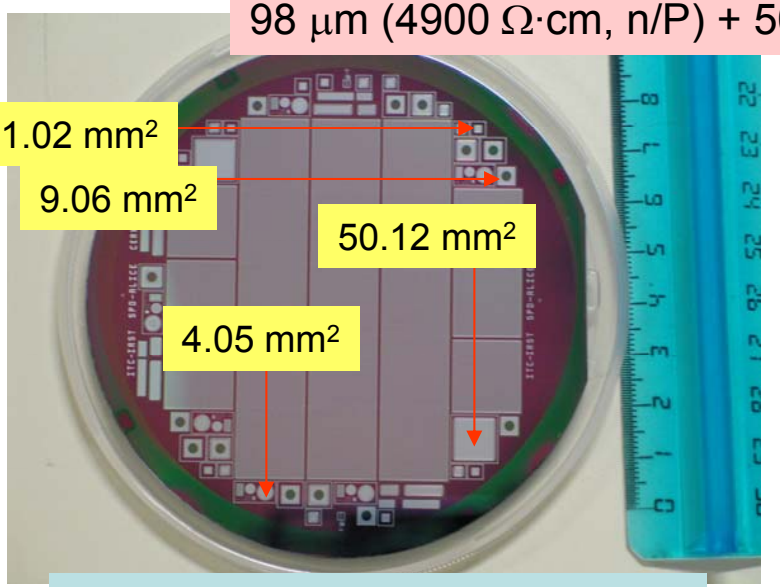


Epitaxial silicon devices

D. Calvo

Diodes and single chip sensor from epi-wafers

49 μm (4060 Ω·cm, n/P) + 500 μm Cz substrate (0.01-0.02 Ω·cm, n^+/Sb) → 100 μm
74 μm (4570 Ω·cm, n/P) + 500 μm Cz substrate (0.01-0.02 Ω·cm, n^+/Sb) → 120 μm
98 μm (4900 Ω·cm, n/P) + 500 μm Cz substrate (0.01-0.02 Ω·cm, n^+/Sb) → 150 μm

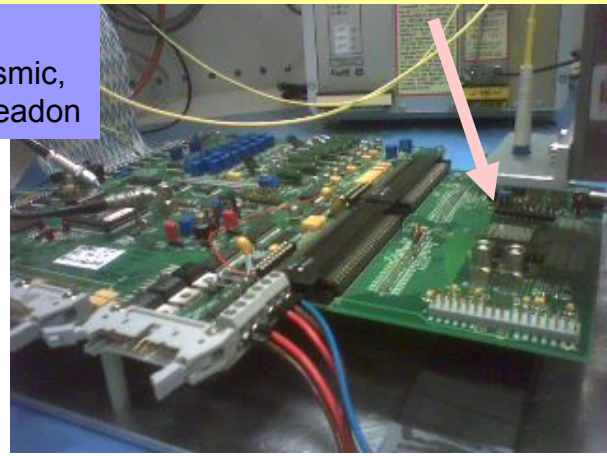


with the ALICE layout at FBK

Single chip assembly

- ✓ pixel obtained with the ALICE masks (50 μm x 425 μm)
- ✓ test performed using ALICE pixel readout chip and test system in collaboration with P. Riedler - CERN

NIM A594 (2008) 29-32;
D. Calvo, P. De Remigis, F. Osmic, P. Riedler, G. Stefanini, R. Wheadon

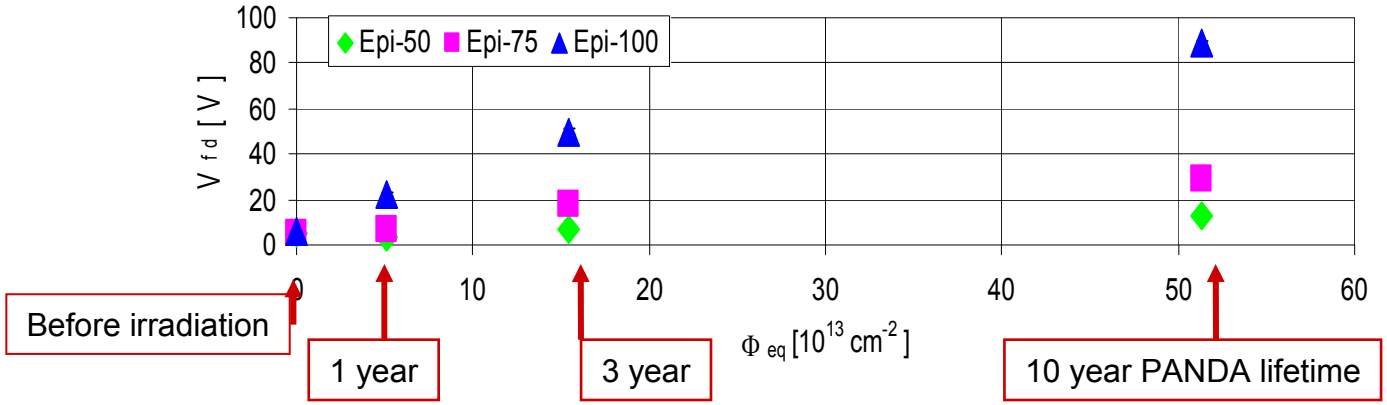


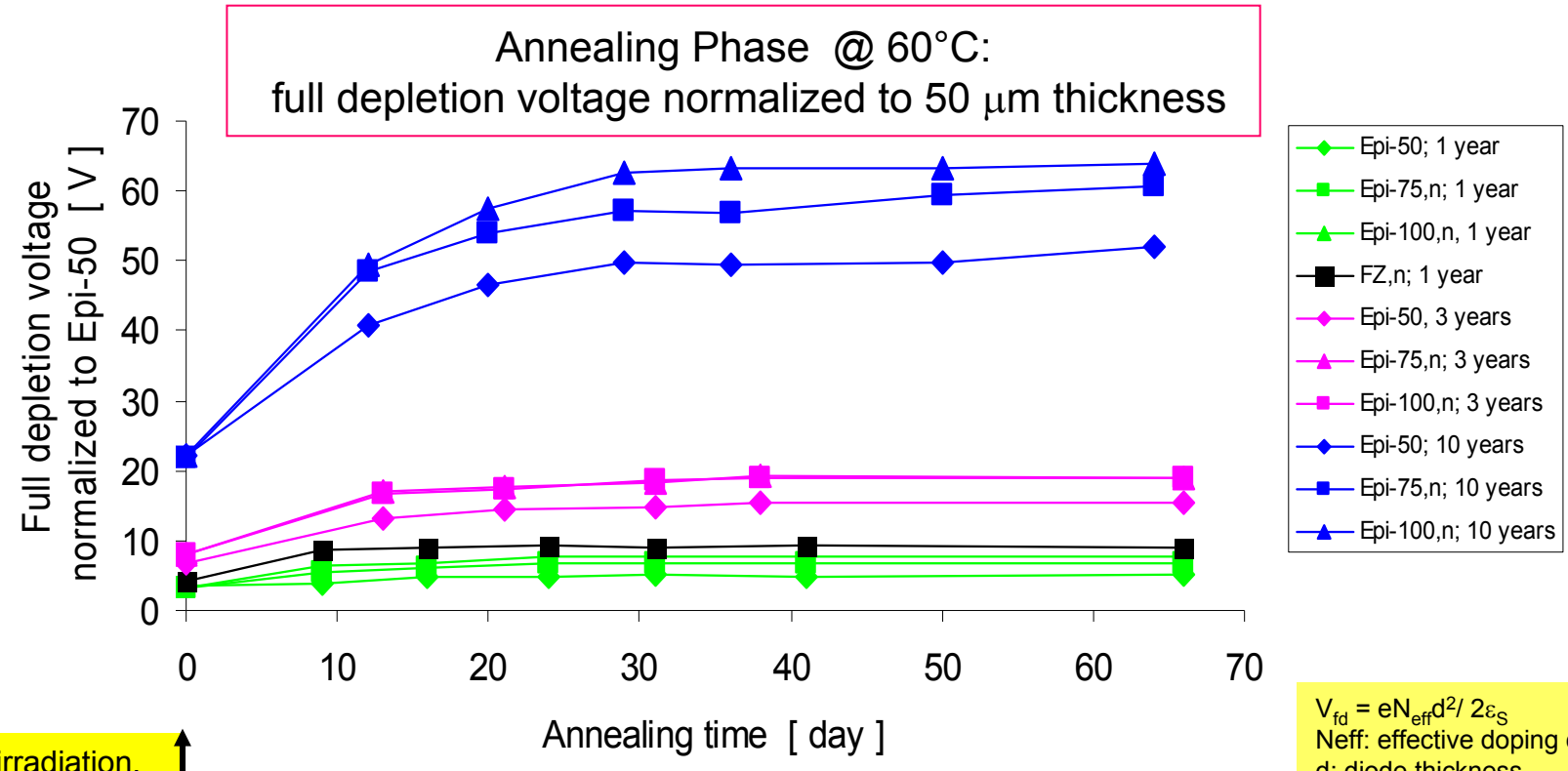
Diodes

Test of radiation damage with neutrons from Pavia nuclear reactor. Equivalent fluence values on the diodes : 5.13×10^{13}, 1.54×10^{14}, 5.13×10^{14} n(1MeV$_{eq}$)/cm^2 corresponding to ~ 1, 3 and 10 years of PANDA lifetime

300 μm FZ diodes have been used as reference

Results from radiation damage test with neutrons

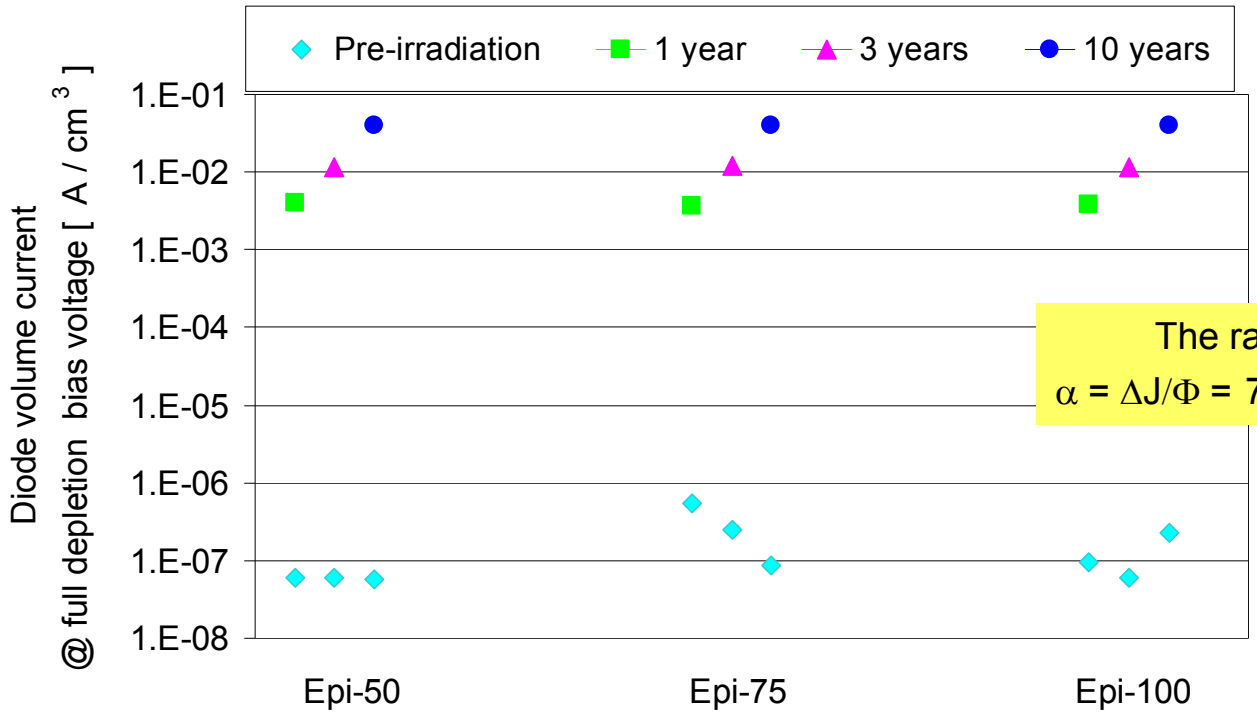




$V_{fd} = eN_{eff}d^2/ 2\varepsilon_S$
Neff: effective doping concentration
d: diode thickness
ε_S : silicon dielectric constant

Results from radiation damage test:
the radiation damage constant

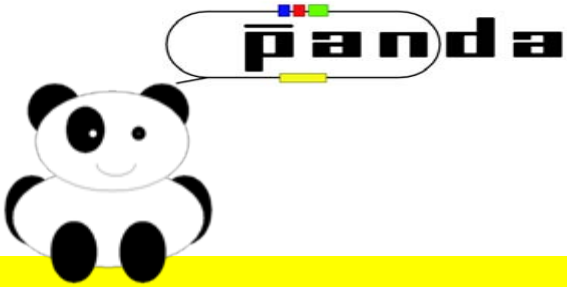
Equivalent fluence values on the diodes : 5.13×10^{13}, 1.54×10^{14}, 5.13×10^{14} n(1MeV$_{eq}$)/cm^2 corresponding to 1, 3 and 10 years of PANDA lifetime



The radiation damage constant is
$\alpha = \Delta J/\Phi = 7.6(\pm 0.3) \times 10^{-17}$ A/cm for all diodes.

Lekage current < 50 nA/pixel (100 μmx100μm size, 100 μm thick)

The diode volume current @ full depletion voltage, after a 65 days annealing phase @ 60°C, decreased by a factor 2.

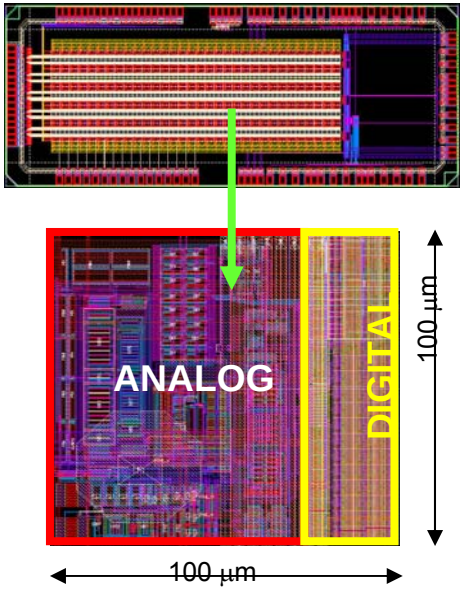


ASIC prototype

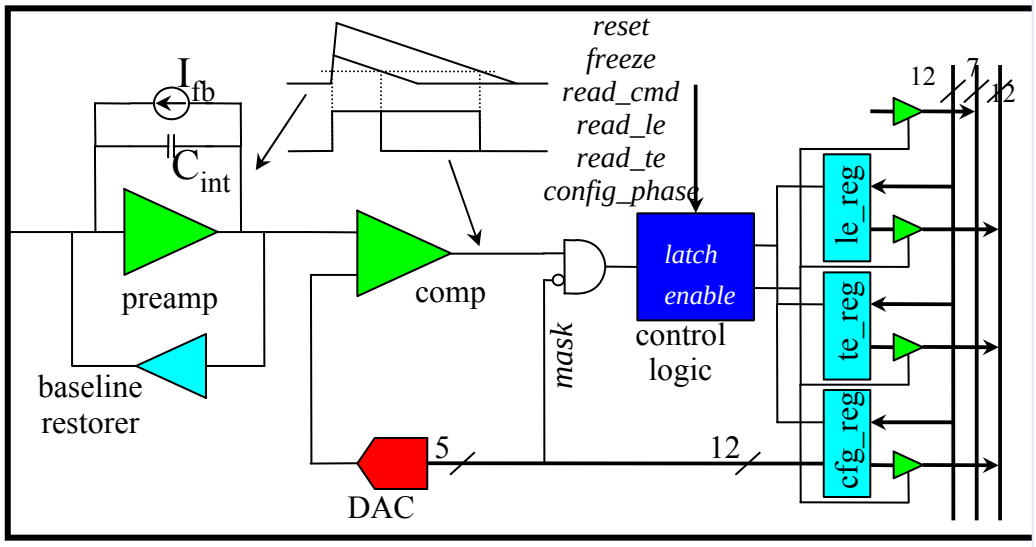
D. Calvo

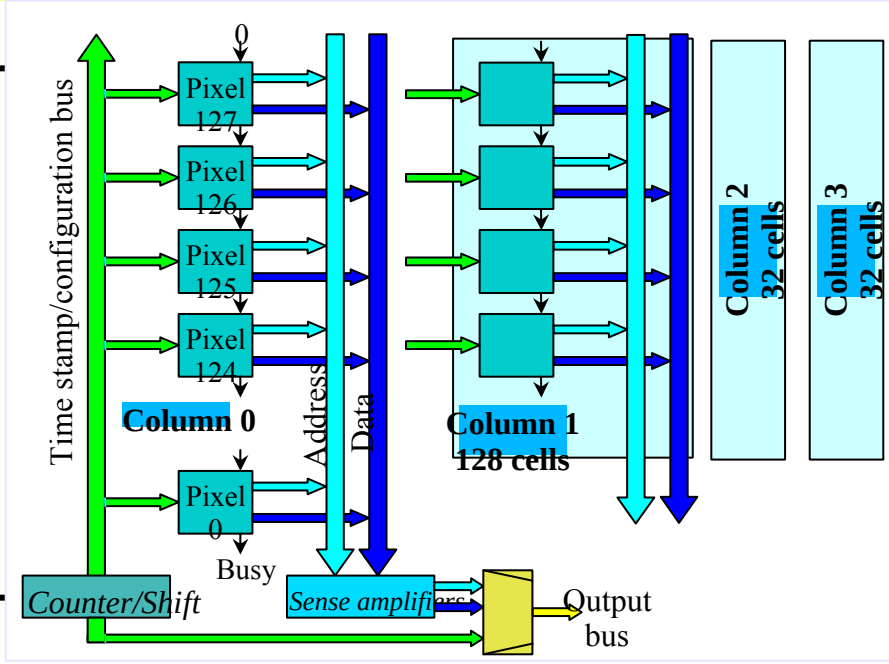
The architecture of ToPix_2

ToPix_2, 130 nm CMOS technology



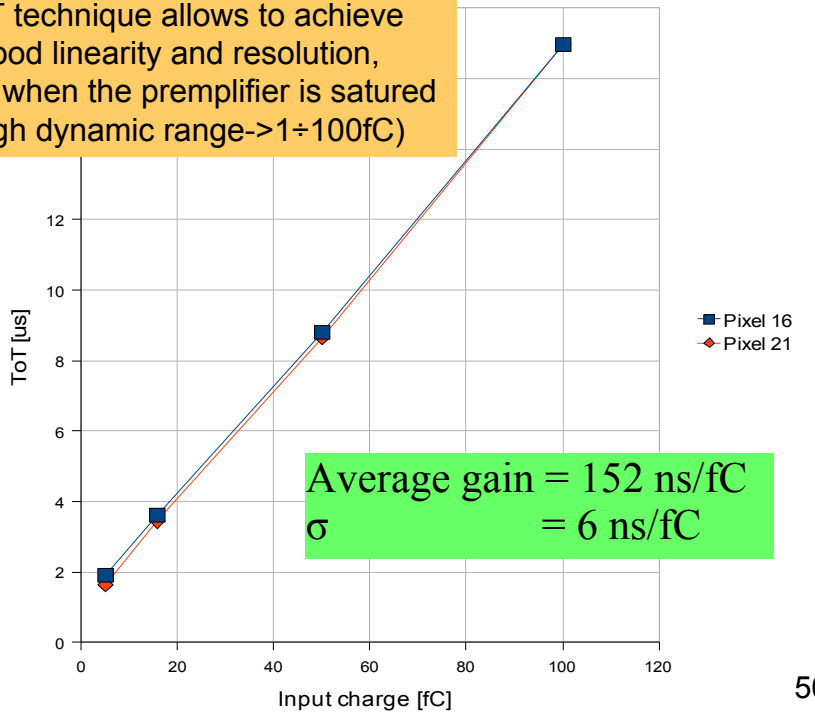
- 5x2 mm^2 area with 4 folded columns with a total of 320 readout cells of 100x100μm^2 size
- analogue + digital circuits (analog power consumption below 12μW @1.2V)
- Clock @ 50MHz
- Time over Threshold technique implemented to obtain a energy loss measurement
- SEU-hardened memory cells (Dice with baseline design:
  all pmos devices are located in the same nWell and don't have guard contact separation)
- absence of enclosed structures to study the radiation tolerance of the 130nm CMOS technology
- inputs for connecting external sensors (selectable input polarity)
- comparator threshold controlled by DAC (5 bits)
- 12 + 12 bits leading and trailing edge and 12 bits configuration registers
- 12 bits bus for time stamp and 12+7 bits output bus for data + address





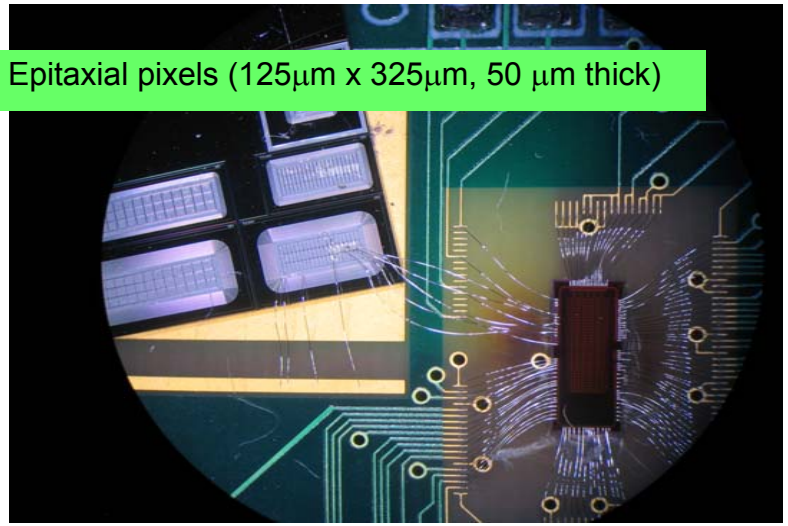
Characterization of ToPix_2

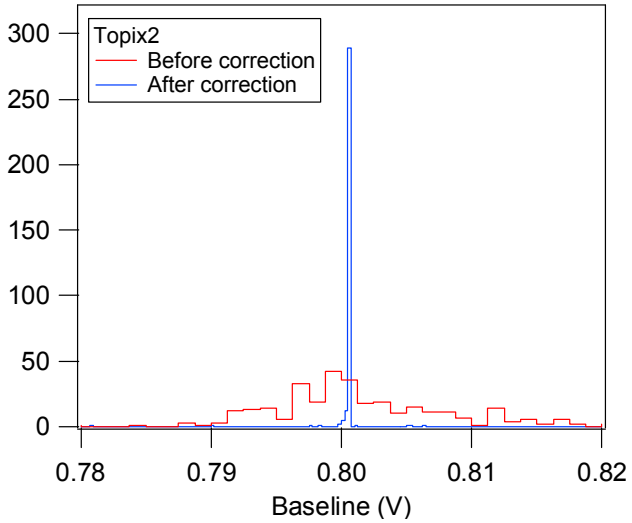
ToT technique allows to achieve good linearity and resolution, even when the premplifier is satured (high dynamic range->1÷100fC)

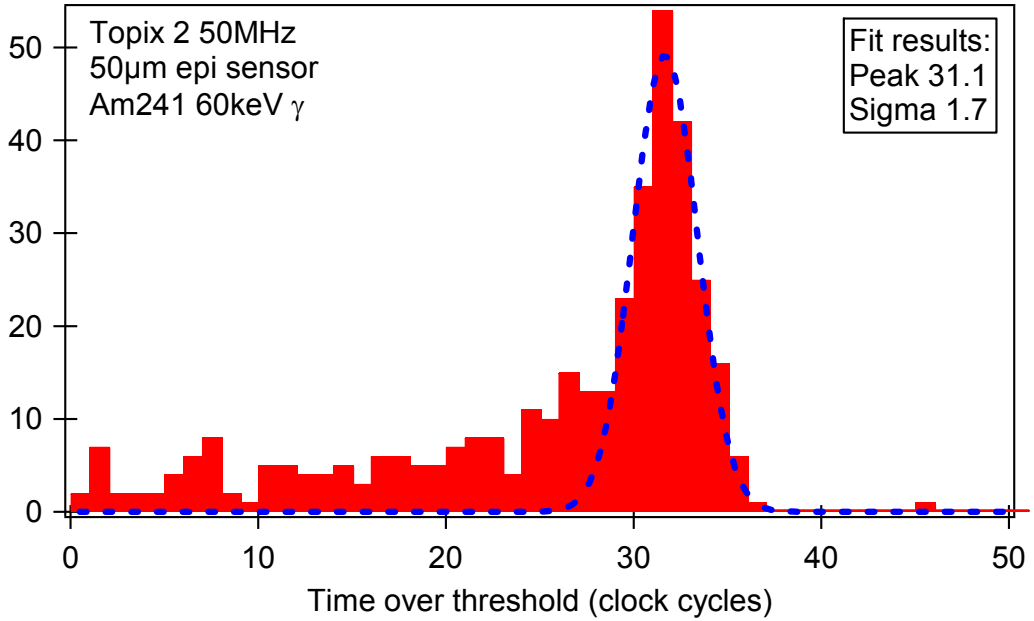


Average gain = 152 ns/fC
σ = 6 ns/fC

Epitaxial pixels (125μm x 325μm, 50 μm thick)



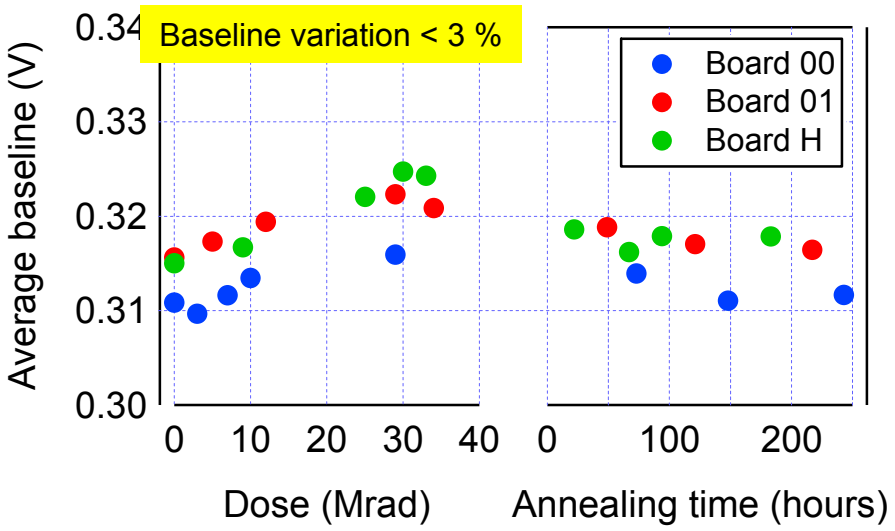


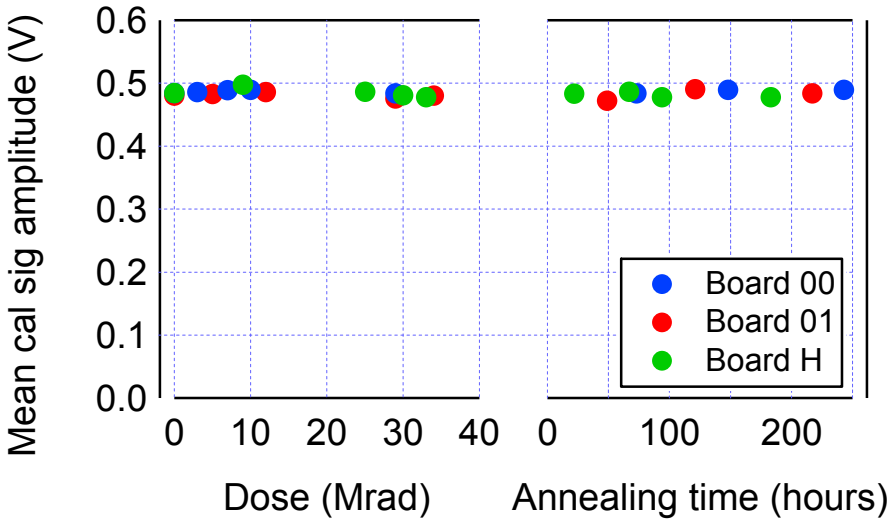


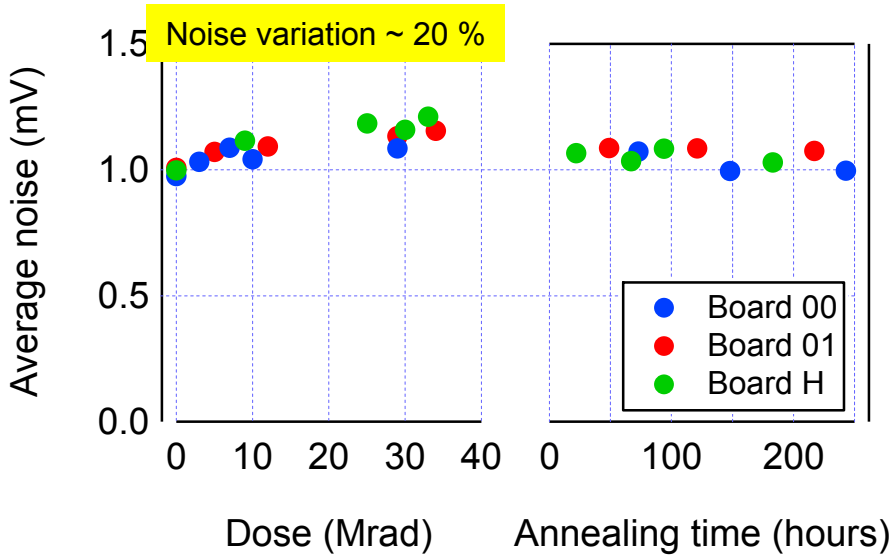
TOT calibration

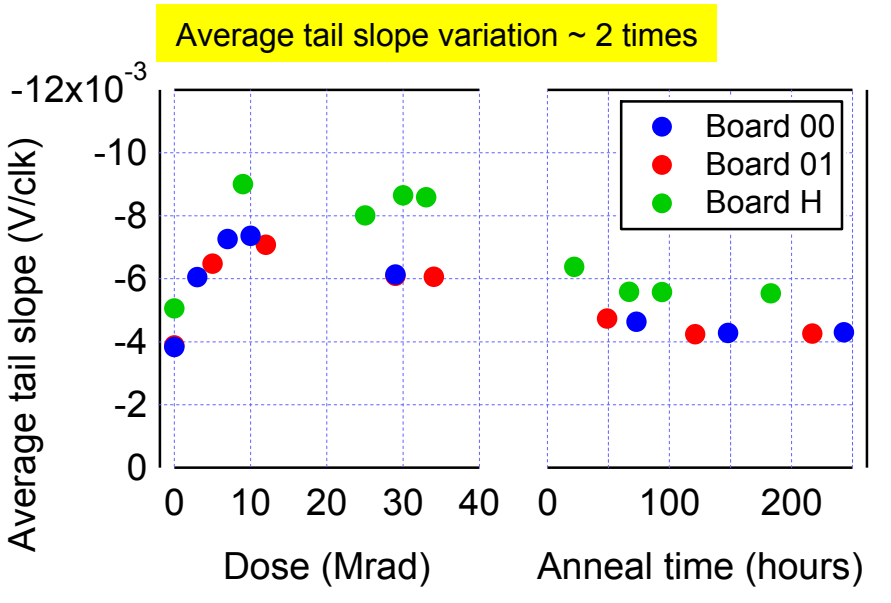
TID test on ToPix_2

Total Ionizing Dose test with the X ray source at CERN (Thanks to F. Faccio)
followed by an annealing phase at 100°C





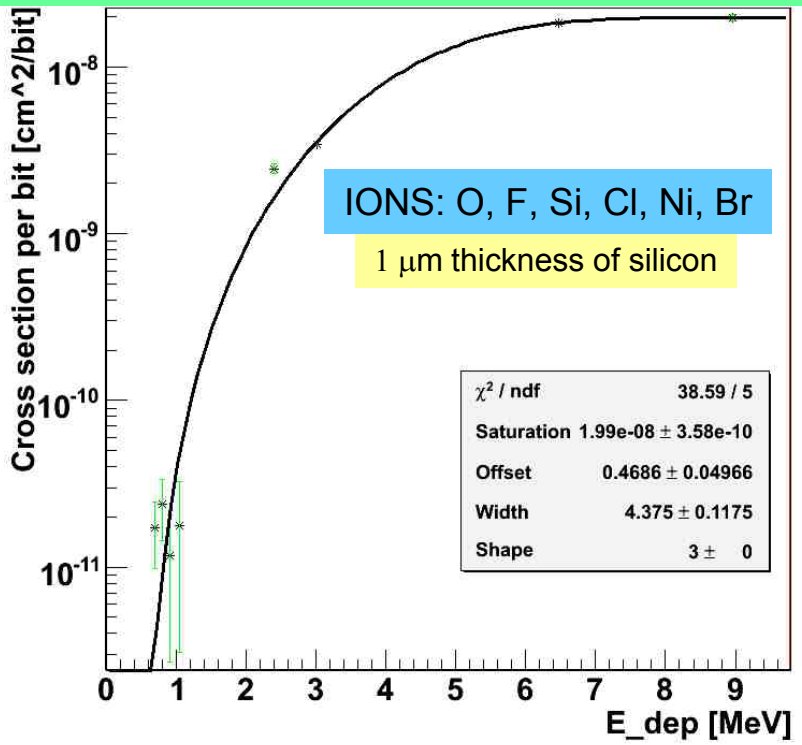




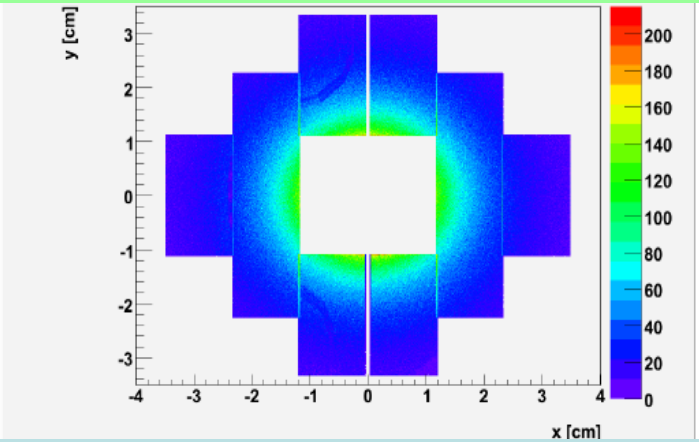
SEU test on ToPix_2

12 bit configuration register made by SEU-hardened memory cells based on first Dice architecture (all pmos devices are located in the same nWell and don't have guard contact separation)

SEU cross section of ToPix2 for heavy ions. The test was performed at the SIRAD facility (INFN-LNL). Thanks to A. Candelori



And using the method described in the paper of
M. Huhtinen, F. Faccio - CERN
"Computational method to estimate SEU rates in an accelerator environment"; NIM A 450 (2000) 155-172



Hadron flux on the disk 2 of the pixel detector, evaluated for pbar-p interactions @15 GeV/c:
5.8 [Mhit /(s·cm^2)]

In the PANDA environment:
$4.1 \cdot 10^{-9}$ SEU/s·bit
(evaluated with a 1μm^3 sensitive volume)

2.3 SEU / hour are expected in the final ToPix readout chip taking into account:

✓a 12 bit configuration register in each pixel readout cell with the same DICE architecture

✓12760 pixel readout cells

Conclusions

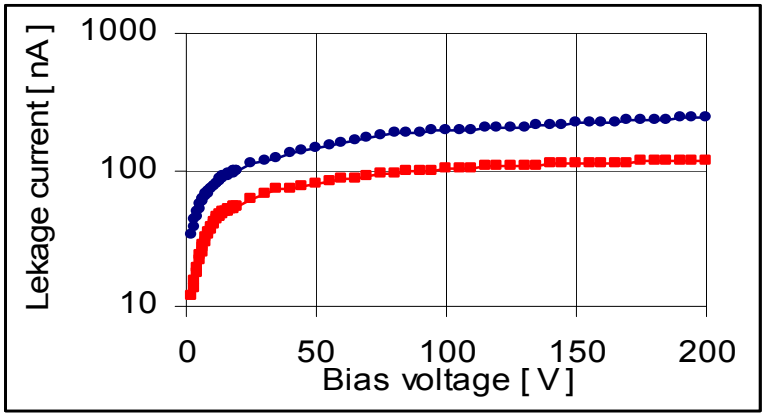
- the carbon foam is an interesting material for the power dissipation of the pixel detector

- the use of epitaxial silicon material could be very promising, also in term of radiation damage, but an epitaxial resistivity tuning has to be performed for the full depletion voltage optimization

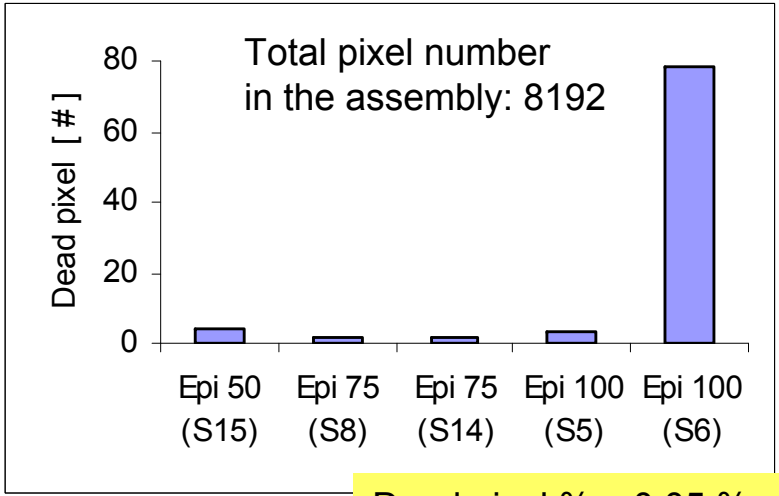
- the 130 nm CMOS technology is suitable to develop the pixel readout for:
  - limited power consumption
  - smaller pixel with many functionalities, but
    - enclosed gate layout is needed for the critical transistors of the discharge circuit or larger current is needed from the capacitor discharge circuit
    - the implemented DICE architecture (first level of radiation hardness) isn't completely satisfactory for the PANDA environment

Results from thin Si-epitaxial pixel assemblies

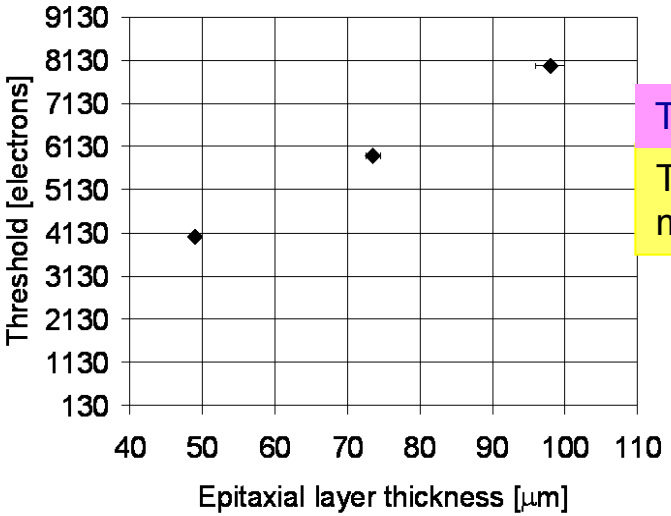
Epi 75 and Epi 50



Test performed with a ^{90}Sr source to verify the bump bonding process



Dead pixel % ≤ 0.05 %; ≤ 1% (worst case)



Test performed with a ^{90}Sr source

Threshold values in electrons corresponding to the Landau most probable value for the different epitaxial layer thicknesses

NIM A594 (2008) 29-32; D. Calvo, P. De Remigis, F. Osmic, P. Riedler, G. Stefanini, R. Wheadon